MAXIM

1995 NEW RELEASES DATA BOOK

Volume IV

Featuring:

- *Product Selection Tables and Trees*
- *Data Sheets*
- *Free Sample Request Cards*

Other Data Books Available from Maxim:

- *High-Frequency ASIC Development Handbook*
- *Maxim 1994 New Releases Data Book, Vol. III*
- *Maxim 1994 Applications & Product Highlights Book*
- *Maxim 1994 Evaluation Kits Data Book*
- *Maxim 1993 New Releases Data Book, Vol. II*
- *Maxim 1993 Applications & Product Highlights Book*
- *Maxim 1992 New Releases Data Book, Vol. I*
- *Maxim 1992 Applications & Product Highlights Book*

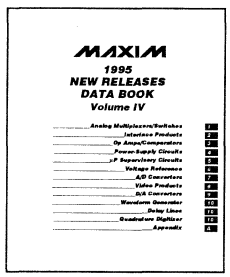
HOW TO USE THE 1995 NEW RELEASES DATA BOOK

Maxim's 1995 New Releases Data Book (Vol. IV) brings together over 130 new devices from 12 product groups in a single, easy-to-use "Design-Guide" format. Each product group contains: (1) Data sheets for all products in the group; (2) Product tables and trees.

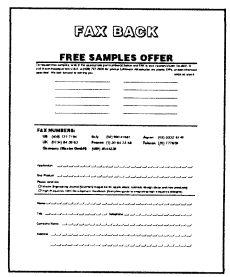
If you need samples for further evaluation, simply fill out and send or FAX one of the sample request cards at the front of the book, or call 1-800-998-8800 for prompt fulfillment.

There are several ways to locate a specific product or product group:

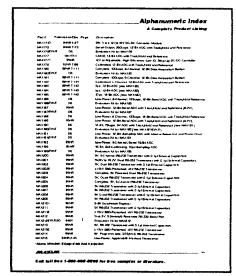
1	Analog Multiplexers/Switches
2	Interface Products
3	Op Amps/Comparators
4	Power-Supply Circuits
5	µP Supervisory Circuits
6	Voltage Reference
7	A/D Converters
8	Video Products
9	D/A Converters
10	Waveform Generator Delay Lines Quadrature Digitizer



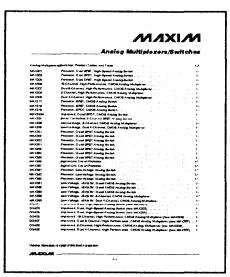
LOCATE PRODUCT SECTIONS BY TAB NUMBER



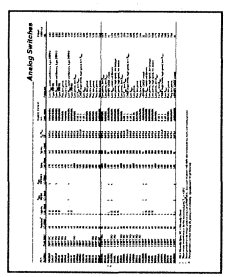
FREE SAMPLES REQUEST CARDS



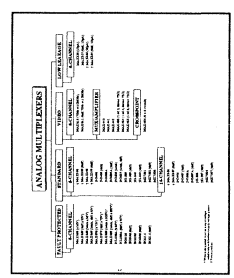
COMPLETE ALPHANUMERIC PART INDEX CROSS REFERENCED TO OTHER MAXIM BOOKS



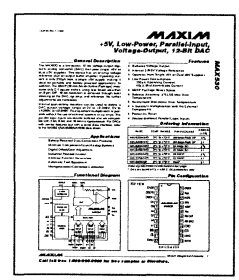
SECTION TABLE OF CONTENTS FOR THE 1995 NEW RELEASES DATA BOOK SORTED BY PRODUCT FAMILY



SELECTION TABLES WITH SPECIFICATIONS, COMMENTS, PRICING



PRODUCT TREES



DATA SHEETS

MAXIM

1995 NEW RELEASES DATA BOOK Volume IV

Introduction

Maxim Integrated Products designs, develops, manufactures, and markets a broad range of linear and mixed-signal integrated circuits (ICs) for use in a variety of electronic products. These ICs "connect" the real (analog) world to the digital world. They detect, measure, amplify, and convert real-world signals—such as temperature, pressure, or sound—into digital signals a computer can process. Over the past eleven years, Maxim has introduced over 700 analog ICs, more than any other company.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. Our product lines include: microprocessor supervisory circuits, data converters, references, RS-232 interface circuits, amplifiers, power-control circuits, timers and counters, display circuits, multiplexers, switches, voltage detectors, and analog filters. And the acquisition of Tektronix Integrated Circuits operation has added high-frequency products to the product line. Recognizing the growing demand for BiCMOS technology, Maxim has focused increasingly on CMOS- and BiCMOS-based products. These circuits are marketed worldwide, principally through distributors and independent sales representatives, and are available in several different packages and temperature ranges to meet varying customer requirements.

New Releases

During the past year, Maxim has released more than 130 new devices. Specifications for these products are collected in this new volume, which gives quick access to Maxim's innovative and exciting new releases. Mature products and some recently introduced second-source products do not appear in this book, but are identified in the Alphanumeric Index. Free samples and data sheets for these products are available from your local sales representative, or directly from the factory by calling 1-800-998-8800.

Customer Service

Maxim provides free samples and literature through a toll-free number: 1-800-998-8800. Plus, evaluation kits or a small quantity of parts can be ordered using VISA or MasterCard.

Customer service representatives are available during normal business hours to provide you with information on orders placed directly with the factory or with any of our franchised distributors. Please see the back cover for a list of domestic and international sales representatives and distributors.

Technical Support

In order to provide full technical support, Maxim has a large, highly qualified group of senior applications engineers available to help you. Simply call (408) 737-7600 extension 4000, or FAX your questions to (408) 736-1831.

Maxim also offers a wide variety of technical publications, including the *Maxim Engineering Journal* (a quarterly magazine explaining the application of our new products), *High-Reliability Products Data Book*, *Applications and Product Highlights Books*, *New Releases Data Books*, 1994 *Evaluation Kits Data Book*, *Design Guides* on each product family, and *High-Frequency ASIC Development Handbook*. Call toll-free 1-800-998-8800 for any literature you may need.

Reliability

Maxim's mission is to provide reliable, innovative analog ICs that solve customer problems. Our programs offering complete lot traceability, life test, and humidity life qualification are unique in the industry.

ISO 9001 Certification

In September 1993, Maxim received formal ISO 9001 certification, validating that our quality system meets the worldwide standard. ISO 9001 is the most stringent of the 9000 series of specifications because it includes review of design, test, manufacturing, and shipment processes.

Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.

4,700,286, 4,679,134, 4,636,930, 4,859,963, 4,857,778, 4,897,774, 4,797,899, 4,806,875, 4,847,522, 4,812,891, 4,809,152, 4,801,888, 4,797,569, 4,777,580, 4,777,577, 4,999,761, 4,752,700, 5,142,242, 5,055,796, 5,051,686.

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94NR – 1994 New Releases Data Book, Vol. III
94EV – 1994 Evaluation Kit Data Book
93NR – 1993 New Releases Data Book, Vol. II
92NR – 1992 New Releases Data Book, Vol. I
DS – Individual Data Sheet

Alphanumeric Index

A Complete Product Listing

Part #	Publication/Doc. Page	Description
ADC0820	MAXFAX	CMOS, High-Speed, 8-Bit ADC with Track/Hold
BB3553	MAXFAX	Very Fast Buffer Amplifier
BB3554	MAXFAX	Wideband, Fast-Settling Op Amp
DG200/A	MAXFAX	Dual SPST, CMOS Analog Switch
DG201/A	MAXFAX	Quad SPST, Normally Closed, CMOS Analog Switch (see MAX361)
DG202	MAXFAX	Quad SPST, Normally Open, CMOS Analog Switch (see MAX362)
DG211	MAXFAX	Quad SPST, Normally Closed, CMOS Analog Switch (see MAX361)
DG212	MAXFAX	Quad SPST, Normally Open, CMOS Analog Switch (see MAX362)
DG300A	MAXFAX	Dual SPST, TTL-Compatible, CMOS Analog Switch
DG301A	MAXFAX	SPDT, TTL-Compatible, CMOS Analog Switch
DG302A	MAXFAX	Dual DPST, TTL-Compatible, CMOS Analog Switch
DG303A	MAXFAX	Dual SPDT, TTL-Compatible, CMOS Analog Switch
DG304A	MAXFAX	Dual SPST, CMOS Analog Switch
DG305A	MAXFAX	SPDT, CMOS Analog Switch
DG306A	MAXFAX	Dual DPST, CMOS Analog Switch
DG307A	MAXFAX	Dual SPDT, CMOS Analog Switch
DG308A	MAXFAX	Quad SPST Analog Switch
DG309	MAXFAX	Quad SPST Analog Switch
DG381A	MAXFAX	Dual SPST, General-Purpose, CMOS Analog Switch
DG384A	MAXFAX	Dual DPST, General-Purpose, CMOS Analog Switch
DG387A	MAXFAX	SPDT, General-Purpose, CMOS Analog Switch
DG390A	MAXFAX	Dual SPDT, General-Purpose, CMOS Analog Switch
DG401	95NR 1-25	Improved, Dual, High-Speed Analog Switch (see MAX301)
DG403	95NR 1-25	Improved, Dual, High-Speed Analog Switch (see MAX303)
DG405	95NR 1-25	Improved, Dual, High-Speed Analog Switch (see MAX305)
DG406	95NR 1-29	Improved,16-Channel, High-Performance CMOS Multiplexer (see MAX306)
DG407	95NR 1-29	Improved, Dual, 8-Channel, High-Performance CMOS Multiplexer (see MAX307)
DG408	93NR 1-31	Improved, 8-Channel, High-Performance CMOS Multiplexer (see MAX308)
DG409	93NR 1-31	Improved, Dual, 4-Channel, High-Performance CMOS Multiplexer (see MAX309)
DG411	DS 1-135	Improved, Quad SPST Analog Switch (see MAX351)
DG412	DS 1-135	Improved, Quad SPST Analog Switch (see MAX352)
DG413	DS 1-135	Improved, Quad SPST Analog Switch (see MAX353)
DG417	95NR 1-139	Improved, SPST, Precision, CMOS Analog Switch (see MAX317)
DG418	95NR 1-139	Improved, SPST, Precision, CMOS Analog Switch (see MAX318)
DG419	95NR 1-139	Improved, SPDT, Precision, CMOS Analog Switch (see MAX319)
DG421	95NR 1-143	Improved, Low On Resistance, CMOS Analog Switch
DG423	95NR 1-143	Improved, Low On Resistance, CMOS Analog Switch
DG425	95NR 1-143	Improved, Low On Resistance, CMOS Analog Switch with Latches
DG441	95NR 1-147	Improved, Quad SPST Analog Switch (see MAX361)
DG442	95NR 1-147	Improved, Quad SPST Analog Switch (see MAX362)
DG444	95NR 1-151	Improved, Quad SPST Analog Switch (see MAX364)
DG445	95NR 1-151	Improved, Quad SPST Analog Switch (see MAX365)
DG506A	MAXFAX	16-Channel CMOS Multiplexer
DG507A	MAXFAX	Differential, 8-Channel CMOS Multiplexer

Part #	Publication/Doc. Page	Description
DG508A	MAXFAX	8-Channel CMOS Multiplexer (see MAX338)
DG509A	MAXFAX	Differential, 4-Channel CMOS Multiplexer (see MAX339)
DG528	MAXFAX	8-Channel, Latchable Multiplexer
DG529	MAXFAX	Differential, 4-Channel, Latchable Multiplexer
HI-201	MAXFAX	Quad SPST, CMOS Analog Switch (see MAX351)
HI-201HS	DS	High-Speed, Quad SPST, CMOS Analog Switch
HI-508A	92NR 1-25	Fault-Protected, 8-Channel Multiplexer (see MAX358)
HI-509A	92NR 1-25	Fault-Protected, Differential 4-Channel Multiplexer (see MAX359)
ICL7106	MAXFAX	3 1/2-Digit ADC with Direct LCD Drivers
ICL7107	MAXFAX	3 1/2-Digit ADC with Direct LCD Drivers
ICL7109	MAXFAX	12-Bit ADC with Three-State Binary Outputs
ICL7116	MAXFAX	3 1/2-Digit ADC with Direct LCD Display Hold
ICL7117	MAXFAX	3 1/2-Digit ADC with Direct LED Display Hold
ICL7126	MAXFAX	Low-Power, 3 1/2-Digit ADC with Direct LCD Drivers
ICL7129A	MAXFAX	Low-Noise, 4 1/2-Digit Single-Chip ADC with Multiplexed LCD Drivers
ICL7135	MAXFAX	4 1/2-Digit ADC with Multiplexed BCD Outputs
ICL7136	MAXFAX	Low-Power, 3 1/2-Digit ADC with Direct LCD Drivers
ICL7137	MAXFAX	Low-Power, 3 1/2-Digit ADC with Direct LED Drivers
ICL7611	MAXFAX	Low-Power Op Amp
ICL7612	MAXFAX	Low-Power Op Amp
ICL7614	MAXFAX	Low-Power Op Amp
ICL7616	MAXFAX	Low-Power Op Amp
ICL7621	MAXFAX	Dual, Low-Power Op Amp
ICL7622	MAXFAX	Dual, Low-Power Op Amp
ICL7631	MAXFAX	Triple, Low-Power Op Amp
ICL7632	MAXFAX	Triple, Low-Power Op Amp
ICL7641	MAXFAX	Quad, Low-Power Op Amp
ICL7642	MAXFAX	Quad, Low-Power Op Amp
ICL7650/B	MAXFAX	Chopper-Stabilized Op Amp
ICL7652/B	MAXFAX	Chopper-Stabilized Op Amp
ICL7660	93NR 4-141	10µA Charge-Pump Voltage Converter (see MAX660, MAX860/861)
ICL7662	MAXFAX	CMOS Switched-Capacitor Voltage Converter (Up to 20V Input)
ICL7663	MAXFAX	Low-Power, Adjustable-Output, Positive Voltage Linear Regulator (see MAX667)
ICL7664	MAXFAX	Low-Power, Adjustable-Output, Negative Voltage Linear Regulator
ICL7665	MAXFAX	Dual, Low-Power Under/Over-Voltage Detector
ICL7667	MAXFAX	Dual Power MOSFET Driver (Inverting) (see MAX626)
ICL8069	MAXFAX	1.2V Voltage Reference
ICM7211	MAXFAX	4-Digit, LCD Decoder/Driver
ICM7212	MAXFAX	4-Digit, LED Decoder/Driver
ICM7217	MAXFAX	4-Digit, Presetable, LED Up/Down Counter
ICM7218	MAXFAX	8-Digit, Multiplexed, LED Decoder/Driver
ICM7224	MAXFAX	4 1/2-Digit, LCD, High-Speed Counter/Decoder/Driver
ICM7225	MAXFAX	4 1/2-Digit, LED, High-Speed Counter/Decoder/Driver
ICM7228	MAXFAX	8-Digit, LED Display Driver
ICM7240	MAXFAX	8-Bit Binary, Programmable, RC Timer/Counter
ICM7242	MAXFAX	7-Bit Binary, Fixed, RC Timer/Counter

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A Complete Product Listing

Part #	Publication/Doc. Page	Description
ICM7250	MAXFAX	Two-Digit BCD, Programmable, RC Timer/Counter
ICM7260	MAXFAX	Module-60, Programmable, RC Timer/Counter
ICM7555	MAXFAX	Low-Power, General-Purpose Timer
ICM7556	MAXFAX	Low-Power, General-Purpose Dual Timer
IH5040	MAXFAX	SPST, Normally Open CMOS Analog Switch
IH5041	MAXFAX	Dual SPST, Normally Open CMOS Analog Switch (see MAX301)
IH5042	MAXFAX	SPDT CMOS Analog Switch
IH5043	MAXFAX	Dual SPDT CMOS Analog Switch (see MAX303)
IH5044	MAXFAX	DPST, Normally Open CMOS Analog Switch
IH5045	MAXFAX	Dual DPST, Normally Open CMOS Analog Switch (see MAX305)
IH5047	MAXFAX	SPST, 5Ω, High-Level CMOS Analog Switch
IH5048	MAXFAX	Dual SPST, Low Charge Injection Analog Switch
IH5048A	MAXFAX	Dual SPST, Low On Resistance, Low Charge Injection Analog Switch
IH5049	MAXFAX	Dual DPST, Low Charge Injection Analog Switch (see MAX305)
IH5050	MAXFAX	SPDT, Low Charge Injection Analog Switch
IH5051	MAXFAX	Dual SPDT, Low Charge Injection Analog Switch (see MAX303)
IH5108	92NR 1-25	See MAX358
IH5140	MAXFAX	Low-Power, SPST Fast, CMOS Analog Switch
IH5141	MAXFAX	Low-Power, Dual Fast, SPST CMOS Analog Switch (see MAX301)
IH5142	MAXFAX	SPDT, Low-Power, Fast CMOS Analog Switch
IH5143	MAXFAX	Dual SPDT, Low-Power, Fast CMOS Analog Switch (see MAX303)
IH5144	MAXFAX	DPST, Low-Power, Fast CMOS Analog Switch
IH5145	MAXFAX	Dual DPST, Low-Power, Fast CMOS Analog Switch (see MAX305)
IH5208	92NR 1-25	See MAX359
IH5341	MAXFAX	Dual SPST, RF/Video Switch
IH5352	MAXFAX	Quad SPST, RF/Video Switch
IH6108	MAXFAX	See DG508A
IH6116	MAXFAX	See DG506A
IH6208	MAXFAX	See DG509A
IH6216	MAXFAX	See DG507A
LH0033/A	MAXFAX	Fast Buffer Amplifier
LH0063	MAXFAX	Very Fast Buffer Amplifier
LH0101	MAXFAX	Power Op Amp
MAX038	95NR 10-3	High-Frequency Waveform Generator
MAX100	95NR 7-9*	250Msps, 8-Bit ADC with Track/Hold
MAX101	95NR 7-11*	500Msps, 8-Bit ADC with Track/Hold
MAX1044	93NR 4-141	10µA Charge-Pump Voltage Converter (see MAX860/861)
MAX110	95NR 7-13*	±5V, Low-Cost, 2-Channel, ±14-Bit Serial ADC
MAX110EVKIT	DS	Evaluation Kit for MAX110
MAX111	95NR 7-13*	Single, 5V, Low-Cost, 2-Channel, ±14-Bit Serial ADC
MAX120	DS	500ksps, 12-Bit Sampling ADC with Track/Hold and Reference
MAX120EVKIT	DS	Evaluation Kit for MAX120
MAX121	DS	308ksps ADC with DSP Interface and 78dB SINAD
MAX121EVKIT	DS	Evaluation Kit for MAX121
MAX122	95NR 7-15	333ksps, 12-Bit Sampling ADC with Track/Hold and Reference
MAX1232	92NR 5-11	µP Monitor

*Advance Information–first page of data sheet in preparation.

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DS – Individual Data Sheet

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A Complete Product Listing

Part #	Publication/Doc. Page	Description
MAX1259	92NR 5-17	Battery Manager
MAX130	MAXFAX	3 1/2-Digit ADC with Bandgap Reference
MAX131	MAXFAX	3 1/2-Digit ADC with Bandgap Reference
MAX132	93NR 7-15	±18-Bit, Low-Power ADC with Serial Interface
MAX132EVKIT	DS	Evaluation Kit for MAX132
MAX133	MAXFAX	9V, 3 3/4-Digit DMM Circuit
MAX134	MAXFAX	±5V, 3 3/4-Digit DMM Circuit
MAX134EVBRD	DS	PC-Based Evaluation System for MAX134
MAX135	93NR 7-15	±15-Bit, Low-Power ADC with Parallel Interface
MAX136	MAXFAX	Low-Power, 3 1/2-Digit ADC with Display Hold and Direct LCD Drivers
MAX138	MAXFAX	3 1/2-Digit ADC with Reference, Charge-Pump and Direct LED Drivers
MAX139	MAXFAX	3 1/2-Digit ADC with Reference, Charge-Pump and Direct LCD Drivers
MAX140	MAXFAX	3 1/2-Digit ADC with Reference, Charge-Pump and Low-Current LED Drivers
MAX1480A	95NR 2-7*	Complete, 2.5Mbps, Isolated RS-485/RS-422 Data Interface
MAX1480B	95NR 2-7	Complete, 250kbps, Isolated RS-485/RS-422 Data Interface
MAX150	MAXFAX	CMOS, 1.3µs, 8-Bit ADC with Voltage Reference and Track/Hold
MAX151	92NR 7-21	300kHz, 10-Bit ADC with Reference and Track/Hold
MAX152	DS	3V, 8-Bit ADC with 1µA Power-Down
MAX152EVKIT	DS	Evaluation Kit for MAX152
MAX153	DS	1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down
MAX154	DS	CMOS, 2µs, 8-Bit ADC with 4-Channel Mux, Track/Hold and Reference
MAX155	93NR 7-33	High-Speed, 8-Bit ADC with 8 Simultaneous Track/Hold and Reference
MAX155EVKIT	DS	Evaluation Kit for MAX155
MAX156	93NR 7-33	High-Speed, 8-Bit ADC with 4 Simultaneous Track/Hold and Reference
MAX158	DS	CMOS, 2.0µs, 8-Bit ADC with 8-Channel Mux, Track/Hold and Reference
MAX160	MAXFAX	CMOS, µP-Compatible, 4µs 8-Bit ADC
MAX161	MAXFAX	CMOS, 20µs, 8-Bit, 8-Channel Data Acquisition System
MAX162	92NR 7-37	CMOS, 3µs, 12-Bit ADC with Reference
MAX163	92NR 7-53	CMOS, 5V Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX164	92NR 7-53	CMOS, 5V Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX1649	95NR 4-11*	5V/3.3V/Adjustable, High-Efficiency, Low Dropout, Step-Down DC-DC Controller
MAX165	93NR 7-53	5µs, 8-Bit ADC with Track/Hold and Reference
MAX1651	95NR 4-11*	5V/3.3V/Adjustable, High-Efficiency, Low Dropout, Step-Down DC-DC Controller
MAX166	93NR 7-53	Differential Input, 5µs, 8-Bit ADC with Track/Hold and Reference
MAX167	92NR 7-53	CMOS, ±2.5V Input, 100ksps 12-Bit ADC with Track/Hold and Reference
MAX168	93NR 7-65	14-Bit, 250ksps ADC with Track/Hold and Voltage Reference
MAX1691	95NR 5-7*	Integrated Microprocessor Supervisory Module with Lithium Backup Battery
MAX170	MAXFAX	Serial-Output, 5.6µs, 12-Bit ADC with Reference (see MAX176)
MAX171	92NR 7-67	Opto-Isolated, Serial-Output, 5.8µs 12-Bit ADC (see MAX176)
MAX172	92NR 7-77	CMOS, 10µs, 12-Bit ADC with Voltage Reference (see MAX120)
MAX173	MAXFAX	CMOS, 5µs, 10-Bit ADC with Voltage Reference
MAX1732	94NR 4-15	12V, 120mA Flash Memory Programmer Module
MAX1738	94NR 4-23	5V, 500mA, Step-Down DC-DC Converter Module
MAX174	DS	Industry-Standard, 12-Bit ADC with Voltage Reference

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A Complete Product Listing

Part #	Publication/Doc. Page	Description
MAX1743	94NR 4-27	3W, 5 to ±12V/±15V DC-DC Converter Module
MAX176	94NR 7-73	Serial-Output, 250ksps, 12-Bit ADC with Track/Hold and Reference
MAX176EVKIT	DS	Evaluation Kit for MAX176
MAX177	MAXFAX	CMOS, 12-Bit ADC with Track/Hold and Reference
MAX1771	95NR 4-13	12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller
MAX178	92NR 7-99	Calibrated, 12-Bit ADC with Track/Hold and Reference
MAX180	92NR 7-111	Complete, 100ksps, 8-Channel, 12-Bit Data Acquisition System
MAX180EVKIT	DS	Evaluation Kit for MAX180
MAX181	92NR 7-111	Complete, 100ksps, 6-Channel, 12-Bit Data Acquisition System
MAX182	92NR 7-131	Calibrated, 4-Channel, 12-Bit ADC with Track/Hold and Reference
MAX183	92NR 7-143	3µs, 12-Bit ADC (see MAX120)
MAX184	92NR 7-143	5µs, 12-Bit ADC (see MAX120)
MAX185	92NR 7-143	10µs, 12-Bit ADC (see MAX120)
MAX186	DS	Low-Power, 8-Channel, 133ksps, 12-Bit Serial ADC with Track/Hold Reference
MAX186EVKIT	DS	Evaluation Kit for MAX186
MAX187	95NR 7-43	Low-Power, 12-Bit Serial ADC with Track/Hold and Reference (8-Pin)
MAX187EVKIT	DS	Evaluation Kit for MAX187
MAX188	DS	Low-Power, 8-Channel, 133ksps, 12-Bit Serial ADC with Track/Hold Reference
MAX189	95NR 7-43	Low-Power, 12-Bit Serial ADC with Track/Hold and Reference (8-Pin)
MAX190	DS	12-Bit, 75ksps, 5V ADC with Track/Hold and Reference (see MAX191)
MAX190EVKIT	DS	Evaluation Kit for MAX190 (see MAX191EVKIT)
MAX191	DS	Low-Power, 12-Bit, Sampling ADC with Internal Reference and Power-Down
MAX191EVKIT	DS	Evaluation Kit for MAX191
MAX192	95NR 7-61	Low-Power, 8-Channel, Serial 10-Bit ADC
MAX195	95NR 7-85*	16-Bit, Self-Calibrating, 10µs Sampling ADC
MAX195EVKIT	DS	Evaluation Kit for MAX195
MAX200	95NR 2-23	5V, 5-Channel RS-232 Transmitter with 0.1µf External Capacitors
MAX201	95NR 2-23	5V/9V to 13.2V, Dual RS-232 Transceiver with 0.1µf External Capacitors
MAX202	95NR 2-23	5V, Dual RS-232 Transceiver with 0.1µf External Capacitors
MAX202E	95NR 2-43	±15kV ESD-Protected, +5V RS-232 Transceiver
MAX203	95NR 2-23	Complete, 5V Powered, Dual RS-232 Transceiver
MAX204	95NR 2-23	5V, Quad RS-232 Transmitter with 0.1µf External Capacitors
MAX205	95NR 2-23	Complete, 5V, 5-Channel RS-232 Transceiver
MAX206	95NR 2-23	5V RS-232 Transceiver with 0.1µf External Capacitors
MAX207	95NR 2-23	5V RS-232 Transceiver with 0.1µf External Capacitors
MAX208	95NR 2-23	5V Quad RS-232 Transceiver with 0.1µf External Capacitors
MAX209	95NR 2-23	5V RS-232 Transceiver with 0.1µf External Capacitors
MAX2101	95NR 10-23*	6-Bit Quadrature Digitizer
MAX211	95NR 2-23	5V RS-232 Transceiver with 0.1µf External Capacitors
MAX211E	95NR 2-43	±15kV ESD-Protected, +5V RS-232 Transceiver
MAX212	95NR 2-57	True 3V, 3 Drivers/5 Receivers RS-232 Serial Port
MAX212EVKITSO	DS	Evaluation Kit for MAX212
MAX213	95NR 2-23	5V, RS-232 Transceiver with 0.1µf External Capacitors
MAX213E	95NR 2-43	±15kV ESD-Protected, +5V RS-232 Transceiver
MAX214	95NR 2-65	5V, Programmable, DTE/DCE RS-232 Transceiver
MAX216	94NR 2-45	Low-Power, Appletalk® Interface Transceiver

*Advance Information–first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX218	95NR 2-77	1.8V to 4.25V VIN, Dual RS-232 Transceiver
MAX220	95NR 2-85	Low-Power, 5V, Dual RS-232 Drivers/Receivers
MAX222	95NR 2-85	High-Speed, 5V, Dual RS-232 Drivers/Receivers with Shutdown
MAX223	95NR 2-85	5V, RS-232 Transceiver with 2 Receivers Active in Shutdown
MAX225	DS	Complete, 5V RS-232 Transceiver with 5 Transmitters and Receivers
MAX230	95NR 2-85	5V, 5 RS-232 Transmitters with Power Shutdown
MAX231	95NR 2-85	5V/12V, Dual RS-232 Transmitters and Receivers
MAX232	95NR 2-85	5V, Dual RS-232 Transmitters and Receivers
MAX232A	95NR 2-85	High-Speed, 5V, Dual RS-232 Transmitters and Receivers
MAX232E	95NR 2-43	±15kV ESD-Protected, +5V RS-232 Transceiver
MAX233	95NR 2-85	No External Component, 5V, Dual RS-232 Transmitters and Receivers
MAX233A	95NR 2-85	High-Speed, No External Component, 5V, Dual RS-232 Transmitters and Receivers
MAX234	95NR 2-85	5V, Quad RS-232 Transmitters
MAX235	95NR 2-85	No External Component, 5V, 5 RS-232 Transmitters/Receivers with Power Shutdown
MAX236	95NR 2-85	5V, 4 RS-232 Transmitters and 3 Receivers with Power Shutdown
MAX237	95NR 2-85	5V, 5 RS-232 Transmitters and 3 Receivers
MAX238	95NR 2-85	5V, 4 RS-232 Transmitters and 4 Receivers
MAX239	95NR 2-85	5V/12V, 3 RS-232 Transmitters and 5 Receivers with Three-State Receiver Enable
MAX240	95NR 2-85	5V, 5 RS-232 Transmitters, 5 Receivers with Power Shutdown, Three-State Receiver
MAX241	95NR 2-85	5V, 4 RS-232 Transmitters, 5 Receivers with Power Shutdown, Three-State Receiver
MAX241E	95NR 2-43	±15kV ESD-Protected, +5V RS-232 Transceiver
MAX242	95NR 2-85	5V, High-Speed, Dual RS-232 Transceiver with Shutdown
MAX243	95NR 2-85	5V, High-Speed, Dual RS-232 Transceiver with Open-Line Detection
MAX244	95NR 2-85	5V, Multi-Channel RS-232 Drivers/Receivers
MAX245	95NR 2-85	5V, Multi-Channel RS-232 Drivers/Receivers
MAX246	95NR 2-85	5V, Multi-Channel RS-232 Drivers/Receivers
MAX247	95NR 2-85	5V, Multi-Channel RS-232 Drivers/Receivers
MAX248	95NR 2-85	5V, Multi-Channel RS-232 Drivers/Receivers
MAX249	95NR 2-85	5V, Multi-Channel RS-232 Drivers/Receivers
MAX250	92NR 2-57	5V, Isolated, RS-232 Drivers/Receivers
MAX251	92NR 2-57	5V, Isolated, RS-232 Drivers/Receivers
MAX252	92NR 2-69	Complete, 5V, Isolated, Dual RS-232 Transceiver Module
MAX253	95NR 2-121	Isolated RS-485 Power Driver
MAX260	92NR 6-13	µP-Programmable, Universal Switched-Capacitor Filter
MAX261	92NR 6-13	µP-Programmable, Universal Switched-Capacitor Filter
MAX262	92NR 6-13	µP-Programmable, Universal Switched-Capacitor Filter
MAX263	92NR 6-37	Pin-Programmable, Universal Switched-Capacitor Filter
MAX264	92NR 6-37	Pin-Programmable, Universal Switched-Capacitor Filter
MAX265	DS	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX266	DS	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX267	92NR 6-37	Pin-Programmable, Bandpass Switched-Capacitor Filter

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DS – Individual Data Sheet

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MAX268	92NR 6-37	Pin-Programmable, Bandpass Switched-Capacitor Filter
MAX270	92NR 6-61	Digitally Programmable, Dual, 2nd-Order Continuous Lowpass Filter
MAX271	92NR 6-61	Digitally Programmable, Dual, 2nd-Order Continuous Lowpass Filter with Track/Hold
MAX274	93NR 6-3	8th-Order, Continuous-Time Analog Filter
MAX274/5SOFT	94EV 2-3	Filter Design Software for MAX274/MAX275
MAX274EVKIT	94EV 2-3	Evaluation Kit for MAX274
MAX275	93NR 6-3	4th-Order, Continuous-Time Analog Filter
MAX280	DS	5th-Order, Zero-Error, Butterworth, Switched Capacitor Lowpass Filter
MAX281	92NR 6-91	5th-Order, Zero-Error, Bessel, Switched-Capacitor Lowpass Filter
MAX291	93NR 6-31	8th-Order Butterworth, Clock-Tunable, 100:1 Lowpass Filter
MAX292	93NR 6-31	8th-Order Bessel, Clock-Tunable, 100:1 Lowpass Filter
MAX293	93NR 6-39	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX294	93NR 6-39	8th-Order, Elliptic, 1.2 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX295	93NR 6-31	8th-Order, Butterworth, Clock-Tunable, 50:1 Lowpass Filter
MAX296	93NR 6-31	8th-Order, Bessel, Clock-Tunable, 50:1 Lowpass Filter
MAX297	93NR 6-39	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 50:1 Lowpass Filter
MAX301	95NR 1-9	Precision, Dual, SPST, High-Speed Analog Switch
MAX303	95NR 1-9	Precision, Dual, SPDT, High-Speed Analog Switch
MAX305	95NR 1-9	Precision, Dual, DPST, High-Speed Analog Switch
MAX306	95NR 1-17	16-Channel, High-Performance, CMOS Analog Multiplexer
MAX307	95NR 1-17	Dual 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX308	95NR 1-29	8-Channel, High-Performance, CMOS Analog Multiplexer
MAX309	95NR 1-29	Dual 4-Channel, High-Performance, CMOS Analog Multiplexer
MAX310	92NR 8-17	8-Channel, CMOS RF/Video Multiplexer
MAX311	92NR 8-17	Differential 4-Channel, CMOS RF/Video Multiplexer
MAX317	95NR 1-41	Precision, SPST, CMOS Analog Switch
MAX318	95NR 1-41	Precision, SPST, CMOS Analog Switch
MAX319	95NR 1-41	Precision, SPST, CMOS Analog Switch
MAX3212	95NR 2-137*	1µA, 2.7V, 3x5 RS-232 Serial Port
MAX3218	95NR 2-139*	1µA Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with Shutdown
MAX3222	95NR 2-141*	3V, True Dual RS-232 Transceiver with 0.1µF External Capacitors
MAX3223	95NR 2-143*	1µA, 3V RS-232 Dual Transceiver
MAX3232	95NR 2-141*	3V, Dual RS-232 Transceiver
MAX3241	95NR 2-145	3V to 5.5V, True RS-232 Transceiver Using Four 0.1µF Capacitors
MAX3243	95NR 2-143*	1µA, 3V, 3 Drivers/5 Receivers RS-232 Serial Port
MAX326	92NR 1-11	Quad SPST, Ultra-Low Leakage, CMOS Analog Switch
MAX3260	95NR 2-153*	622Mbps to 1Gbps Transimpedance Amplifier
MAX3261	95NR 2-155*	622Mbps to 1Gbps Laser Diode Driver
MAX3262	95NR 2-157*	622Mbps to 1Gbps Fiberoptic Post Amplifier
MAX327	92NR 1-11	Quad SPST, Ultra-Low Leakage, CMOS Analog Switch
MAX328	92NR 1-17	8-Channel, Ultra-Low Leakage, Monolithic CMOS Multiplexer
MAX329	92NR 1-17	Differential 4-Channel, Ultra-Low Leakage, Monolithic CMOS Multiplexer
MAX331	MAXFAX	Quad SPST, Normally Closed, CMOS Analog Switch
MAX332	MAXFAX	Quad SPST, Normally Open, CMOS Analog Switch
MAX333	MAXFAX	Quad SPDT, CMOS Analog Switch

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MAX333A	95NR 1-51	Improved, Quad, SPDT, CMOS Analog Switch
MAX334	MAXFAX	Quad SPST, High-Speed, Break-Before-Make Analog Switch
MAX335	95NR 1-59	Serial Controlled, 8-Channel SPST Analog Switch
MAX338	95NR 1-69	Low-Leakage, 8-Channel, CMOS Analog Multiplexer
MAX339	95NR 1-69	Low-Leakage, Dual 4-Channel, CMOS Analog Multiplexer
MAX341	MAXFAX	Dual SPST, High-Voltage, CMOS/DMOS Analog Switch
MAX343	MAXFAX	Dual SPDT, High-Voltage, CMOS/DMOS Analog Switch
MAX345	MAXFAX	Dual DPST, High-Voltage, CMOS/DMOS Analog Switch
MAX348	MAXFAX	Low On-Resistance, Dual SPST, High-Voltage, CMOS/DMOS Analog Switch
MAX351	95NR 1-81	Precision, Quad, SPST Analog Switch
MAX352	95NR 1-81	Precision, Quad, SPST Analog Switch
MAX353	95NR 1-81	Precision, Quad, Normally Closed SPST Analog Switch
MAX358	92NR 1-25	8-Channel, Fault-Protected Multiplexer
MAX359	92NR 1-25	Differential 4-Channel, Fault-Protected Multiplexer
MAX361	95NR 1-91	Precision, Quad SPST Analog Switch
MAX362	95NR 1-91	Precision, Quad SPST Analog Switch
MAX364	95NR 1-99	Precision, Quad SPST Analog Switch
MAX365	95NR 1-99	Precision, Quad SPST Analog Switch
MAX366	95NR 1-109*	Signal-Line Circuit Protector
MAX367	95NR 1-109*	Signal-Line Circuit Protector
MAX368	92NR 1-37	8-Channel, Fault-Protected, Latched Multiplexer
MAX369	92NR 1-37	Differential 4-Channel, Fault-Protected, Latched Multiplexer
MAX378	92NR 1-49	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX379	92NR 1-49	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX381	95NR 1-111*	Precision, Low-Voltage Analog Switch
MAX383	95NR 1-111*	Precision, Low-Voltage Analog Switch
MAX385	95NR 1-111*	Precision, Low-Voltage Analog Switch
MAX388	93NR 1-7	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX389	93NR 1-7	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX391	95NR 1-113	Low-Voltage, +5V/±5V Quad, CMOS Analog Switch
MAX392	95NR 1-113	Low-Voltage, +5V/±5V Quad, CMOS Analog Switch
MAX393	95NR 1-113	Low-Voltage, +5V/±5V Quad, CMOS Analog Switch
MAX398	95NR 1-123*	Low-Voltage, +5V/±5V, 8-Channel, CMOS Analog Multiplexer
MAX399	95NR 1-123*	Low-Voltage, +5V/±5V, Dual 4-Channel, CMOS Analog Multiplexer
MAX400	MAXFAX	Ultra-Low Offset Op Amp
MAX402	94NR 3-7	High-Speed, Low-Voltage, Micropower Op Amp
MAX403	94NR 3-7	Improved, Dual, High-Speed Analog Switch
MAX404	92NR 8-25	Video Op Amp
MAX405	92NR 8-29	Precision Video Buffer Amplifier
MAX406	94NR 3-19	1.2µA Max, Single-Supply Op Amp
MAX407	94NR 3-19	1.2µA Max, Dual, Single-Supply Op Amp
MAX408	DS	High-Speed, High Output Current Op Amp
MAX409	94NR 3-19	1.2µA Max, 150kHz, Single-Supply Op Amp
MAX410	94NR 3-33	Single, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX412	94NR 3-33	Dual, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX414	94NR 3-33	Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp

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MAX417	94NR 3-19	Dual, 1.2µA Max, Single-Supply Op Amp
MAX418	94NR 3-19	Quad, 1.2µA Max, Single-Supply Op Amp
MAX419	94NR 3-19	Quad, 1.2µA Max, Single-Supply Op Amp
MAX4193	92NR 4-45	CMOS, Micropower, Step-Up Switching Regulator
MAX420	MAXFAX	±15V Chopper-Stabilized Op Amp
MAX421	MAXFAX	±15V Chopper-Stabilized Op Amp
MAX422	MAXFAX	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX423	MAXFAX	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX427	94NR 3-45	Low-Noise, High-Precision Op Amp
MAX428	MAXFAX	Dual, High-Speed, High Output Current Op Amp
MAX430	MAXFAX	±15V Chopper-Stabilized Op Amp
MAX432	MAXFAX	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX435	94NR 8-5	250MHz Wideband Transconductance Amplifier with Differential Output
MAX436	94NR 8-5	250MHz Wideband Transconductance Amplifier with Single-Ended Output
MAX437	94NR 3-45	Low-Noise, High-Precision Op Amp
MAX438	94NR 3-7	High-Speed, Low-Voltage, Micropower Op Amp
MAX439	94NR 3-7	High-Speed, Low-Voltage, Micropower Op Amp
MAX4391	92NR 4-65	CMOS, Micropower, Inverting Switching Regulator
MAX440	93NR 8-5	8-Channel, High-Speed, Video Multiplexer/Amplifier
MAX441	93NR 8-5	4-Channel, High-Speed, Video Multiplexer/Amplifier
MAX442	93NR 8-17	2-Channel, 140 MHz, Video Multiplexer/Amplifier
MAX4420	94NR 4-31	High-Speed 6A MOSFET Driver (Non-inverting)
MAX4426	DS	Dual, High-Speed, 1.5A MOSFET Driver (Inverting)
MAX4427	DS	Dual, High-Speed, 1.5A MOSFET Driver (Non-inverting)
MAX4428	DS	Dual, High-Speed, 1.5A MOSFET Driver (Inverting & Non-inverting)
MAX4429	94NR 4-31	High-Speed, 6A MOSFET Driver (Inverting)
MAX445	95NR 8-5*	Low-Cost, High Resolution, Z-Axis Video Display Driver
MAX448	MAXFAX	Quad, High-Speed, High Output Current Op Amp
MAX450	MAXFAX	10MHz CMOS Video Amplifier
MAX451	MAXFAX	Low Bias Current, 10MHz Video Amplifier
MAX452	92NR 8-37	50MHz Video Amplifier
MAX453	92NR 8-37	2-Channel, 50MHz Video Multiplexer/Amplifier
MAX454	92NR 8-37	4-Channel, 50MHz Video Multiplexer/Amplifier
MAX455	92NR 8-37	8-Channel, 50MHz Video Multiplexer/Amplifier
MAX456	DS	8x8 Crosspoint Video Switch
MAX457	92NR 8-47	Dual 70MHz Video Amplifier
MAX458	95NR 8-7	8x4, 100MHz Video Crosspoint Switch with Buffers
MAX459	95NR 8-7	8x4, 90MHz Video Crosspoint Switch with AV = 2V/V Output Drivers
MAX459EVKit	DS	Evaluation Kit for MAX459
MAX460	MAXFAX	High-Accuracy Fast Buffer
MAX463	95NR 8-23	100MHz, Triple RGB Video Switch with Buffer
MAX464	95NR 8-23	100MHz, Quad RGB Video Switch with Buffer
MAX464EVKit	DS	Evaluation Kit for MAX464
MAX465	95NR 8-23	90MHz, Triple RGB Video Switch with AV=2V/V Buffer
MAX466	95NR 8-23	90MHz, Quad RGB Video Switch with AV=2V/V Buffer
MAX466EVKit	DS	Evaluation Kit for MAX466

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MAX467	95NR 8-23	100MHz, Triple (RGB) Video Buffer
MAX468	95NR 8-23	100MHz, Quad Video Buffer
MAX469	95NR 8-23	90MHz, Triple RGB Video Buffer (AV=2V/V)
MAX470	95NR 8-23	90MHz, Quad Video Buffer (AV=2V/V)
MAX471	95NR 3-9*	Precision, Low-Power Current-Sense Amplifier with Internal Sense Resistor
MAX472	95NR 3-9*	Precision, Low-Power, High Side Current-Sense Amplifier
MAX473	95NR 3-11	Single, 10MHz Single-Supply Op Amp
MAX474	95NR 3-11	Dual, 10MHz Single-Supply Op Amp
MAX475	95NR 3-11	Quad, 10MHz Single-Supply Op Amp
MAX476	95NR 8-39*	425MHz Ultra High-Speed Video Amplifier
MAX477	95NR 8-39*	425MHz Ultra High-Speed Video Buffer
MAX478	94NR 3-59	17µA Max, Dual, Single-Supply Precision Op Amp
MAX479	94NR 3-59	17µA Max, Quad, Single-Supply Precision Op Amp
MAX480	92NR 3-47	High-Precision, Low-Voltage, Micropower Op Amp
MAX481	95NR 2-159	500µA RS-485 Transceiver with Low-Power Shutdown
MAX483	95NR 2-159	Slew-Rate Limited, 350µA RS-485 Transceiver with Low-Power Shutdown
MAX485	95NR 2-159	500µA RS-485 Transceiver—Direct LTC485 Replacement
MAX487	95NR 2-159	Slew-Rated Limited, 350µA RS-485 Transceiver with 1/4-Unit Load
MAX488	95NR 2-159	Slew-Rated Limited, 350µA Full-Duplex RS-485 Transceiver
MAX489	95NR 2-159	Slew-Rated Limited, 350µA Full-Duplex RS-485 Transceiver
MAX490	95NR 2-159	500µA Full-Duplex RS-485 Transceiver
MAX491	95NR 2-159	500µA Full-Duplex RS-485 Transceiver
MAX492	95NR 3-23	Dual, Micropower, Single-Supply Rail-to-Rail Op Amp
MAX494	95NR 3-23	Quad, Micropower, Single-Supply Rail-to-Rail Op Amp
MAX495	95NR 3-23	Single, Micropower, Single-Supply Rail-to-Rail Op Amp
MAX500	MAXFAX	CMOS, Quad, Serial 8-Bit DAC
MAX501	93NR 9-5	Voltage-Output, 12-Bit Multiplying DAC with 8+4 Interface
MAX502	93NR 9-5	Voltage-Output, 12-Bit Multiplying DAC with 12-Bit Interface
MAX503	95NR 9-107*	5V, Low-Power. Parallel-Input, Voltage-Output 10-Bit DAC
MAX504	95NR 9-109*	5V, Low-Power, Voltage-Output, Serial 10-Bit DAC
MAX505	DS	Quad 8-Bit DACs with Rail-to-Rail Outputs
MAX506	DS	Quad 8-Bit DACs with Rail-to-Rail Output
MAX507	93NR 9-33	Voltage-Output 12-Bit DAC with Internal Reference and 12-Bit Interface
MAX508	93NR 9-33	Voltage-Output 12-Bit DAC with Internal Reference and 8+4 Interface
MAX509	DS	Quad, Serial 8-Bit DAC with Rail-to-Rail Outputs
MAX510	DS	Quad, Serial 8-Bit DAC with Rail-to-Rail Outputs
MAX512	95NR 9-7	5V, Triple, 8-Bit Voltage-Output DAC with Serial Interface
MAX513	95NR 9-7	3V, Triple Voltage-Output DAC with Serial Interface
MAX514	93NR 9-45	Quad, CMOS, 12-Bit, Serial Multiplying DAC
MAX515	95NR 9-109*	5V, Low-Power, Voltage-Output, Serial 10-Bit DAC in an 8-Pin SSOP
MAX516	92NR 9-21	Quad, DAC-Programmed, CMOS Comparator
MAX526	93NR 9-53	Calibrated, Quad, 12-Bit, CMOS Voltage-Output DAC
MAX527	93NR 9-53	±5V, Calibrated, Quad, 12-Bit Voltage-Output DAC
MAX528	93NR 9-69	Octal, 8-Bit Serial DAC with Output Buffers
MAX529	93NR 9-69	±5V, Octal, 8-Bit Serial DAC with Output Buffers
MAX530	95NR 9-23	5V, Low-Power, Voltage-Output, Parallel 12-Bit DAC with Reference

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MAX531	95NR 9-39	5V, Low-Power, Voltage-Output, Serial 12-Bit DAC with Reference
MAX532	95NR 9-53	Dual, Serial-Input, Voltage-Output, 12-Bit Multiplying DAC
MAX536	95NR 9-67	Quad, Serial, Voltage-Output, -5V/12V/15V 12-Bit DAC
MAX537	95NR 9-67	Quad, Serial, Voltage-Output, ±5V 12-Bit DAC
MAX538	95NR 9-39	5V, Low-Power, Voltage-Output, Serial 12-Bit DAC, 0-2.5V Output
MAX539	95NR 9-39	5V, Low-Power, Voltage-Output, Serial 12-Bit DAC, 0-2.5V Output
MAX543	DS	12-Bit, Serial, CMOS Multiplying DAC in 8-Pin Package
MAX547	95NR 9-91	Octal, 13-Bit Voltage-Output DAC with Parallel Interface
MAX555	95NR 9-105*	250MHz, 12-Bit Multiplying DAC with Complementary Voltage Output
MAX560	93NR 2-53	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX561	93NR 2-53	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX562	95NR 2-175	2.7V to 5.25V, High-Speed RS-232 Serial Port
MAX563	95NR 2-183	3.3V, Dual EIA/TIA-562 Transceiver
MAX600	MAXFAX	Low-Cost AC-DC Regulator (110/220VAC to 5VDC—Full Wave) (see MAX610)
MAX601	MAXFAX	Low-Cost AC-DC Regulator (110/220VAC to 5VDC—Half Wave) (see MAX611)
MAX602	MAXFAX	Low-Cost AC-DC Regulator (8V RMS to 5VDC—Full Wave) (see MAX612)
MAX603	95NR 4-29*	5V/Adjustable, 500mA, P-Channel LDO Linear Regulator
MAX604	95NR 4-29*	3.3V/Adjustable, 500mA, P-Channel LDO Linear Regulator
MAX610	MAXFAX	AC-DC Regulator (110/220VAC to 5VDC—Full Wave)
MAX611	MAXFAX	AC-DC Regulator (110/220VAC to 5VDC—Half Wave)
MAX612	MAXFAX	AC-DC Regulator (8V RMS to 5VDC—Full Wave)
MAX613	95NR 4-31	Dual-Slot PCMCIA Analog Power Controller
MAX614	95NR 4-31	Dual-Slot PCMCIA Analog Power Controller
MAX619	95NR 4-39	Regulated 5V Charge-Pump DC-DC Converter
MAX619EVKIT	DS	Regulated 5V Charge-Pump DC-DC Converter
MAX620	DS	Quad, High-Side MOSFET Driver
MAX621	DS	Quad, High-Side MOSFET Driver with Internal Capacitors
MAX622	92NR 4-31	High-Side Power Supply
MAX623	92NR 4-31	High-Side Power Supply with Internal Capacitors
MAX625	93NR 4-7	Quad, High-Side Power Switch with Internal FETs and Capacitors
MAX626	DS	Dual-Power MOSFET Driver (Inverting)
MAX627	DS	Dual-Power MOSFET Driver (Non-inverting)
MAX628	DS	Dual-Power MOSFET Driver (Inverting & Non-inverting)
MAX630	92NR 4-45	CMOS, Micropower, Step-Up Switching Regulator (see MAX756/856)
MAX631	92NR 4-57	5V/Adjustable, Step-Up Switching Regulator (see MAX756/856)
MAX632	92NR 4-57	12V/Adjustable, CMOS, Step-Up Switching Regulator (see MAX756/856)
MAX633	92NR 4-57	15V/Adjustable, CMOS, Step-Up Switching Regulator (see MAX756/856)
MAX634	92NR 4-65	CMOS, Micropower, Inverting Switching Regulator
MAX635	92NR 4-77	-5V/Adjustable, CMOS, Inverting Switching Regulator (see MAX764/765/766)
MAX636	92NR 4-77	-12V/Adjustable, CMOS, Inverting Switching Regulator (see MAX764/765/766)
MAX637	92NR 4-77	-15V/Adjustable, CMOS, Inverting Switching Regulator (see MAX764/765/766)
MAX638	92NR 4-85	5V/Adjustable, CMOS, Step-Down Switching Regulator (see MAX639)
MAX639	95NR 4-47	5V/Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Converter
MAX639EVKIT	DS	Evaluation Kit for MAX639
MAX640	95NR 4-47	3.3V/Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Converter

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MAX641	92NR 4-93	5V/Adjustable, 10W, CMOS, Step-up, Switching Regulator Controller (see MAX1771)
MAX642	92NR 4-93	12V/Adjustable, 10W, CMOS, Step-up, Switching Regulator Controller (see MAX1771)
MAX643	92NR 4-93	15V/Adjustable, 10W, CMOS, Step-up, Switching Regulator Controller (see MAX1771)
MAX644		Replaced by MAX654
MAX645		Replaced by MAX655
MAX646		Replaced by MAX656
MAX647		Replaced by MAX657
MAX649	95NR 4-59	5V/Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controller (see MAX1649)
MAX649EVKIT	DS	Evaluation Kit for the MAX649/651/652
MAX650	MAXFAX	-48V Input to 5V Switching DC-DC Converter (see MAX773)
MAX651	95NR 4-59	3.3V/Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controller (see MAX1651)
MAX652	95NR 4-59	3V/Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controller (see MAX1651)
MAX653	95NR 4-47	3V/Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Converter
MAX654	92NR 4-105	Low-Voltage, 5V Step-Up DC-DC Converter (see MAX777/778/779)
MAX655	92NR 4-105	Low-Voltage, 5V Step-Up DC-DC Converter (see MAX777/778/779)
MAX655EVKIT	DS	Evaluation Kit For MAX655
MAX656	DS	Low-Voltage, 5V Step-Up DC-DC Converter with External FET (see MAX777/778/779)
MAX657	92NR 4-105	Low-Voltage, 3V Step-Up DC-DC Converter (see MAX777/778/779)
MAX658	92NR 4-105	Low-Voltage, 5V Step-Up DC-DC Converter with External FET (see MAX777/778/779)
MAX660	92NR 4-117	100mA, Charge-Pump Voltage Converter
MAX661		Replaced by MAX662
MAX662	94NR 4-43	12V, 30mA Flash Memory Programming Supply Charge Pump (see MAX662A)
MAX662A	95NR 4-75	12V, 30mA Flash Memory Programming Supply
MAX662EVKIT	DS	Evaluation Kit for MAX662
MAX663	92NR 4-125	CMOS, 5V/Adjustable, Micropower, Positive Linear Regulator (see MAX667)
MAX664	92NR 4-125	CMOS, -5V/Adjustable, Micropower, Negative Linear Regulator
MAX665	93NR 4-25	100mA, 1.5 to 8V, CMOS, Switched-Capacitor Voltage Converter
MAX666	92NR 4-125	5V/Adj, Micropower, Positive Linear Regulator with Low-Battery Detect (see MAX667)
MAX667	DS	5V/Adjustable, Low-Dropout Linear Voltage Regulator (see MAX603/604, MAX882/883/884)
MAX670	MAXFAX	Precision, 10V Kelvin-Sensed Reference -3 ppm/°C
MAX671	MAXFAX	Precision, 10V Kelvin-Sensed Reference -1 ppm/°C
MAX672		Replaced by MAX674
MAX673		Replaced by MAX675
MAX674	92NR 3-1	Precision 10V Voltage Reference
MAX675	92NR 3-5	Precision 5V Voltage Reference
MAX676	95NR 6-5*	Calibrated, Low-Drift, 4.096V Precision Voltage Reference

*Advance Information–first page of data sheet in preparation.

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MAX677	95NR 6-5*	Calibrated, Low-Drift, 5V Precision Voltage Reference
MAX678	95NR 6-5*	Calibrated, Low-Drift, 10V Precision Voltage Reference
MAX680	92NR 4-141	5V to ±10V, Switched-Capacitor Voltage Converter
MAX681	92NR 4-141	5V to ±10V, Switched-Capacitor Voltage Converter with Internal Capacitors
MAX687	95NR 4-81*	3V, High-Accuracy Linear-Regulator Controller for Portable Phones
MAX688	95NR 4-81*	3.3V, High-Accuracy Linear-Regulator Controller for Portable Phones
MAX689	95NR 4-81*	3V, High-Accuracy Linear-Regulator Controller for Portable Phones
MAX690	DS	Reset with Watchdog and Battery Switchover (see MAX690A)
MAX690A	95NR 5-9	Reset with Watchdog and Battery Switchover
MAX690R/S/T	95NR 5-19	Reset with Watchdog and Battery Switchover
MAX691	DS	µP Watchdog/Battery Switchover/Reset Generator (see MAX691A)
MAX691A	95NR 5-31	Reset with Watchdog, Chip Enable, and Battery Backup
MAX692	DS	µP Watchdog/Battery Switchover/Reset Generator (see MAX692A)
MAX692A	95NR 5-7	Reset with Watchdog and Battery Switchover
MAX693	DS	µP Watchdog/Battery Switchover/Reset Generator (see MAX693A)
MAX693A	DS	Reset with Watchdog, Chip Enable, and Battery Backup
MAX694	DS	µP Watchdog/Battery Switchover/Reset Generator (see MAX690A)
MAX695	DS	µP Watchdog/Battery Switchover/Reset Generator (see MAX691A)
MAX696	92NR 5-33	µP Supervisory Circuit/Battery Switchover/Programmable Reset
MAX697	92NR 5-33	µP Supervisory Circuit/Programmable Reset
MAX698	92NR 5-45	Low-Cost Power-On Reset (see MAX707)
MAX699	92NR 5-45	Low-Cost Power-On Reset and Watchdog Controller (see MAX705)
MAX700	92NR 5-49	Adjustable-Threshold Power-Supply Monitor with Reset
MAX701	92NR 5-49	Power-Supply Monitor with Reset (see MAX707)
MAX702	92NR 5-49	Power-Supply Monitor with Reset (see MAX709)
MAX703	94NR 5-35	Reset with Battery Backup
MAX704	94NR 5-35	Reset with Battery Backup
MAX704R/S/T	95NR 5-19	3V Reset with Battery Backup
MAX705	95NR 5-47	Reset with Watchdog
MAX706	95NR 5-47	Reset with Watchdog
MAX706P/R/S/T	95NR 5-57	3V Reset with Watchdog
MAX707	95NR 5-47	Reset with Power-Fail Warning
MAX708	95NR 5-47	Reset with Power-Fail Warning
MAX708R/S/T	95NR 5-57	3V Reset with Power-Fail Warning
MAX709L	94NR 5-67	Power-Supply Monitor with 4.65V Reset Threshold
MAX709M	94NR 5-67	Power-Supply Monitor with 4.40V Reset Threshold
MAX709R	94NR 5-67	Power-Supply Monitor with 2.63V Reset Threshold
MAX709S	94NR 5-67	Power-Supply Monitor with 2.93V Reset Threshold
MAX709T	94NR 5-67	Power-Supply Monitor with 3.08V Reset Threshold
MAX712	94NR 4-51	Battery Fast-Charge Controller (NiMH)
MAX712EVKIT	DS	Evaluation Kit for MAX712
MAX713	94NR 4-51	Battery Fast-Charge Controller (NiMH)
MAX714	93NR 4-35	3-Output, Battery-Powered Supply System
MAX715	93NR 4-35	6-Output, Battery-Powered Supply System
MAX716	93NR 4-35	7-Output, Battery-Powered Supply System
MAX716EVKIT	DS	Evaluation Kit for MAX716

*Advance Information–first page of data sheet in preparation.

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Part #	Publication/Doc. Page	Description
MAX717	94NR 4-67	3.3V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718	94NR 4-67	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718EVKIT	DS	Evaluation Kit for MAX718
MAX719	94NR 4-67	3.0/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX720	94NR 4-67	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX721	94NR 4-67	3.0/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX7219	DS	Serially Interfaced, 8-Digit, LED Display Driver
MAX722	93NR 4-49	3.3/5V Palmtop Computer and LCD Power-Supply Regulator
MAX722EVKIT	93NR 4-49	Evaluation Kit for MAX722
MAX723	93NR 4-49	3.0V Palmtop Computer and LCD Power-Supply Regulator
MAX7231	MAXFAX	8-Digit, Triplexed LCD Decoder/Driver
MAX7232	MAXFAX	10-Digit, Triplexed LCD Decoder/Driver
MAX7233	MAXFAX	4-Character, Triplexed LCD Decoder/Driver
MAX7234	MAXFAX	5-Character, Triplexed LCD Decoder/Driver
MAX724	94NR 4-79	5A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX726	94NR 4-79	2A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX727	94NR 4-95	2A, 5V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX728	94NR 4-95	2A, 3.3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX729	94NR 4-95	2A, 3.0V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX730	93NR 4-69	5V, Step-Down, PWM, Current-Mode DC-DC Converter (see MAX730A)
MAX730A	95NR 4-85	5V, Step-Down, PWM, DC-DC Converter
MAX731	DS	5V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX731EVKIT	DS	Evaluation Kit for MAX731
MAX732	93NR 4-93	12V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX732EVKIT	DS	Evaluation Kit for MAX732
MAX733	93NR 4-93	15V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX734	94NR 4-103	12V, 120mA Flash Memory Programming Supply
MAX734EVKIT	DS	Evaluation Kit for MAX734
MAX735	94NR 4-41	-5V, Inverting, PWM DC-DC Converter
MAX736	DS	-12V, Inverting, PWM, Current-Mode DC-DC Converter
MAX737	DS	-15V, Inverting, PWM, Current-Mode DC-DC Converter
MAX738	93NR 4-69	5V, Step-Down, PWM, Current-Mode DC-DC Converter (see MAX738A)
MAX738EVKIT	DS	Evaluation Kit for MAX738
MAX738A	95NR 4-85	5V, Step-Down, PWM DC-DC Converter
MAX739	DS	-5V, Inverting, PWM, Current-Mode DC-DC Converter
MAX739EVKIT-DIP	DS	Evaluation Kit for MAX739
MAX741	94NR 4-119	Pin-Programmed, Low-Voltage, PWM Current-Mode Controller
MAX741EVKIT	DS	Evaluation Kit for MAX741
MAX742	92NR 4-153	Dual-Output, PWM Switch-Mode Regulator (+5V to ±15V or ±12V)
MAX743	92NR 4-169	Dual-Output, PWM Switch-Mode Regulator (+5V to ±15V or ±12V)
MAX743EVKIT	DS	Evaluation Kit for MAX743
MAX744A	95NR 4-85	5V, Step-Down, PWM DC-DC Converter
MAX746	DS	High-Efficiency, PWM, Step-Down, N-Channel DC-DC Controller
MAX747	DS	High-Efficiency, PWM, Step-Down Controller (External P-Channel Driver)
MAX748A	95NR 4-87	3.3V, PWM, Step-Down DC-DC Converter
MAX749	94NR 4-149	Digitally Adjustable LCD Bias Supply

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MAX749EVKIT-DIP	DS	Evaluation Kit for MAX749
MAX750	93NR 4-69	Adjustable, PWM, Step-Down DC-DC Converter (see MAX750A)
MAX750A	95NR 4-99	Adjustable, PWM, Step-Down Regulator
MAX751	94NR 4-161	5V, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752	DS	Adjustable, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752EVKIT	DS	Evaluation Kit for MAX752
MAX753	DS	CCFT Backlight and LCD Negative Contrast Controller
MAX754	DS	CCFT Backlight and LCD Positive Contrast Controller
MAX755	94NR 4-111	Adjustable, PWM, Inverting DC-DC Converter
MAX756	DS	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX756EVKIT	DS	Evaluation Kit for MAX756
MAX757	DS	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX758	93NR 4-69	Adjustable, Step-Down, PWM, Current-Mode DC-DC Converter (see MAX758A)
MAX758EVKIT	DS	Evaluation Kit for MAX758
MAX758A	95NR 4-99	Adjustable, PWM, Step-Down DC-DC Converter
MAX759	DS	Adjustable, Inverting, PWM, Current-Mode DC-DC Converter
MAX759LCDEVKIT	DS	Evaluation Kit for MAX759
MAX761	95NR 4-101	12V/Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Converter
MAX761EVKIT	DS	Evaluation Kit for MAX761
MAX762	95NR 4-101	15V/Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Converter
MAX7624	MAXFAX	Improved MX7524
MAX763A	95NR 4-85	3.3V, PWM, Step-Down DC-DC Converter
MAX764	95NR 4-113	-5V/Adjustable, High-Efficiency, Low IQ, Inverting DC-DC Converter
MAX7645	MAXFAX	Improved MX7545
MAX765	95NR 4-113	-12V/Adjustable, High-Efficiency, Low IQ, Inverting DC-DC Converter
MAX766	95NR 4-113	-15V/Adjustable, High-Efficiency, Low IQ, Inverting DC-DC Converter
MAX767	95NR 4-113	5V-3.3V, Synchronous, Step-Down Power-Supply Controller
MAX767EVKIT	DS	Evaluation Kit for MAX767
MAX770	95NR 4-141	5V/Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller (see MAX1771)
MAX7705	DS	µP Power-Supply Monitor with Reset
MAX770EVKIT	DS	Evaluation Kit for MAX770
MAX771	95NR 4-141	12V/Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller (see MAX1771)
MAX772	95NR 4-141	15V/Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller (see MAX1771)
MAX773	95NR 4-141	5V/12V/15V/Adjustable, High-Voltage, High-Efficiency, Low IQ, Step-Up DC-DC Controller
MAX774	95NR 4-161	-5V or Adjustable, High-Efficiency, Low IQ, Inverting DC-DC Controller
MAX774EVKIT	DS	Evaluation Kit for MAX774
MAX775	95NR 4-161	-12V or Adjustable, High-Efficiency, Low IQ, Inverting DC-DC Controller
MAX776	95NR 4-161	-15V or Adjustable, High-Efficiency, Low IQ, Inverting DC-DC Controller
MAX777	95NR 4-177	1V-Input, 5V-Output, Step-Up DC-DC Converter
MAX778	95NR 4-177	1V-Input, 3V-/3.3V-Output, Step-Up DC-DC Converter
MAX778EVKIT	DS	Evaluation Kit for MAX778
MAX779	95NR 4-177	1V-Input, Adjustable-Output, Step-Up DC-DC Converter

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Part #	Publication/Doc. Page	Description
MAX780	DS	Dual-Slot, PCMCIA Analog Power Controller
MAX781	DS	Subnotebook Computer Power Controller with Dual PCMCIA VPP Outputs
MAX782	DS	Triple-Output Power-Supply Controller for Notebook Computers
MAX782EVKIT	DS	Evaluation Kit for MAX782
MAX783	DS	3.3V/5V Notebook Computer Power Supply, Dual PCMCIA VPP Outputs
MAX783EVKIT	DS	Evaluation Kit for MAX783
MAX786	95NR 4-189	3.3V/5V Notebook Computer Power-Supply with 25µA Shutdown
MAX786EVKIT	DS	Evaluation Kit for MAX786
MAX787	95NR 4-205	5A, 5V Step-Down, PWM Switch-Mode DC-DC Converter
MAX788	95NR 4-205	5A, 3.3V Step-Down, PWM Switch-Mode DC-DC Converter
MAX789	95NR 4-205	5A, 3V Step-Down, PWM Switch-Mode DC-DC Converter
MAX791	DS	Microprocessor Supervisory Circuit (see MAX807L)
MAX792	DS	Microprocessor and Non-Volatile Memory Supervisory Circuits
MAX793	95NR 5-67*	3V Reset with Watchdog, Chip Enable, and Battery Backup
MAX794	95NR 5-67*	3V Reset, Adjustable Threshold with Watchdog, Chip Enable, and Battery Backup
MAX795	95NR 5-67*	3V Reset with Chip Enable, and Battery Backup
MAX796	95NR 4-211*	3.3V/5V High-Efficiency, High-Power PWM Step-Down Controller with Positive Secondary
MAX797	95NR 4-211*	3.3V/5V High-Efficiency, High-Power PWM Step-Down Controller with Low Noise Mode
MAX798	95NR 4-211*	3.3V/5V High-Efficiency, High-Power PWM Step-Down Controller with Low Noise Mode
MAX799	95NR 4-211*	3.3V/5V High-Efficiency, High-Power PWM Step-Down Controller with Negative Secondary
MAX800L	DS	µP Supervisory Circuit with 4.65V Reset (see MAX807L)
MAX800M	DS	µP Supervisory Circuit with 4.4V Reset (see MAX807M)
MAX802L/M	95NR 5-7	High-Accuracy Reset with Watchdog and Battery Backup (see MAX801L/M)
MAX802R/S/T	95NR 5-19	3V High-Accuracy Reset with Watchdog and Battery Backup
MAX804R/S/T	95NR 5-19	3V High-Accuracy Reset (asserted high) with Watchdog/Battery Backup
MAX805L	95NR 5-7	Reset (asserted high) with Watchdog and Battery Backup
MAX805R/S/T	95NR 5-19	3V Reset (asserted high) with Watchdog and Battery Backup
MAX806R/S/T	95NR 5-19	3V High-Accuracy Reset with Battery Backup
MAX807	95NR 5-69	±1.5%-Accurate Reset with Watchdog, Chip Enable, and Battery Backup
MAX809	95NR 5-71*	3-Pin µP Reset Monitor
MAX810	95NR 5-71*	3-Pin µP Reset Monitor
MAX813L	95NR 5-47	Reset (asserted high) with Watchdog
MAX814	95NR 5-73*	±1%-Accurate Reset
MAX815	95NR 5-73*	±1%-Accurate Reset and Watchdog
MAX816	95NR 5-73*	±1%-Accurate Reset with Adjustable Threshold
MAX820	DS	Microprocessor and Non-Volatile Memory Supervisory Circuits
MAX8211	DS	Programmable Voltage Detector
MAX8212	DS	Programmable Voltage Detector
MAX8213	DS	Five Universal Voltage Monitors, Complete µP Voltage Monitoring
MAX8214	DS	Five Universal Voltage Monitors with Active Pull-Ups
MAX8215	DS	±5V, ±12V Dedicated Microprocessor Voltage Monitor

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MAX8216	DS	±5V, ±12V Dedicated Microprocessor Voltage Monitor
MAX830	95NR 4-213*	1A, Adjustable VOUT, Step-Down PWM DC-DC Converter, Surface Mountable
MAX831	95NR 4-213*	1A, 5V, Step-Down PWM DC-DC Converter, Surface Mountable
MAX831EVKIT	DS	Evaluation Kit for MAX831/832/833
MAX832	95NR 4-213*	1A, 3.3V, Step-Down PWM DC-DC Converter, Surface Mountable
MAX833	95NR 4-213*	1A, 3V, Step-Down PWM DC-DC Converter, Surface Mountable
MAX850	95NR 4-215	-4V/1V/Adjustable, GaAsFET Bias Supply
MAX850EVKIT	DS	Evaluation Kit for the MAX850–853
MAX851	95NR 4-215	-4V/1V/Adjustable, GaAsFET Bias Supply
MAX852	95NR 4-215	-4V/1V/Adjustable, GaAsFET Bias Supply with Adjustable Oscillator
MAX853	95NR 4-215	Adjustable Output, GaAsFET Bias Supply and Adjustable Reference Level
MAX856	95NR 4-223	3.3V/5V High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX857	95NR 4-223	Adjustable Output, High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX858	95NR 4-223	3.3V/5V High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX859	95NR 4-223	Adjustable Output, High-Efficiency, Low IQ, DC-DC Step-Up Converter
MAX860	95NR 4-235	50mA Charge-Pump Voltage Converter
MAX861	95NR 4-235	50mA Charge-Pump Voltage Converter
MAX872	94NR 6-7	10µA, Low-Dropout, 2.5V Precision Voltage Reference
MAX873	94NR 6-15	Low-Power, Low-Drift, 2.5V Precision Voltage Reference
MAX874	94NR 6-7	10µA, Low-Dropout, 4.096V Precision Voltage Reference
MAX875	94NR 6-15	Low-Power, Low-Drift, 5V Precision Voltage Reference
MAX876	94NR 6-15	Low-Power, Low-Drift, 10V Precision Voltage Reference
MAX877	95NR 4-243	5V-Output, 1.8V- to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX877EVKIT	DS	Evaluation Kit for MAX877/878
MAX878	95NR 4-243	3.3V/3V-Output, 1.8V- to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX879	95NR 4-243	Adjustable-Output, 1.8V- to 6V-Input, Step-Up/Step-Down DC-DC Converter
MAX882	95NR 4-255*	3.3V/Adjustable, 250mA, P-Channel LDO Linear Regulator with Standby Mode
MAX883	95NR 4-255*	5V/Adjustable, 250mA, P-Channel LDO Linear Regulator with OFF Mode
MAX884	95NR 4-255*	3.3V/Adjustable, 250mA, P-Channel LDO Linear Regulator with OFF Mode
MAX900	92NR 8-51	Quad, High-Speed, Low-Power Voltage Comparator
MAX901	92NR 8-51	Quad, High-Speed, Low-Power Voltage Comparator
MAX902	92NR 8-51	Dual, High-Speed, Low-Power Voltage Comparator
MAX903	92NR 8-51	High-Speed, Low-Power Voltage Comparator
MAX905	93NR 3-41	High-Speed, Clocked D - Flip Flop, ECL Voltage Comparator
MAX906	93NR 3-41	Dual, High-Speed, Clocked D - Flip Flop, ECL Voltage Comparator
MAX907	94NR 3-91	Dual, High-Speed, Ultra-Low Power, Single 5V TTL Comparator
MAX908	94NR 3-91	Quad, High-Speed, Ultra-Low Power, Single 5V TTL Comparator
MAX909	94NR 3-91	Single, High-Speed, Ultra-Low Power, Single 5V TTL Comparator
MAX910	93NR 3-57	High-Speed, Threshold-Programmable Voltage Comparator
MAX911	93NR 3-57	High-Speed, Threshold-Programmable Voltage Comparator
MAX912	95NR 3-39	Dual, Ultra-Fast, Low-Power, Precision TTL Comparator
MAX913	95NR 3-39	Single Ultra-Fast, Low-Power, Precision TTL Comparator
MAX915	DS	Ultra High-Speed, TTL Comparator
MAX916	DS	Master/Slave, Dual Ultra High-Speed, TTL Comparator
MAX921	94NR 3-115	Ultra Low-Power, Single-Supply Comparator with 1% Precision Reference

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MAX922	94NR 3-115	Dual, Ultra Low-Power Single-Supply Comparator
MAX923	94NR 3-115	Dual, Ultra Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX924	94NR 3-115	Quad, Ultra Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX931	95NR 3-47	Ultra Low-Power, Low-Cost Comparator with 2% Accurate Reference
MAX932	95NR 3-47	Dual, Ultra Low-Power, Low-Cost Comparator with 2% Accurate Reference
MAX933	95NR 3-47	Dual, Ultra Low-Power, Low-Cost Comparator with 2% Accurate Reference
MAX934	95NR 3-47	Quad, Ultra Low-Power, Low-Cost Comparator with 2% Accurate Reference
MAX941	95NR 3-61	3V and 5V, 75ns, Rail-to-Rail Input Comparator
MAX942	95NR 3-61	Dual, 3V and 5V, 75ns, Rail-to-Rail Input Comparator
MAX944	95NR 3-61	Quad, 3V and 5V, 75ns, Rail-to-Rail Input Comparator
MAX951	95NR 3-71*	7µA Max, Unity-Gain-Stable Op Amp plus Comparator and 1.2V Reference
MAX952	95NR 3-71*	7µA Max, 400kHz GBWP Op Amp plus Comparator and 1.2V Reference
MAX953	95NR 3-71*	5µA Max, Unity-Gain-Stable Op Amp plus Comparator
MAX954	95NR 3-71*	5µA Max, 400kHz GBWP Op Amp plus Comparator
MAX9685	MAXFAX	Ultra-Fast ECL-Output Comparator with Latch Enable
MAX9686	MAXFAX	Very Fast TTL-Latched Output Comparator
MAX9687	MAXFAX	Dual, Ultra-Fast ECL-Output Comparator
MAX9690	MAXFAX	Ultra-Fast ECL-Output Comparator
MAX9698	MAXFAX	Dual, Very Fast, TTL-Latched Output Comparator
MAXC001	MAXFAX	150µF, Low-ESR Aluminum Electrolytic Capacitor
MAXL001	92NR 4-185	100µH Toroid Inductor
MF10	DS	Dual, Second-Order, Universal Switched-Capacitor Filter
MM74C945	MAXFAX	4-Digit, Up/Down Counter/Decoder/Driver
MM74C947	MAXFAX	4-Digit, Up/Down Counter/Decoder/Driver
MX2700	MAXFAX	Precision, 10V Reference, 3 ppm/°C
MX2701	MAXFAX	Precision, -10V Reference, 3 ppm/°C
MX2710	MAXFAX	Precision, 10V Reference, 1 ppm/°C
MX3554	MAXFAX	Wideband, Fast-Setting Op Amp
MX390	DS	Quad, CMOS 12-Bit DAC
MX536A	MAXFAX	True RMS-to-DC Converter
MX565A	MAXFAX	High-Speed, 12-Bit, Monolithic DAC with Voltage Reference
MX566A	MAXFAX	High-Speed, 12-Bit, Monolithic DAC
MX574A	DS	Industry-Standard, Complete 12-Bit ADC
MX578	MAXFAX	High-Speed, 3µs 12-Bit ADC
MX580	MAXFAX	Precision 2.5V Voltage Reference
MX581	MAXFAX	Precision 10V Voltage Reference
MX584	MAXFAX	Pin-Programmable 10V, 7.5V, 5V, 2.5V, Precision Voltage Reference
MX636	MAXFAX	True RMS-to-DC Converter
MX674A	DS	Industry-Standard, Complete 12-Bit ADC
MX7224	MAXFAX	CMOS, Double-Buffered, 8-Bit DAC with Voltage-Output Amplifier
MX7225	MAXFAX	CMOS, Quad, 8-Bit DAC with Voltage-Output Amplifier Latches (see MAX505)
MX7226	MAXFAX	CMOS, Quad, 8-Bit DAC with Voltage-Output Amplifier (see MAX506)
MX7228	MAXFAX	CMOS, Octal, 8-Bit DAC (see MAX528)
MX7245	DS	Complete, 12-Bit, Voltage-Output Multiplying DAC (see MAX507)
MX7248	DS	Complete, 12-Bit, Voltage-Output Multiplying DAC (see MAX508)
MX7501	MAXFAX	8-Channel, Low-Power, Monolithic, CMOS Multiplexer

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MX7502	MAXFAX	Differential 4-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7503	MAXFAX	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7506	MAXFAX	Monolithic CMOS Multiplexer
MX7507	MAXFAX	Monolithic CMOS Multiplexer
MX7520	MAXFAX	CMOS, 10-Bit Multiplying DAC
MX7521	MAXFAX	CMOS, 12-Bit Multiplying DAC
MX7523	MAXFAX	CMOS, 8-Bit Multiplying DAC
MX7524	MAXFAX	CMOS, 8-Bit Buffered, Multiplying DAC
MX7528	MAXFAX	CMOS, Dual, 8-Bit, Buffered Multiplying DAC (see MAX512)
MX7530	MAXFAX	CMOS, 10-Bit Multiplying DAC
MX7531	MAXFAX	CMOS, 12-Bit Multiplying DAC
MX7533	MAXFAX	CMOS, Low-Cost, 10-Bit Multiplying DAC
MX7534	MAXFAX	µP-Compatible, 14-Bit DAC
MX7535	MAXFAX	µP-Compatible, 14-Bit DAC
MX7536	MAXFAX	µP-Compatible, 14-Bit DAC
MX7537	MAXFAX	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7538	MAXFAX	µP-Compatible, CMOS 14-Bit DAC
MX7541	MAXFAX	CMOS, 12-Bit Multiplying DAC
MX7541A	MAXFAX	CMOS, 12-Bit Multiplying DAC
MX7542	MAXFAX	CMOS, 12-Bit, µP-Compatible DAC
MX7543	MAXFAX	CMOS, 12-Bit, Serial Input DAC (see MAX543)
MX7545	MAXFAX	CMOS, 12-Bit, Buffered, Multiplying DAC
MX7545A	MAXFAX	CMOS, 12-Bit, Buffered, Multiplying DAC
MX7547	MAXFAX	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7548	MAXFAX	CMOS, 8-Bit-Compatible, 12-Bit DAC
MX7549	MAXFAX	CMOS, Dual, 12-Bit, Double-Buffered, µP-Compatible DAC
MX7572	92NR 7-37	Complete, High-Speed, CMOS 12-Bit ADC (see MAX120)
MX7574	MAXFAX	CMOS, µP-Compatible, 8-Bit ADC
MX7575	MAXFAX	CMOS, µP-Compatible, 5µs, 8-Bit ADC (see MAX165)
MX7576	MAXFAX	CMOS, µP-Compatible, 10µs, 8-Bit ADC (see MAX166)
MX7578	DS	Calibrated 12-Bit ADC (see MAX178)
MX7581	MAXFAX	CMOS, 8-Bit, 8-Channel Data Acquisition System (see MAX161)
MX7582	MAXFAX	Calibrated, 4-Channel, 12-Bit ADC (see MAX182)
MX7628	MAXFAX	CMOS, Dual, 8-Bit, Buffered, Multiplying DAC
MX7672	DS	High-Speed 12-Bit ADC with External Reference Input (see MAX120)
MX7820	MAXFAX	CMOS, 1.3µs, 8-Bit ADC with Track/Hold (see MAX150)
MX7821	92NR 7-157	µP-Compatible, 660ns, 8-Bit ADC with Track/Hold (see MAX153)
MX7824	DS	CMOS, High-Speed, 8-Bit ADC with 4-Channel Multiplexer (see MAX154)
MX7828	DS	CMOS, High-Speed, 8-Bit ADC with 8-Channel Multiplexer (see MAX158)
MX7837	DS	Complete, Dual, 12-Bit Multiplying DAC with 8-Bit Bus Interface
MX7845	MAXFAX	Complete, 12-Bit Multiplying DAC (see MAX502)
MX7847	DS	Complete, Dual, 12-Bit Multiplying DAC with 12-Bit Bus Interface
MXD1000	95NR 10-19*	5-Tap Silicon Delay Line
MXD1013	95NR 10-21*	3-in-1 Silicon Delay Line
MXD1210	DS	Nonvolatile RAM Controller
MXL1001	MAXFAX	Low-Offset Op Amp (see MAX400)

*Advance Information–first page of data sheet in preparation.

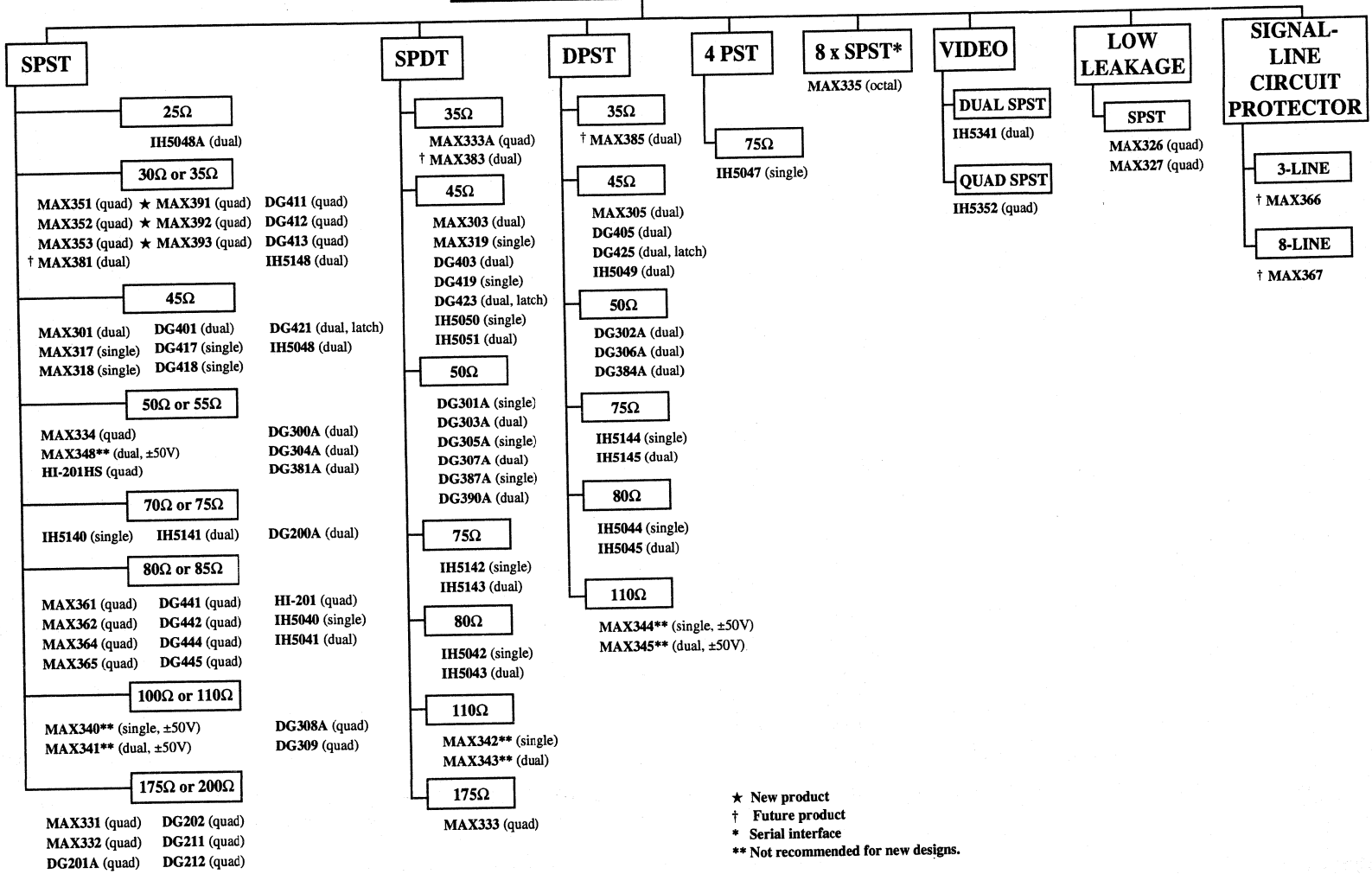
MXL1007	DS	Low-Noise, Precision Op Amp (see MAX427)
MXL1013	DS	Dual Precision Op Amp
MXL1014	DS	Dual Precision Op Amp
MXL1016	DS	Ultra-Fast Precision TTL Comparator (see MAX913)
MXL1028	DS	Ultra Low-Noise, High-Speed, Precision Op Amp
MXL1062	DS	5th-Order, Zero-Error, Butterworth, Switched Capacitor Lowpass Filter
MXL1074	MAXFAX	5A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1076	MAXFAX	2A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1116	DS	Ultra-Fast, Single-Supply, Precision TTL Comparator (see MAX913)
MXL1178	DS	Dual, Micropower, Single-Supply, Precision Op Amp (see MAX478)
MXL1179	DS	Quad, Micropower, Single-Supply, Precision Op Amp (see MAX479)
MXT429	DS	High-Speed, 6A MOSFET Driver (Inverting)
OP07	MAXFAX	Precision Op Amp (see MAX400)
OP27	DS	Low-Noise, Precision Op Amp (see MAX427)
OP37	DS	Low-Noise, Precision Op Amp (see MAX437)
OP90	MAXFAX	Precision, Low-Voltage Micropower Op Amp (see MAX480)
PGA100	MAXFAX	Programmable Gain Amplifier
REF01	MAXFAX	Precision, 10V Voitage Reference (see MAX674)
REF02	MAXFAX	Precision, 5V Voltage Reference (see MAX675)
Si7661	MAXFAX	CMOS Switched-Capacitor Voltage Converter (Up to 20V Input)
TSC426	MAXFAX	Dual-Power MOSFET Driver (Inverting) (see MAX626)
TSC427	MAXFAX	Dual-Power MOSFET Driver (Non-inverting) (see MAX627)
TSC428	MAXFAX	Dual-Power MOSFET Driver (Inverting and Non-inverting) (see MAX628)

MAXIM

Analog Multiplexers/Switches

*Advance Information–first page of data sheet in preparation.

ANALOG SWITCHES



★ New product
† Future product
* Serial interface
** Not recommended for new designs.

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Features	Price† 1000-up ($)
MAX317	SPST NC	45	0.25		3	175	145	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness, 8-pin DIP/SO	1.05
DG417	SPST NC	45	0.25			175	145	0.8/2.4	0.001/0.001	8-pin DIP/SO	0.96
MAX318	SPST NO	45	0.25		3	175	145	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness, 8-pin DIP/SO	1.05
DG418	SPST NO	45	0.25			175	145	0.8/2.4	0.001/0.001	8-pin DIP/SO	0.96
IH5140	SPST NO	75	1			150	125	0.8/2.4	0.01/0.01	Fast, low power	2.89
IH5040	SPST NO	80	5			400	200	0.8/2.4	0.01/0.01	Very low power	2.06
MAX319	SPDT	45	0.25	2	3	175	145	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness, 8-pin DIP/SO	1.39
DG419	SPDT	45	0.25			175	145	0.8/2.4	0.001/0.001	8-pin DIP/SO	1.32
IH5050	SPDT NO	45	5			1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	3.94
DG301A	SPDT	50	1			300	250	0.8/4.0	0.1/0.1	2.4 V_{IH}, low R_{ON}	1.94
DG305A	SPDT	50	1			250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.55
DG387A	SPDT	50	1			300	250	0.8/4.0	0.1/0.1	Low R_{ON}	2.08
IH5142	SPDT	75	1			200	125	0.8/2.4	0.01/0.01	Fast, low power	3.23
IH5042	SPDT	80	5			400	200	0.8/2.4	0.01/0.01	Very low power	1.84
IH5144	DPST NO	75	1			200	125	0.8/2.4	0.01/0.01	Fast, low power	3.23
IH5044	DPST NO	80	5			400	200	0.8/2.4	0.01/0.01	Very low power	2.29
IH5047	4PST NC	75	1			400	200	0.8/2.4	0.001/0.001	Very low power	2.44
IH5048A	2 SPST NO	25	5			1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.49
IH5148	2 SPST	30	1			1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.94
MAX381	2 SPST	35	0.1	2	4	150	75	0.8/2.4	-0.001/0.001	+5V/±5V CMOS switch	††
MAX301	2 SPST NO	45	0.25	2	3	150	100	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	1.23
DG401	2 SPST NO	45	0.25			150	100	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	1.23
DG421	2 SPST	45	0.25			250	200	0.8/2.4	0.001/0.001	Low power, high speed, has latches	1.59
IH5048	2 SPST NO	45	5			1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.49
DG300A	2 SPST NC	50	1			300	250	0.8/4.0	0.5/0.1	2.4 V_{IH}, low R_{ON}	1.94
DG304A	2 SPST NC	50	1			250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.18
DG381A	2 SPST NO	50	1			300	250	0.8/4.0	0.1/0.1	Low R_{ON}	2.08
DG200A	2 SPST NC	70	2			1000	500	0.8/2.4	0.3/0.01	Low power	0.93
IH5141	2 SPST NO	75	1			150	125	0.8/2.4	0.01/0.01	Fast, low power	3.23
IH5041	2 SPST NC	80	1			400	200	0.8/2.4	0.001/0.001	Very low power	1.84
MAX383	2 SPDT	35	0.1	2	4	150	75	0.8/2.4	-0.001/0.001	+5V/±5V CMOS switch	††
MAX303	2 SPDT	45	0.25	2	3	150	100	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	2.57
DG403	2 SPDT	45	0.25			150	100	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	2.57
DG423	2 SPDT	45	0.25			250	200	0.8/2.4	0.001/0.001	Low power, high speed, has latches	3.30
IH5051	2 SPDT	45	5			1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	4.73
DG303A	2 SPDT	50	1			300	250	0.8/4.0	0.1/0.1	2.4 V_{IH}, low R_{ON}	2.36
DG307A	2 SPDT	50	1			250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.36
DG390A	2 SPDT	50	1			300	250	0.8/4.0	0.1/0.1	Low R_{ON}	2.60
IH5143	2 SPDT	75	1			200	125	0.8/2.4	0.01/0.01	Fast, low power	3.49
IH5043	2 SPDT	80	1			400	200	0.8/2.4	0.001/0.001	Very low power	2.36
MAX385	2 DPST	35	0.1	2	4	150	75	0.8/2.4	-0.001/0.001	+5V/±5V CMOS switch	††

1 NO = Normally Open, NC = Normally Closed.

2 Drain-source on resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Features	Price† 1000-up ($)
MAX305	2 DPST NO	45	0.25	2	3	150	100	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	2.57
DG405	2 DPST NO	45	0.25			150	100	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	2.57
DG425	2 DPST	45	0.25			250	200	0.8/2.4	0.001/0.001	Low power, high speed, has latches	3.30
IH5049	2 DPST NO	45	5			1000	500	0.8/2.4	0.01/0.01	Low power, low R_{ON}	5.35
DG302A	2 DPST NC	50	1			300	250	0.8/4.0	0.1/0.1	2.4 V_{IH}, low R_{ON}	2.50
DG306A	2 DPST NC	50	1			250	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	2.53
DG384A	2 DPST NC	50	1			300	250	0.8/4.0	0.1/0.1	Low R_{ON}	2.92
IH5145	2 DPST NO	75	1			200	125	0.8/2.4	0.01/0.01	Fast, low power	3.82
IH5045	2 DPST NC	80	1			400	200	0.8/2.4	0.001/0.001	Very low power	2.44
MAX391	4 SPST NC	35	0.1			130	75	0.8/2.4	0.001/0.001	Low-voltage +5V/±5V operation	1.87
MAX392	4 SPST NO	35	0.1			130	75	0.8/2.4	0.001/0.001	Low-voltage +5V/±5V operation	1.87
MAX393	4 SPST	35	0.1			130	75	0.8/2.4	0.001/0.001	Low-voltage +5V/±5V operation	1.87
MAX351	4 SPST NC	35	0.25	2	3	175	145	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	1.76
DG411	4 SPST NC	35	0.25			175	145	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	1.85
DG412	4 SPST NO	35	0.25			175	145	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	1.85
MAX352	4 SPST NO	35	0.25	2	3	175	145	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	1.76
DG413	4 SPST	35	0.25			175	145	0.8/2.4	0.001/0.001	Low power, high speed, low leakage	1.85
MAX353	4 SPST	35	0.25	2	3	175	145	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	1.76
MAX334	4 SPST NC	50	1			100	50	0.8/3.0	4.5/3.5	Most switches per package, high-speed with break-before-make	2.88
HI-201HS	4 SPST NC	50	1			50	50	0.8/3.0	4.0/1.5	Low R_{ON}, high speed	2.64
HI-201	4 SPST NC	80	5			400	300	0.8/2.4	0.3/0.1	Low R_{ON}, quad SPST	2.00
MAX361	4 SPST NC	85	0.5	2	5	250	120	0.8/2.4	0.1/0.001	Low R_{ON} match and flatness	1.29
DG441	4 SPST NC	85	0.5			250	120	0.8/2.4	0.1/0.001	Low power, low leakage	1.29
MAX362	4 SPST NO	85	0.5	2	5	250	120	0.8/2.4	0.1/0.001	Low R_{ON} match and flatness	1.29
DG442	4 SPST NO	85	0.5			250	120	0.8/2.4	0.1/0.001	Low power, low leakage	1.29
MAX364	4 SPST NC	85	0.5	2	5	250	120	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	1.14
DG444	4 SPST NC	85	0.5			250	120	0.8/2.4	0.001/0.001	Low cost, quad SPST	1.03
MAX365	4 SPST NO	85	0.5	2	5	250	120	0.8/2.4	0.001/0.001	Low R_{ON} match and flatness	1.14
DG445	4 SPST NO	85	0.5			250	120	0.8/2.4	0.001/0.001	Low cost, quad SPST	1.03
DG308A	4 SPST NO	100	1			200	150	3.1/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	0.95
DG309	4 SPST NC	100	1			200	150	3.5/11.0	0.1/0.1	CMOS logic levels, high speed, low R_{ON}	0.95
MAX331	4 SPST NC	175	1			600	450	0.8/2.4	0.01/0.01	Improved DG201	3.37
MAX332	4 SPST NO	175	1			600	450	0.8/2.4	0.01/0.01	Improved DG201	3.37
DG211	4 SPST NC	175	5			1000	500	0.8/2.4	0.1/0.1	No V_{LOGIC} supply	0.91
DG212	4 SPST NO	175	5			1000	500	0.8/2.4	0.1/0.1	Normally open	0.91
DG201A	4 SPST NC	200	1			600	450	0.8/2.4	0.1/0.1	Low power	0.95
DG202	4 SPST NO	200	1			600	450	0.8/2.4	0.1/0.1	Normally open	0.95
MAX326	4 SPST NC	3500	0.01			1000	500	0.8/2.4	0.25/0.1	Ultra-low leakage, 10pA max	2.78
MAX327	4 SPST NO	3500	0.01			1000	500	0.8/2.4	0.25/0.1	Ultra-low leakage, 10pA max	2.78
MAX333A	4 SPDT	35	0.25	2	3	175	145	0.8/2.4	0.001/0.001	Improved MAX333, low R_{ON}	3.60
MAX333	4 SPDT	175	5			1000	500	0.8/2.4	0.25/0.25		2.87
MAX335	8 SPST	175	1			400	400	0.8/2.4	0.3/0.01	Serial interface with break-before-make	2.84

1 NO = Normally Open, NC = Normally Closed.

2 Drain-source on resistance is for the commercial grade, T_A = +25°C.

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High-Voltage Analog Switches

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Features	Price† 1000-up ($)
MAX340*	SPST NO	110	60	1000	750	3.5/12	0.3/0.02		6.27
MAX342*	SPDT	110	60	1000	750	3.5/12	0.3/0.02		6.31
MAX344*	DPST NO	110	60	1000	750	3.5/12	0.3/0.02	↑	5.21
MAX348*	2 SPST NO	55	60	1000	750	3.5/12	0.3/0.02	High-voltage, ±50V operation with ±50 analog signal range	7.83
MAX341*	2 SPST NO	110	60	1000	750	3.5/12	0.3/0.02	↓	6.27
MAX343*	2 SPDT	110	60	1000	750	3.5/12	0.3/0.02		8.71
MAX345*	2 DPST NO	110	60	1000	750	3.5/12	0.3/0.02		8.71

Video Switching Products

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	V_{OS} (mV max)	Output Current (mA max)	Supply Voltage (V)	I_{BIAS} (µA max)	Features	Price† 1000-up ($)
MAX440	160 110 (A_V≥2)	370	10	35	±5	2	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain error, 15ns switch time, high-Z output state	8.95
MAX441	160 110 (A_V≥2)	370	10	35	±5	2	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain error, 15ns switch time	5.90
MAX442	140	250	5	35	±5	2	Video amp with 4-channel mux, 15ns switch time, 8-pin DIP/SO	4.45

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (µs max)	V_{IL}/V_{IH} (V)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX453	1-of-2 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	3.94
MAX454	1-of-4 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	5.25
MAX455	1-of-8 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	8.75
MAX310	1-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	5.18
MAX311	2-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	7.20
IH5341	2 SPST NO	75	0.5	300	0.8/2.4	±10	70dB isolation at 10MHz	2.48
IH5352	4 SPST NO	75	0.5	300	0.8/2.4	±10	70dB isolation at 10MHz	4.50
MAX456 (See Video/High-Speed Products table)								–

Signal-Line Circuit Protectors

Part Number	Function	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX366	3-Line	100	1.0	-12.5 to 13.5	±35V overvoltage protected	††
MAX367	8-Line	100	1.0	-12.5 to 13.5	±35V overvoltage protected	††

* Not recommended for new designs

1 NO = Normally Open, NC = Normally Closed

2 Drain-source on resistance is for the commercial grade, T_A = + 25°C.

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ANALOG MULTIPLEXERS

FAULT PROTECTED

8-CHANNEL

MAX358 (±35V)
MAX359 (diff ±35V)
MAX368 (latch ±35V)
MAX369 (latch, diff ±35V)
MAX378 (±75V)*
MAX379 (diff ±75V)*
MAX388 (latch ±100V)*
MAX389 (latch, diff ±100V)*
HI-508A (±35V)
HI-509A (diff ±35V)
IH5108
IH5208 (diff)
IH6108
IH6208 (diff)
IH6116
IH6216 (diff)

STANDARD

8-CHANNEL

† **MAX308**
† **MAX309** (diff)
† **MAX398**
† **MAX399** (diff)
DG408
DG409 (diff)
DG508A
DG509A (diff)
DG528 (latch)
DG529 (latch, diff)
HI-508
HI-509 (diff)
HI-548
HI-549 (diff)
MX7501
MX7502 (diff)
MX7503

16-CHANNEL

† **MAX306**
† **MAX307** (diff)
DG406
DG407 (diff)
DG506A
DG507A (diff)
HI-506
HI-507 (diff)
MX7506
MX7507 (diff)

VIDEO

8-CHANNEL

MAX310 (70db at 10MHz)
MAX311 (diff 70db at 10MHz)

MUX/AMPLIFIER

MAX440
MAX441
MAX442
MAX453 (1 of 2, drives 75Ω)
MAX454 (1 of 4, drives 75Ω)
MAX455 (1 of 8, drives 75Ω)

CROSSPOINT

MAX456 (8 x 8 switch)

LOW LEAKAGE

8-CHANNEL

MAX328 (10pA)
MAX329 (diff, 10pA)
† **MAX338** (20pA)
† **MAX339** (diff, 10pA)

* Withstands quoted input or output voltage indefinitely with/without supply voltage present
† Future product

Part Number	Function	$R_{DS(ON)}$* (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
DG408	1-of-8	100	1	0.225/0.150	±15	Industry standard	2.59
MAX308	1-of-8	100	1	0.225/0.150	±15	Improved R_{ON} match and flatness, industry standard	††
MAX398	1-of-8	100	0.1	0.15/0.15	+5, ±5	Low-voltage +5V/±5V operation	††
MX7501	1-of-8	350	5	1.5/1.0	±15	Industry standard	5.58
MX7503	1-of-8	350	5	1.5/1.0	±15	Industry standard	5.58
DG508A	1-of-8	350	2	1.0/1.7	±15	Industry standard	1.67
MAX338	1-of-8	400	0.02	0.50/0.50	±15	Low-leakage upgrade	††
HI-508	Use DG508A (pin-for-pin compatible upgrade)						–
IH6108	Use DG508A (pin-for-pin compatible upgrade)						–
DG528	1-of-8	450	10	1.5	±15	Industry standard with latches	2.28
MAX358	1-of-8	1800	1.0	0.5	-12.5 to +13.5	Fault protected to ±35V	2.45
IH5108	Use MAX358 (pin-for-pin compatible upgrade)						–
MAX368	1-of-8	1800	2	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	3.50
HI-508A	1-of-8	1800	2	0.5	-12.5 to +13.5	Overvoltage	2.75
HI-548	Use MAX358 (pin-for-pin compatible upgrade)						–
MAX378	1-of-8	3500	1.0	0.75/0.5	-12.5 to +13.5	Fault protected to ±75V	3.50
MAX388	1-of-8	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±100V	4.50
MAX328	1-of-8	5000	0.02	1	±15	Ultra-low leakage	3.61
DG409	2-of-8	100	1	0.225/0.150	±15	Industry standard	2.59
MAX309	2-of-8	100	1	0.225/0.150	±15	Improved R_{ON} match and flatness, industry standard	††
MAX399	2-of-8	100	0.1	0.15/0.15	±15	Low-voltage +5V/±5V operation	††
DG509A	2-of-8	350	2	1.0/1.7	±15	Industry standard	1.95
MAX339	2-of-8	400	0.02	0.50/0.50	±15	Low-leakage upgrade	††
IH6208	Use DG509A (pin-for-pin compatible upgrade)						–
HI-509	Use DG509A (pin-for-pin compatible upgrade)						–
MX7502	2-of-8	350	3	1.5/1.0	±15	Industry standard	5.58
DG529	2-of-8	450	10	1.5	±15	Industry standard with latches	2.28
MAX359	2-of-8	1800	1.0	0.5	-12.5 to +13.5	Fault protected to ±35V	2.45
IH5208	Use MAX359 (pin-for-pin compatible upgrade)						–
MAX369	2-of-8	1800	1.0	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	3.50
HI-509A	2-of-8	1800	2	0.5	-12.5 to +13.5	Overvoltage	2.75
HI-549	Use MAX359 (pin-for-pin compatible upgrade)						–
MAX379	2-of-8	3500	1.0	0.75/0.5	-12.5 to +13.5	Fault protected to ±75V	3.50
MAX389	2-of-8	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±100V	4.50
MAX329	2-of-8	5000	0.02	1	±15	Ultra-low leakage	3.61
DG406	1-of-16	100	2	0.2/0.15	±15	Industry standard	4.53
MAX306	1-of-16	100	2	0.2/0.15	±15	Improved R_{ON} match and flatness, industry standard	††
DG506A	1-of-16	450	5	1.0/0.4(typ)	±15	Industry standard	3.68
IH6116	Use DG506A (pin-for-pin compatible upgrade)						–
HI-506	Use DG506A (pin-for-pin compatible upgrade)						–
MX7506	1-of-16	450	5	15/1.0	±15	Industry standard	10.25
DG407	2-of-16	100	2	0.2/0.15	±15	Industry standard	4.53
MAX307	2-of-16	100	2	0.2/0.15	±15	Improved R_{ON} match and flatness, industry standard	††
MX7507	2-of-16	450	5	1.5/1.0	±15	Industry standard	10.25
DG507A	2-of-16	450	5	1.0/0.4(typ)	±15	Industry standard	3.68
HI-507	Use DG507A (pin-for-pin compatible upgrade)						–
IH6216	Use DG507A (pin-for-pin compatible upgrade)						–

* Drain-source on resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-0159; Rev 0; 9/93

MAXIM

Precision, Dual, High-Speed Analog Switches

General Description

The MAX301/MAX303/MAX305 are precision, dual, high-speed analog switches. The single-pole single-throw (SPST) MAX301 and double-pole single-throw (DPST) MAX305 dual switches are normally open (NO). The single-pole double-throw (SPDT) MAX303 has two NO and two normally closed (NC) poles. All three parts offer low on resistance (less than 35Ω), guaranteed to match to within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 150ns and turn-off time less than 100ns).

The MAX301/MAX303/MAX305 are fabricated with Maxim's new improved silicon-gate process for high system accuracy. Design improvements guarantee extremely low charge injection (15pC) and low power consumption (35μW). A 44V maximum breakdown voltage allows rail-to-rail analog signal capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits	Military Radios
Test Equipment	Communication Systems
Heads-Up Displays	Battery-Operated Systems
Guidance and Control Systems	PBX, PABX

Features

- ♦ **Low On Resistance <22Ω Typical (35Ω Max)**
- ♦ **Guaranteed Matched On Resistance Between Channels <2Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection <15pC**
- ♦ **Guaranteed Off-Channel Leakage <6nA at +85°C**
- ♦ **Single-Supply Operation (+10V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ **TTL-/CMOS-Logic Compatible**
- ♦ **Rail-to-Rail Analog Signal Handling Capability**

Ordering Information

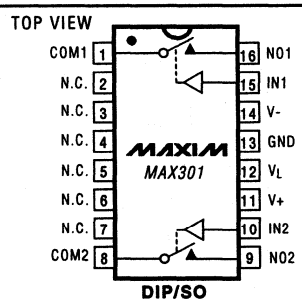
PART	TEMP. RANGE	PIN-PACKAGE
MAX301CPE	0°C to +70°C	16 Plastic DIP
MAX301CSE	0°C to +70°C	16 Narrow SO
MAX301CJE	0°C to +70°C	16 CERDIP
MAX301C/D	0°C to +70°C	Dice*
MAX301EPE	-40°C to +85°C	16 Plastic DIP
MAX301ESE	-40°C to +85°C	16 Narrow SO
MAX301EJE	-40°C to +85°C	16 CERDIP
MAX301MJE	-55°C to +125°C	16 CERDIP
MAX301MLP	-55°C to +125°C	20 LCC**

Ordering Information continued on last page.

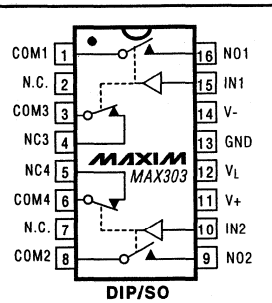
* *Contact factory for dice specifications.*

** *Contact factory for package availability.*

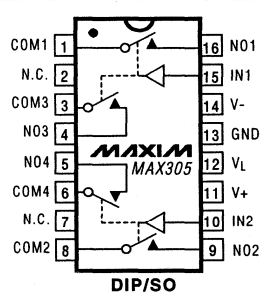
Pin Configurations/Block Diagrams/Truth Tables



MAX301	
LOGIC	SWITCH
0	OFF
1	ON



MAX303		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	OFF	ON
1	ON	OFF



MAX305	
LOGIC	SWITCH
0	OFF
1	ON

LCC packages on last page.

SWITCHES SHOWN FOR LOGIC "0" INPUT

Precision, Dual, High-Speed Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND-0.3V) to (V+) +0.3V
NO_, NC_, IN_, COM_ ..... (V- - 2V) to (V+ + 2V) or 30mA, whichever occurs first
Continuous Current, COM_, NO_, NC_ 30mA
Peak Current, COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX30_C_ _ ..... 0°C to +70°C
MAX30_E_ _ ..... -40°C to +85°C
MAX30_M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on NO_, NC_, or COM_ beyond V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog-Signal Range	V_{ANA}	(Note 3)			V-		V+	V
On Resistance	R_{ON}	$I_{(NC\ or\ NO)}$ = -10mA, $V_{COM\_}$ = ±10V, V_{INH} = 2.4V, V_{INL} = 0.8V	T_A = +25°C	C, E		20	35	Ω
				M		20	30	
			T_A = T_{MIN} to T_{MAX}	C, E			55	
				M			45	
On Resistance Match Between Channels (Note 4)	R_{ON}	$I_{(NC\ or\ NO)}$ = -10mA, $V_{COM\_}$ = ±10V, V+ = 15V, V- = -15V	T_A = +25°C	C, E, M		0.5	2	Ω
			T_A = T_{MIN} to T_{MAX}	C, E, M			3	
On Resistance Flatness (Note 4)	R_{ON}	I_S = -10mA, $V_{COM\_}$ = ±5V, V+ = 15V, V- = -15V	T_A = +25°C	C, E, M			3	Ω
			T_A = T_{MIN} to T_{MAX}	C, E, M			5	
NC or NO Off Leakage Current	$NC_{-(OFF)}$ or $NO_{-(OFF)}$	$V_{COM\_}$ = ±15.5V, $V_{NC\_}$ or $V_{NO\_}$ = ±15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	C, E	-0.50	-0.01	0.50	nA
				M	-0.25	-0.01	0.25	
			T_A = T_{MIN} to T_{MAX}	C, E	-6		6	
				M	-20		20	
COM Off Leakage Current	COM_{OFF}	$V_{COM\_}$ = ±15.5V, $V_{NC\_}$ or $V_{NO\_}$ = ±15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	C, E	-0.50	-0.01	0.50	nA
				M	-0.25	-0.01	0.25	
			T_A = T_{MIN} to T_{MAX}	C, E	-6		6	
				M	-20		20	
COM On Leakage Current	COM_{ON}	$V_{COM\_}$ = ±15.5V, $V_{NC\_}$ or $V_{NO\_}$ = ±15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	C, E	-1.0	-0.04	1.0	nA
				M	-0.4	-0.04	0.4	
			T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
				M	-40.0		40.0	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	$V_{IN\_}$ = 2.4V, all others = 0.8V		-1.000	0.005	1.000	µA
Input Current with Input Voltage Low	I_{INH}	$V_{IN\_}$ = 0.8V, all others = 2.4V		-1.000	0.005	1.000	µA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1.00	0.01	1.00	µA
			T_A = T_{MIN} to T_{MAX}	-5.00		5.00	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1.00	-0.01	1.00	µA
			T_A = T_{MIN} to T_{MAX}	-5.00		5.00	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1.00	0.01	1.00	µA
			T_A = T_{MIN} to T_{MAX}	-5.00		5.00	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1.00	-0.01	1.00	µA
			T_A = T_{MIN} to T_{MAX}	-5.00		5.00	
DYNAMIC							
Turn-On Time	t_{ON}	Figure1	T_A = +25°C		100	150	ns
Turn-Off Time	t_{OFF}	Figure 1	T_A = +25°C		60	100	ns
Break-Before-Make Time Delay (Note 3)	t_D	MAX303 only, Figure 2	T_A = +25°C	10	20		ns
Charge Injection (Note 3)	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		10	15	pC
Off Isolation (Note 5)	OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		72		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		90		dB
Off Capacitance	C_{OFF}	f = 1MHz, Figure 6	T_A = +25°C		12		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		12		pF
Channel-On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 7	T_A = +25°C		39		pF

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used on this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON}MAX - \Delta R_{ON}MIN$. On resistance match between channels and flatness are guaranteed only with specified voltages.

Note 5: See Figure 4. Off isolation = $20\log_{10} V_{COM}/V_{NC\ or}V_{NO}$, V_{COM} = output, $V_{NC\ or}$ V_{NO} = input to off switch.

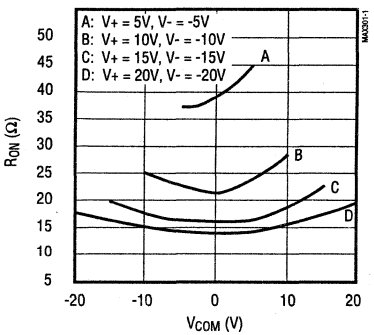
Note 6: Between any two switches. See Figure 5.

Precision, Dual, High-Speed Analog Switches

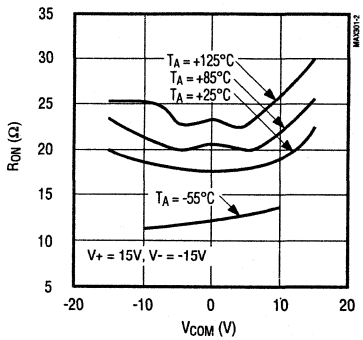
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted).

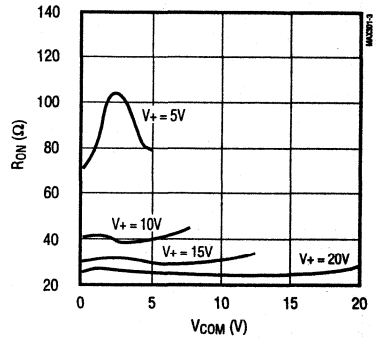
ON RESISTANCE vs. V_{COM} AND POWER-SUPPLY VOLTAGE



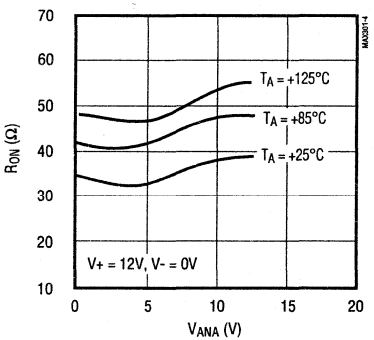
ON RESISTANCE vs. V_{COM} AND TEMPERATURE



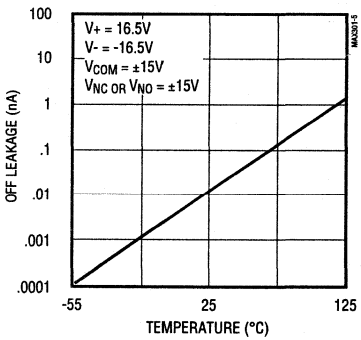
ON RESISTANCE vs. V_{COM} WITH V- = 0V



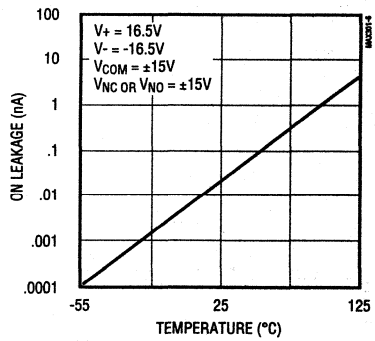
ON RESISTANCE vs. V_{COM} AND V- = 0V



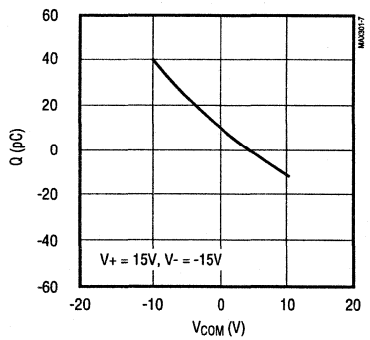
OFF LEAKAGE CURRENTS vs. TEMPERATURE



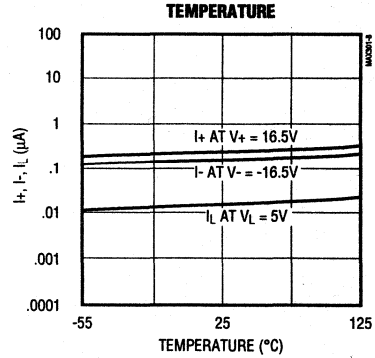
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Pin Descriptions

MAX301 PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 8	2, 10	COM1, COM2	Drain (Analog Signal)
2-7	1, 3-9, 11, 16	N.C.	Not internally connected
9, 16	5, 7, 12, 20	NC1, NC2	Source (Analog Signal)
10, 15	13, 19	IN2, IN1	Digital Logic Inputs
11	14	V+	Positive Supply-Voltage Input—connected to substrate
12	15	V_L	Logic Supply-Voltage Input
13	17	GND	Ground
14	18	V-	Negative Supply Voltage Input
MAX303 PIN		**NAME**	**FUNCTION**
DIP/SO	**LCC**		
1, 8, 3, 6	2, 4, 8, 10	COM_	Drain (Analog Signal)
2-7	1, 3, 6, 9, 11, 16	N.C.	Not internally connected
11	14	V+	Positive Supply-Voltage Input—connected to substrate
12	15	V_L	Logic Supply-Voltage Input
13	17	GND	Ground
14	18	V-	Negative Supply Voltage Input
15, 10	19, 13	IN1, IN2	Digital Logic Inputs
16, 9, 5, 4	5, 7, 12, 20	NC_, NO_	Source (Analog Signal)
MAX305 PIN		**NAME**	**FUNCTION**
DIP/SO	**LCC**		
1, 8, 3, 6	2, 4, 8, 10	COM_	Drain (Analog Signal)
2-7	1, 3, 6, 9, 11, 16	N.C.	Not internally connected
11	14	V+	Positive Supply-Voltage Input—connected to substrate
12	15	V_L	Logic Supply-Voltage Input
13	17	GND	Ground
14	18	V-	Negative Supply Voltage
15, 10	19, 13	IN1, IN2	Digital Logic Inputs
16, 9, 5, 4	5, 7, 12, 20	NO_	Source (Analog Signal)

Applications Information

Operation with Supply Voltages Other than ±15V

The MAX301/MAX303/MAX305 switches operate with ±4.5V to ±20V bipolar supplies and a +10V to +30V single supply. In either case, analog signals ranging from V+ to V- can be switched. The *Typical Operating Characteristics* graphs show the typical on-resistance variation with analog signal and supply voltage. The usual on-resistance temperature coefficent is 0.5%/°C (typ).

Logic Inputs

The MAX301/MAX303/MAX305 operate with a single positive supply or with bipolar supplies. The devices maintain TTL compatibility with supplies anywhere in the ±4.5V to ±20V range as long as V_L = +5V. If V_L is connected to V+ or another supply at voltages other than +5V, the devices will operate at CMOS-logic level inputs.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. It is important not to exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with the supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ to V- should not exceed +44V.

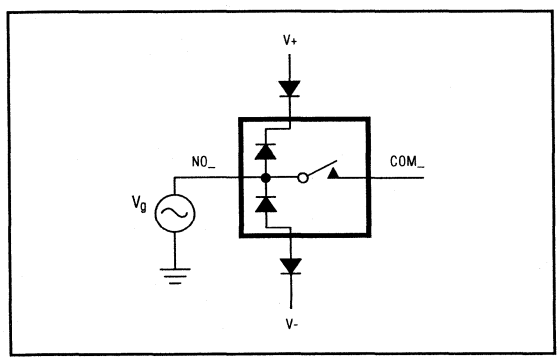


Figure 1. Overvoltage Protection Using Blocking Diodes

Precision, Dual, High-Speed Analog Switches

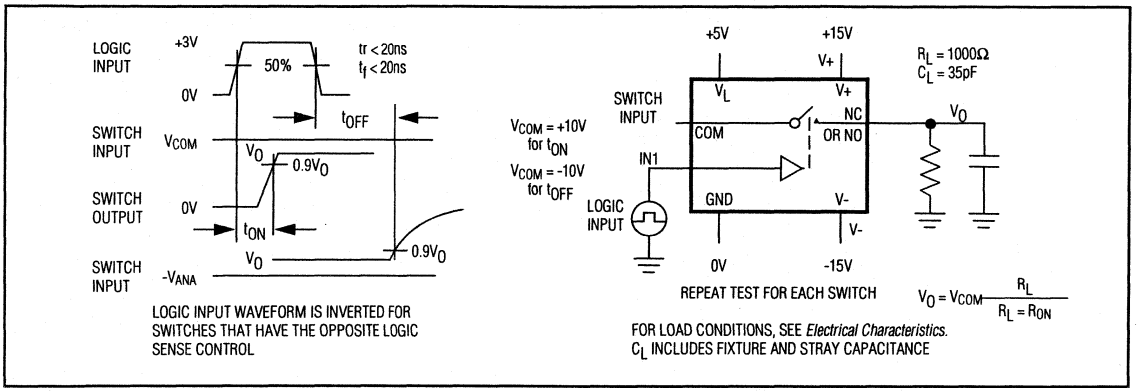


Figure 2. Switching-Time Test Circuit

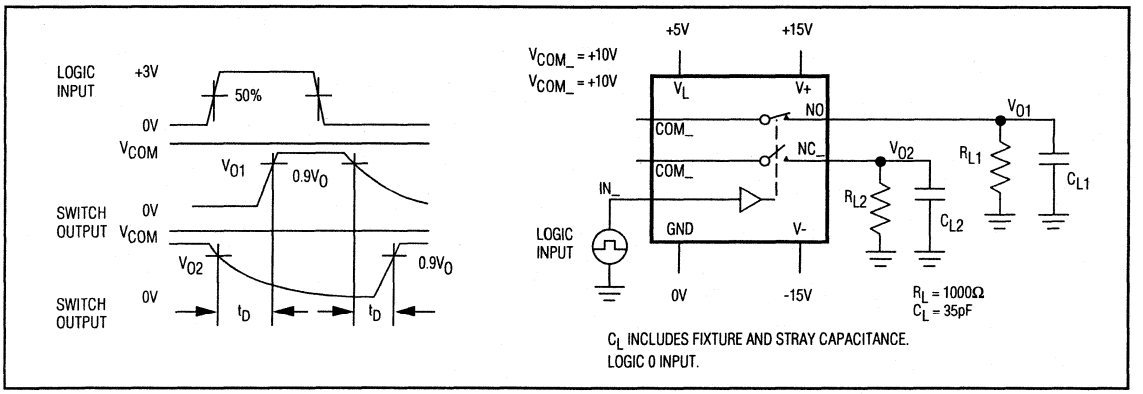


Figure 3. Break-Before-Make Test Circuit

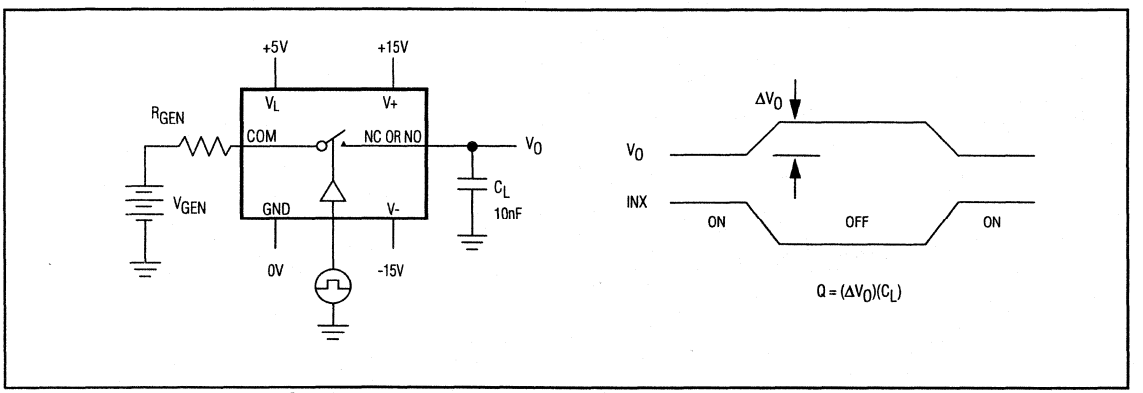
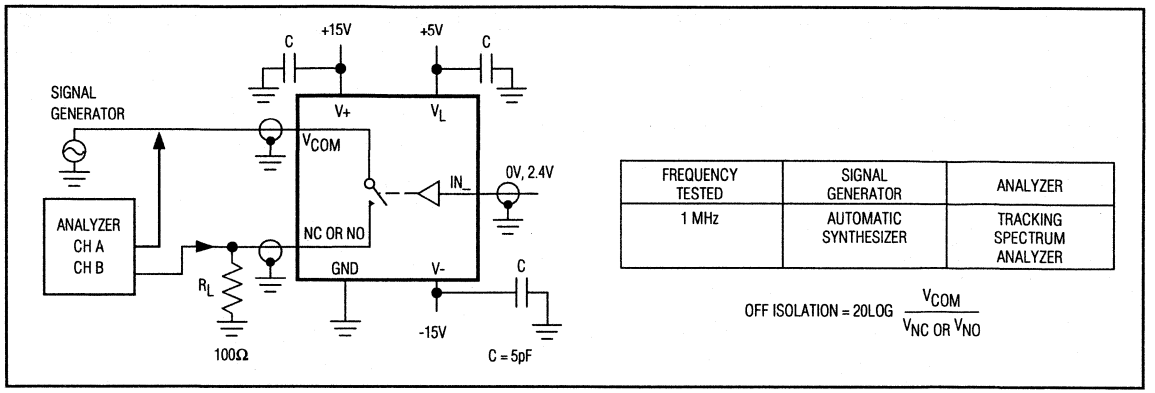


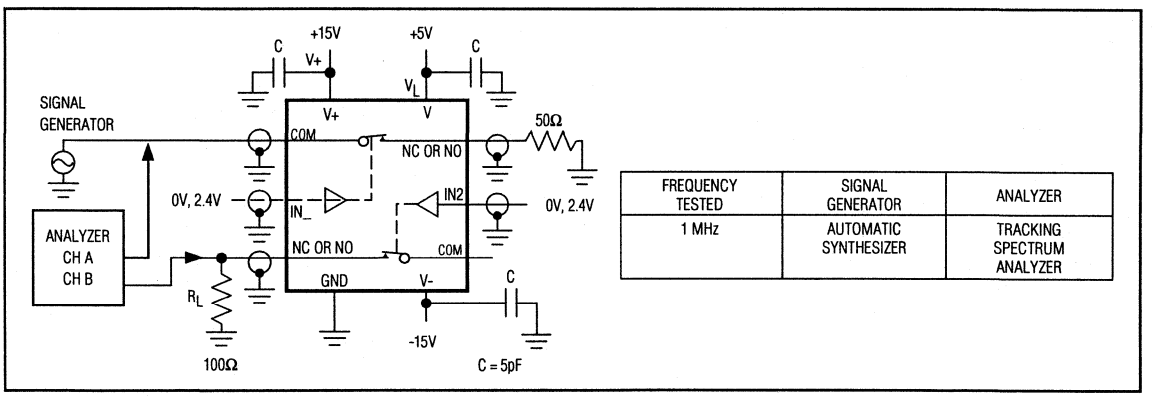
Figure 4. Charge-Injection Test Circuit



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
1 MHz	AUTOMATIC SYNTHESIZER	TRACKING SPECTRUM ANALYZER

$$\text{OFF ISOLATION} = 20\text{LOG}\ \frac{V_{COM}}{V_{NC\ OR\ V_{NO}}}$$

Figure 5. Off Isolation



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
1 MHz	AUTOMATIC SYNTHESIZER	TRACKING SPECTRUM ANALYZER

Figure 6. Crosstalk Test Circuit

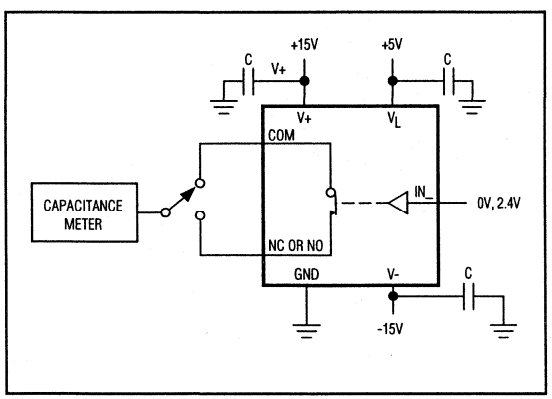


Figure 7. Channel-Off Capacitance

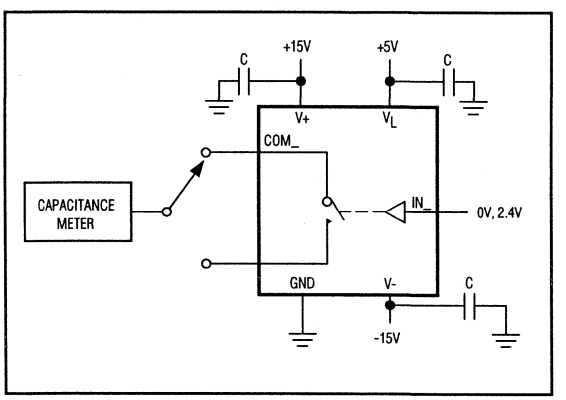


Figure 8. Channel-On Capacitance

Precision, Dual, High-Speed Analog Switches

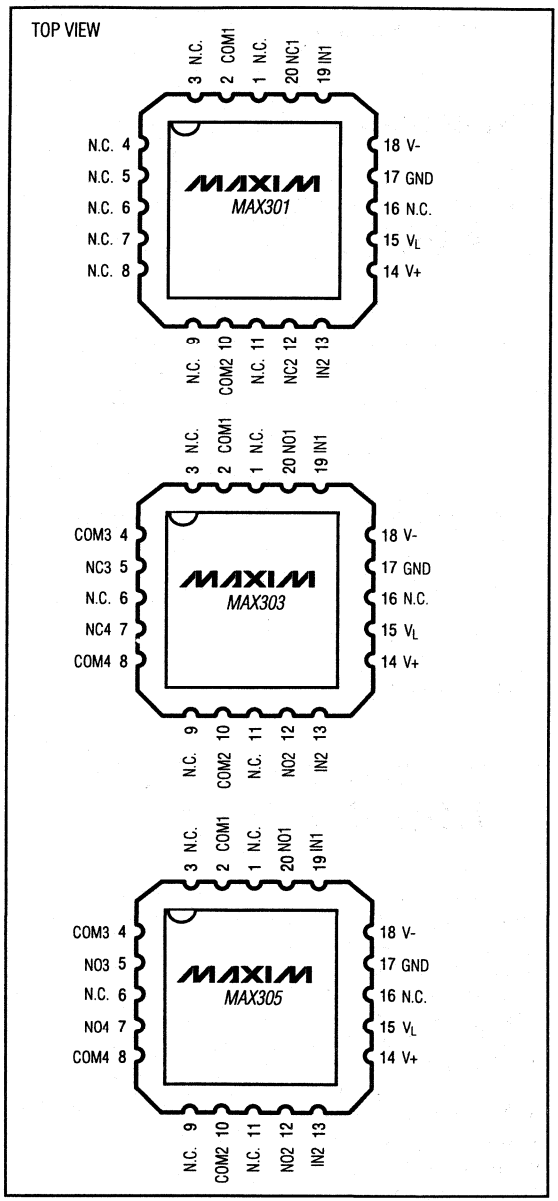
Ordering Information (continued)

PART	TEMP.RANGE	PIN-PACKAGE
MAX303CPE	0°C to +70°C	16 Plastic DIP
MAX303CSE	0°C to +70°C	16 Narrow SO
MAX303CJE	0°C to +70°C	16 CERDIP
MAX303C/D	0°C to +70°C	Dice*
MAX303EPE	-40°C to +85°C	16 Plastic DIP
MAX303ESE	-40°C to +85°C	16 Narrow SO
MAX303EJE	-40°C to +85°C	16 CERDIP
MAX303MJE	-55°C to +125°C	16 CERDIP
MAX303MLP	-55°C to +125°C	20 LCC**
MAX305CPE	0°C to +70°C	16 Plastic DIP
MAX305CSE	0°C to +70°C	16 Narrow SO
MAX305CJE	0°C to +70°C	16 CERDIP
MAX305C/D	0°C to +70°C	Dice*
MAX305EPE	-40°C to +85°C	16 Plastic DIP
MAX305ESE	-40°C to +85°C	16 Narrow SO
MAX305EJE	-40°C to +85°C	16 CERDIP
MAX305MJE	-55°C to +125°C	16 CERDIP
MAX305MLP	-55°C to +125°C	20 LCC**

* *Dice are tested at T_A = +25°C only.*

** *Contact factory for availability.*

Pin Configuration (continued)



19-0270; Rev 0; 8/94

MAXIM

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

General Description

The MAX306/MAX307 precision, monolithic, CMOS analog multiplexers (muxes) offer low on-resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the specified analog signal range (7Ω max). They also offer low leakage over temperature ($I_{NO(OFF)}$ less than 2.5nA at +85°C) and fast switching speeds (t_{TRANS} less than 250ns). The MAX306 is a single-ended 1-of-16 device, and the MAX307 is a differential 2-of-8 device.

The MAX306/MAX307 are fabricated with Maxim's improved 44V silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and guarantee electrostatic discharge (ESD) protection greater than 2000V.

These muxes operate with a single +4.5V to +30V supply, or bipolar ±4.5V to ±20V supplies, while retaining TTL/CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. These improved parts are plug-in upgrades for the industry-standard DG406, DG407, DG506A, and DG507A.

Applications

Sample-and-Hold Circuits
Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing

Features

- ♦ **Guaranteed On-Resistance Match Between Channels, <5Ω Max**
- ♦ **Low On-Resistance, <100Ω Max**
- ♦ **Guaranteed Flat On-Resistance over Specified Signal Range, 7Ω Max**
- ♦ **Guaranteed Charge Injection, <10pC**
- ♦ **$I_{NO(OFF)}$ Leakage <2.5nA at +85°C**
- ♦ **$I_{COM(OFF)}$ Leakage <20nA at +85°C**
- ♦ **ESD Protection >2000V**
- ♦ **Plug-In Upgrade for Industry-Standard DG406/DG407/DG506A/DG507A**
- ♦ **Single-Supply Operation (+4.5V to +30V) Bipolar-Supply Operation (±4.5V to ±20V)**
- ♦ **Low Power Consumption, <1.25mW**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **TTL/CMOS-Logic Compatible**

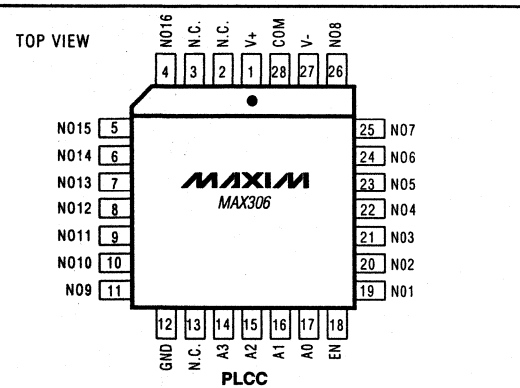
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX306CPI	0°C to +70°C	28 Plastic DIP
MAX306CWI	0°C to +70°C	28 Wide SO
MAX306C/D	0°C to +70°C	Dice*
MAX306EPI	-40°C to +85°C	28 Plastic DIP
MAX306EWI	-40°C to +85°C	28 Wide SO
MAX306EQI	-40°C to +85°C	28 PLCC
MAX306MJI	-55°C to +125°C	28 CERDIP

Ordering Information continued at end of data sheet.

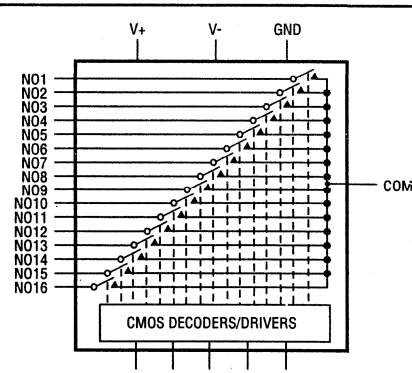
** Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams/Truth Tables



N.C. = NO INTERNAL CONNECTION

Continued at end of data sheet.



MAX306 16-CHANNEL SINGLE-ENDED MULTIPLEXER

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ .....-0.3V, 44V
GND .....-0.3V, 25V
Digital Inputs, NO, COM (Note 1).....(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal).....30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle max) 100mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
Wide SO (derate 12.50mW/°C above +70°C).....1000mW
PLCC (derate 10.53mW/°C above +70°C) 842mW
CERDIP (derate 16.67mW/°C above +70°C).....1333mW
Operating Temperature Ranges
MAX30_C_ _ .....0°C to +70°C
MAX30_E_ _.....-40°C to +85°C
MAX30_MJI.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NO, COM, A0, A1, A2, A3, or EN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)				-15		15	V
On-Resistance	R_{ON}	I_{NO} = -1.0mA, V_{COM} = ±10V		T_A = +25°C			60	100	Ω
				T_A = T_{MIN} to T_{MAX}				125	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{NO} = -1.0mA, V_{COM} = ±10V (Note 4)		T_A = +25°C			1.5	5	Ω
				T_A = T_{MIN} to T_{MAX}				8	
On-Resistance Flatness	R_{FLAT}	I_{NO} = -1.0mA, V_{COM} = ±5V or 0V		T_A = +25°C			1.8	7	Ω
				T_A = T_{MIN} to T_{MAX}				10	
NO-Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V_{COM} = ∓10V, V_{NO} = ±10V, V_{EN} = 0V		T_A = +25°C		-0.5	0.01	0.5	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
					M	-5.0		5.0	
COM-Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V_{NO} = ±10V, V_{COM} = ∓10V, V_{EN} = 0V	MAX306	T_A = +25°C		-0.75	0.02	0.75	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-20		20	
					M	-40		40	
		V_{NO} = ∓10V, V_{COM} = ±10V, V_{EN} = 0V	MAX307	T_A = +25°C		-0.75	0.02	0.75	
				T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
					M	-20		20	
COM-On Leakage Current (Note 5)	$I_{COM(ON)}$	V_{COM} = ±10V, V_{NO} = ±10V, sequence each switch on	MAX306	T_A = +25°C		-0.75	0.02	0.75	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-25		25	
					M	-50		50	
			MAX307	T_A = +25°C		-0.75	0.02	0.75	
				T_A = T_{MIN} to T_{MAX}	C, E	-12.5		12.5	
					M	-25		25	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V or 15V		-1.0		1.0	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V or 2.4V, V_A = 0V		-1.0		1.0	µA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V or 4.5V	T_A = +25°C		16	30	µA
			T_A = T_{MIN} to T_{MAX}			75	
		V_{EN} = 2.4V, $V_{A(ALL)}$ = 0V or 2.4V	T_A = +25°C		0.075	0.5	mA
			T_A = T_{MIN} to T_{MAX}			1	
Negative Supply Current	I-	V_{EN} = 2.4V, $V_{A(ALL)}$ = 0V or 2.4V	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC							
Transition Time	t_{TRANS}	Figure 2	T_A = +25°C		110	300	ns
			T_A = T_{MIN} to T_{MAX}			400	
Break-Before-Make Interval	t_{OPEN}	Figure 4	T_A = +25°C	10	40		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	T_A = +25°C		130	200	ns
			T_A = T_{MIN} to T_{MAX}			400	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	T_A = +25°C		55	150	ns
			T_A = T_{MIN} to T_{MAX}			300	
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω, Figure 5	T_A = +25°C		2	10	pC
Off Isolation (Note 6)	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz, Figure 6	T_A = +25°C		-69		dB
Crosstalk Between Channels	V_{CT}	V_{EN} = 2.4V, f = 100kHz, V_{GEN} = $1V_{P-P}$, R_L = 1kΩ, Figure 7	T_A = +25°C		-92		dB
Logic Input Capacitance	C_{IN}	f = 1MHz	T_A = +25°C		8		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, V_{EN} = V_{NO} = 0V, Figure 8	T_A = +25°C		8		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, V_{EN} = 0.8V, V_{COM} = 0V, Figure 8	MAX306, T_A = +25°C		130		pF
			MAX307, T_A = +25°C		65		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, V_{EN} = 2.4V, V_{COM} = 0V, Figure 8	MAX306, T_A = +25°C		140		pF
			MAX307, T_A = +25°C		70		

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)		0		12	V
On-Resistance	R_{ON}	I_{NO} = -1.0mA V_{COM} = 3V or 10V	T_A = +25°C		120	175	Ω
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	V_{NO1} = 8V, V_{NO8} = 0V, V_{IN} = 2.4V, Figure 1	T_A = +25°C		130	450	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3	T_A = +25°C		105	600	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3	T_A = +25°C		80	300	ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

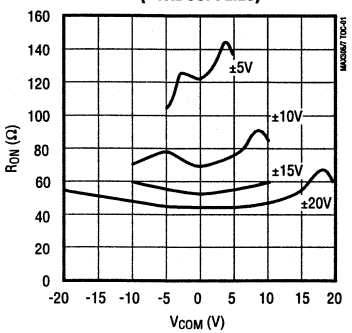
Note 6: Off isolation = 20log V_{COM}/V_{NO}, where V_{COM} = output and V_{NO} = input to off switch.

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

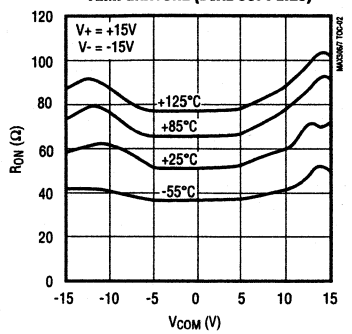
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

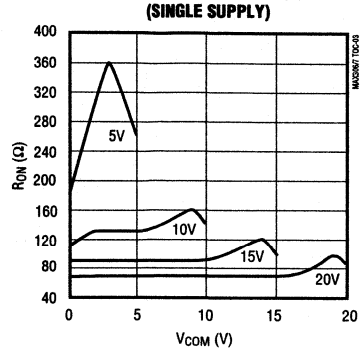
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



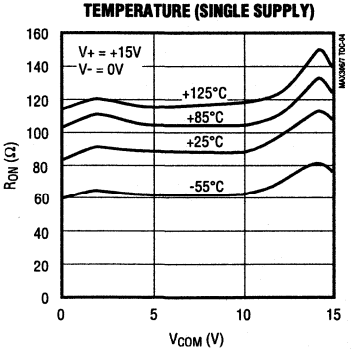
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



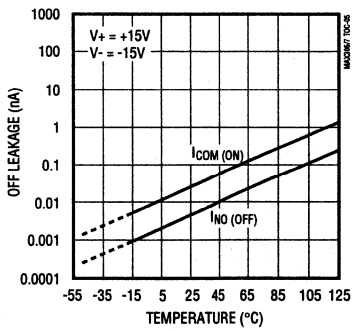
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



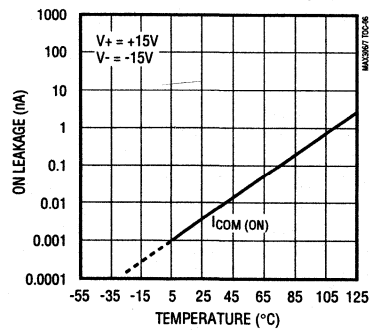
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



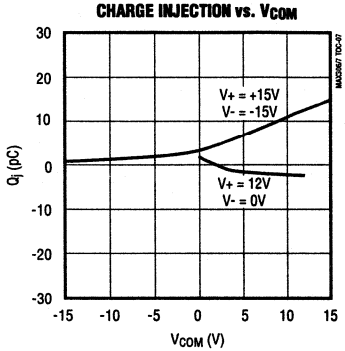
OFF LEAKAGE vs. TEMPERATURE



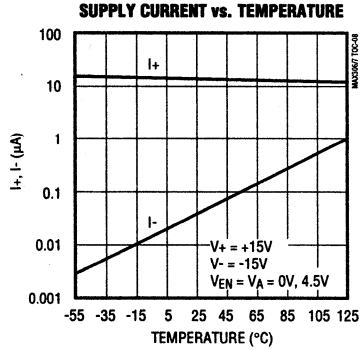
ON LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

Pin Descriptions

MAX306 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2, 3, 13	N.C.	No Internal Connections
4–11	NO16–NO9	Analog Inputs–bidirectional
12	GND	Ground
14–17	A3–A0	Address Inputs
18	EN	Enable Inputs
19–26	NO1–NO8	Analog Inputs–bidirectional
27	V-	Negative Supply Voltage Input
28	COM	Output–bidirectional

MAX307 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2	COMB	Output B–bidirectional
3, 13, 14	N.C.	No Internal Connection
4–11	NO8B–NO1B	Analog Inputs–bidirectional
12	GND	Ground
15, 16, 17	A2, A1, A0	Address Inputs
18	EN	Enable Input
19–26	NO1A–NO8A	Analog Inputs–bidirectional
27	V-	Negative Supply Voltage Input
28	COMA	Output A–bidirectional

Applications Information

Operation with Supply Voltages Other than ±15V

Using supply voltages other than ±15V will reduce the analog signal range. The MAX306/MAX307 switches operate with ±4.5V to ±20V bipolar supplies or with a +4.5V to +30V single supply; connect V- to GND when operating with a single supply. Also, both device types can operate with unbalanced supplies such as +24V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by either the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V above V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

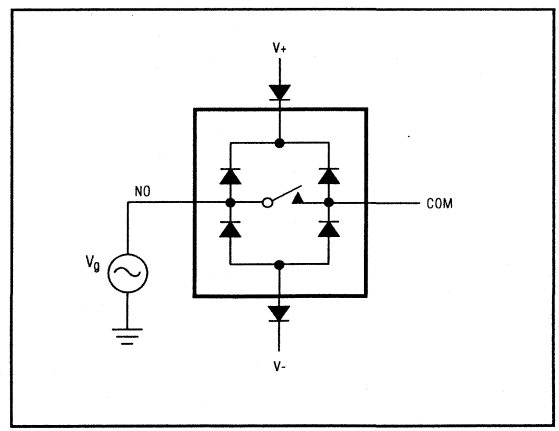


Figure 1. Overvoltage Protection Using External Blocking Diodes

Test Circuits/Timing Diagrams

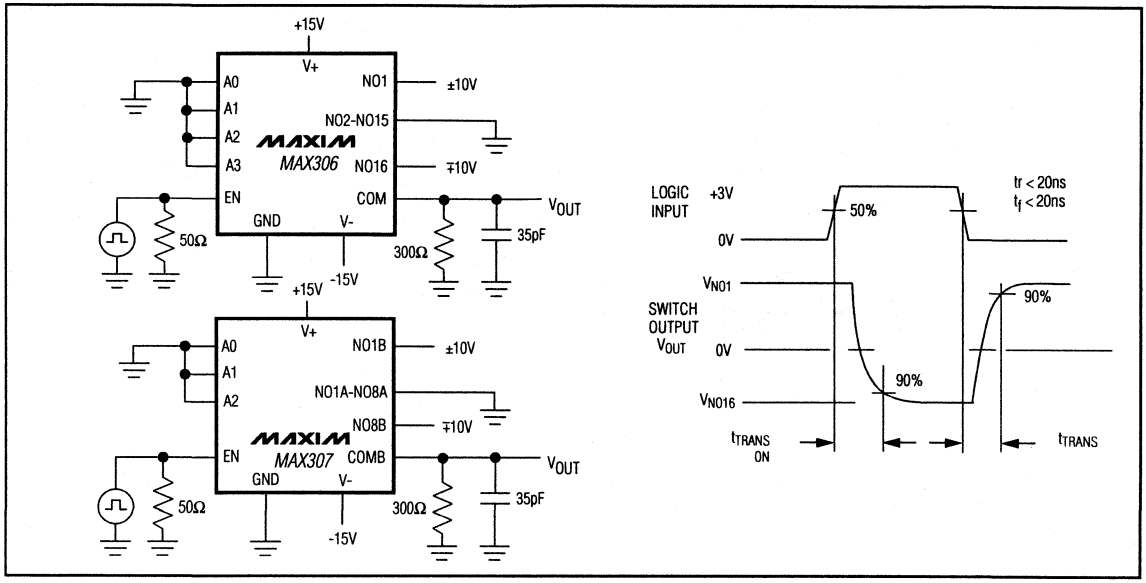


Figure 2. Transition Time

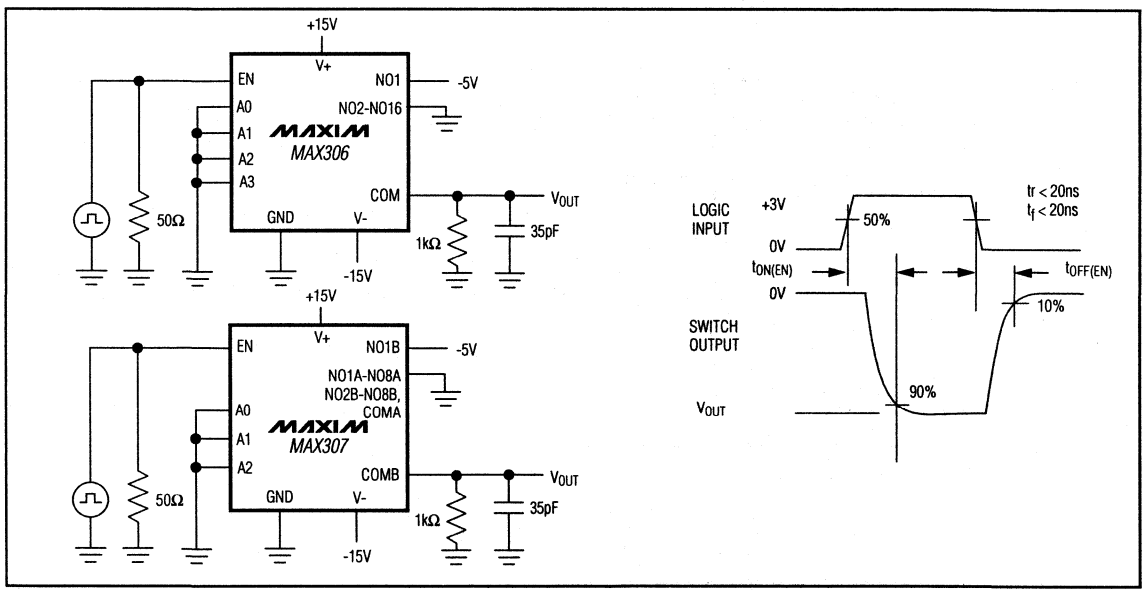


Figure 3. Enable Switching Time

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

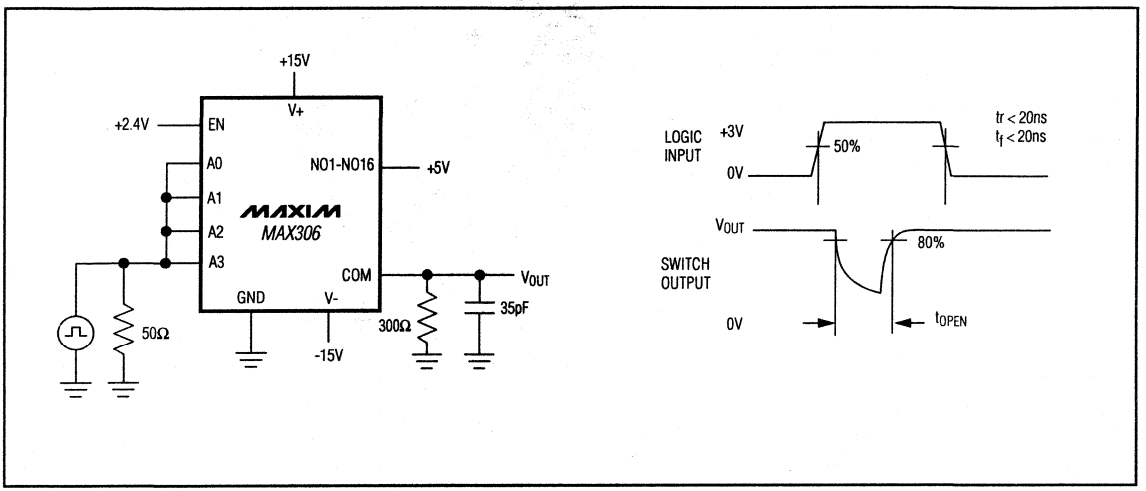


Figure 4. Break-Before-Make Interval

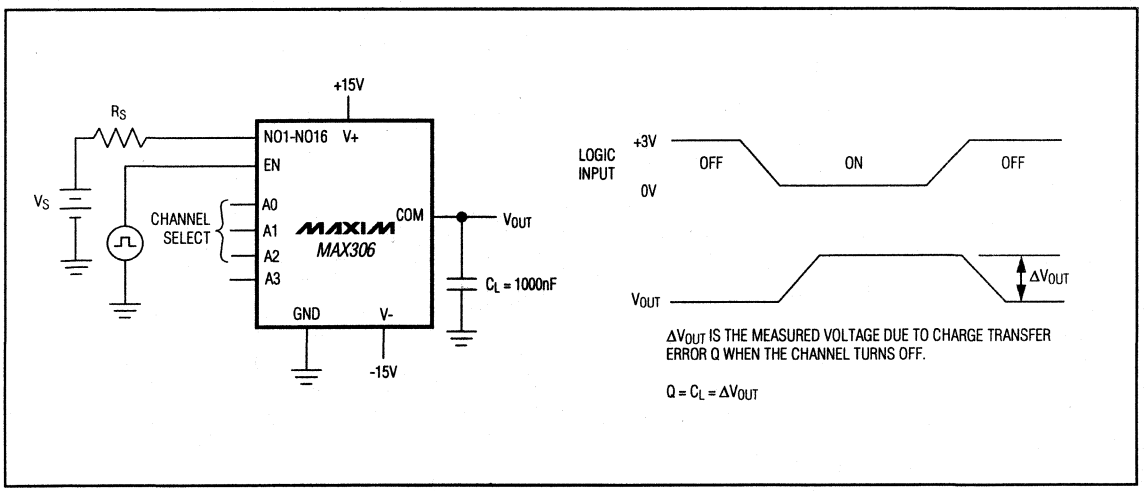


Figure 5. Charge Injection

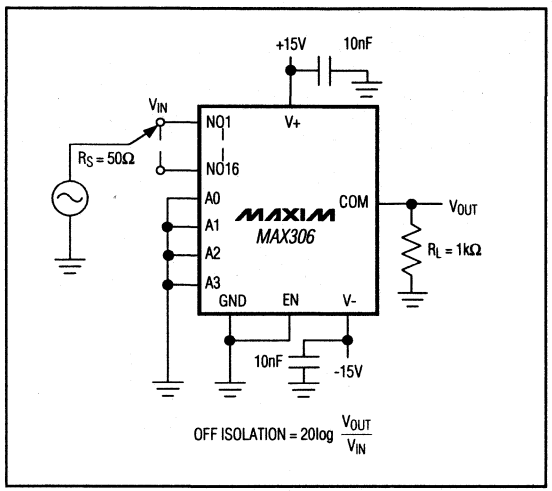


Figure 6. Off Isolation

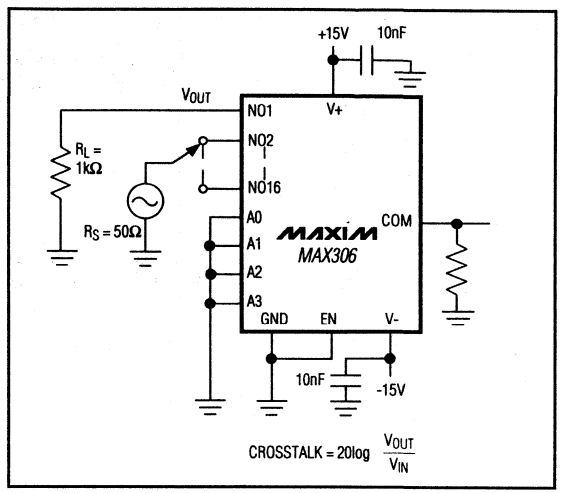


Figure 7. Crosstalk

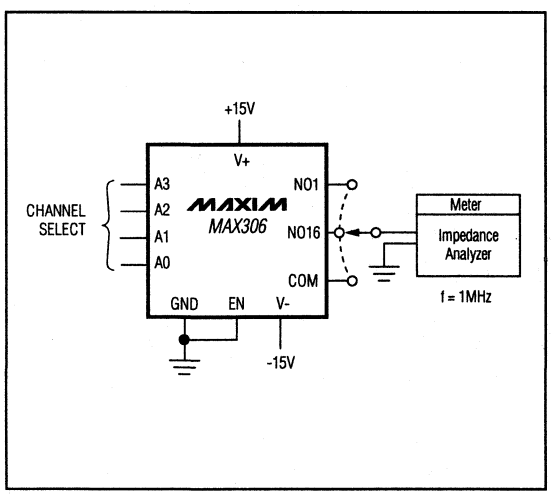
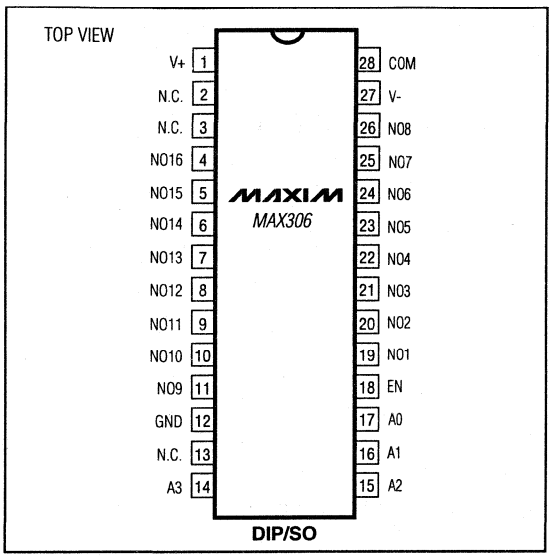


Figure 8. NO/COM Capacitance

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

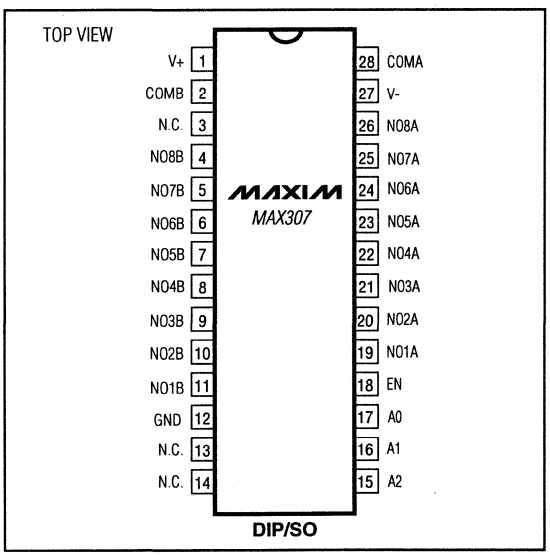
Pin Configurations/Functional Diagrams/Truth Tables (continued)



A3	A2	A1	A0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MAX306

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$



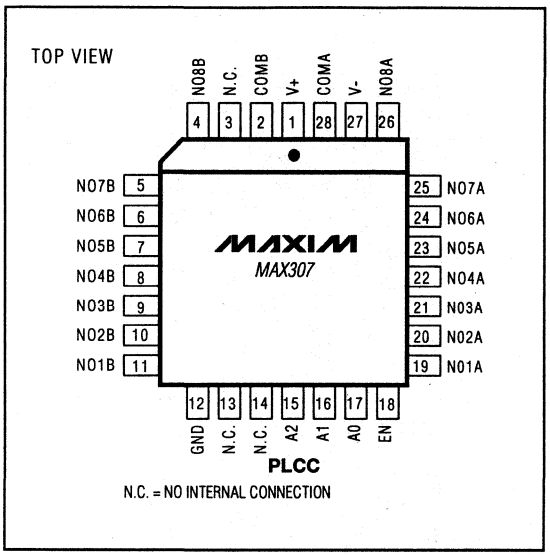
A2	A1	A0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

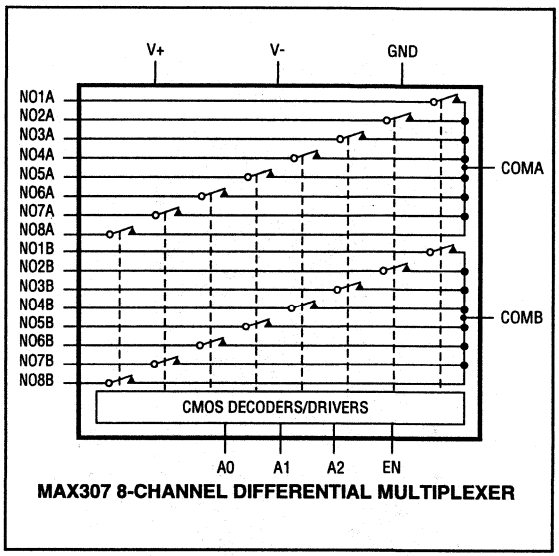
MAX307

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)





MAX307 8-CHANNEL DIFFERENTIAL MULTIPLEXER

Ordering Information (continued)

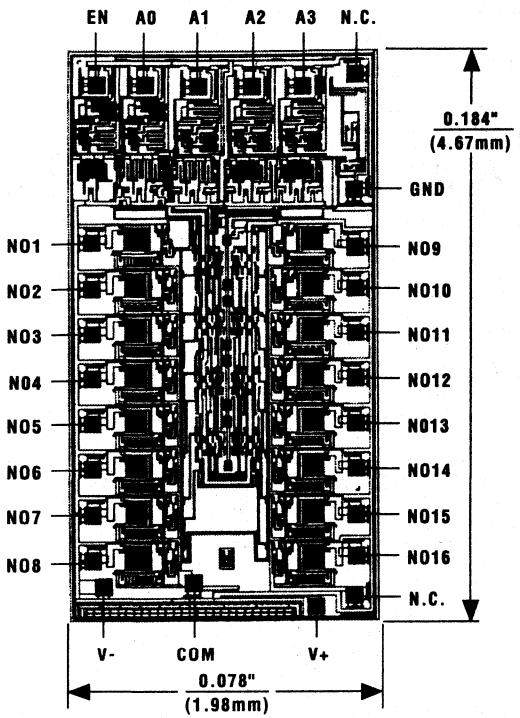
PART	TEMP. RANGE	PIN-PACKAGE
MAX307CPI	0°C to +70°C	28 Plastic DIP
MAX307CWI	0°C to +70°C	28 Wide SO
MAX307C/D	0°C to +70°C	Dice*
MAX307EPI	-40°C to +85°C	28 Plastic DIP
MAX307EWI	-40°C to +85°C	28 Wide SO
MAX307EQI	-40°C to +85°C	28 PLCC
MAX307MJI	-55°C to +125°C	28 CERDIP

** Contact factory for dice specifications.*

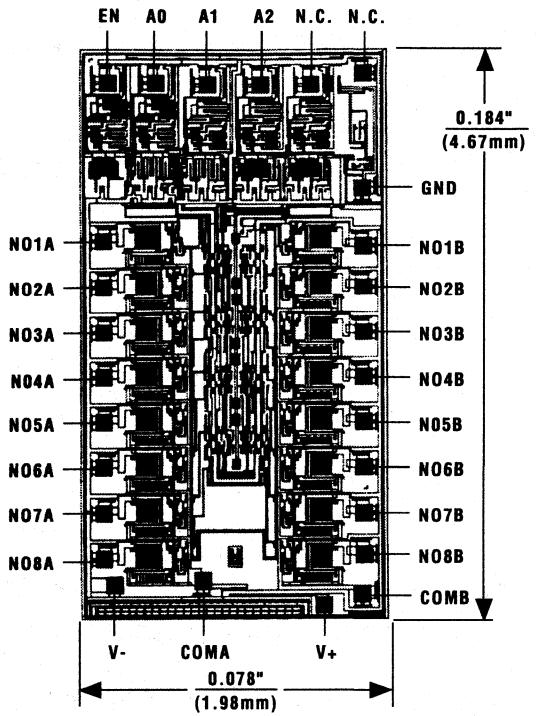
Precision, 16-Channel/Dual 8-Channel, High-Performance, CMOS Analog Multiplexers

Chip Topographies

MAX306



MAX307



N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 269
SUBSTRATE IS INTERNALLY CONNECTED TO V+

TRANSISTOR COUNT: 269
SUBSTRATE IS INTERNALLY CONNECTED TO V+

19-0271; Rev 0; 7/94

MAXIM

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

General Description

The MAX308/MAX309 precision, monolithic, CMOS analog multiplexers (muxes) offer low on-resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the specified analog signal range (7Ω max). They also offer low leakage over temperature (NO-off leakage current less than 5nA at +85°C) and fast switching speeds (transition time less than 250ns). The MAX308 is a single-ended 1-of-8 device, and the MAX309 is a differential 2-of-4 device.

The MAX308/MAX309 are fabricated with Maxim's improved 44V silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and guarantee electrostatic discharge protection greater than 2000V.

These muxes operate with a single +4.5V to +30V supply or bipolar ±4.5V to ±20V supplies, while retaining TTL/CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. These improved parts are plug-in upgrades for the industry-standard DG408, DG409, DG508A, and DG509A.

Applications

Sample-and-Hold Circuits
Automatic Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing

Features

- **Guaranteed On-Resistance Match Between Channels, <5Ω Max**
- **Low On-Resistance, <100Ω Max**
- **Guaranteed Flat On-Resistance over Specified Signal Range, 7Ω Max**
- **Guarateed Low Charge Injection, <10pC**
- **NO-Off Leakage Current <5nA at +85°C**
- **COM-Off Leakage Current <20nA at +85°C**
- **ESD Protection >2000V**
- **Plug-In Upgrade for Industry-Standard DG408/DG409/DG508A/DG509A**
- **Single-Supply Operation (+4.5V to +30V) Bipolar-Supply Operation (±4.5V to ±20V)**
- **Low Power Consumption, <300µW**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX308CPE	0°C to +70°C	16 Plastic DIP
MAX308CSE	0°C to +70°C	16 Narrow SO
MAX308C/D	0°C to +70°C	Dice*
MAX308EPE	-40°C to +85°C	16 Plastic DIP
MAX308ESE	-40°C to +85°C	16 Narrow SO
MAX308EJE	-40°C to +85°C	16 CERDIP
MAX308MJE	-55°C to +125°C	16 CERDIP**

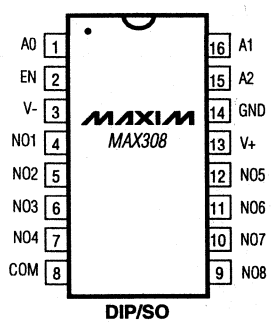
Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for availability.*

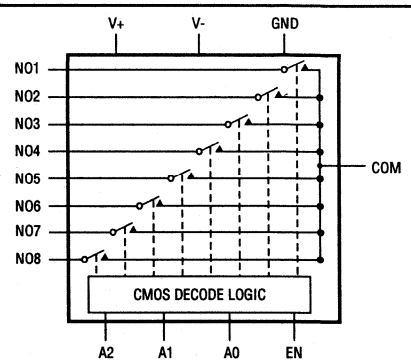
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

Continued at end of data sheet.



MAX308 8-CHANNEL SINGLE-ENDED MULTIPLEXER

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ .....-0.3V, 44V
GND .....-0.3V, 25V
Digital Inputs, NO, COM (Note 1).....(V- - 2V) to (V+ + 2V) or 30mA, (whichever occurs first)
Continuous Current (any terminal).....30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX30_C_ _ .....0°C to +70°C
MAX30_E_ _.....-40°C to +85°C
MAX30_MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NO, COM, EN, A0, A1, or A2 exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)				-15		15	V
On-Resistance	R_{ON}	I_{NO} = -1.0mA, V_{COM} = ±10V		T_A = +25°C			60	100	Ω
				T_A = T_{MIN} to T_{MAX}				125	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{NO} = -1.0mA, V_{COM} = ±10V (Note 4)		T_A = +25°C			1.5	5	Ω
				T_A = T_{MIN} to T_{MAX}				8	
On-Resistance Flatness	R_{FLAT}	I_{NO} = -1.0mA, V_{COM} = ±5V or 0V		T_A = +25°C			1.8	7	Ω
				T_A = T_{MIN} to T_{MAX}				10	
NO-Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V_{COM} = ∓10V, V_{NO} = ±10V, V_{EN} = 0V		T_A = +25°C		-0.5	0.01	0.5	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
					M	-5.0		5.0	
COM-Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V_{NO} = ±10V, V_{COM} = ∓10V, V_{EN} = 0V	MAX308	T_A = +25°C		-0.75	0.02	0.75	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
					M	-20		20	
		V_{NO} = ∓10V, V_{COM} = ±10V, V_{EN} = 0V	MAX309	T_A = +25°C		-0.75	0.02	0.75	
				T_A = T_{MIN} to T_{MAX}	C, E	-5		5	
					M	-10		10	
COM-On Leakage Current (Note 5)	$I_{COM(ON)}$	V_{COM} = ±10V, V_{NO} = ±10V, sequence each switch on	MAX308	T_A = +25°C		-0.75	0.02	0.75	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
					M	-20		20	
			MAX309	T_A = +25°C		-0.75	0.02	0.75	
				T_A = T_{MIN} to T_{MAX}	C, E	-5		5	
					M	-10		10	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
INPUT								
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V or 15V			-1.0		1.0	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V or 2.4V, V_A = 0V			-1.0		1.0	µA
SUPPLY								
Power-Supply Range					±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V or 4.5V		T_A = +25°C		16	30	µA
				T_A = T_{MIN} to T_{MAX}			75	
		V_{EN} = 2.4V, $V_{A(ALL)}$ = 0V or 2.4V		T_A = +25°C		0.075	0.5	mA
				T_A = T_{MIN} to T_{MAX}				
Negative Supply Current	I-	V_{EN} = 2.4V, $V_{A(ALL)}$ = 0V or 2.4V		T_A = +25°C	-1		1	µA
				T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC								
Transition Time	t_{TRANS}	Figure 2		T_A = +25°C		85	175	ns
				T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_{OPEN}	Figure 4		T_A = +25°C	10	40		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		T_A = +25°C		85	150	ns
				T_A = T_{MIN} to T_{MAX}			225	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		T_A = +25°C			150	ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω, Figure 5		T_A = T_{MIN} to T_{MAX}			300	pC
				T_A = +25°C		2	10	
Off Isolation (Note 6)	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz, Figure 6		T_A = +25°C		-75		dB
Crosstalk Between Channels	V_{CT}	V_{EN} = 2.4V, f = 100kHz, V_{GEN} = $1V_{P-P}$, R_L = 1kΩ, Figure 7		T_A = +25°C		-92		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		8		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, V_{EN} = V_{NO} = 0V, Figure 8		T_A = +25°C		3		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, V_{EN} = 0.8V, V_{COM} = 0V, Figure 8	MAX308	T_A = +25°C		26		pF
			MAX309			14		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, V_{EN} = 2.4V, V_{COM} = 0V, Figure 8	MAX308	T_A = +25°C		37		pF
			MAX309			25		

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)		0		12	V
On-Resistance	R_{ON}	I_{NO} = -1.0mA V_{COM} = 3V or 10V	T_A = +25°C		120	175	Ω
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	V_{NO1} = 8V, V_{NO8} = 0V, V_{IN} = 2.4V, Figure 2	T_A = +25°C		115	450	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3	T_A = +25°C		100	600	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3	T_A = +25°C		75	300	ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		2	10	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

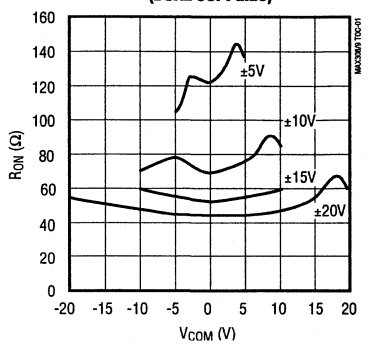
Note 6: Off isolation = 20log V_{COM}/V_{NO}, where V_{COM} = output and V_{NO} = input to off switch.

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

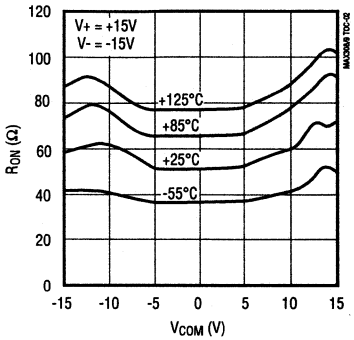
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

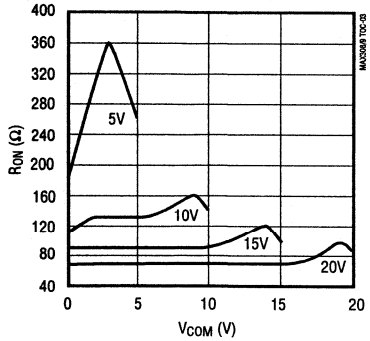
ON-RESISTANCE vs. VCOM (DUAL SUPPLIES)



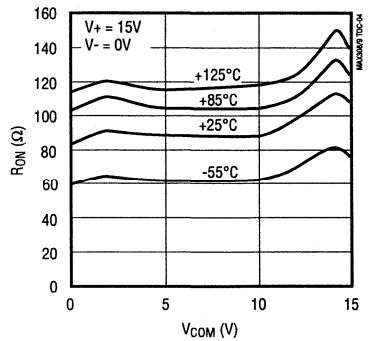
ON-RESISTANCE vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



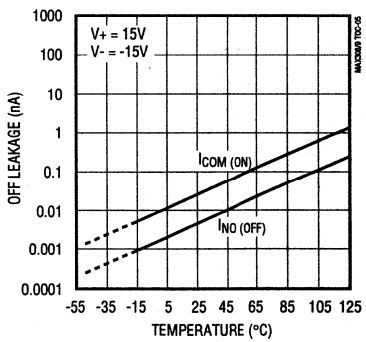
ON-RESISTANCE vs. VCOM (SINGLE SUPPLY)



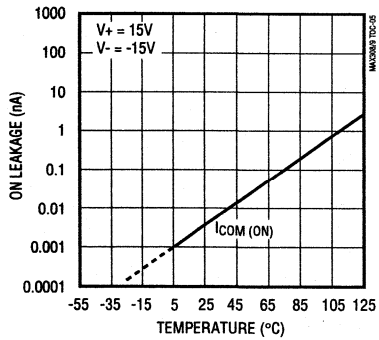
ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



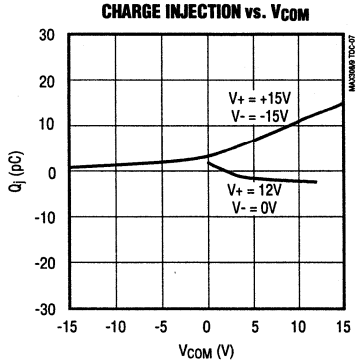
OFF LEAKAGE vs. TEMPERATURE



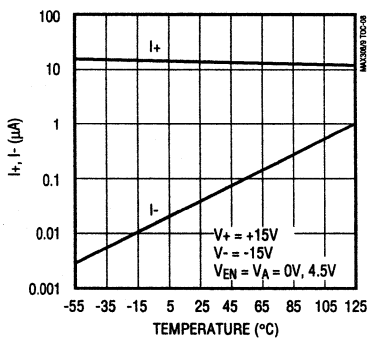
ON LEAKAGE vs. TEMPERATURE



CHARGE INJECTION vs. VCOM



SUPPLY CURRENT vs. TEMPERATURE



Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

Pin Description

PIN		NAME	FUNCTION
MAX308	MAX309		
1, 15, 16	—	A0, A2, A1	Address Inputs
—	1, 16	A0, A1	Address Inputs
2	2	EN	Enable Input
3	3	V-	Negative Supply Voltage Input
4–7	—	NO1–NO4	Analog Inputs—bidirectional
—	4–7	NO1A–NO4A	Analog Inputs—bidirectional
8	—	COM	Analog Output—bidirectional
—	8, 9	COMA, COMB	Analog Outputs—bidirectional
9–12	—	NO8–NO5	Analog Inputs—bidirectional
—	10–13	NO4B–NO1B	Analog Inputs—bidirectional
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

Applications Information

Operation with Supply Voltages Other than 15V

Using supply voltages less than ±15V will reduce the analog signal range. The MAX308/MAX309 switches operate with ±4.5V to ±20V bipolar supplies or with a +4.5V to +30V single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies, such as +24V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs, NO, or COM. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

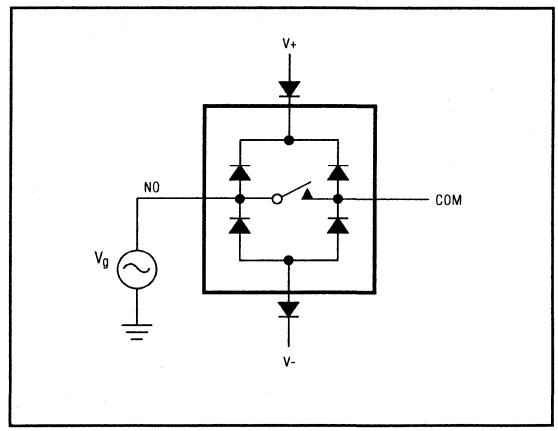


Figure 1. Overvoltage Protection Using External Blocking Diodes

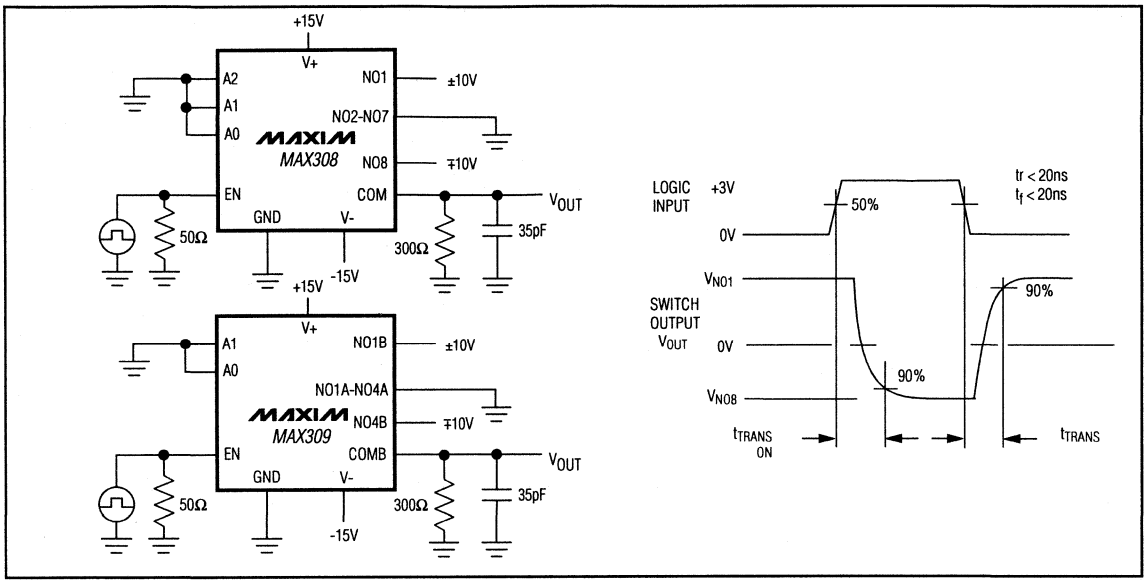


Figure 2. Transition Time

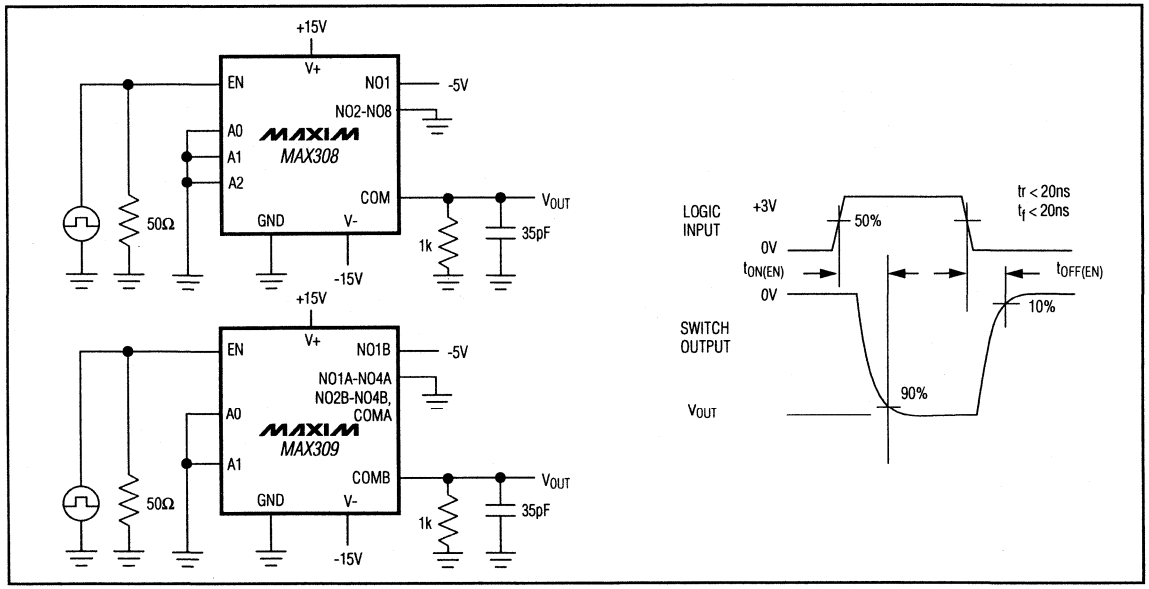


Figure 3. Enable Switching Time

Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

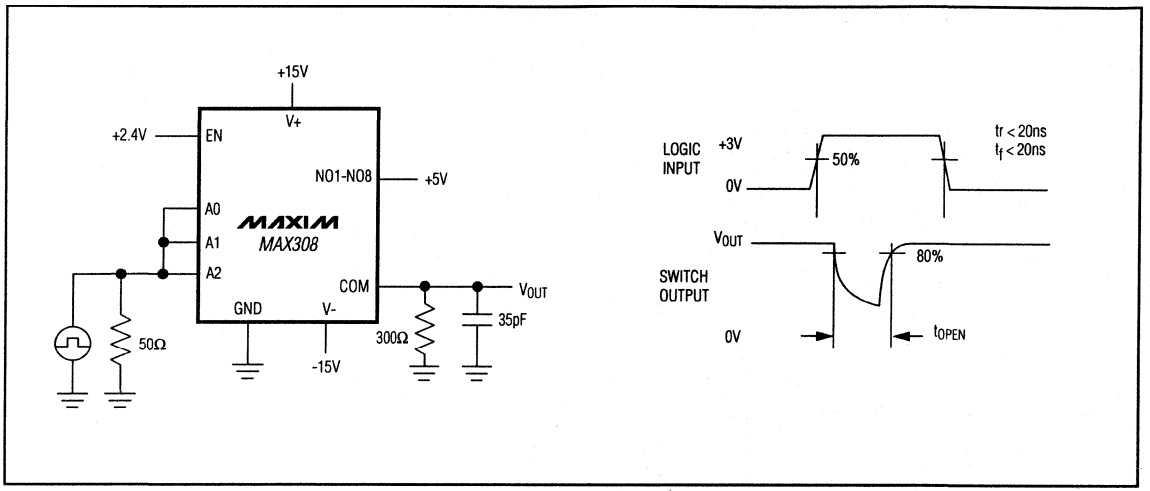


Figure 4. Break-Before-Make Interval

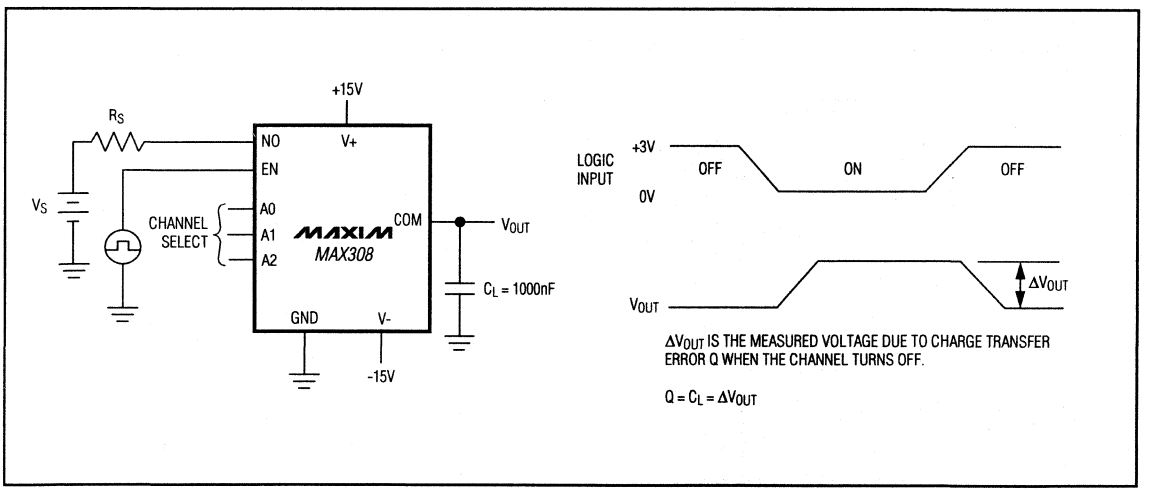


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)

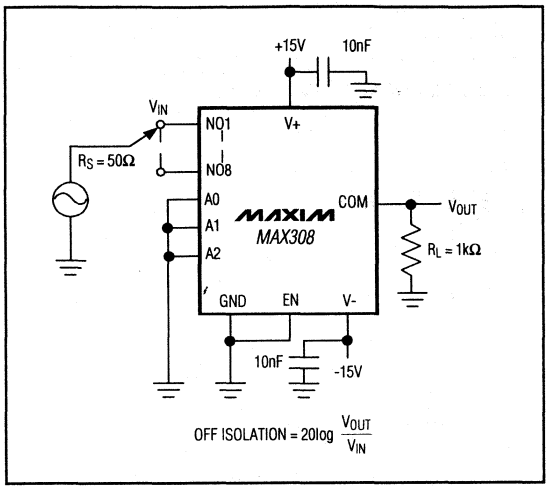


Figure 6. Off Isolation

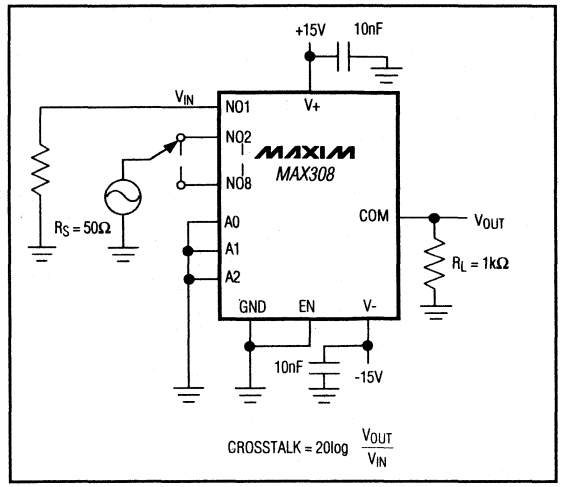


Figure 7. Crosstalk

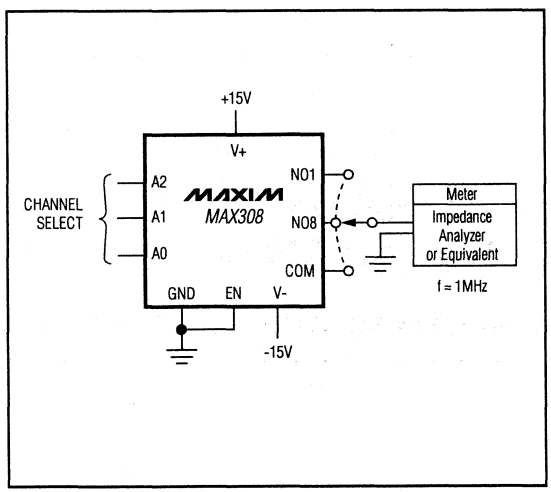
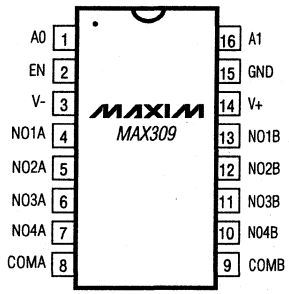


Figure 8. NO/COM Capacitance

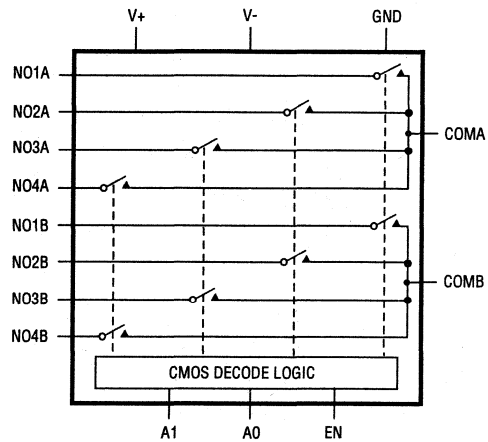
Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



DIP/SO



MAX309 4-CHANNEL DIFFERENTIAL MULTIPLEXER

A2	A1	A0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

MAX308

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

A1	A0	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

MAX309

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

_Ordering Information (continued)

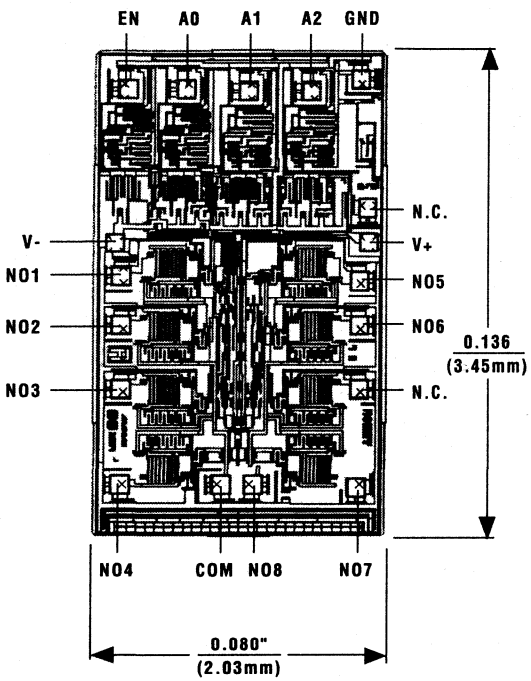
PART	TEMP. RANGE	PIN-PACKAGE
MAX309CPE	0°C to +70°C	16 Plastic DIP
MAX309CSE	0°C to +70°C	16 Narrow SO
MAX309C/D	0°C to +70°C	Dice*
MAX309EPE	-40°C to +85°C	16 Plastic DIP
MAX309ESE	-40°C to +85°C	16 Narrow SO
MAX309EJE	-40°C to +85°C	16 CERDIP
MAX309MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

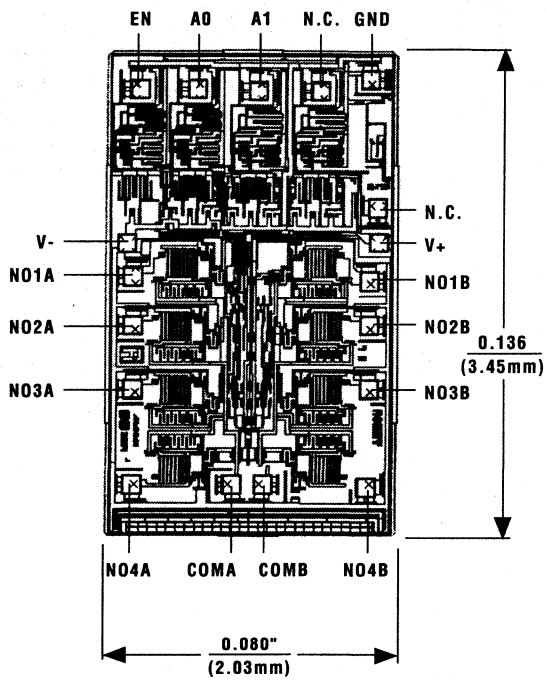
Precision, 8-Channel/Dual 4-Channel, High-Performance, CMOS Analog Multiplexers

Chip Topographies

MAX308



MAX309



N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 122
SUBSTRATE CONNECTED TO V+

TRANSISTOR COUNT: 122
SUBSTRATE CONNECTED TO V+

19-0185; Rev 0; 9/93

MAXIM

Precision, CMOS Analog Switches

General Description

The MAX317/MAX318/MAX319 are precision, CMOS, monolithic analog switches. The single-pole single-throw (SPST) MAX317 is normally closed (NC), the SPST MAX318 is normally open (NO), and the single-pole double-throw (SPDT) MAX319 has one normally open and one normally closed switch. All three parts offer low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 175ns and turn-off time less than 145ns).

The MAX317/MAX318/MAX319 are fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than ±2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Heads-Up Displays
Test Equipment
Military Radios
Communications Systems
Battery-Powered Systems
PBX, PABX

Features

- ♦ **Low On Resistance <20Ω Typical (35Ω Max)**
- ♦ **Guaranteed Matched On Resistance Between Channels <2Ω**
- ♦ **Guaranteed Flat On Resistance over Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection <10pC**
- ♦ **Guaranteed Off-Channel Leakage <6nA at +85°C**
- ♦ **ESD Guaranteed > 2000V per Method 3015.7**
- ♦ **Single-Supply Operation (+10V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ **TTL-/CMOS-Logic Compatible**
- ♦ **Rail-to-Rail Analog Signal Handling Capability**

Ordering Information

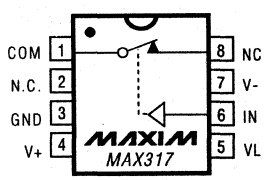
PART	TEMP. RANGE	PIN-PACKAGE
MAX317CPA	0°C to +70°C	8 Plastic DIP
MAX317CSA	0°C to +70°C	8 SO
MAX317CJA	0°C to +70°C	8 CERDIP
MAX317C/D	0°C to +70°C	Dice*
MAX317EPA	-40°C to +85°C	8 Plastic DIP
MAX317ESA	-40°C to +85°C	8 SO
MAX317EJA	-40°C to +85°C	8 CERDIP
MAX317MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

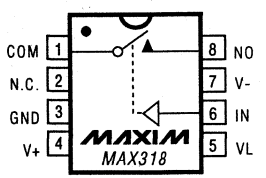
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



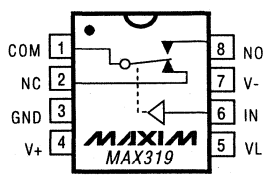
DIP/SO

MAX317	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX318	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

MAX319		
LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

N.C. = No Connect
NC = Normally Closed

SWITCHES SHOWN FOR LOGIC "0" INPUT

Precision, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... +44V
GND ..... +25V
V_L ..... (GND - 0.3V) to (V+ + 0.3V)
IN, COM, NC, NO ..... (V- - 2V) to (V+ + 2V) or 30mA, whichever occurs first
Continuous Current (any terminal) 30mA
Peak Current, NC, NO, COM
(pulsed at 1ms, 10% duty cycle max) 100mA
ESD ..... ±2000V

Continuous Power Dissipation (T_A = +70°C) (Note 1)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges:
MAX31_C_ _ ..... 0°C to +70°C
MAX31_E_ _ ..... -40°C to +85°C
MAX31_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS — Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP.		MIN	TYP (Note 2)	MAX	UNITS
Analog-Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)				-15		15	V
On Resistance	R_{ON}	V_{COM} = ±12.5V, $I_{(NC\ or\ NO)}$ = -10mA, V+ = 13.5V, V- = -13.5V		T_A = +25°C	C, E		20	35	Ω
					M			30	
				T_A = T_{MIN} to T_{MAX}				45	
On Resistance Match Between Channels (Note 4)	R_{ON}	$I_{(NC\ OR\ NO)}$ = -10mA, V_{COM} = 10V or -10V, V+ = 15V, V- = -15V		T_A = +25°C				2	Ω
				T_A = T_{MIN} to T_{MAX}				3	
On Resistance Flatness (Note 4)	R_{ON}	$I_{(NC\ OR\ NO)}$ = -10mA, V_{COM} = 5V or -5V, V+ = 15V, V- = -15V		T_A = +25°C				3	Ω
				T_A = T_{MIN} to T_{MAX}				5	
NO or NC Off Leakage Current	$I_{NC(OFF)}$ or $I_{NO(OFF)}$	V+ = 16.5V, V- = -16.5V, V_{COM} = ±15.5V, V_{NC} or V_{NO} = ±15.5V		T_A = +25°C		-0.25		0.25	nA
				C, E		-6		6	
				M		-20		20	
COM Off Leakage Current	$I_{COM(OFF)}$	V+ = 16.5V, V- = -16.5V, V_{COM} = ±15.5V, V_{NC} or V_{NO} = ±15.5V	MAX317, MAX318	T_A = +25°C		-0.25	-0.1	0.25	nA
				C, E		-6		6	
				M		-20		20	
			MAX319	T_A = +25°C		-0.75	-0.1	0.75	
				C, E		-10		10	
				M		-60		60	
COM On Leakage Current	$I_{COM(ON)}$	V+ = 16.5V, V- = -16.5V, V_{NC} or V_{NO} = V_D = ±15.5V	MAX317, MAX318	T_A = +25°C		-0.4		0.4	nA
				C, E		-10		10	
				M		-40		40	
			MAX319	T_A = +25°C		-0.75		0.75	
				C, E		-10		10	
				M		-60		60	

ELECTRICAL CHARACTERISTICS — Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP.	MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT								
Logic Input Current (Input Voltage High)	I_{IH}	V_{IN} = 2.4V			-0.5	0.005	0.5	µA
Logic Input Current (Input Voltage Low)	I_{IL}	V_{IN} = 0.8V			-0.5	0.005	0.5	µA
DYNAMIC								
Turn-On Time	t_{ON}	MAX317, MAX318, Figure 2, V_{COM} = ±10V		T_A = +25°C		100	175	ns
				T_A = T_{MIN} to T_{MAX}			250	
Turn-Off Time	t_{OFF}	MAX317, MAX318, Figure 2, V_{COM} = ±10V		T_A = +25°C		60	145	ns
				T_A = T_{MIN} to T_{MAX}			210	
Transition Time	t_{TRANS}	MAX319, Figure 3, V_{NO} = ±10V, V_{NC} = ±10V		T_A = +25°C			175	ns
				T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_D	MAX319, Figure 4, V_{NO} = V_{NC} = ±10V		T_A = +25°C	5	13		ns
Charge Injection	Q	V_{GEN} = 0V, Figure 5		T_A = +25°C		3	10	pC
Off Isolation (Note 5)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 7		T_A = +25°C		68		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 8		T_A = +25°C		85		dB
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} = 0V, f = 1MHz, Figure 8		T_A = +25°C		8		pF
Off Capacitance NC or NO	$C_{(OFF)}$	V_{COM} = 0V, f = 1MHz, Figure 8		T_A = +25°C		8		pF
Channel-On Capacitance COM Terminal	$C_{COM(ON)}$	V_S = 0V, f = 1MHz, Figure 9	MAX317, MAX318	T_A = +25°C		30		pF
			MAX319			35		
SUPPLY								
Positive Supply Current	I+	V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V		T_A = +25°C	-1	0.0001	1	µA
				T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V		T_A = +25°C	-1	-0.0001	1	µA
				T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V		T_A = +25°C	-1	0.0001	1	µA
				T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V		T_A = +25°C	-1	-0.0001	1	µA
				T_A = T_{MIN} to T_{MAX}	-5		5	

ELECTRICAL CHARACTERISTICS — Single Supply

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog-Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)	0		12	V
Drain-Source On Resistance	$R_{(ON)}$	$I_{(NC\ or\ NO)}$ = -10mA, V_{COM} = 3.8V, V+ = 10.8V		40	100	Ω
DYNAMIC						
Turn-On Time	t_{ON}	V_{COM} = 8V, Figure 2		110		ns
Turn-Off Time	t_{OFF}	V_{COM} = 8V, Figure 2		40		ns
Break-Before-Make Time Delay	t_D	MAX319, R_L = 1000Ω, C_L = 35pF, Figure 4		60		ns
Charge Injection	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 5		2	10	pC
SUPPLY						
Positive Supply Current	I+	V+ = 13.2V, all channels on or off, V_{IN} = 0V or 5V, V_L = 5.25V		0.0001		µA
Negative Supply Current	I-	V+ = 13.2V, all channels on or off, V_{IN} = 0V or 5V, V_L = 5.25V		0.0001		µA
Logic Supply Current	I_L	V_L = 5.25V, all channels on or off, V_{IN} = 0V or 5V		0.0001		µA
Ground Current	I_{GND}	V_L = 5.25V, all channels on or off, V_{IN} = 0V or 5V		-0.0001		µA

Note 2: Typical values are for **design aid only**, not guaranteed, not subject to production testing.

Note 3: Guaranteed by design.

Note 4: On resistance match between channels and flatness are guaranteed only with bipolar-supply operation.

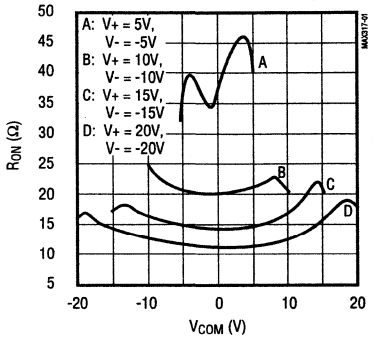
Note 5: Off Isolation = $20\log_{10}\left(\frac{V_{COM}}{V_{NC}\ or\ V_{NO}}\right)$, V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

Note 6: Between any two switches.

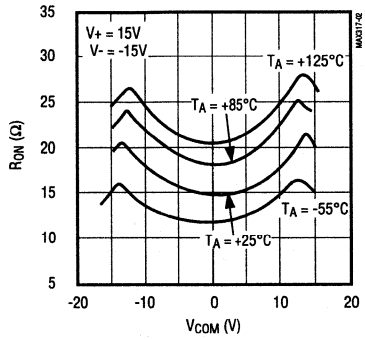
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted).

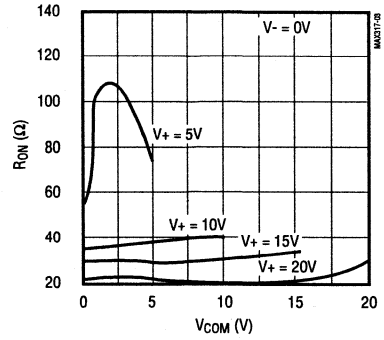
ON RESISTANCE vs. VCOM AND POWER-SUPPLY VOLTAGE



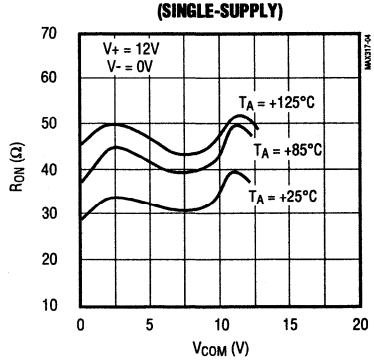
ON RESISTANCE vs. VCOM AND TEMPERATURE



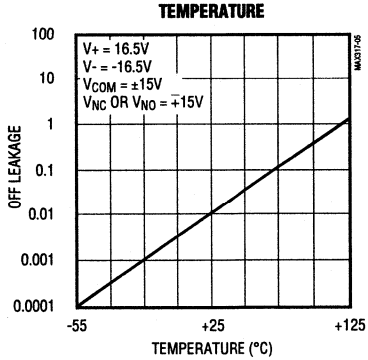
ON RESISTANCE vs. VCOM AND TEMPERATURE



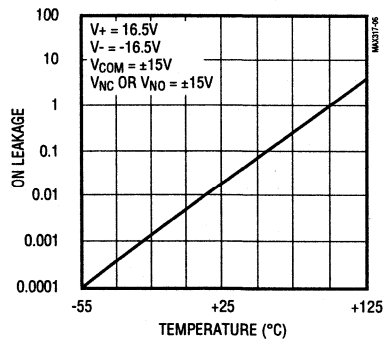
ON RESISTANCE vs. VCOM (SINGLE-SUPPLY)



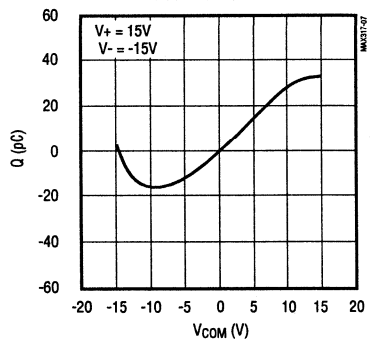
OFF LEAKAGE CURRENTS vs. TEMPERATURE



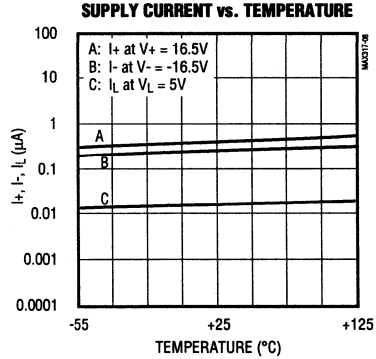
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Precision, CMOS Analog Switches

Pin Description

PIN			NAME	FUNCTION
MAX317	MAX318	MAX319		
1	1	1	COM	Analog-switch common terminal
2	2	—	N.C.	No connect — not internally connected
—	—	2	NO	Analog-switch normally open terminal
3	3	3	GND	Logic ground
4	4	4	V+	Analog-signal positive supply input
5	5	5	VL	Logic-level positive supply input
6	6	6	IN	Logic-level input
7	7	7	V-	Analog-signal negative supply input
8	—	8	NC	Analog-switch normally closed terminal
—	8	—	NO	Analog-switch normally open terminal

Applications Information

Operation with Supply Voltages Other Than ±15V

The main limitation of supply voltages other than ±15V is analog signal range reduction. The MAX317/MAX318/MAX319 switches operate with bipolar supplies of ±5V to ±20V. Typical Operating Characteristics graphs show typical on resistance for ±15V, ±10V, and ±5V supplies. Switching times increase by a factor of two or more for operation at ±5V. The MAX317/MAX318/MAX319 can operate from unipolar supplies of +10V to +30V. Both parts can also operate from unbalanced supplies such as +24V and -5V.

Connect V- to 0V when operating with a single supply. This means that VL must be connected to +5V to be TTL compatible, or to V+ for CMOS logic input levels.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. It is important not to exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, protect the devices from overvoltage by adding two small signal diodes in series with the supply pins (Figure 1). Adding the diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ to V- should not exceed +44V.

Test Circuits/Timing Diagrams

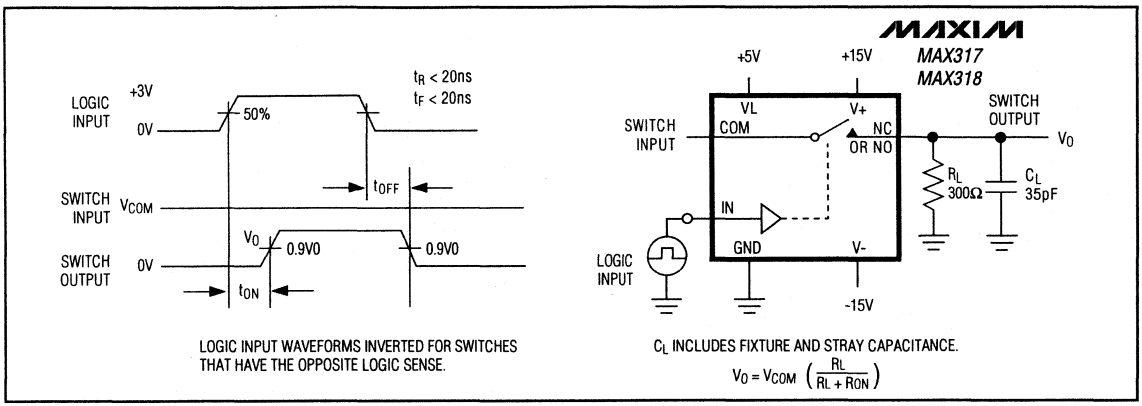


Figure 2. MAX317/MAX318 Switching-Time Test Circuit

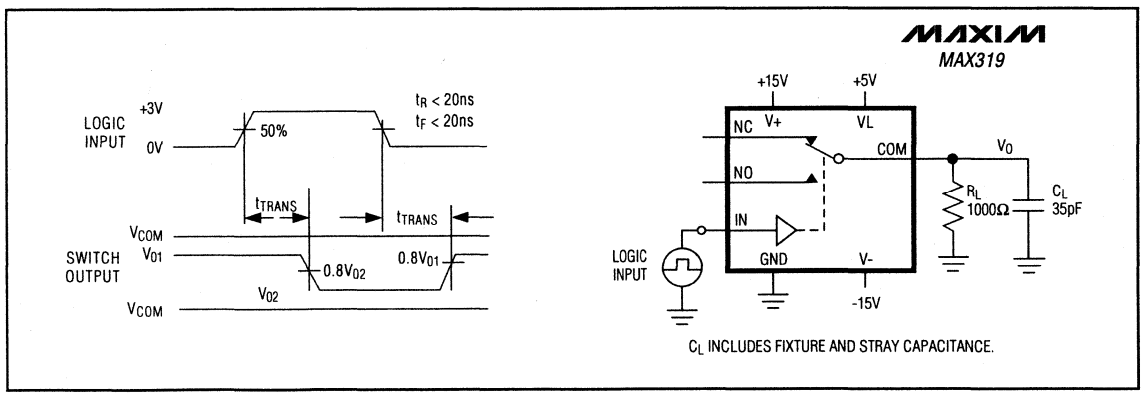


Figure 3. MAX319 Transition Time

Precision, CMOS Analog Switches

Test Circuits/Timing Diagrams (continued)

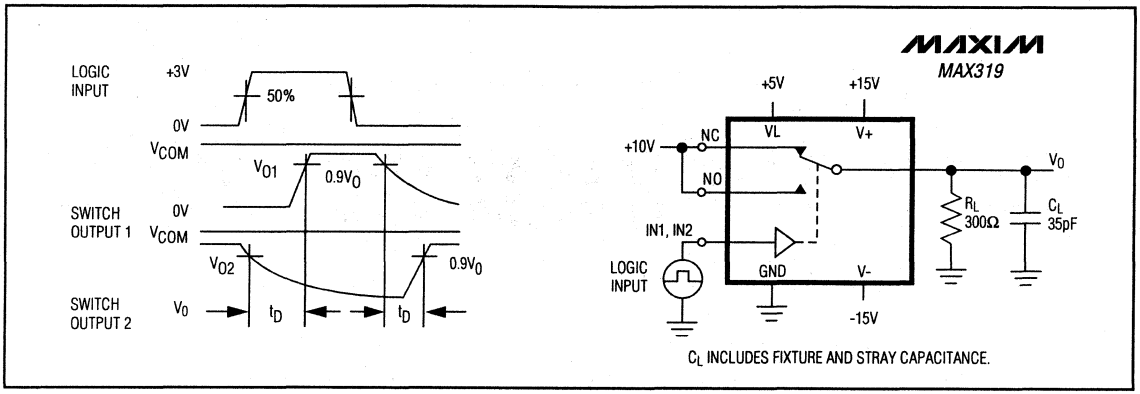


Figure 4. MAX319 Break-Before-Make Test Circuit

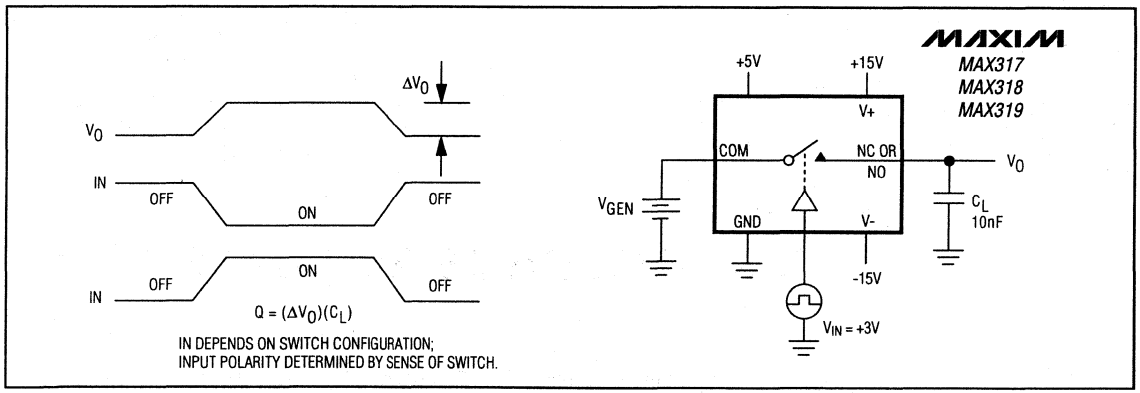


Figure 5. Charge-Injection Test Circuit

Test Circuits/Timing Diagrams (continued)

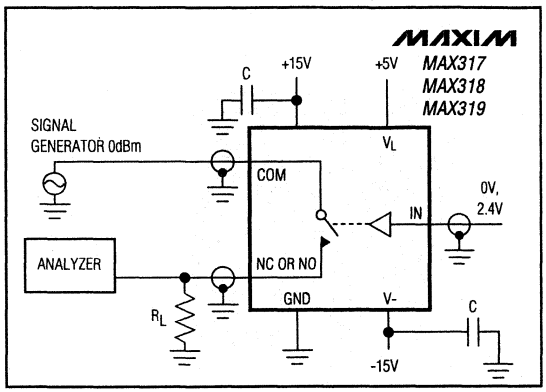


Figure 6. Off-Isolation Test Circuit

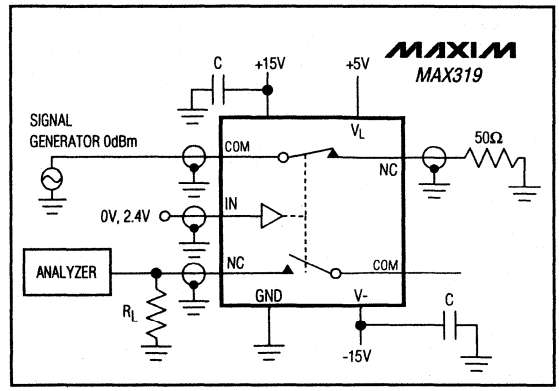


Figure 7. MAX319 Crosstalk Test Circuit

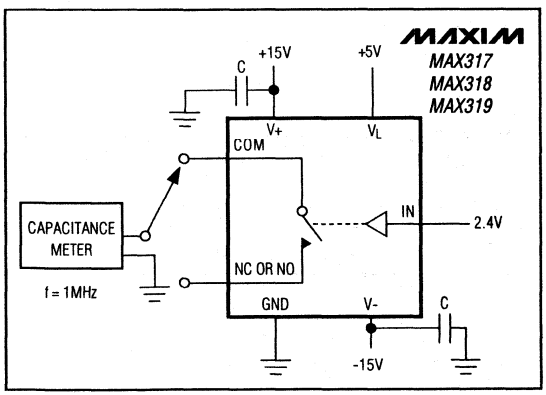


Figure 8. Channel-Off Capacitance Test Circuit

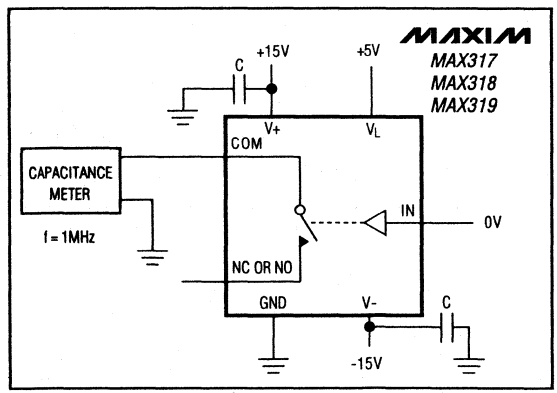


Figure 9. Channel-On Capacitance Test Circuit

Precision, CMOS Analog Switches

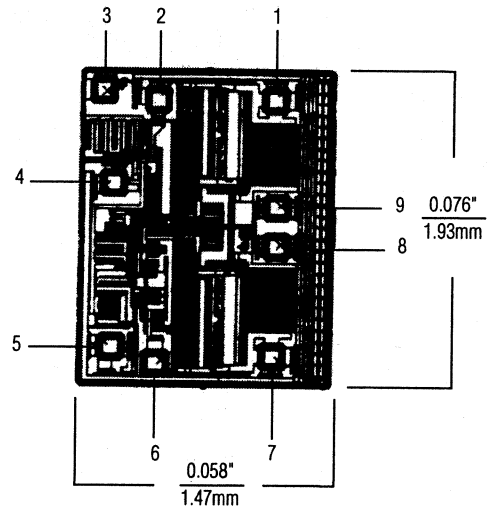
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX318CPA	0°C to +70°C	8 Plastic DIP
MAX318CSA	0°C to +70°C	8 SO
MAX318CJA	0°C to +70°C	8 CERDIP
MAX318C/D	0°C to +70°C	Dice*
MAX318EPA	-40°C to +85°C	8 Plastic DIP
MAX318ESA	-40°C to +85°C	8 SO
MAX318 EJA	-40°C to +85°C	8 CERDIP
MAX318MJA	-55°C to +125°C	8 CERDIP**
MAX319CPA	0°C to +70°C	8 Plastic DIP
MAX319CSA	0°C to +70°C	8 SO
MAX319CJA	0°C to +70°C	8 CERDIP
MAX319C/D	0°C to +70°C	Dice*
MAX319EPA	-40°C to +85°C	8 Plastic DIP
MAX319ESA	-40°C to +85°C	8 SO
MAX319EJA	-40°C to +85°C	8 CERDIP
MAX319MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 32;
SUBSTRATE CONNECTED TO V+.

DIE PAD	MAX317	MAX318	MAX319
1	COM	NC	NO
2	GND	GND	GND
3	V+	V+	V+
4	VL	VL	VL
5	IN	IN	IN
6	V-	V-	V-
7	N.C.	NO	NC
8	N.C.	COM	COM
9	NC	NC	COM

19-0189; Rev 0; 9/93

MAXIM

Precision, Quad, SPDT, CMOS Analog Switch

General Description

The MAX333A is a precision, quad, single-pole double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from ±4.5V to ±20V, or with a single-ended supply between +10V and +30V. The MAX333A offers low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range (Δ3Ω max). It also offers break-before-make switching (10ns typical), with turn-off times less than 145ns and turn-on times less than 175ns. The MAX333A is ideal for portable operation since quiescent current runs less than 50µA with all inputs high or low.

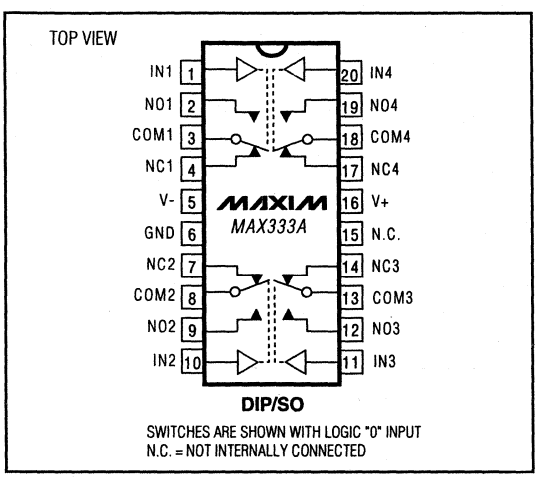
This monolithic, quad switch is fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (3.75mW), and electrostatic discharge (ESD) greater than 2000V.

Logic inputs are TTL and CMOS compatible and guaranteed over a +0.8V to +2.4V range—regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage.

Applications

Test Equipment
Communications Systems
PBX, PABX
Heads-Up Displays
Portable Instruments

Pin Configuration



Features

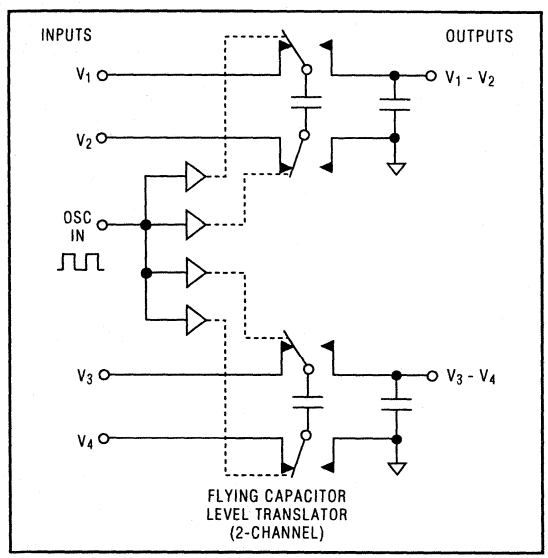
- ♦ **Upgraded Replacement for a DG211/DG212 Pair or Two DG403s**
- ♦ **Low On Resistance < 17Ω Typical (35Ω Max)**
- ♦ **Guaranteed Matched On Resistance Between Channels < 2Ω**
- ♦ **Guaranteed Flat On Resistance over Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection < 10pC**
- ♦ **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ♦ **ESD Guaranteed > 2000V per Method 3015.7**
- ♦ **Single-Supply Operation (+10V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ **TTL-/CMOS-Logic Compatibility**
- ♦ **Rail-to-Rail Analog Signal Handling Capability**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX333ACPP	0°C to +70°C	20 Plastic DIP
MAX333ACWP	0°C to +70°C	20 Wide SO
MAX333AC/D	0°C to +70°C	Dice*
MAX333AEPP	-40°C to +85°C	20 Plastic DIP
MAX333AEWP	-40°C to +85°C	20 Wide SO
MAX333AMJP	-55°C to +125°C	20 CERDIP

* *Contact factory for dice specifications.*

Typical Operating Circuit



Precision, Quad, SPDT, CMOS Analog Switch

ABSOLUTE MAXIMUM RATINGS

V+ to V- 44V
V_{IN}, V_{COM}, V_{NO}, V_{NC} ..... V- to V+
(V_{NO} - V_{NC}) 32V
V+ to Ground 30V
V- to Ground ..... -30V
Current, Any Terminal Except V_{COM}, V_{NO}, or V_{NC} 30mA
Continuous Current, V_{COM}, V_{NO}, or V_{NC} 20mA
Peak Current, V_{COM}, V_{NO}, or V_{NC}
(Pulsed at 1ms, 10% duty cycle max) 70mA
ESD 2000V

Continuous Power Dissipation (T_A = +70°C) (Note 1)
Plastic DIP (derate above +70°C by 11.11mW/°C) 889mW
SO (derate above +70°C by 10.00mW/°C) 800mW
CERDIP (derate above +70°C by 11.11mW/°C) 889mW
Operating Temperature Ranges:
MAX333AC_ _ ..... 0°C to +70°C
MAX333AE_ _ ..... -40°C to +85°C
MAX333AMJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Device mounted with all leads soldered to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(GND = 0V, V+ = +15V, V- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Notes 2, 3)	MAX	UNITS
POWER REQUIREMENTS							
Positive Supply Current	I+	V_{IN} = 0V/5V, V+ = 16.5V, V- = -16.5V			0.05	0.25	mA
Supply Voltage Range	V+/V-	Dual supply, |V+| = |V-|		±4.5V		±20	V
	V+	Single supply, V- = GND		10		30	
Negative Supply Current	I-	V_{IN} = 0V/5V, V+ = 16.5V, V- = -16.5V			0.01	1	µA
LOGIC INPUT							
Input Voltage Low	V_{IL}			V-		0.8	V
Input Voltage High	V_{IH}			2.4		V+	V
Input Current	I_{IN}	V_{IN} = V-, V+		-1.0	0.0001	1.0	µA
SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}			V-		V+	V
On Circuit Resistance	R_{ON}	V_{COM} = +10V, $I_{(NC\ or\ NO)}$ = 1mA; V_{COM} = -10V, $I_{(NC\ or\ NO)}$ = 1mA	M		20	35	Ω
			C, E			45	
On Resistance Match Between Channels (Note 4)	R_{ON}	$I_{(NC\ or\ NO)}$ = -10mA, V_D = 10V or -10V, V+ = 15V, V- = -15V	T_A = +25°C			2	Ω
			T_A = T_{MIN} to T_{MAX}			4	
On Resistance Flatness (Note 4)	R_{ON}	$I_{(NC\ or\ NO)}$ = -10mA, V_D = 5V or -5V, V+ = 15V, V- = -15V	T_A = +25°C			3	Ω
			T_A = T_{MIN} to T_{MAX}			5	
On Circuit Leakage Current	I_{COM}	V_{COM} = ±15.5V, V_{NC} or V_{NO} = ∓15.5V, V+ = 16.5V, V- = -16.5V	M	-0.75		0.75	nA
			C, E	-1.00	0.20	1.00	
Off Circuit Leakage Current	I_{NC} or I_{NO}	V_{COM} = ±15.5V V_{NC} or V_{NO} = ∓15.5V, V+ = 16.5V, V- = -16.5V	M	-0.25	0.01	0.25	nA
			C, E	-0.50	0.02	0.05	
DYNAMIC							
Turn-Off Time	t_{OFF}	Figure 1				145	ns
Turn-On Time	t_{ON}					175	ns
Break-Before-Make Time	t_{OPEN}			10			ns
Off Capacitance	C_{OFF}				5		pF
On Capacitance	C_{ON}				5		pF
Charge Injection	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 6	T_A = +25°C		2	10	pC
Off Isolation	OIRR	f = 1MHz, RL = 75Ω, V_{COM} = 2.3V_{RMS}			72		dB
Crosstalk	CCRR				78		dB

ELECTRICAL CHARACTERISTICS–DUAL SUPPLIES (continued)

(GND = 0V, V+ = +15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Notes 2, 3)	MAX	UNITS
LOGIC INPUT							
Input Voltage Low	V_{IL}			V-		0.8	V
Input Voltage High	V_{IH}			2.4		V+	V
Input Current	I_{IN}	V_{IN} = V-, V+		-1.0	0.0001	1.0	µA
SWITCH							
Analog Signal Range	V_{COM}			V-		V+	V
On Circuit Resistance	R_{ON}	V_{COM} = 10V, $I_{(NC \text{ or } NO)}$ = 1mA; V_{COM} = -10V, $I_{(NC \text{ or } NO}$ = 1mA	C, E			45	Ω
			M			45	
On Circuit Leakage Current	I_{COM}	V_{COM} = ±15V, V_{NC} or V_{NO} = -15V, V+ = 16.5V, V- = -16.5V	C, E	-10		10	nA
			M	-60		60	
On Circuit Leakage Current	I_{NC} or I_{NO}	V_{COM} = ±15V, V_{NC} or V_{NO} = -15V, V+ = 16.5V, V- = -16.5V	C, E	-6		6	nA
			M				

ELECTRICAL CHARACTERISTICS—Single Supply

(GND = 0V, V+ = +12V, V- = 0V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Notes 2, 3)	MAX	UNITS
SUPPLY						
Supply Voltage Range	V_+	Single supply, V- = GND	10		30	V
Positive Supply Current	I+				0.25	mA
INPUT						
Input Voltage Low	V_{INLO}		0		0.8	V
Input Voltage High	V_{INHI}		2.4		V+	V
Input Current	I_{IN}	V_{IN} = V+, 0V			1	µA
SWITCH						
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}		V-		V+	V
On Circuit Resistance	r_{ON}	V_{COM} = 10V, $I_{(NC \text{ or } NO)}$ = 1mA, V_{COM} = 1V, $I_{(NC \text{ or } NO)}$ = 1mA		35	75	Ω
On Circuit Leakage Current	I_{COM}	V_{COM} = 11V, V_{NC} or V_{NO} = 0V; V_{COM} = 1V, V_{NC} or V_{NO} = V+			0.75	nA
Off Circuit Leakage Current	I_{NC} or I_{NO}	V_{COM} = 11V, V_{NC} or V_{NO} = 1V			0.25	nA
DYNAMIC						
Turn-Off Time	t_{OFF}	Figure 1		45		ns
Turn-On Time	t_{ON}			90		ns
Break-Before-Make Time	t_{OPEN}		5	10		ns
Off Isolation	OIRR	f = 1MHz, R_L = 75Ω, V_{COM} = 2.3V_{RMS}		70		dB
Crosstalk	CCRR			72		dB

Note 2: The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.

Note 3: Typical values are for design aid only, not guaranteed or subject to production testing.

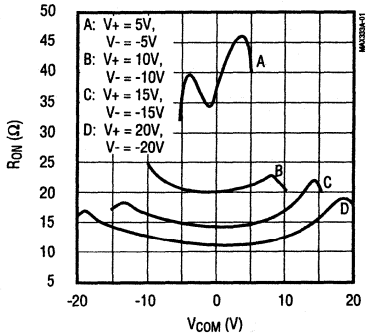
Note 4: On resistance match between channels and flatness are guaranteed only with bipolar-supply operation.

Precision, Quad, SPDT, CMOS Analog Switch

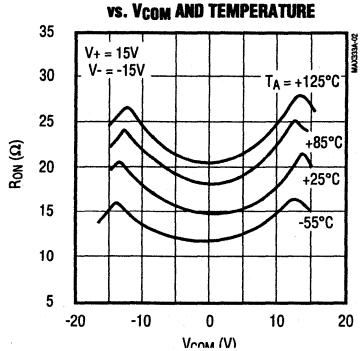
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted).

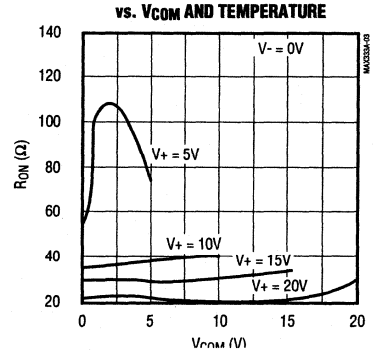
ON RESISTANCE vs. V_{COM} AND POWER SUPPLY VOLTAGE



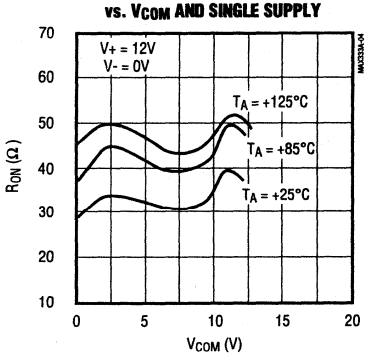
ON RESISTANCE vs. V_{COM} AND TEMPERATURE



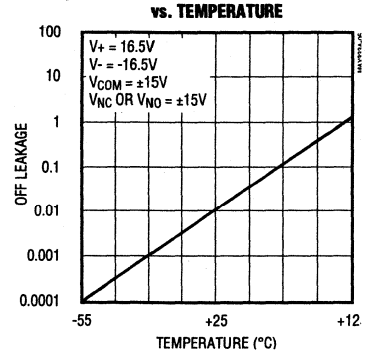
ON RESISTANCE vs. V_{COM} AND TEMPERATURE



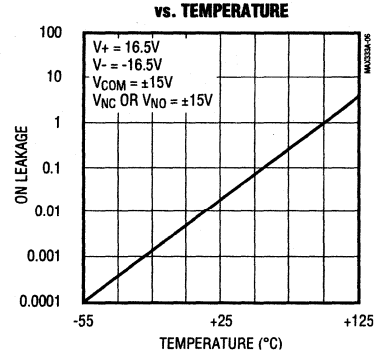
ON RESISTANCE vs. V_{COM} AND SINGLE SUPPLY



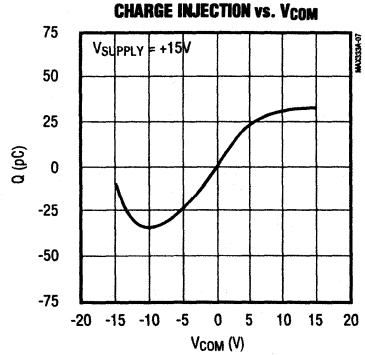
OFF LEAKAGE CURRENTS vs. TEMPERATURE



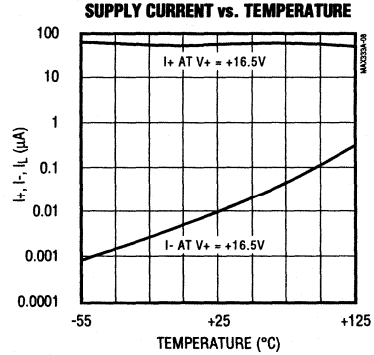
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



Precision, Quad, SPDT, CMOS Analog Switch

Pin Description

PIN	NAME	FUNCTION
1, 10, 11, 20	IN1-IN4	Logic-Level Inputs
2, 9, 12, 19	NO1-NO4	Normally Open Switches
3, 8, 13, 18	COM1-COM4	Common Switch Poles
4, 7, 14, 17	NC1-NC4	Normally Closed Switches
5	V-	Negative Power Supply
6	GND	Ground
15	N.C.	Not Internally Connected
16	V+	Positive Power Supply

Applications Information

Operation with Supply Voltages Other than ±15V

The main limitation of supply voltages other than ±15V is a reduction in the analog signal range. The MAX333A operates with ±5V to ±20V bipolar supplies. The *Typical Operating Characteristics* and graphs show typical on resistance for ±15V, ±10V, ±5 supplies. Switching times increase by a factor of two or more for ±5V operation. The MAX333A can operate from +10V to +24V unipolar supplies. It can be powered from a single +10V to +24V supply, as well as from unbalanced supplies such as +24V and -5V. Connect V- to 0V when operating with a single supply.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. It is important not to exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with the supply pins (Figure 1). Adding the diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected.

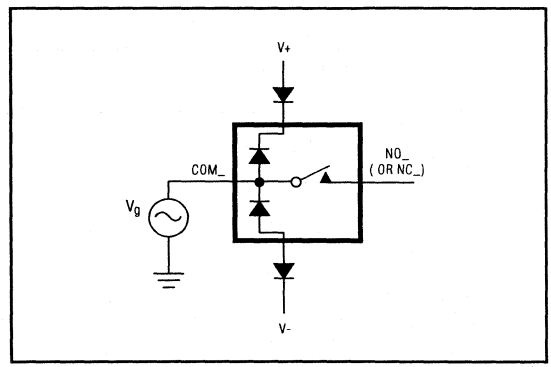


Figure 1. Overvoltage Protection Using Blocking Diodes

Test Circuits/Timing Diagrams

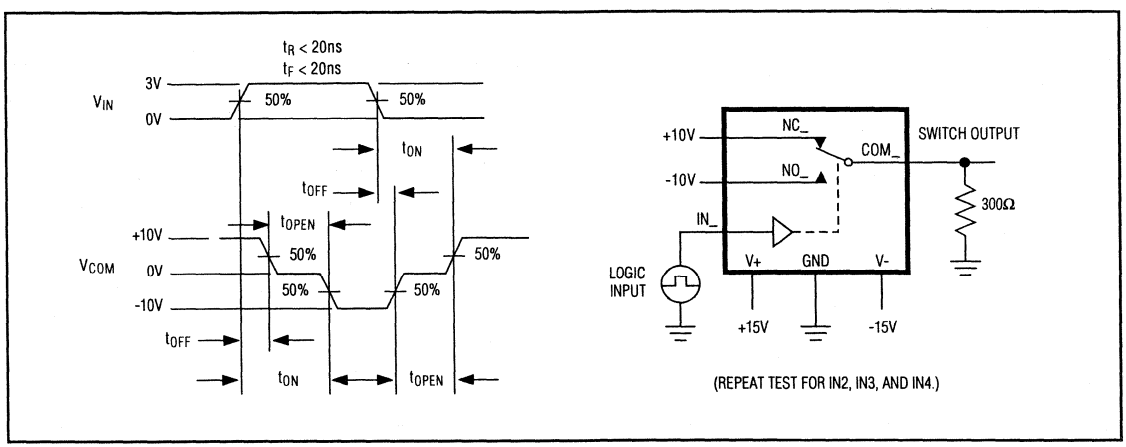


Figure 2. Switching-Time Test Circuit

Precision, Quad, SPDT, CMOS Analog Switch

Test Circuits/Timing Diagrams

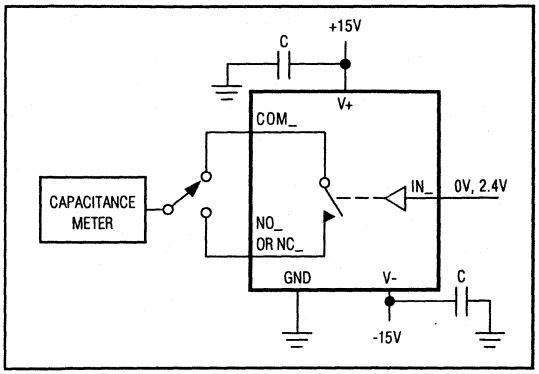


Figure 3. Channel-Off Capacitance

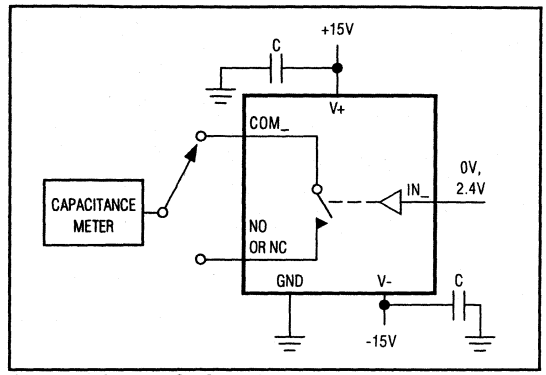


Figure 4. Channel-On Capacitance

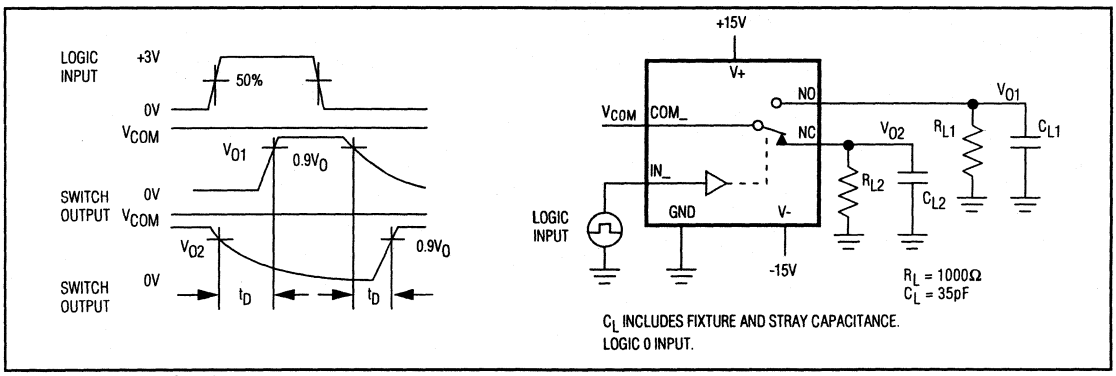


Figure 5. Break-Before-Make

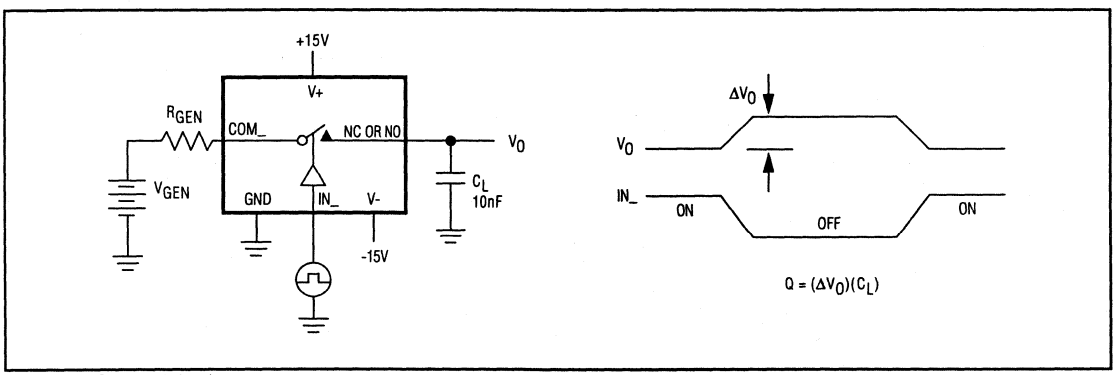
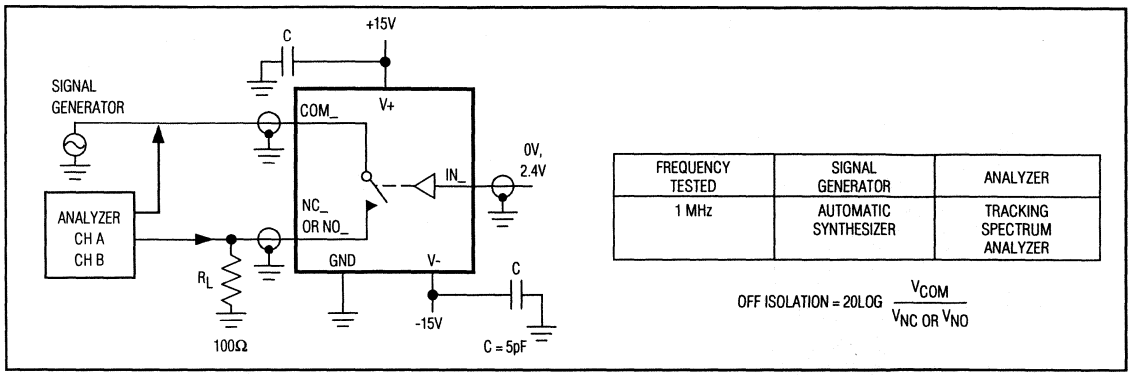


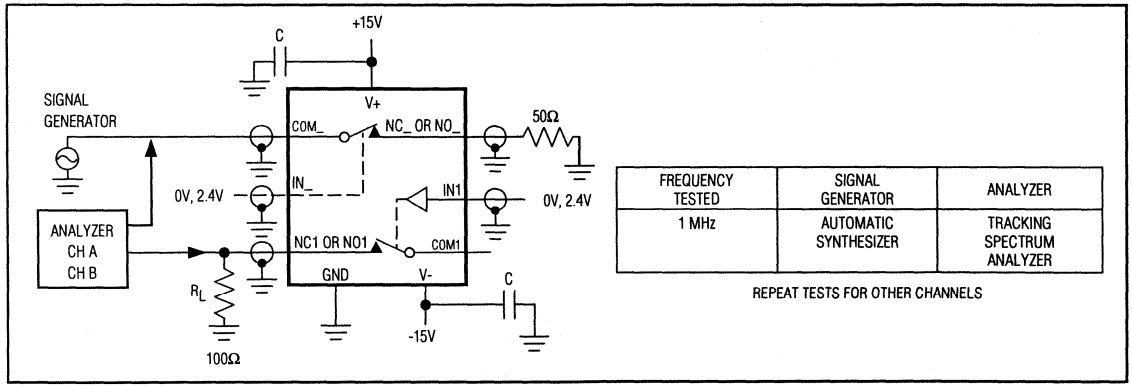
Figure 6. Charge Injection



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
1 MHz	AUTOMATIC SYNTHESIZER	TRACKING SPECTRUM ANALYZER

$$\text{OFF ISOLATION} = 20\text{LOG}\ \frac{V_{COM}}{V_{NC\ OR}\ V_{NO}}$$

Figure 7. Off-Isolation



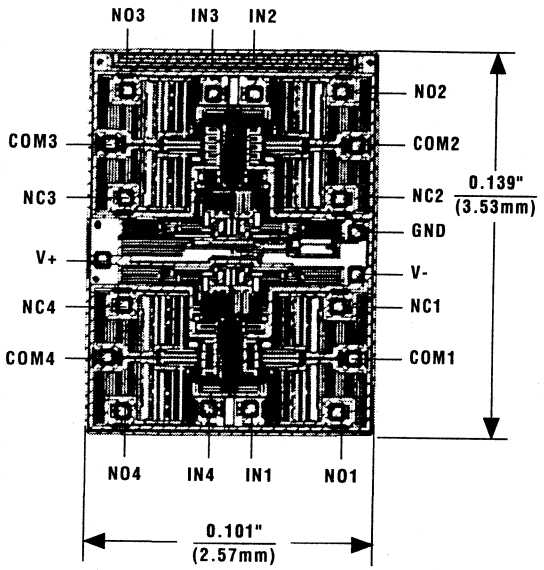
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
1 MHz	AUTOMATIC SYNTHESIZER	TRACKING SPECTRUM ANALYZER

REPEAT TESTS FOR OTHER CHANNELS

Figure 8. Crosstalk

Precision, Quad, SPDT, CMOS Analog Switch

Chip Topography



TRANSISTOR COUNT: 145;
SUBSTRATE CONNECTED TO V+.

19-0220; Rev 1; 4/94

MAXIM

Serial Controlled, 8-Channel SPST Switch

General Description

The MAX335 analog switch with serial digital interface offers eight separately controlled single-pole-single-throw (SPST) switches. All switches conduct equally in either direction and on resistance (100Ω) is constant over the analog signal range.

These CMOS switches can continuously operate with power supplies ranging from ±4.5V to ±20V and handle rail-to-rail analog signals. Upon power-up, all switches are off, and the internal serial and parallel shift registers are reset to zero. The MAX335 is equivalent to two DG211 quad switches but controlled by a serial interface.

The interface is compatible with the Motorola SPI interface standard. Functioning as a shift register, this serial interface allows data (at DIN) to be locked in synchronous with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several MAX335s to be daisy-chained.

Applications

Serial Data Acquisition and Process Control

Avionics

Signal Routing

Networking

Features

- ♦ 8 Separately Controlled SPST Switches
- ♦ SPI-Compatible Serial Interface
- ♦ Accepts ±15V Analog Swings
- ♦ Multiple Devices Can Be Daisy-Chained

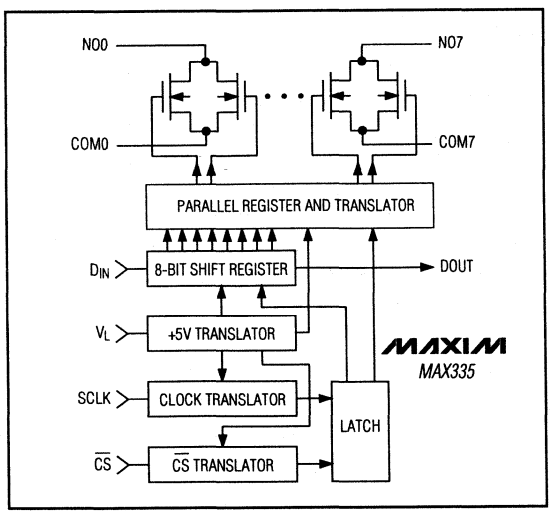
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX335CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX335CWG	0°C to +70°C	24 Wide SO
MAX335C/D	0°C to +70°C	Dice*
MAX335ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX335EWG	-40°C to +85°C	24 Wide SO
MAX335MRG	-55°C to +125°C	24 Narrow CERDIP**

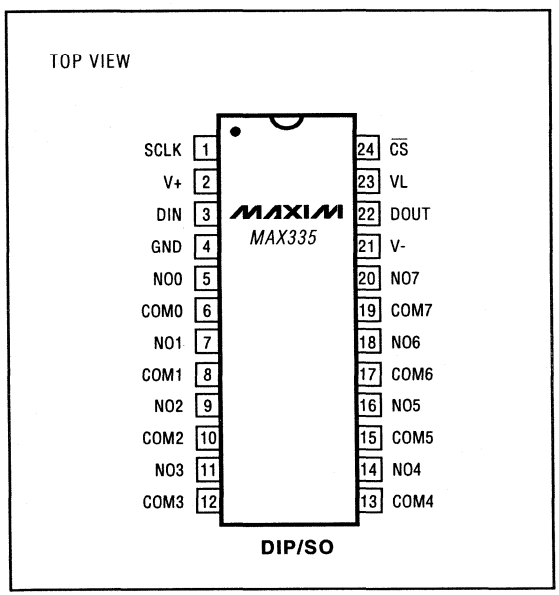
** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



™ SPI is a trademark of Motorola Corp.

Serial Controlled, 8-Channel SPST Switch

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND - 0.3V) to (V+ + 0.3V)
SCLK, $\overline{CS}$, DIN, DOUT, NO_, COM_ ..... V- -2V to V+ +2V
or 30mA, whichever occurs first
Continuous Current (any terminal) 30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle MAX) 100mA

Continuous Power Dissipation (T_A = +70°C) (Note 1)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C) ..1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW
Operating Temperature Ranges
MAX335C_ _ ..... 0°C to +70°C
MAX335E_ _ ..... -40°C to +85°C
MAX335MRG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: All leads are soldered or welded to PC boards.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_L = +5V ±10%, V+ = 15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	T_A = T_{MIN} to T_{MAX}		-15		15	V
On Resistance	R_{ON}	V_{COM} = ±10V, I_{NO} = 1mA	T_A = +25°C		100	150	Ω
						200	
NO Off Leakage Current	$I_{NO(OFF)}$	V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	nA
				-20		20	
		V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	
				-20		20	
COM Off Leakage Current	$I_{COM(OFF)}$	V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	nA
				-20		20	
		V_{COM} = -14V, V_{NO} = +14V	T_A = +25°C	-1	0.002	1	
				-20		20	
COM On Leakage Current	$I_{COM(ON)}$	V_{COM} = V_{NO} = +14V	T_A = +25°C	-2	0.01	2	nA
				-40		40	
		V_{COM} = V_{NO} = -14V	T_A = +25°C	-2	0.01	2	
				-40		40	
DIGITAL I/O							
DIN, SCLK, $\overline{CS}$ Input Logic Threshold High	V_{IH}	V_L = +5V		2.4			V
		V_L = +15V		11			
DIN, SCLK, $\overline{CS}$ Input Logic Threshold Low	V_{IL}	V_L = +5V				0.8	V
		V_L = +15V				3	
DIN, SCLK, $\overline{CS}$ Input Current Logic High	I_{INH}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 2.4V		-1	0.03	1	µA
		V_L = +15V, V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 11V		-1	0.03	1	
DIN, SCLK, $\overline{CS}$ Input Current Logic Low	I_{INL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V		-1	0.03	1	µA
		V_L = +15V, V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 3V		-1	0.03	1	
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		3.5		V_L	V

ELECTRICAL CHARACTERISTICS (continued)

(V_L = +5V ±10%, V+ = 15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL I/O							
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = -1.6mA				0.4	V
V_L RESET Voltage	V_{LL}	(Note 2)		0.8			V
V_L RESET Voltage	V_{LH}		T_A = +25°C			2.4	V
SCLK Input Hysteresis	$SCLK_{HYST}$		T_A = +25°C		100		mV
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25°C		200	400	ns
						500	
Turn-Off Time	t_{OFF}	From rising edge of $\overline{CS}$	T_A = +25°C		90	400	ns
						500	
NO Off Capacitance	$C_{NO(OFF)}$	V_S = GND, f = 1MHz	T_A = +25°C		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_D = GND, f = 1MHz	T_A = +25°C		2		pF
Channel-On Capacitance	$C_{COM(ON)}$	V_D = V_S = GND, f = 1MHz	T_A = +25°C		8		pF
Off Isolation	OIRR	R_L = 100Ω, C_L = 15pF, V_S = $1V_{RMS}$, f = 100kHz	T_A = +25°C		90		dB
Channel-to-Channel Crosstalk	CCRR	R_L = 50Ω, C_L = 15pF, V_S = $1V_{RMS}$, f = 100kHz	T_A = +25°C		100		dB
Break-Before-Make Delay	T_{BBM}			25	15		ns
Clock Feedthrough at S, D (Note 3)	ESCLK	D_{LOAD} = S_{LOAD} = 75Ω, measured at S and D	T_A = +25°C			100	nV-sec
POWER SUPPLIES							
Power-Supply Voltage Range	V+/V-			±4.5		±20	V
V_L Power-Supply Voltage Range	V_L			4.5		V+	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V/5V	T_A = +25°C		150	300	µA
						500	
V- Supply Current	I-	DIN = $\overline{CS}$ = SCLK = 0V/5V	T_A = +25°C		0.01	10	µA
						10	
V_L Supply Current	I_L	DIN = $\overline{CS}$ = SCLK = 0V/5V	T_A = +25°C		50	100	µA
						200	

Note 2: When V_L falls below this voltage, all switches are set off, and the internal shift register is cleared (all zero).
Note 3: Guaranteed, not Production tested.

TIMING CHARACTERISTICS OF SERIAL DIGITAL INTERFACE (Figure 1)

(V_L = +5V ±10%, V+ = +15V, V- = -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

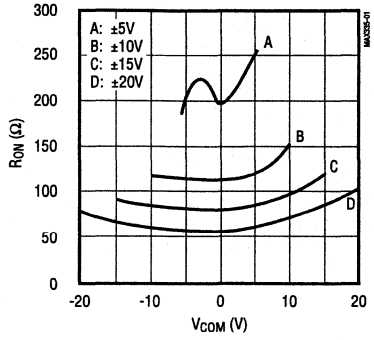
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK Maximum Frequency	f_{SCLK}			2.1			MHz
Cycle Time				480			ns
$\overline{CS}$ Lead Time				240			ns
$\overline{CS}$ Lag Time				240			ns
SCLK High Time	t_{CH}			190			ns
SCLK Low Time	t_{CL}			190			ns
Data-Setup Time	t_{DS}			200			ns
Data-Hold Time	t_{DH}			0			ns
DOUT Data Valid After Falling SCLK		50% of SCLK to 10% of DOUT CL = 10pF	T_A = +25°C		240		ns
						400	
DOUT Data-Hold Time After Rising SCLK (Note 4)		C_L = 10pF		0			ns
Rise Time of DOUT (Note 3)		20% V_L to 70% V_L, C_L = 10pF				100	ns
Allowable Rise Time at DIN, SCLK, $\overline{CS}$ (Note 3)		20% V_L to 70% V_L, C_L = 10pF				2	µs
Fall Time of DOUT (Note 3)		70% V_L to 20% V_L, C_L = 10pF				100	ns
Allowable Fall Time at DIN, SCLK, $\overline{CS}$ (Note 3)		70% V_L to 20% V_L, C_L = 10pF				2	µs

Note 4: This specification guarantees that data at D_{OUT} never appears before SCLK's falling edge.

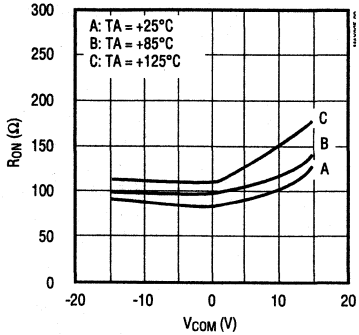
Typical Operating Characteristics

(V+ = +15V, V- = -15V, V_L = 5V, T_A = +25°C, unless otherwise noted.)

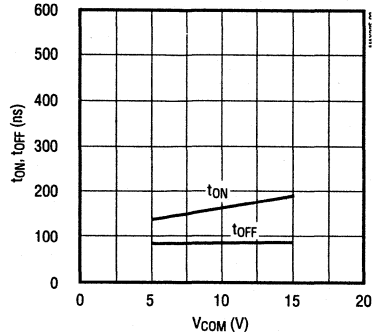
RON vs. VCOM AND POWER SUPPLY VOLTAGE



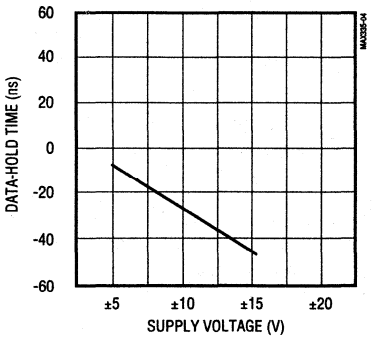
RON vs. VCOM AND TEMPERATURE



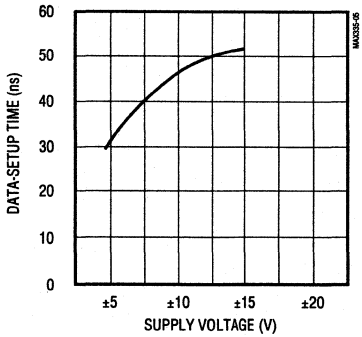
tON, tOFF vs. VCOM



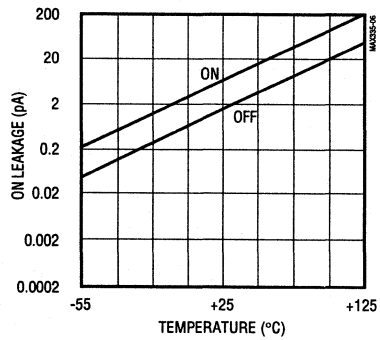
DATA-HOLD TIME vs. POWER-SUPPLY VOLTAGE



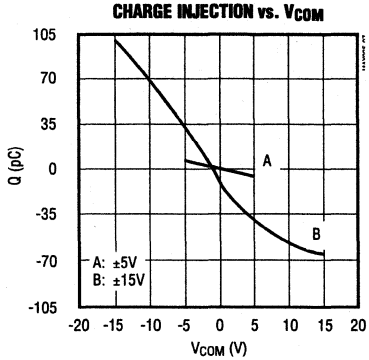
DATA-SETUP TIME vs. POWER SUPPLY



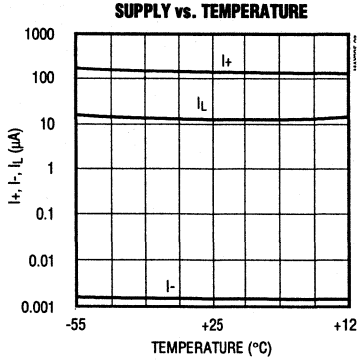
LEAKAGE CURRENT vs. TEMPERATURE



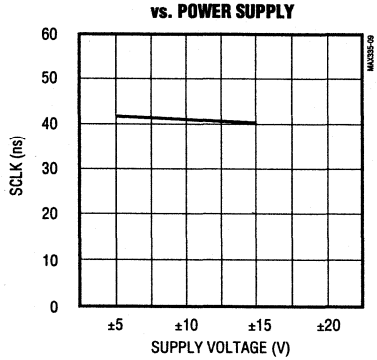
CHARGE INJECTION vs. VCOM



SUPPLY vs. TEMPERATURE



MINIMUM SCLK PULSE WIDTH vs. POWER SUPPLY



Serial Controlled, 8-Channel SPST Switch

Pin Description

PIN	NAME	FUNCTION
1	SCLK	Serial clock input
2	V+	Positive supply voltage
3	DIN	Serial data input
4	GND	Ground
5	NOØ	Switch 0
6	COMØ	Switch 0
7	NO1	Switch 1
8	COM1	Switch 1
9	NO2	Switch 2
10	COM2	Switch 2
11	NO3	Switch 3
12	COM3	Switch 3
13	COM4	Switch 4
14	NO4	Switch 4
15	COM5	Switch 5
16	NO5	Switch 5
17	COM6	Switch 6
18	NO6	Switch 6
19	COM7	Switch 7
20	NO7	Switch 7
21	V-	Negative supply voltage
22	DOUT	Serial data output
23	V_L	Logic supply/Reset
24	$\overline{CS}$	Chip select

Detailed Description

Serial Digital Interface

Basic Operation

Refer to Figure 2. The MAX335 interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$. While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronous with SCLK's rising edge. The data is an 8-bit word, each bit controlling one of eight switches in the MAX335 (see Table 1). DOUT is the output of the shift register, with data appearing synchronous with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their original configuration. When the 8 bits of data have been shifted in, $\overline{CS}$ is brought high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when $\overline{CS}$ is high, and DOUT holds the last bit in the shift register.

The MAX335 three-wire serial interface is compatible with the SPI™ and Microwire™ standards. If interfacing with a Motorola processor serial interface, set CPOL = 0. The MAX335 is considered a slave device. See Figures 2 and 3. Upon power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is only updated on the rising edge of $\overline{CS}$ when SCLK is low. If SCLK is high when $\overline{CS}$ rises, the latch will not be updated until SCLK goes low. The CPOL = 1, CPHA = 1 SPI configuration does not update the latch correctly.

Daisy Chaining

For a simple interface using several MAX335s, "daisy-chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected together, and a stream of data is shifted through the MAX335s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the MAX335 data chain.

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each MAX335 are connected together (Figure 6). Address decode logic individually controls $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ is brought low, data is shifted in, and $\overline{CS}$ is brought high to latch the data. Typically, only one slave is addressed at a time. DOUT is not used.

Digital Feedthrough

Digital feedthrough energy measures 100nV-sec, which means that with no filtering at the signal channel, feedthrough from a sharply rising clock edge into an unfiltered switch channel can be measured at $1V_{P-P}$ for 100ns. However, even 100pF capacitance in the switch channel, when combined with the switch resistance yields a filter which reduces this transient to $10mV_{P-P}$ typical. To reduce digital feedthrough, hysteresis (150mV typ) was added to the SCLK input so triangle or sine waves may be used.

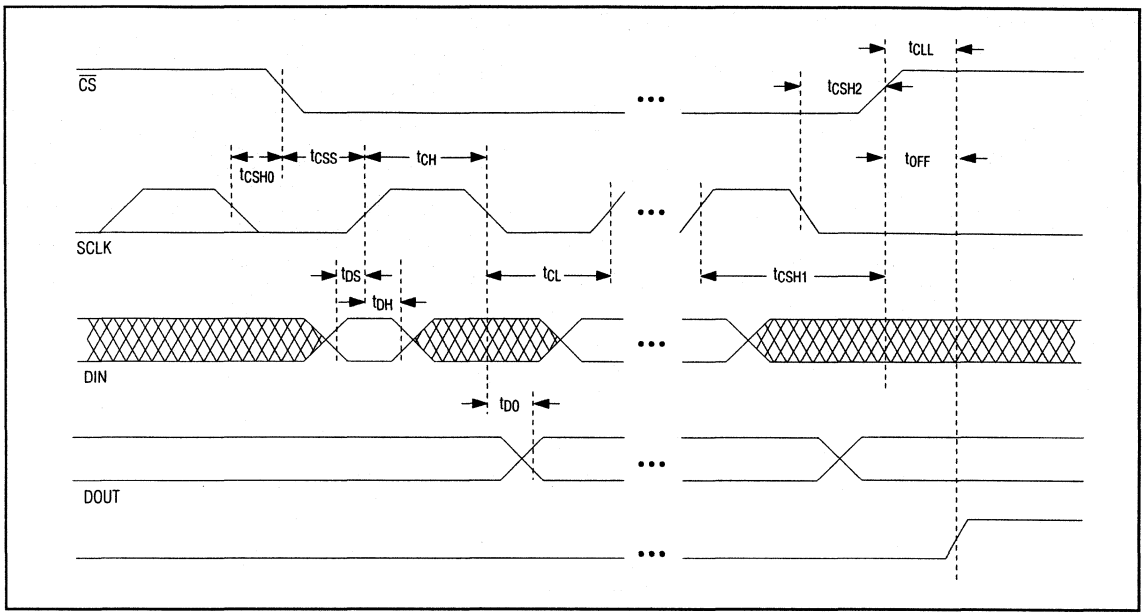


Figure 1. Timing Diagram

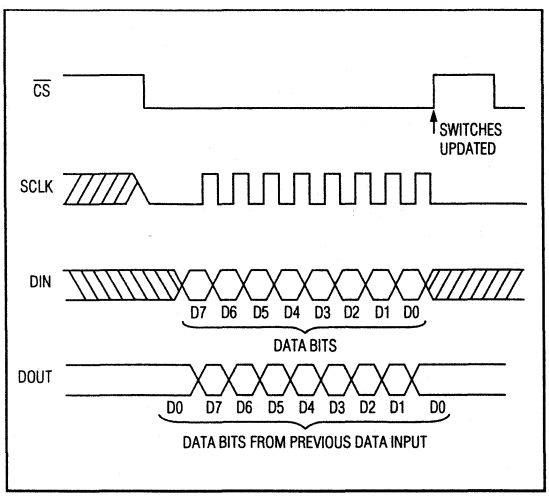


Figure 2. Three-Wire Interface Timing

Serial Controlled, 8-Channel SPST Switch

Table 1. Serial-Interface Switch Programming

DATA BITS								FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	Switch 7 open (off)
1	X	X	X	X	X	X	X	Switch 7 closed (on)
X	0	X	X	X	X	X	X	Switch 6 open
X	1	X	X	X	X	X	X	Switch 6 closed
X	X	0	X	X	X	X	X	Switch 5 open
X	X	1	X	X	X	X	X	Switch 5 closed
X	X	X	0	X	X	X	X	Switch 4 open
X	X	X	1	X	X	X	X	Switch 4 closed
X	X	X	X	0	X	X	X	Switch 3 open
X	X	X	X	1	X	X	X	Switch 3 closed
X	X	X	X	X	0	X	X	Switch 2 open
X	X	X	X	X	1	X	X	Switch 2 closed
X	X	X	X	X	X	0	X	Switch 1 open
X	X	X	X	X	X	1	X	Switch 1 closed
X	X	X	X	X	X	X	0	Switch 0 open
X	X	X	X	X	X	X	1	Switch 0 closed

X = Don't care

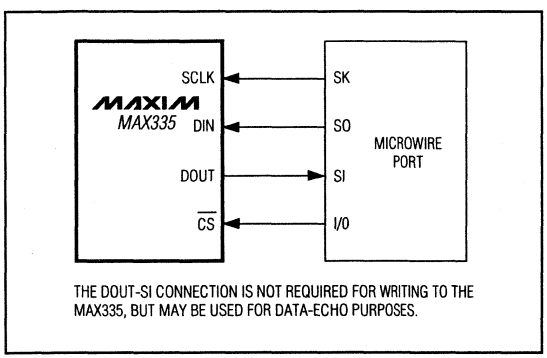


Figure 3. Connections for Microwire

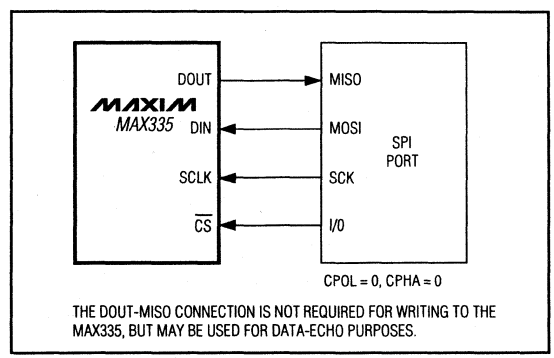


Figure 4. Connections for SPI

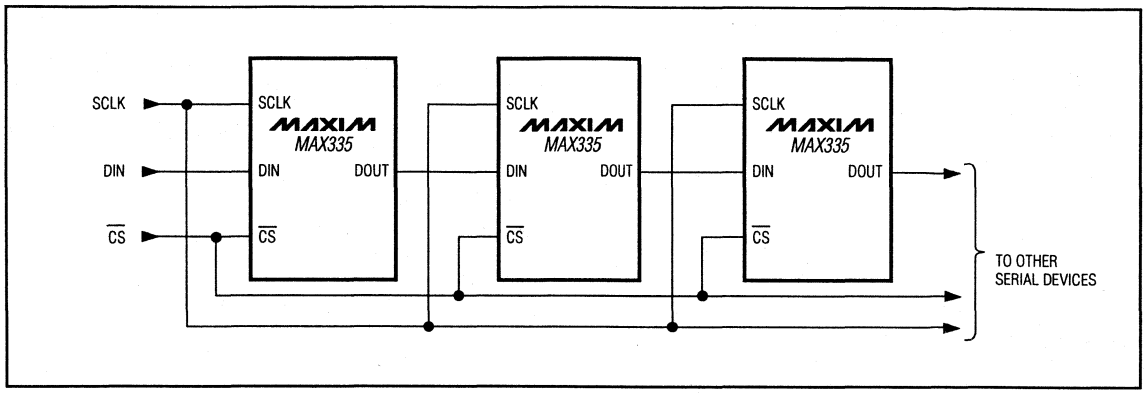


Figure 5. Daisy-Chained Connection

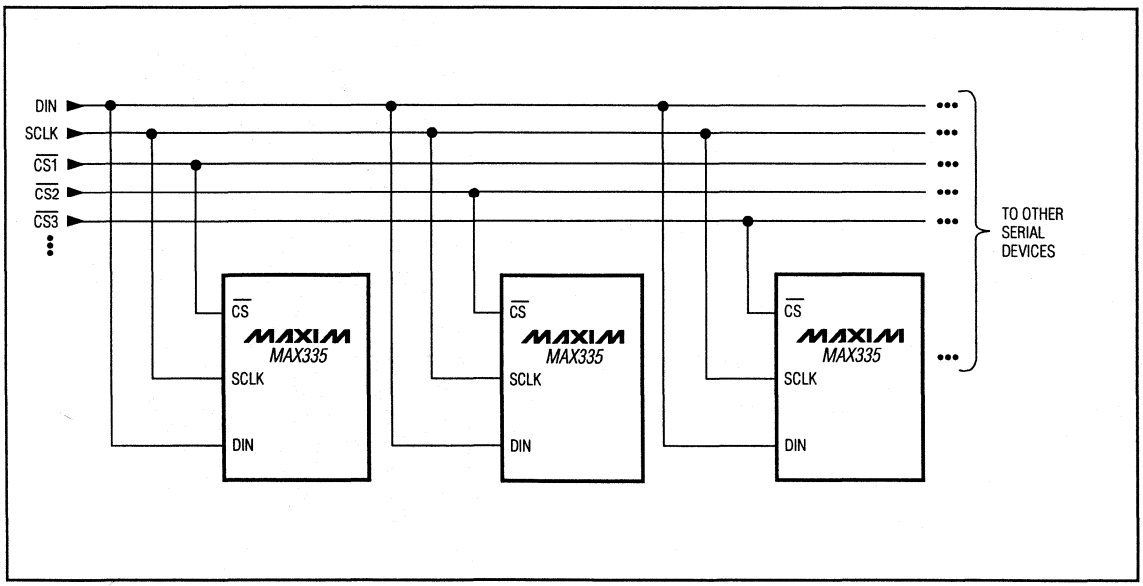


Figure 6. Addressable Serial Interface

Serial Controlled, 8-Channel SPST Switch

Applications Information

8 x 1 Multiplexer

To use the MAX335 as an 8 x 1 multiplexer, tie all drains together (COM0 to COM7); the mux inputs now source each switch (NO0 to NO7). Input a single 0V to +3V pulse at DIN. As this is clocked through the register by SCLK, each switch will sequence on one at a time.

4-2 Differential Multiplexer

To use the MAX335 as a 4-2 differential multiplexer, tie COM0 through COM3 together and COM4 through COM7 together. Differential inputs will be the source inputs as follows: (NO0, NO4), (NO1, NO5), (NO2, NO6), (NO3, NO7). Figure 7 shows the serial input control at DIN required to turn on two switches making a differential multiplexer.

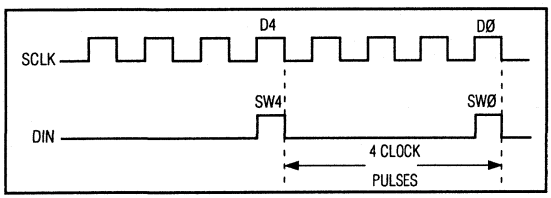


Figure 7. Differential Multiplexer Input Control

CS is held low for four clock pulses; the first pulse is clocked into the fifth switch position as the second pulse is clocked into the first switch position. $\overline{CS}$ is pulled high to update switches; then $\overline{CS}$ is pulled low, and SCLK advances pulses to S1 and S5 positions, where $\overline{CS}$ is pulled high to update, etc.

SPDT Switches

Tie COM0 to NO1 so that NO0 and COM1 are now inputs and COM0/NO1 is the common output. SP is common output. Up to four SPDT switches can be made from each MAX335. Multiples of four or more can be made by daisy-chaining devices. In Figure 8 DIN is a pulse train. Again, $\overline{CS}$ is held low to clock in pulses and $\overline{CS}$ is pulled high to update; $\overline{CS}$ is held low to shift pulses, then pulled high to update, etc.

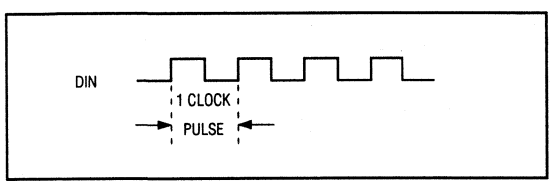


Figure 8. Serial Input Control for SPDT Switch

Reset Function

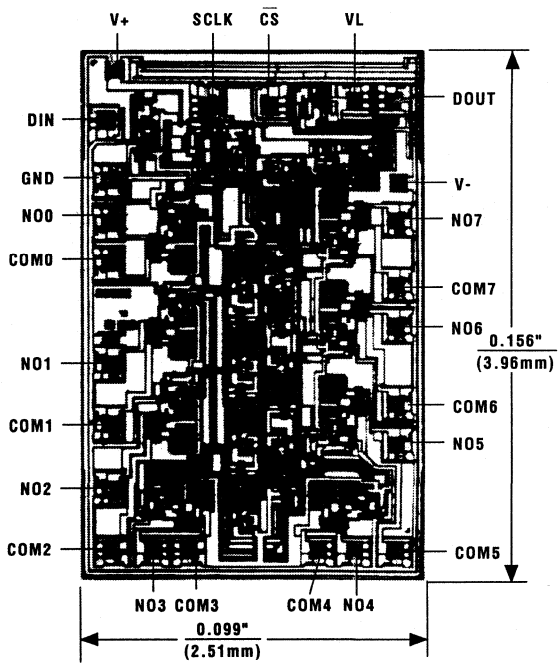
Pulsing V_L below +0.8V initiates the power-up reset function. The switches are set to the off position, and the serial shift register is reset to all zeros.

Power-Supply Operation

The MAX335 operates with V = ±4.5V to ±20V and V_L = +5V. With V- tied to ground, the part operates with V+ = +10V to +30V.

The V_L supply sets TTL input compatibility at a 1.6V switching threshold. As V_L is raised, the switching threshold is raised, so the part is no longer TTL compatible. The MAX335 also operates with a single power supply: V_L = V+ and V- = 0V. With V_L tied to V+, the V_L supply cannot be used as a reset function.

Chip Topography



TRANSISTOR COUNT: 387

SUBSTRATE CONNECTED TO V+.

19-0272; Rev 0; 8/94

MAXIM

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

General Description

The MAX338/MAX339 are monolithic, CMOS analog multiplexers (muxes). The 8-channel MAX338 is designed to connect one of eight inputs to a common output by control of a 3-bit binary address. The dual, 4-channel MAX339 is designed to connect one of four inputs to a common output by control of a 2-bit binary address. Both devices can be used as either a mux or a demux. On-resistance is 400Ω max, and the devices conduct current equally well in both directions.

These muxes feature extremely low off leakages (less than 20pA at +25°C), and extremely low on-channel leakages (less than 50pA at +25°C). The new design offers guaranteed low charge injection (1.5pC typ) and electrostatic discharge (ESD) protection greater than 2000V, per method 3015.7. These improved muxes are pin-compatible upgrades for the industry-standard DG508A and DG509A. For similar Maxim devices with lower leakage and charge injection but higher on-resistance, see the MAX328 and MAX329.

The MAX338/MAX339 operate from a single +4.5V to +30V supply or from dual supplies of ±4.5V to ±20V. All control inputs (whether address or enable) are TTL compatible (+0.8V to +2.4V) over the full specified temperature range and over the ±4.5V to ±18V supply range. These parts are fabricated with Maxim's 44V silicon-gate process.

Applications

Data-Acquisition Systems
Test Equipment
Military Radios
Guidance and Control Systems
PBX, PABX
Sample-and-Hold Circuits
Heads-Up Displays
Communications Systems

Features

- ♦ **On-Resistance, <400Ω max**
- ♦ **Transition Time, <500ns**
- ♦ **On-Resistance Match, <10Ω**
- ♦ **NO-Off Leakage Current, <20pA at +25°C**
- ♦ **1.5pC Charge Injection**
- ♦ **Single-Supply Operation (+4.5V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ **Plug-In Upgrade for Industry-Standard DG508A/DG509A**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **TTL/CMOS-Logic Compatible**
- ♦ **ESD Protection >2000V, per Method 3015.7**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX338CPE	0°C to +70°C	16 Plastic DIP
MAX338CSE	0°C to +70°C	16 Narrow SO
MAX338C/D	0°C to +70°C	Dice*
MAX338EPE	-40°C to +85°C	16 Plastic DIP
MAX338ESE	-40°C to +85°C	16 Narrow SO
MAX338EJE	-40°C to +85°C	16 CERDIP
MAX338MJE	-55°C to +125°C	16 CERDIP**

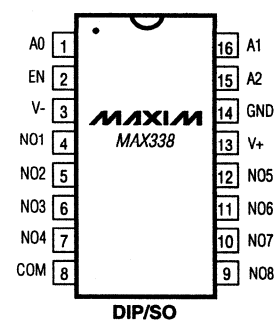
Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for availability.*

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

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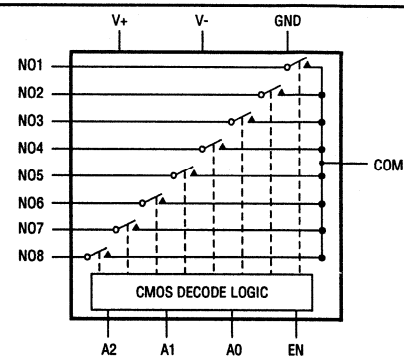


MAX338 8-CHANNEL SINGLE-ENDED MULTIPLEXER

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ .....-0.3V, 44V
GND .....-0.3V, 25V
Digital Inputs, NO, COM (Note 1).....(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal).....30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (TA = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C).....800mW
Operating Temperature Ranges
MAX33_C__ .....0°C to +70°C
MAX33_E__.....-40°C to +85°C
MAX33_MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: Signals on NO, COM, EN, A0, A1, or A2 exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)				-15		15	V
On-Resistance	R_{ON}	I_{NO} = 0.2mA, V_{COM} = ±10V		T_A = +25°C			220	400	Ω
				T_A = T_{MIN} to T_{MAX}				500	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{NO} = 0.2mA, V_{COM} = ±10V (Note 4)		T_A = +25°C			4	10	Ω
				T_A = T_{MIN} to T_{MAX}				15	
NO-Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V_{COM} = ∓10V, V_{NO} = ±10V, V_{EN} = 0V		T_A = +25°C		-0.02	0.001	0.02	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-1.25		1.25	
					M	-20		20	
COM-Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V_{NO} = ±10V, V_{COM} = ∓10V, V_{EN} = 0V	MAX338	T_A = +25°C		-0.05	0.005	0.05	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-3.25		3.25	
					M	-40		40	
		V_{NO} = ∓10V, V_{COM} = ±10V, V_{EN} = 0V	MAX339	T_A = +25°C		-0.05	0.005	0.05	
				T_A = T_{MIN} to T_{MAX}	C, E	-1.65		1.65	
					M	-20		20	
COM-On Leakage Current (Note 5)	$I_{COM(ON)}$	V_{COM} = ±10V, V_{NO} = ±10V, sequence each switch on	MAX338	T_A = +25°C		-0.05	0.006	0.05	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-3.25		3.25	
					M	-40		40	
			MAX339	T_A = +25°C		-0.05	0.008	0.05	
				T_A = T_{MIN} to T_{MAX}	C, E	-1.65		1.65	
					M	-20		20	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
INPUT								
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V or 15V			-1.0	0.001	1.0	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V or 2.4V, V_A = 0V			-1.0		1.0	µA
SUPPLY								
Power-Supply Range					±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V		T_A = +25°C		50	100	µA
				T_A = T_{MIN} to T_{MAX}			150	
		V_{EN} = 2.4V, $V_{A(ALL)}$ = 2.4V		T_A = +25°C		290	500	µA
				T_A = T_{MIN} to T_{MAX}			600	
Negative Supply Current	I-	V_{EN} = 0V or 2.4V, $V_{A(ALL)}$ = 0V, 2.4V or 5V		T_A = +25°C	-1		1	µA
				T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC								
Transistion Time	t_{TRANS}	Figure 2		T_A = +25°C		200	500	ns
Break-Before-Make Interval	t_{OPEN}	Figure 4		T_A = +25°C	10	140		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		T_A = +25°C		160	500	ns
				T_A = T_{MIN} to T_{MAX}			750	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		T_A = +25°C		100	500	ns
				T_A = T_{MIN} to T_{MAX}			750	
Charge Injection (Note 3)	Q	C_L = 100pF, V_{NO} = 0V, R_S = 0Ω, Figure 6		T_A = +25°C		1.5	5	pC
Off Isolation (Note 6)	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz		T_A = +25°C		-75		dB
Crosstalk Between Channels	V_{CT}	V_{EN} = 2.4V, f = 100kHz, V_{GEN} = $1V_{P-P}$, R_L = 1kΩ, Figure 7		T_A = +25°C		-92		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		2		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, V_{EN} = V_{NO} = 0V, Figure 8		T_A = +25°C		3		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, V_{EN} = 0.8V, V_{COM} = 0V, Figure 8	MAX338	T_A = +25°C		11		pF
			MAX339			6		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, V_{EN} = 2.4V, V_{COM} = 0V, Figure 8	MAX338	T_A = +25°C		16		pF
			MAX339			9		

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)		0		12	V
On-Resistance	R_{ON}	I_{NO} = 0.2mA V_{COM} = 3V or 10V	T_A = +25°C		460	650	Ω
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	V_{NO1} = 8V, V_{NO8} = 0V, V_{IN} = 2.4V, Figure 1	T_A = +25°C		210	500	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3	T_A = +25°C		280	500	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3	T_A = +25°C		110	500	ns
Charge Injection (Note 3)	Q	C_L = 100pF, V_{NO} = 0V, R_S = 0Ω	T_A = +25°C		1.8	5	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

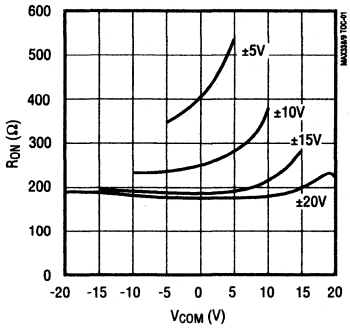
Note 6: Worst-case isolation is on channel 4 because of its proximity to the drain pin. Off isolation = 20log V_{COM}/V_{NO}, where V_{COM} = output and V_{NO} = input to off switch.

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

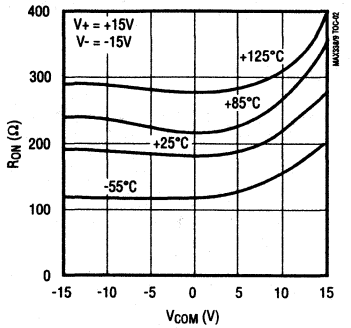
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

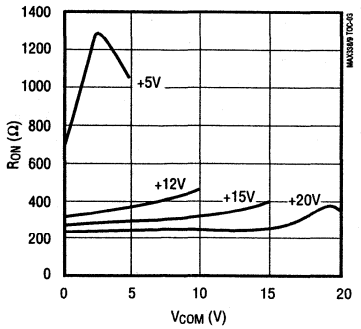
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



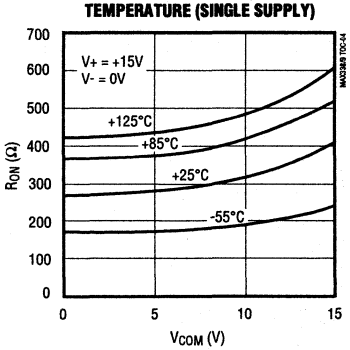
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE (DUAL SUPPLIES)



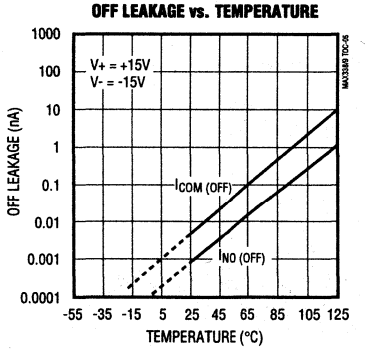
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



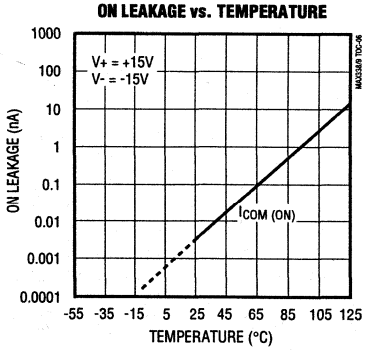
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE (SINGLE SUPPLY)



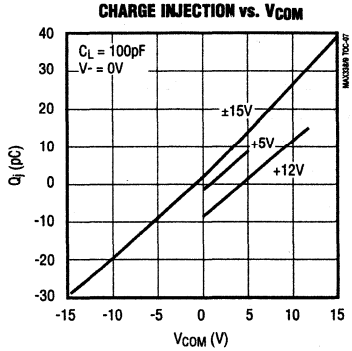
OFF LEAKAGE vs. TEMPERATURE



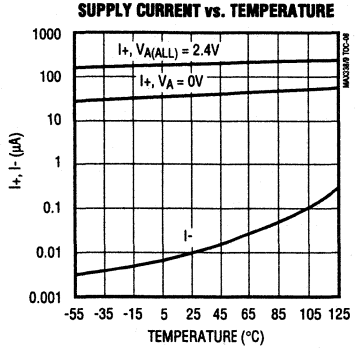
ON LEAKAGE vs. TEMPERATURE



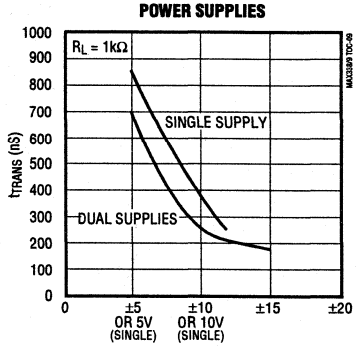
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



TRANSITION TIME vs. POWER SUPPLIES



8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Pin Description

PIN		NAME	FUNCTION
MAX338	MAX339		
1, 15, 16	—	A0, A2, A1	Address Inputs
—	1, 16	A0, A1	Address Inputs
2	2	EN	Enable Input
3	3	V-	Negative Supply Voltage Input
4–7	—	NO1–NO4	Analog Inputs—bidirectional
—	4–7	NO1A–NO4A	Analog Inputs—bidirectional
8	—	COM	Analog Output—bidirectional
—	8, 9	COMA, COMB	Analog Outputs—bidirectional
9–12	—	NO8–NO5	Analog Inputs—bidirectional
—	10–13	NO4B–NO1B	Analog Inputs—bidirectional
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

Applications Information

Operation with Supply Voltages Other than 15V

Using supply voltages less than ±15V will reduce the analog signal range. The MAX338/MAX339 switches operate with ±4.5V to ±20V bipolar supplies or with a +4.5V to +30V single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies such as +24V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs NO and COM. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 44V.

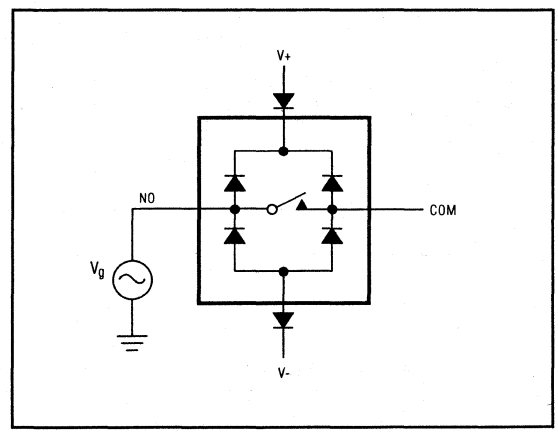


Figure 1. Overvoltage Protection Using External Blocking Diodes

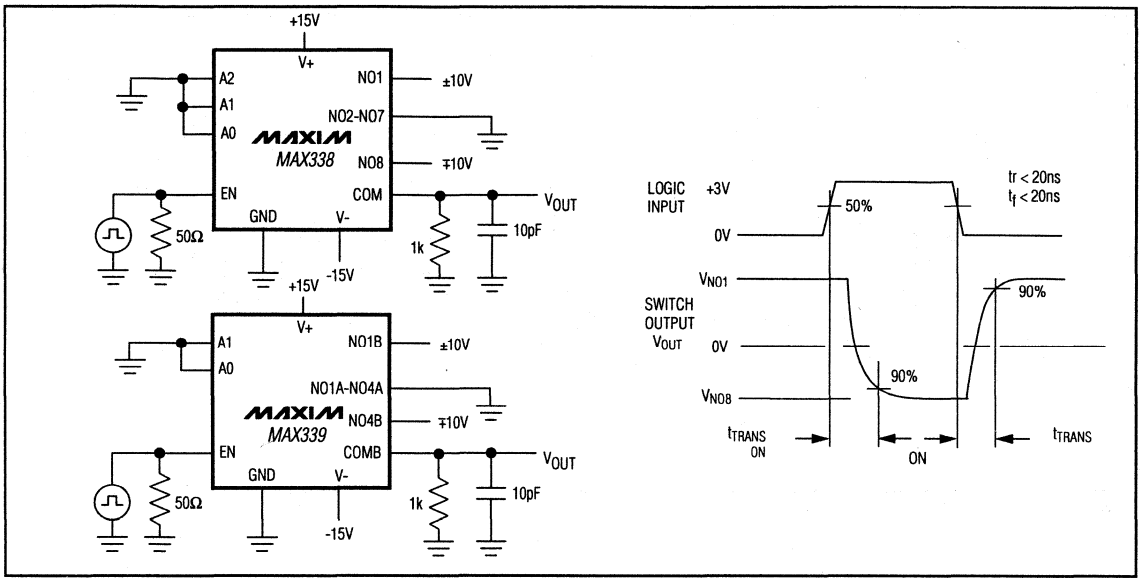


Figure 2. Transition Time

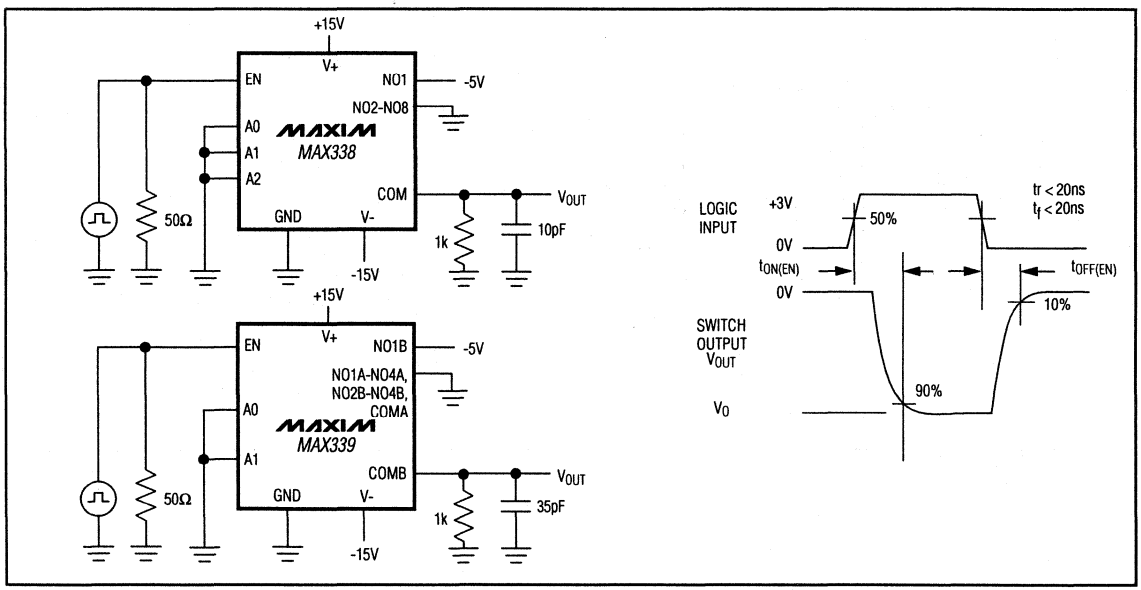


Figure 3. Enable Switching Time

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

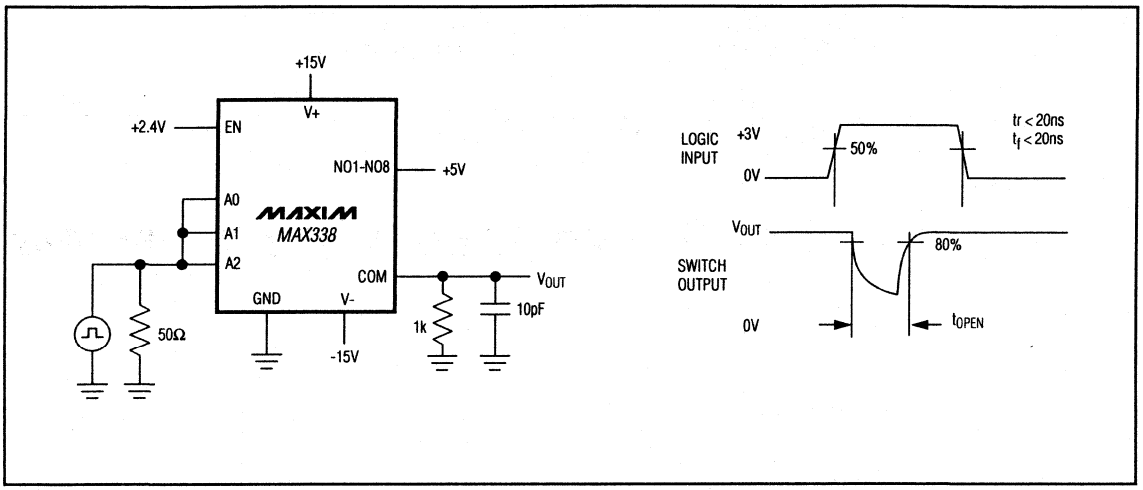


Figure 4. Break-Before-Make Interval

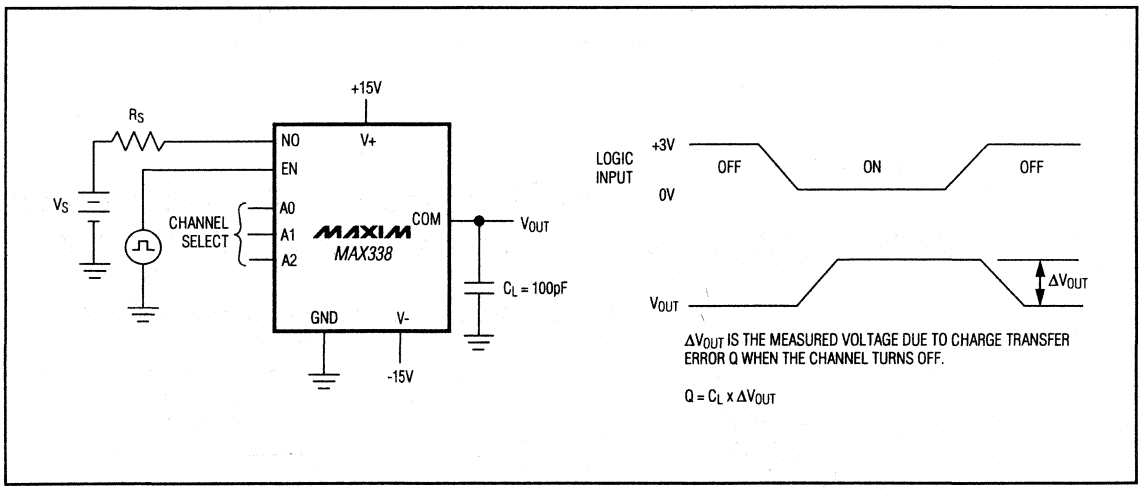


Figure 5. Charge Injection

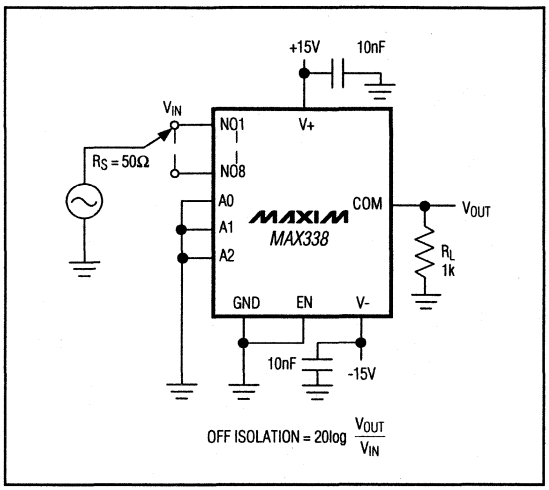


Figure 6. Off Isolation

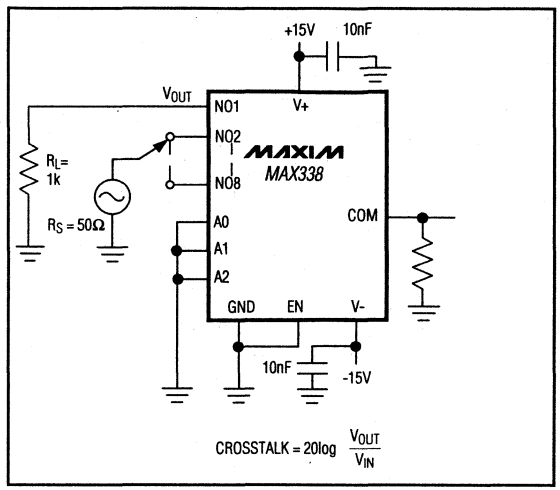


Figure 7. Crosstalk

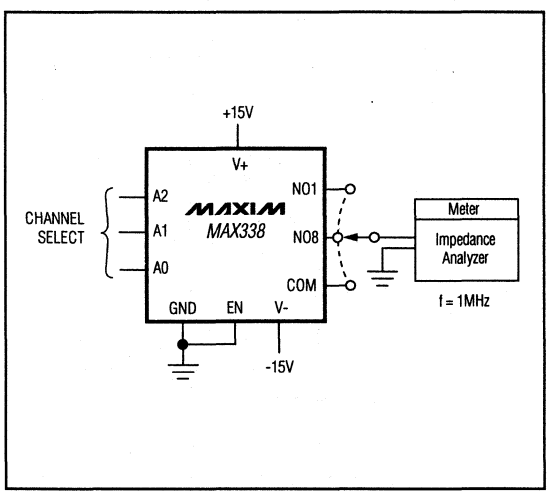
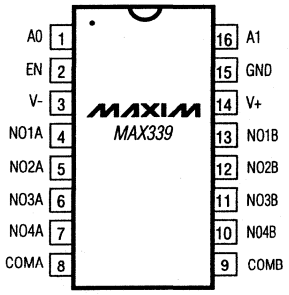


Figure 8. NO/COM Capacitance

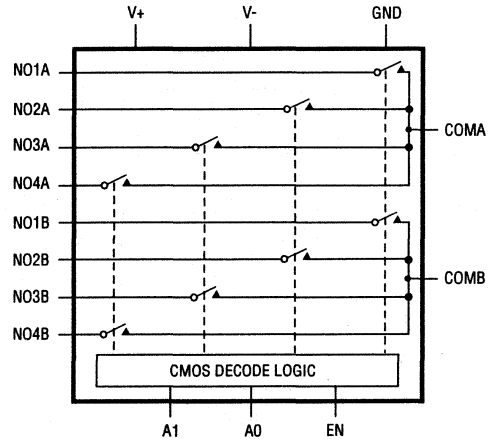
8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



DIP/SO



MAX339 8-CHANNEL SINGLE-ENDED MULTIPLEXER

A2	A1	A0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

MAX338

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

A1	A0	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

MAX339

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" $V_{AH} \geq 2.4V$

_Ordering Information (continued)

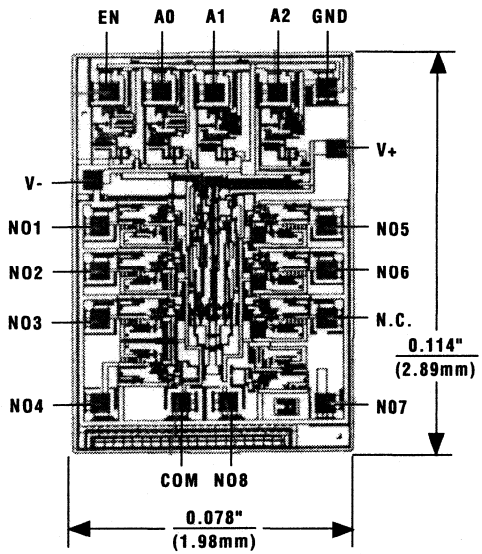
PART	TEMP. RANGE	PIN-PACKAGE
MAX339CPE	0°C to +70°C	16 Plastic DIP
MAX339CSE	0°C to +70°C	16 Narrow SO
MAX339C/D	0°C to +70°C	Dice*
MAX339EPE	-40°C to +85°C	16 Plastic DIP
MAX339ESE	-40°C to +85°C	16 Narrow SO
MAX339EJE	-40°C to +85°C	16 CERDIP
MAX339MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

8-Channel/Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexers

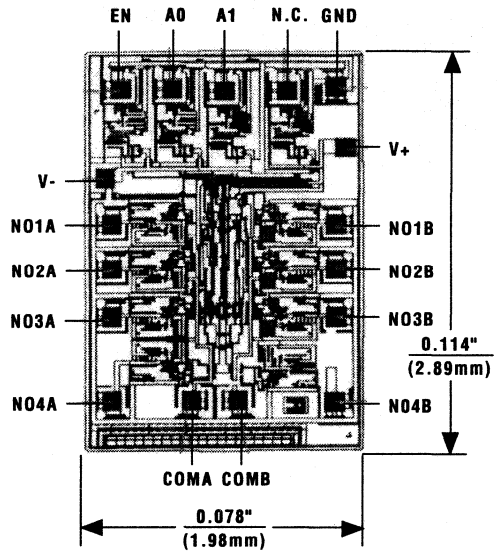
Chip Topographies

MAX338



TRANSISTOR COUNT: 224
SUBSTRATE IS INTERNALLY CONNECTED TO V+

MAX339



TRANSISTOR COUNT: 224
SUBSTRATE IS INTERNALLY CONNECTED TO V+

N.C. = NO INTERNAL CONNECTION

19-0212; Rev 1; 4/94

MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX351/MAX352/MAX353 are precision, quad, single-pole single-throw (SPST) analog switches. The MAX351 has four normally closed (NC), and the MAX352 has four normally open (NO) switches. The MAX353 has two NO and two NC switches. All three parts offer low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 6nA at +85°C) and fast switching (turn-on time less than 175ns and turn-off time less than 145ns).

The MAX351/MAX352/MAX353 are fabricated with Maxim's new improved 44V silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits	Military Radios
Guidance and Control Systems	Communications Systems
Heads-Up Displays	Battery-Operated Systems
Test Equipment	PBX, PABX

Features

- ♦ **Low On Resistance < 22Ω Typical (35Ω Max)**
- ♦ **Guaranteed Matched On Resistance Between Channels < 2Ω**
- ♦ **Guaranteed Flat On Resistance Over Analog Signal Range Δ3Ω Max**
- ♦ **Guaranteed Charge Injection < 10pC**
- ♦ **Guaranteed Off-Channel Leakage < 6nA at +85°C**
- ♦ **ESD Guaranteed > 2000V per Method 3015.7**
- ♦ **Single-Supply Operation (+10V to +30V) Bipolar-Supply Operation (±4.5V to ±20V)**
- ♦ **TTL-/CMOS-Logic Compatibility**
- ♦ **Rail-to-Rail Analog Signal Handling Capability**

Ordering Information

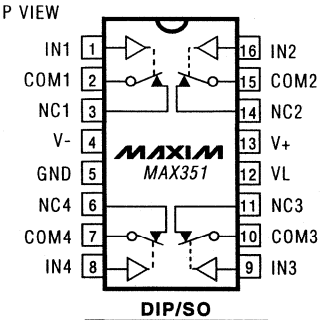
PART	TEMP. RANGE	PIN-PACKAGE
MAX351CPE	0°C to +70°C	16 Plastic DIP
MAX351CSE	0°C to +70°C	16 Narrow SO
MAX351C/D	0°C to +70°C	Dice*
MAX351EPE	-40°C to +85°C	16 Plastic DIP
MAX351ESE	-40°C to +85°C	16 Narrow SO
MAX351EJE	-40°C to +85°C	16 CERDIP
MAX351MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued on last page.

** Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations/Functional Diagrams/Truth Tables

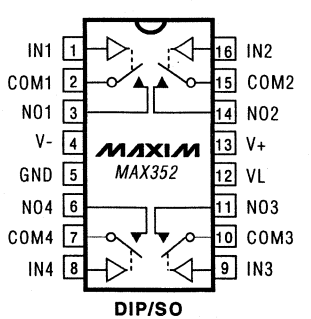
TOP VIEW



DIP/SO

MAX351

LOGIC	SWITCH
0	ON
1	OFF

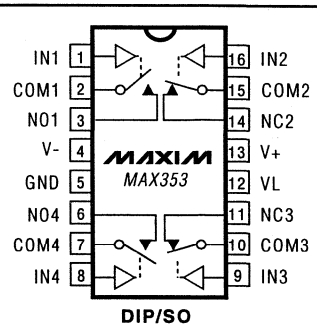


DIP/SO

MAX352

LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



DIP/SO

MAX353

LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

Precision, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
VL ..... (GND - 0.3V) to (V+ + 0.3V)
Digital Inputs, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... (V- - 2V) to (V+ + 2V)
..... or 30mA (whichever occurs first)
Current (any terminal) 30mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle max) 100mA
ESD per Method 3015.7 ..... >2000V

Continuous Power Dissipation (T_A = +70°C) (Note 2)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges:
MAX35_C_ _ ..... 0°C to +70°C
MAX35_E_ _ ..... -40°C to +85°C
MAX35_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on NC_, NO_, COM_, or IN_ exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 3)	MAX	UNITS
SWITCH								
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Notes 1, 4)			V-		V+	V
On Resistance	R_{ON}	I_{COM} = -10mA, $V_{NO\_}$ or $V_{NC\_}$ = ±8.5V, V+ = 13.5V, V- = -13.5V	T_A = +25°C	C, E		17	35	Ω
				M		17	30	
			T_A = T_{MIN} to T_{MAX}				45	
On Resistance Match Between Channels (Note 5)	R_{ON}	I_{COM} = -10mA, $V_{NO\_}$ or $V_{NC\_}$ = ±10V, V+ = 15V, V- = - 15V	T_A = +25°C				2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
On Resistance Flatness (Note 5)	R_{ON}	I_{COM} = -10mA, $V_{NO\_}$ or $V_{NC\_}$ = ±5V, V+ = 15V, V- = - 15V	T_A = +25°C				3	Ω
			T_A = T_{MIN} to T_{MAX}				5	
Off Leakage Current (NO_ or NC_)	I_{NO} I_{NC}	V_{COM} = -15.5V, $V_{NO\_}$ or $V_{NC\_}$ = 15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		-0.25	-0.10	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-6		6	
				M	-20		20	
COM_ Off Leakage Current	$I_{NC(OFF)}$	V_{COM} = -15.5V, $V_{NO\_}$ or $V_{NC\_}$ = 15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		-0.25	-0.10	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-6		6	
				M	-20		20	
COM_ On Leakage Current	$I_{COM(ON)}$	V_{COM} = ±15.5V, $V_{NO\_}$ or $V_{NC\_}$ = ±15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		-0.4	-0.1	0.4	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	
				M	-40		40	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	IN_ = 2.4V, all others = 0.8V		-0.500	0.005	0.500	µA
Input Current with Input Voltage Low	I_{INL}	IN_ = 0.8V, all others = 2.4V		-0.500	0.005	0.500	µA
SUPPLY							
Power-Supply Range				±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V V- = -16.5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V V- = -16.5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V V- = -16.5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V V- = -16.5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2, V_{COM} = ±10V	T_A = +25°C		110	175	ns
			T_A = T_{MIN} to T_{MAX}			220	
Turn-Off Time	t_{OFF}	Figure 2, V_{COM} = ±10V	T_A = +25°C		100	145	ns
			T_A = T_{MIN} to T_{MAX}			160	
Break-Before-Make Time Delay	t_D	MAX353 only, Figure 3, R_L = 300Ω, C_L = 35pF	T_A = +25°C		25		ns
Charge Injection	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C		5	10	pC
Off Isolation (Note 6)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		68		dB
Crosstalk (Note 7)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		85		dB
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
COM Off Capacitance	$C_{(COM)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
On Capacitance	$C_{(COM)}$	f = 1MHz, Figure 8	T_A = +25°C		35		pF

Precision, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 3)	MAX	UNITS
SWITCH							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, V_{NC}	(Notes 1, 4)		0		V+	V
Channel On Resistance	R_{ON}	I_{COM} = -10mA, $V_{NC\_}$ or $V_{NO\_}$ = 3.8V, V+ = 10.8V	T_A = +25°C		40	80	Ω
			T_A = T_{MIN} to T_{MAX}			100	
SUPPLY							
Positive Supply Current	I+	V+ = 13.2V, all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Negative Supply Current	I-	V+ = 13.2V, all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Logic Supply Current	I_L	VL = 5.25V, all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Ground Current	I_{GND}	VL = 5.25V, all channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2, $V_{NO\_}$ or $V_{NC\_}$ = 8V	T_A = +25°C		175	250	ns
			T_A = T_{MIN} to T_{MAX}			315	
Turn-Off Time	t_{OFF}	Figure 2, $V_{NO\_}$ or $V_{NC\_}$ = 8V	T_A = +25°C		95	125	ns
			T_A = T_{MIN} to T_{MAX}			140	
Break-Before-Make Time Delay	t_D	MAX353 only, Figure 3, R_L = 300Ω, C_L = 35pF	T_A = +25°C		25		ns
Charge Injection	Q	Figure 8, C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V	T_A = +25°C		5	10	pC

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: Guaranteed by design.

Note 5: $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min. On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation.

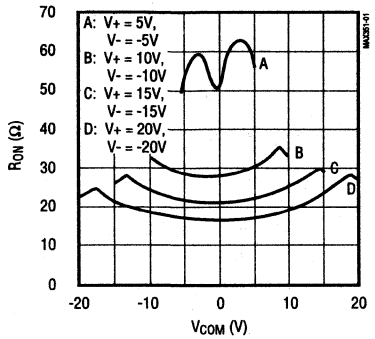
Note 6: See Figure 5. Off Isolation = 20 $\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

Note 7: Between any two switches. See Figure 6.

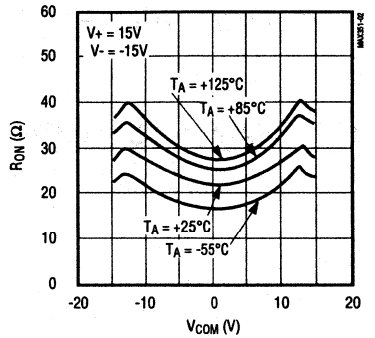
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

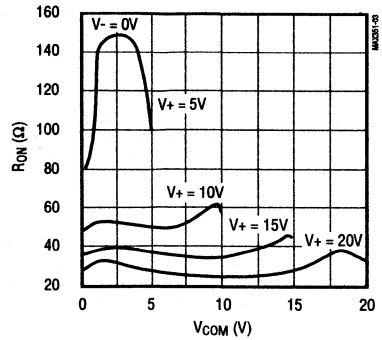
ON RESISTANCE vs. V_{COM} AND POWER-SUPPLY VOLTAGE



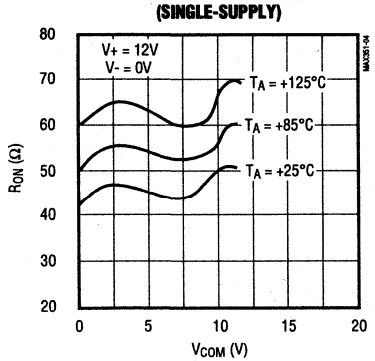
ON RESISTANCE vs. V_{COM} AND TEMPERATURE



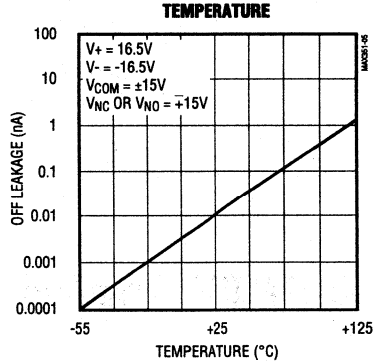
ON RESISTANCE vs. V_{COM} AND TEMPERATURE



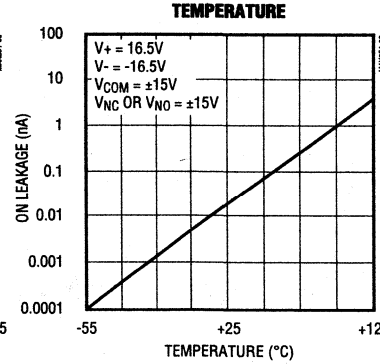
ON RESISTANCE vs. V_{COM} (SINGLE-SUPPLY)



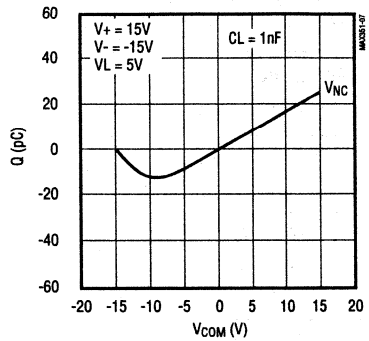
OFF LEAKAGE CURRENTS vs. TEMPERATURE



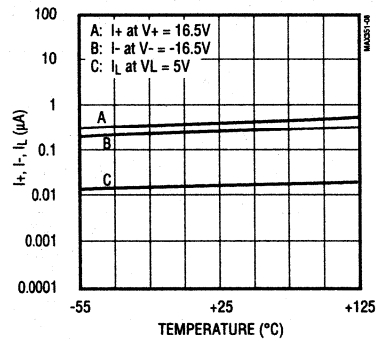
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Precision, Quad, SPST Analog Switches

Pin Description

PIN	NAME	FUNCTION
1, 8, 9, 16	IN1-IN4	Inputs
2, 7, 10, 15	COM1-COM4	Analog Switch Common Terminal
3, 6, 11, 14	NO or NC	Switch Inputs
4	V-	Negative Supply-Voltage Input
5	GND	Ground
12	VL	Logic Supply Voltage
13	V+	Positive Supply-Voltage Input—connected to substrate

Applications Information

Operation with Supplies Other than ±15V

The main limitation of supply voltages other than ±15V is reduced analog-signal range. The MAX351/MAX352/MAX353 operate with ±5V to ±20V bipolar supplies. The *Typical Operating Characteristics* graphs show typical on resistance (R_{ON}) for ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.) The MAX351/MAX352/MAX353 can operate from +10V to +30V unipolar supplies. Each device can also be powered from unbalanced supplies such as +24V and -5V. Connect V- to 0V when operating with a single supply. VL must be connected to +5V to be TTL compatible or to V+ for CMOS-logic input levels.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with the supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low-leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ to V- should not exceed +44V.

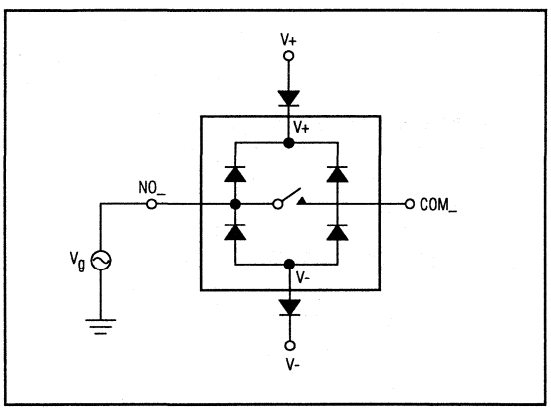


Figure 1. Overvoltage Protection Using External Blocking Diodes

Test Circuits/Timing Diagrams

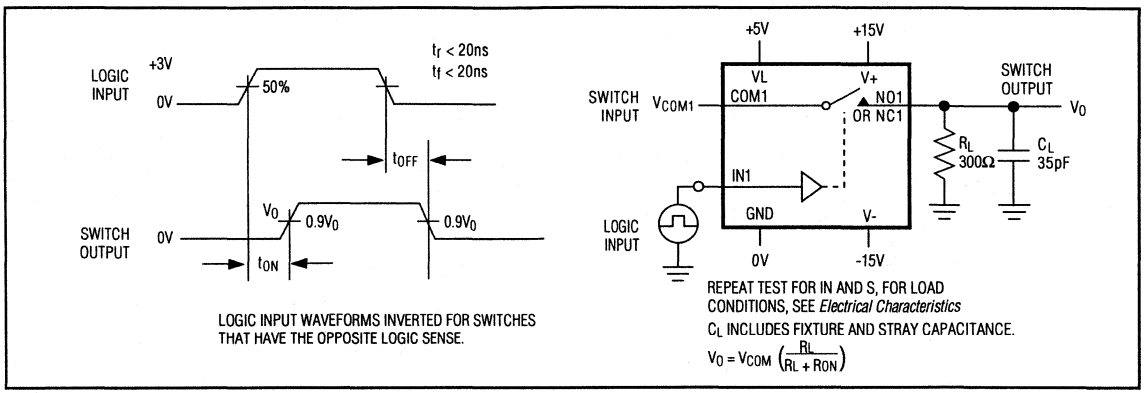


Figure 2. Switching-Time Test Circuit

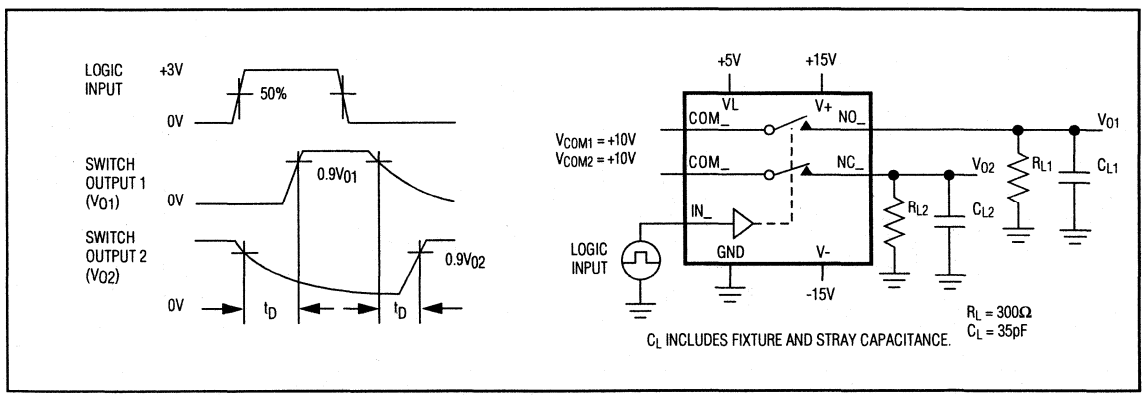


Figure 3. Break-Before-Make Test Circuit (MAX353 only)

Precision, Quad, SPST Analog Switches

Test Circuits/Timing Diagrams (continued)

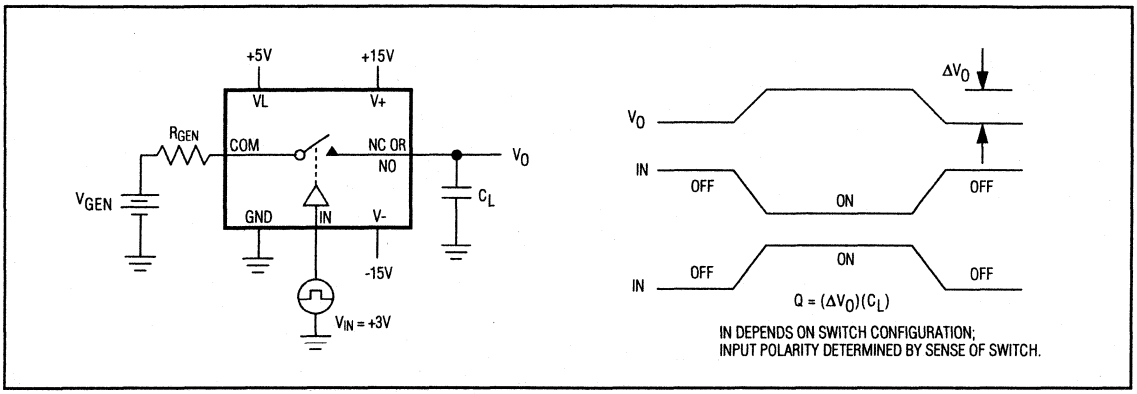


Figure 4. Charge-Injection Test Circuit

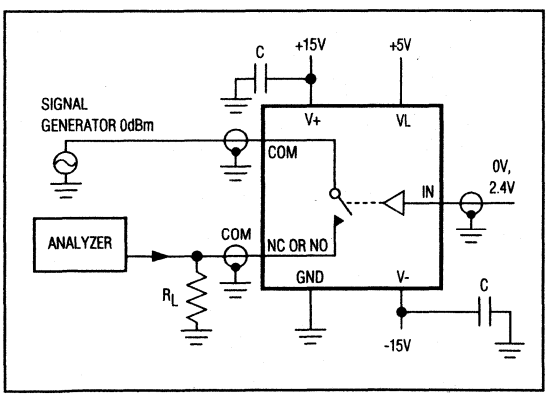


Figure 5. Off-Isolation Test Circuit

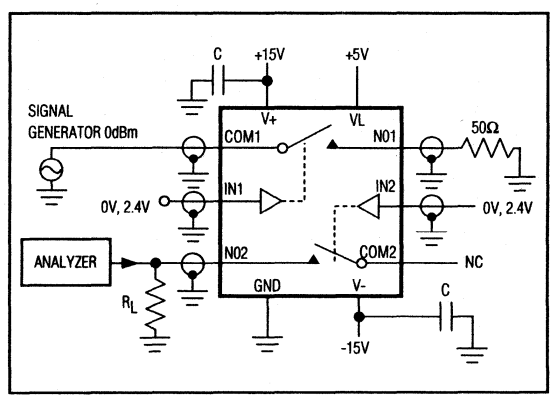


Figure 6. Crosstalk Test Circuit

Test Circuits/Timing Diagrams (continued)

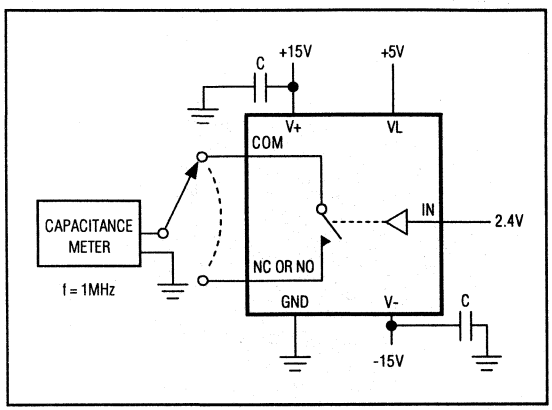


Figure 7. Channel-Off Capacitance

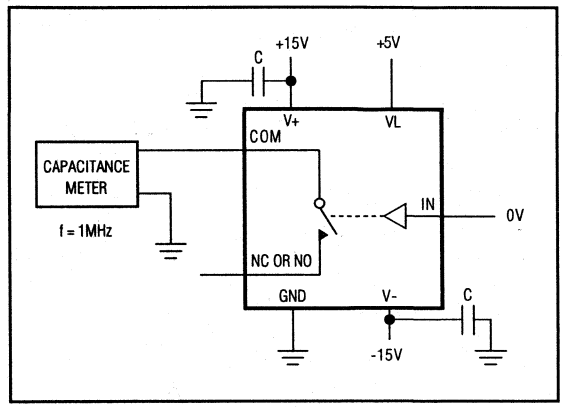


Figure 8. Channel-On Capacitance Test Circuit

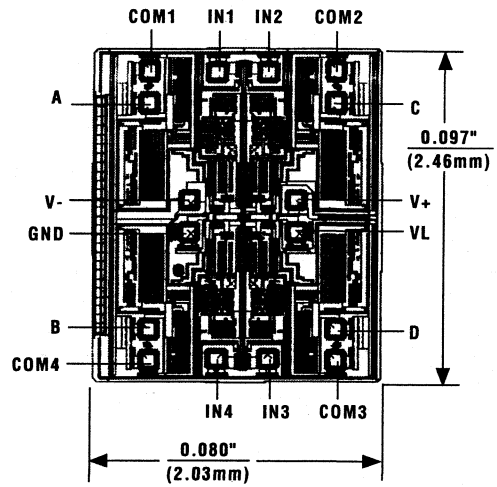
Precision, Quad, SPST Analog Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX352CPE	0°C to +70°C	16 Plastic DIP
MAX352CSE	0°C to +70°C	16 Narrow SO
MAX352C/D	0°C to +70°C	Dice*
MAX352EPE	-40°C to +85°C	16 Plastic DIP
MAX352ESE	-40°C to +85°C	16 Narrow SO
MAX352EJE	-40°C to +85°C	16 CERDIP
MAX352MJE	-55°C to +125°C	16 CERDIP
MAX353CPE	0°C to +70°C	16 Plastic DIP
MAX353CSE	0°C to +70°C	16 Narrow SO
MAX353C/D	0°C to +70°C	Dice*
MAX353EPE	-40°C to +85°C	16 Plastic DIP
MAX353ESE	-40°C to +85°C	16 Narrow SO
MAX353EJE	-40°C to +85°C	16 CERDIP
MAX353MJE	-55°C to +125°C	16 CERDIP

** Contact factory for dice specifications.*

Chip Topography



TRANSISTOR COUNT: 136;
SUBSTRATE CONNECTED TO V+.

MAX351		MAX352		MAX353	
PIN	NAME	PIN	NAME	PIN	NAME
A	NC	A	NO	A	NO
B	NC	B	NO	B	NO
C	NC	C	NO	C	NC
D	NC	D	NO	D	NC

19-0180; Rev 0; 9/93

MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX361/MAX362 are precision, quad, single-pole single-throw (SPST) analog switches. The MAX361 has four normally closed (NC) switches, and the MAX362 has four normally open (NO) switches. Both parts offer low channel on resistance (less than 85Ω), guaranteed to match within 3Ω between channels and to remain flat over the analog signal range (Δ9Ω max). Both parts also offer low leakage (less than 500pA at +25°C and less than 4nA at +85°C) and fast switching (turn-on time less than 250ns and turn-off time less than 170ns).

The MAX361/MAX362 are fabricated with Maxim's new improved 44V silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35µW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Heads-Up Displays
Test Equipment
Communications Systems
Battery-Operated Systems
PBX, PABX

Features

- **Low On Resistance: < 45Ω Typical (85Ω Max)**
- **Guaranteed Matched On Resistance Between Channels: < 2Ω**
- **Guaranteed Flat On Resistance over Analog Signal Range: Δ9Ω Max**
- **Guaranteed Charge Injection: < 10pC**
- **Guaranteed Off-Channel Leakage: <4nA at +85°C**
- **ESD Guaranteed > 2000V per Method 3015.7**
- **Single-Supply Operation (+10V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- **TTL-/CMOS-Logic Compatible**
- **Rail-to-Rail Analog Signal Handling Capability**

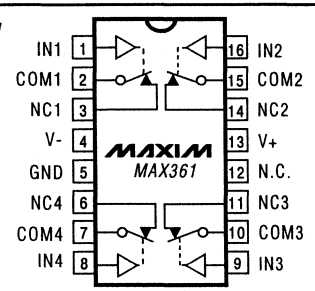
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX361CPE	0°C to +70°C	16 Plastic DIP
MAX361CSE	0°C to +70°C	16 Narrow SO
MAX361C/D	0°C to +70°C	Dice*
MAX361EPE	-40°C to +85°C	16 Plastic DIP
MAX361ESE	-40°C to +85°C	16 Narrow SO
MAX361EJE	-40°C to +85°C	16 CERDIP
MAX361MJE	-55°C to +125°C	16 CERDIP
MAX362CPE	0°C to +70°C	16 Plastic DIP
MAX362CSE	0°C to +70°C	16 Narrow SO
MAX362C/D	0°C to +70°C	Dice*
MAX362EPE	-40°C to +85°C	16 Plastic DIP
MAX362ESE	-40°C to +85°C	16 Narrow SO
MAX362EJE	-40°C to +85°C	16 CERDIP
MAX362MJE	-55°C to +125°C	16 CERDIP

* *Contact factory for dice specifications.*

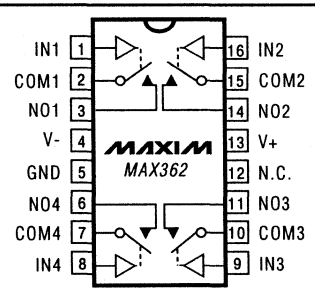
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

MAX361	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX362	
LOGIC	SWITCH
0	OFF
1	ON

N.C. = Not Internally Connected

SWITCHES SHOWN FOR LOGIC "0" INPUT

Precision, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
IN_, COM_, NO_, NC_ ..... (V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current COM, NO, NC
(pulsed at 1ms, 10% duty cycle max) 100mA
ESD 2000V

Continuous Power Dissipation (T_A = +70°C) (Note 1)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges:
MAX36_C_ _ ..... 0°C to +70°C
MAX36_E_ _ ..... -40°C to +85°C
MAX36_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG								
Analog-Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)			-15		15	V
On Resistance (COM_ to NO_ or COM_ to NC_ terminals)	R_{ON}	$I_{(NO\ or\ NC)}$ = -10mA, $V_{COM\_}$ = 8.5V or -8.5V, V+ = 13.5V, V- = -13.5V	T_A = +25°C			50	85	Ω
			T_A = T_{MIN} to T_{MAX}				100	
On Resistance Match Between Channels (Note 4)	R_{ON}	$I_{(NO\ or\ NC)}$ = -10mA, $V_{COM\_}$ = 10V or -10V, V+ = 15V, V- = -15V	T_A = +25°C				2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
On Resistance Flatness (Note 4)	R_{ON}	$I_{(NO\ or\ NC)}$ = -10mA, $V_{COM\_}$ = 5V or -5V, V+ = 15V, V- = -15V	T_A = +25°C				9	Ω
			T_A = T_{MIN} to T_{MAX}				15	
Off Leakage Current (NO_ or NC_ terminal)	$I_{NO\_}$, $I_{NC\_}$	$V_{COM\_}$ = ±15.5V, $V_{NC\_}$ or $V_{NO\_}$ = ∓15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		-0.50	0.01	0.50	nA
			T_A = T_{MAX}	C, E	-4		4	
				M	-20		20	
Off Leakage Current (COM_ terminal)	I_{COM}	$V_{NC\_}$ or $V_{NO\_}$ = ±15.5V, $V_{COM\_}$ = ∓15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		-0.50	0.01	0.50	nA
			T_A = T_{MAX}	C, E	-4		4	
				M	-20		20	
On Leakage Current (COM_ and NC_ or NO_ terminal)	I_{COM} or I_{NO}, I_{NC}	$V_{COM\_}$ = ±15.5V, $V_{NC\_}$ or $V_{NO\_}$ = ±15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		-0.50	0.08	0.50	nA
			T_A = T_{MAX}	C, E	-6		6	
				M	-40		40	
DIGITAL								
Input Current with Input Voltage High	I_{INH}	$V_{IN\_}$ = 2.4V			-500	0.01	500	nA
Input Current with Input Voltage Low	I_{INH}	$V_{IN\_}$ = 0.8V			-500	0.01	500	nA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SUPPLY							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V			15	100	µA
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V		-100	-15		µA
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1, V_S = ±10V, R_L = 1kΩ	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	MAX361, Figure 1, V_{COM} = ±10V	T_A = +25°C		90	120	ns
		MAX362, Figure 1, V_{COM} = ±10V	T_A = +25°C		110	170	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	T_A = +25°C		5	10	pC
Off Isolation (Note 5)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 3	T_A = +25°C		60		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		-100		dB
Off Capacitance NC or NO	$C_{(OFF)}$	f = 1MHz, Figure 5	T_A = +25°C		4		pF
Off Capacitance COM_	$C_{COM(OFF)}$	f = 1MHz, Figure 5	T_A = +25°C		4		pF
Channel-On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 5	T_A = +25°C		16		pF

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog-Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)		0		12	V
On Resistance (COM_ to NO_ or COM_ to NC_ terminals)	R_{ON}	$I_{(NC\ or\ NO)}$ = 1.0mA, $V_{COM\_}$ = 3V, 8V, V+ = 10.8V	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range	V+			10		30	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V			15	100	µA
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		+5	µA
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V		-100	-15		
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1, V_S = 8V	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	Figure 1, V_S = 8V	T_A = +25°C		60	200	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V,	T_A = +25°C		5	10	pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On resistance match between channels and flatness are guaranteed only with bipolar-supply operation.

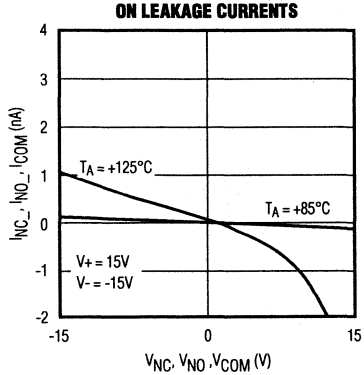
Note 5: See Figure 3. Off Isolation = $20 \log_{10} \left(\frac{V_{COM}}{V_{NC\_ \text{ or } NO\_}} \right)$, V_{COM} = output, $V_{NC\ or\ NO}$ = input to off switch.

Note 6: Between any two switches. See Figure 4.

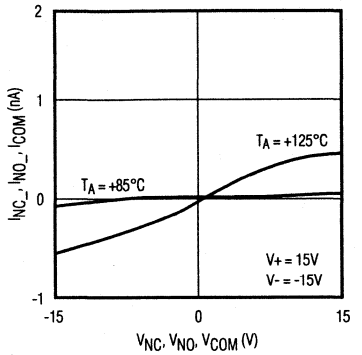
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

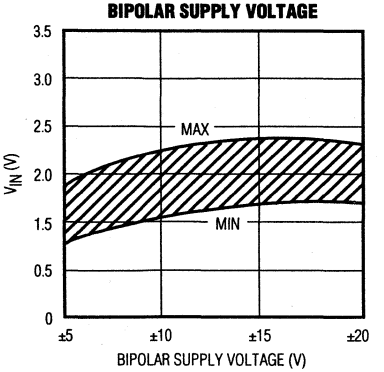
ON LEAKAGE CURRENTS



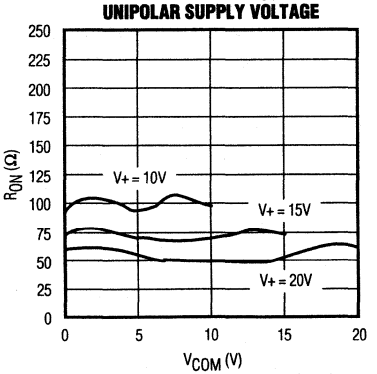
OFF LEAKAGE CURRENTS



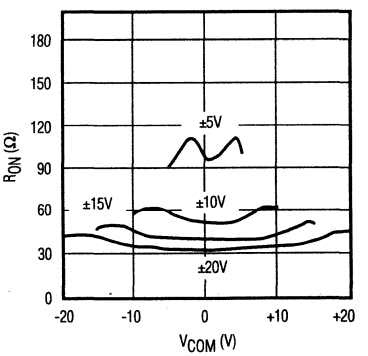
SWITCHING THRESHOLD vs. BIPOLAR SUPPLY VOLTAGE



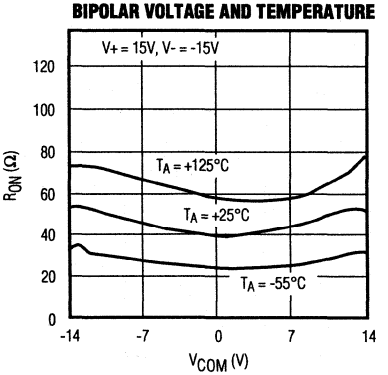
ON RESISTANCE vs. VCOM AND UNIPOLAR SUPPLY VOLTAGE



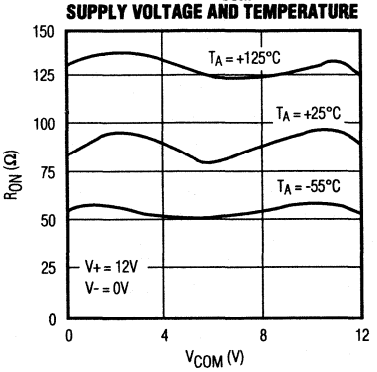
ON RESISTANCE vs. VCOM AND BIPOLAR SUPPLY VOLTAGE



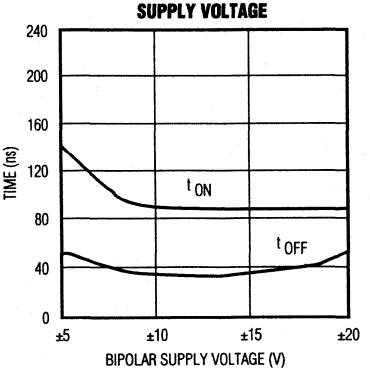
ON RESISTANCE vs. VCOM AND BIPOLAR VOLTAGE AND TEMPERATURE



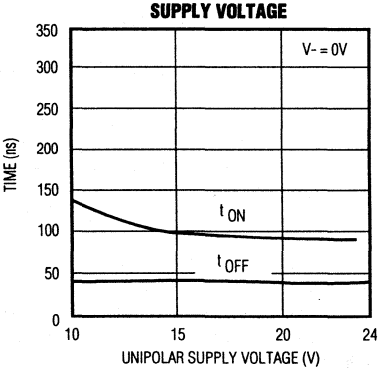
ON RESISTANCE vs. VCOM AND UNIPOLAR SUPPLY VOLTAGE AND TEMPERATURE



SWITCHING TIME vs. BIPOLAR SUPPLY VOLTAGE



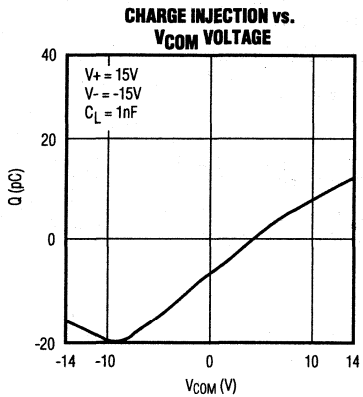
SWITCHING TIMES vs. UNIPOLAR SUPPLY VOLTAGE

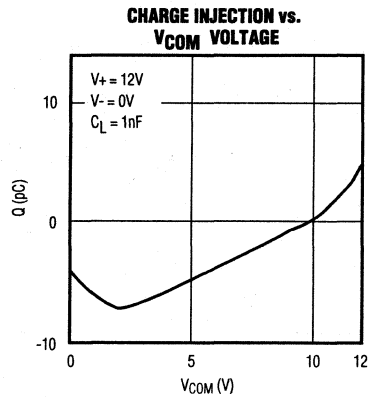


Precision, Quad, SPST Analog Switches

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





Pin Description

PIN	NAME		FUNCTION
	MAX361	MAX362	
1, 16, 9, 8	IN1-IN4	IN1-IN4	Logic-level input
2, 15, 10, 7	COM1-COM4	COM1-COM4	Analog switch common terminal
3, 14, 11, 6	NC1-NC4	NO1-NO4	NC (normally closed, MAX361) NO (normally open, MAX362) Analog switch terminal
4	V-	V-	Negative supply voltage input
5	GND	GND	Ground
12	N.C.	N.C.	Not internally connected
13	V+	V+	Positive supply voltage input—connected to substrate.

Applications Information

Operation with Supply Voltages Other Than ±15V

Using supply voltages other than ±15V is reduces the analog signal range. The MAX361/MAX362 switches operate with bipolar supplies of ±4.5V to ±20V. Typical operating characteristic graphs show typical on resistance for ±15V, ±10V, and ±5V supplies. Switching times increase by a factor of two or more for ±5V operation. The MAX361/MAX362 can also operate from +10V to +30V unipolar supplies. Both parts can also be powered from unbalanced supplies such as +24V and -5V. Connect V- to 0V when operating with a single supply.

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with the supply pins for overvoltage protection (Figure 6). Adding the diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference from V+ to V- should not exceed +44V.

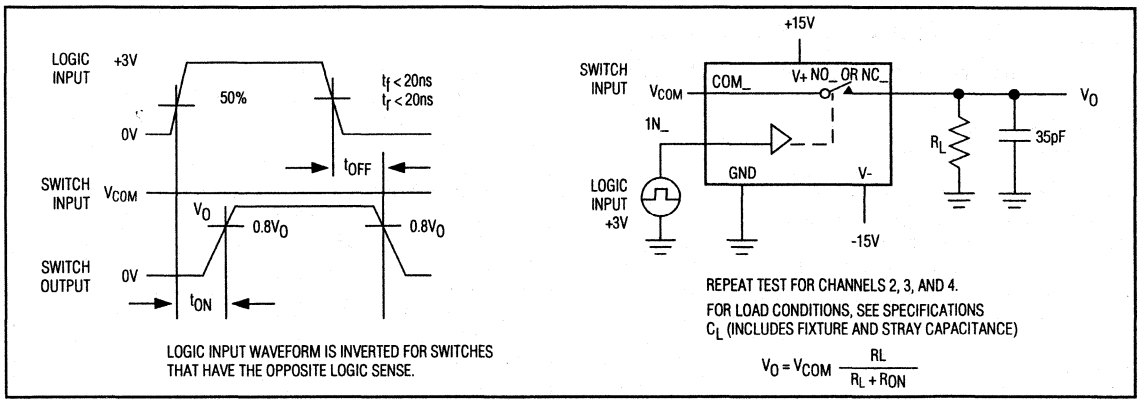


Figure 1. Switching-Time Test Circuit

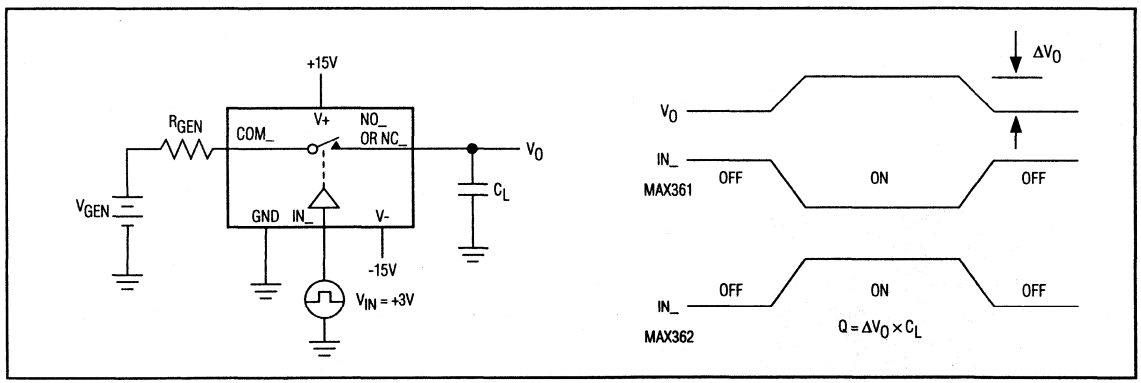


Figure 2. Charge-Injection Test Circuit

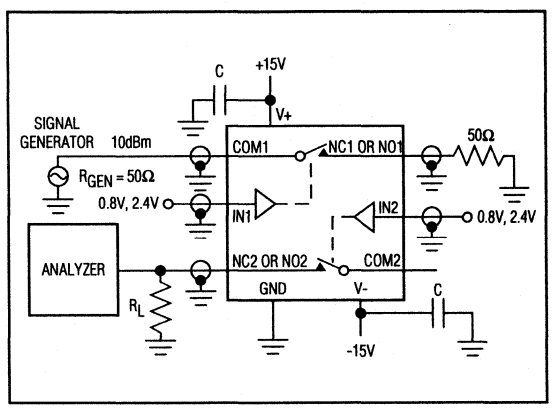


Figure 3. Crosstalk Test Circuit (repeat for channels 3 and 4)

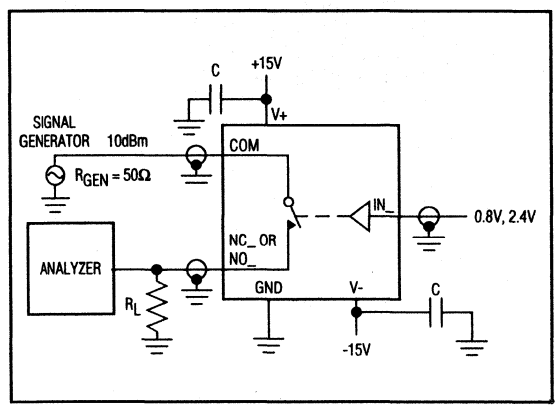


Figure 4. Off-Isolation Test Circuit

Precision, Quad, SPST Analog Switches

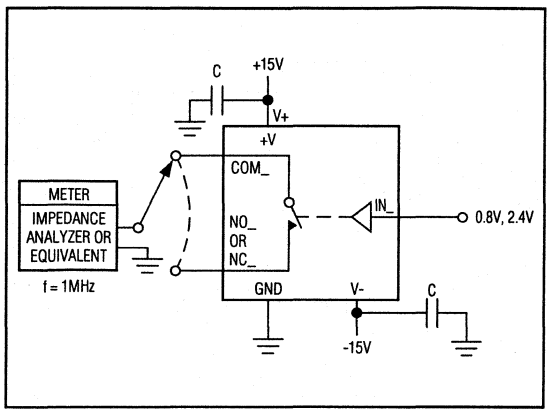


Figure 5. Channel Capacitance Test Circuit

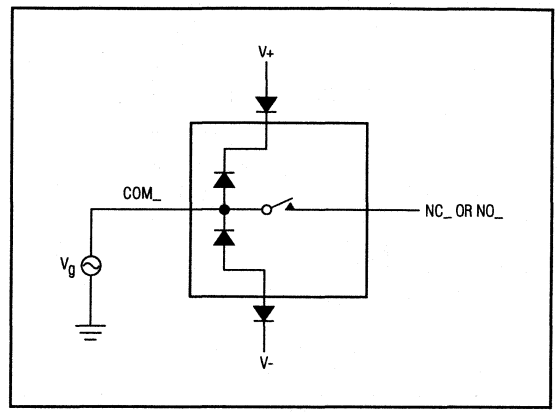
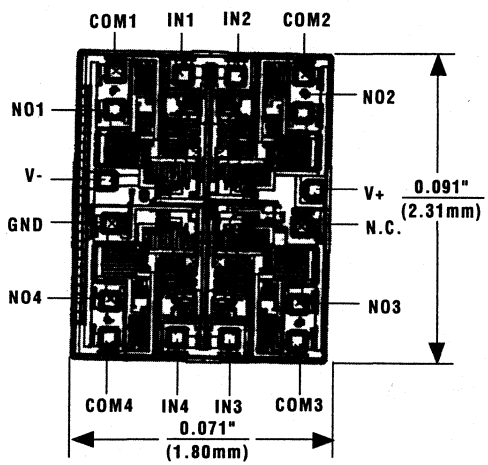


Figure 6. Overvoltage Protection Using Blocking Diodes

Chip Topography



TRANSISTOR COUNT: 126;
SUBSTRATE CONNECTED TO V+.

19-0181; Rev 0; 9/93

MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX364/MAX365 are precision, quad, single-pole single-throw (SPST) analog switches. The MAX364 has four normally closed (NC), and the MAX365 has four normally open (NO) switches. Both parts offer low-channel on resistance (less than 85Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range (Δ9Ω max). Both parts also offer low leakage (less than 500pA at +25°C and less than 4nA at +85°C) and fast switching (turn-on time less than 250ns and turn-off time less than 170ns).

The MAX364/MAX365 are fabricated with Maxim's new improved 44V silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), low power consumption (35μW), and electrostatic discharge (ESD) greater than 2000V. The 44V maximum breakdown voltage allows rail-to-rail analog signal handling capability.

These monolithic switches operate with a single positive supply (+10V to +30V) or with split supplies (±4.5V to ±20V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits	Communication Systems
Guidance and Control Systems	Battery-Operated Systems
Heads-Up Displays	PBX, PABX
Test Equipment	Military Radios

Features

- ♦ **Low On Resistance: < 45Ω Typical (85Ω Max)**
- ♦ **Guaranteed Matched On Resistance Between Channels: < 2Ω**
- ♦ **Guaranteed Flat On Resistance over Full Analog Signal Range: Δ9Ω Max**
- ♦ **Guaranteed Charge Injection: < 10pC**
- ♦ **Guaranteed Off-Channel Leakage: < 4nA at +85°C**
- ♦ **ESD Guaranteed > 2000V per Method 3015.7**
- ♦ **Single-Supply Operation (+10V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- ♦ **TTL-/CMOS-Logic Compatible**
- ♦ **Rail-to-Rail Analog Signal Handling Capability**

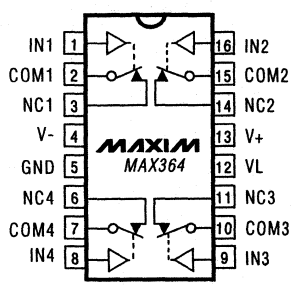
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX364CPE	0°C to +70°C	16 Plastic DIP
MAX364CSE	0°C to +70°C	16 Narrow SO
MAX364C/D	0°C to +70°C	Dice*
MAX364EPE	-40°C to +85°C	16 Plastic DIP
MAX364ESE	-40°C to +85°C	16 Narrow SO
MAX365CPE	0°C to +70°C	16 Plastic DIP
MAX365CSE	0°C to +70°C	16 Narrow SO
MAX365C/D	0°C to +70°C	Dice*
MAX365EPE	-40°C to +85°C	16 Plastic DIP
MAX365ESE	-40°C to +85°C	16 Narrow SO

** Contact factory for dice specifications.*

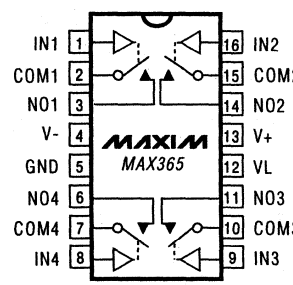
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

MAX364	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

MAX365	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Precision, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
VL ..... (GND - 0.3V) to (V+ + 0.3V)
IN_, COM_, NO_, or NC_ ..... (V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current COM_, NO_, or NC_ (pulsed at 1ms, 10% duty cycle max) 100mA
ESD 2000V

Note 1: All leads are soldered or welded to PC board.

Continuous Power Dissipation (T_A = +70°C) (Note 1)
Plastic DIP (derate 10.53mW/°C above +70°C 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Ranges:
MAX36_C_ _ ..... 0°C to +70°C
MAX36_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG							
Analog-Signal Range	$V_{COM\_}$, $V_{NO\_}$, V_{NC}	(Note 3)		-15		15	V
On Resistance	R_{ON}	COM_ to NO_ or NC, I_{COM} = -10mA, V_{COM} = 8.5V or -8.5V, V+ = 13.5V, V- = -13.5V	T_A = +25°C		50	85	Ω
			T_A = T_{MIN} to T_{MAX}			100	
On Resistance Match Between Channels (Note 4)	R_{ON}	I_{COM} = -10mA, V_{COM} = 10V or -10V, V+ = 15V, V- = -15V	T_A = +25°C			2	Ω
			T_A = T_{MIN} to T_{MAX}			4	
On Resistance Flatness (Note 4)	R_{ON}	I_{COM} = -10mA, V_{COM} = 5V or -5V, V+ = 15V, V- = -15V	T_A = +25°C			9	Ω
			T_A = T_{MIN} to T_{MAX}			15	
NC_ or NO_ Leakage Current	$I_{NO\_}$, I_{NC}	NO_ or NC_ terminal, V_{COM} = ±15.5V, V_{NO} or V_{NC} = ∓15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-4		4	
COM_ Off Leakage Current	I_{NO}, I_{NC}	COM_ terminal, V_{NO} or V_{NC} = ±15.5V, V_{COM} = ∓15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-4		4	
COM_, NC_ or NO_ On Leakage Current	I_{COM} or I_{NO}, I_{NC}	COM_ to NC_ or NO_, V_{COM} = ±15.5V, V_{NO} or V_{NC} = ±15.5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-0.50	0.08	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-6		6	
INPUT							
Input Current with Input Voltage High	I_{INH}	$V_{IN\_}$ = 2.4V, all others = 0.8V		-0.5	-0.00001	0.5	µA
Input Current with Input Voltage Low	I_{INL}	$V_{IN\_}$ = 0.8V, all others = 2.4V		-0.5	-0.00001	0.5	µA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SUPPLY							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = ±10V, Figure 2	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	MAX364, V_{NO} or V_{NC} = ±10V, Figure 2	T_A = +25°C		90	120	ns
		MAX365, V_{NO} or V_{NC} = ±10V, Figure 2	T_A = +25°C		110	170	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		5	10	pC
Off Isolation (Note 5)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		60		dB
Crosstalk (Note 6)		RL - 50Ω, CL = 5pF, f = 1MHz, Figure 5	T_A = +25°C		100		dB
NC_ or NO_ Off Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
COM_ Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Channel-On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6	T_A = +25°C		16		pF

Precision, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG							
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$	(Note 3)		0		12	V
On Resistance	R_{ON}	COM_ to NO_ or NC_, I_{NC} or I_{NO} = -10mA, VL = 5.25V, V_{COM} = 3V, 8V, V+ = 10.8V	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range	V+, V-			10.8		24.0	V
Power-Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_{NC} or V_{NO}= 8V, Figure 2	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	V_{NC} or V_{NO} = 8V, Figure 2	T_A = +25°C		60	200	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		5	10	pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On resistance match between channels and flatness are guaranteed only with bipolar-supply operation.

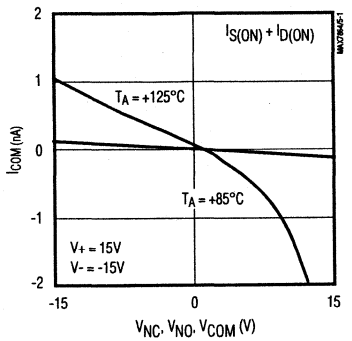
Note 5: See Figure 2. Off Isolation = $20 \log_{10} \left(\frac{V_{COM}}{V_{NC \text{ or } V_{NO}}} \right)$, V_{COM} = output, V_{NO} or V_{NC} = input to off switch.

Note 6: Between any two switches. See Figure 5.

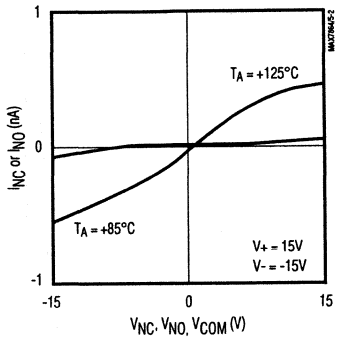
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

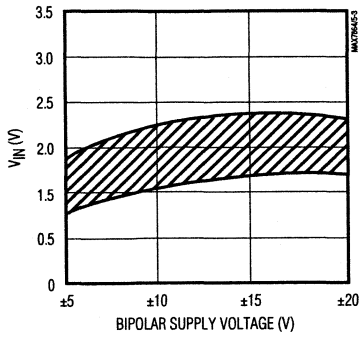
ON LEAKAGE CURRENTS



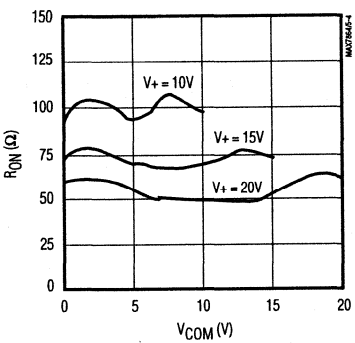
OFF LEAKAGE CURRENTS



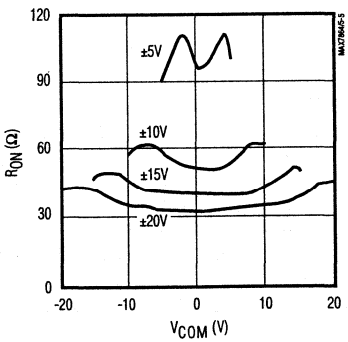
SWITCHING THRESHOLD vs. BIPOLAR SUPPLY VOLTAGE



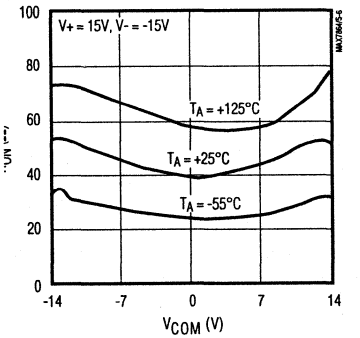
ON RESISTANCE vs. V_{COM} AND UNIPOLAR SUPPLY VOLTAGE



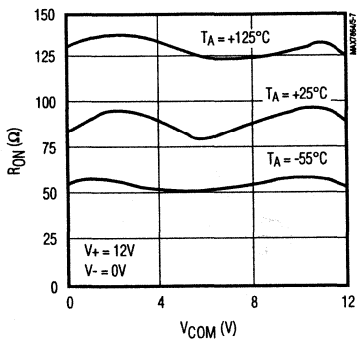
ON RESISTANCE vs. V_{COM} AND BIPOLAR SUPPLY VOLTAGE



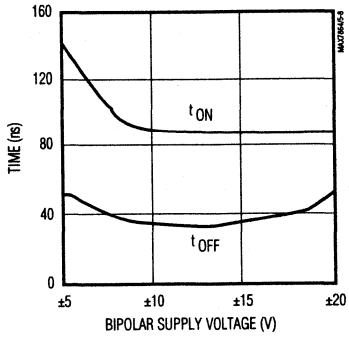
ON RESISTANCE vs. V_{COM}, BIPOLAR SUPPLY VOLTAGE AND TEMPERATURE



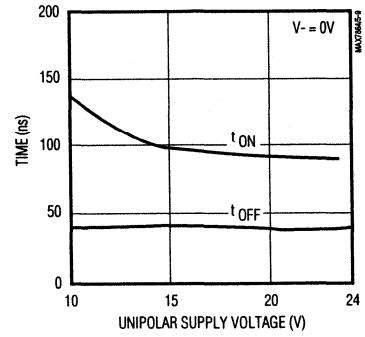
ON RESISTANCE vs. V_{COM}, UNIPOLAR SUPPLY VOLTAGE AND TEMPERATURE



SWITCHING TIME vs. BIPOLAR SUPPLY VOLTAGE



SWITCHING TIMES vs. UNIPOLAR SUPPLY VOLTAGE

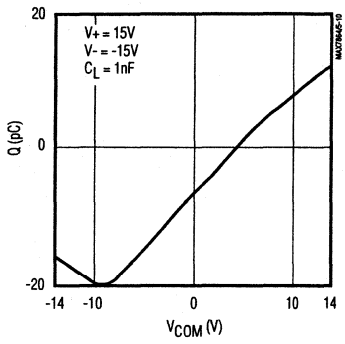


Precision, Quad, SPST Analog Switches

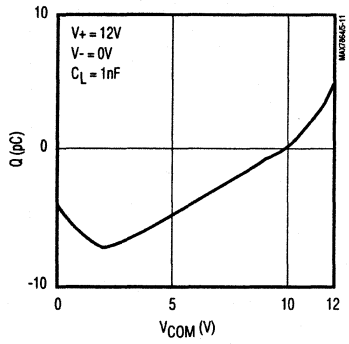
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

CHARGE INJECTION vs. V_{COM} VOLTAGE



CHARGE INJECTION vs. V_{COM} VOLTAGE



Pin Description

PIN	NAME	FUNCTION
1, 16, 9, 8	IN1-IN4	Logic-Level Input
2, 15, 10, 7	COM1-COM4	Analog Switch Common Terminal
3, 14, 11, 6	NC1-NC4 (MAX364)	Normally Closed Analog Switch Terminal
	NO1-NO4 (MAX365)	Normally Open Analog Switch Terminal
4	V-	Negative Supply Voltage Input
5	GND	Ground
12	VL	Logic Supply Voltage Input
13	V+	Positive Supply Voltage Input—connected to substrate

Applications Information

Application Hints

1. Switches are open when power is off.
2. IN_, COM_, NO_, and NC_ should not exceed V+ or V-, even with the power off.
3. Switch leakage is from each analog switch terminal to V+ or V-, not to the other switch terminal.

Operation with Supply Voltages Other than ±15V

The main limitation of supply voltages other than ±15V is reduction in the analog signal range. The MAX364/MAX365 switches operate with ±5V to ±20V bipolar supplies. The *Typical Operating Characteristics* graphs show typical on resistance for ±15V, ±10V, and ±5V supplies. Switching times increase by a factor of two or more for ±5V operation. The MAX364/MAX365 operate from unipolar supplies of +10V to +24V. Both parts can be powered from a single +10V to +24V supply, as well as from unbalanced supplies, such as +24V and -5V. Connect V- to 0V when operating with a single supply. VL must be connected to +5V to be TTL compatible or to V+ for CMOS logic input levels.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. It is important not to exceed the absolute maximum ratings, because stresses beyond those listed may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, protect the devices from overvoltage by adding two small signal diodes in series with the supply pins (Figure 1). Adding the diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ to V- should not exceed +44V.

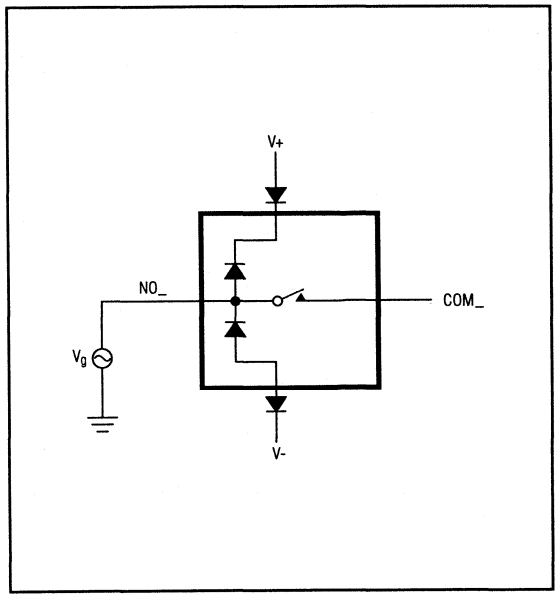


Figure 1. Overvoltage Protection Using Blocking Diodes

Precision, Quad, SPST Analog Switches

Test Circuits/Timing Diagrams

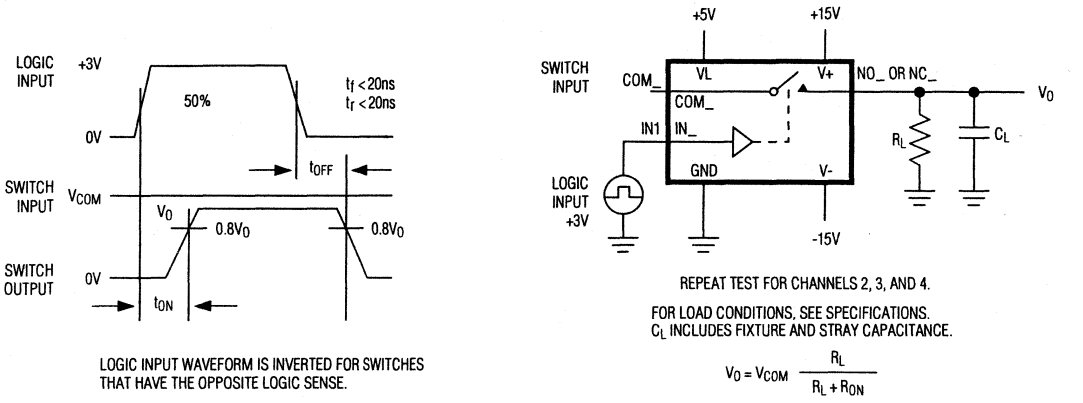


Figure 2. Switching-Time Test Circuit

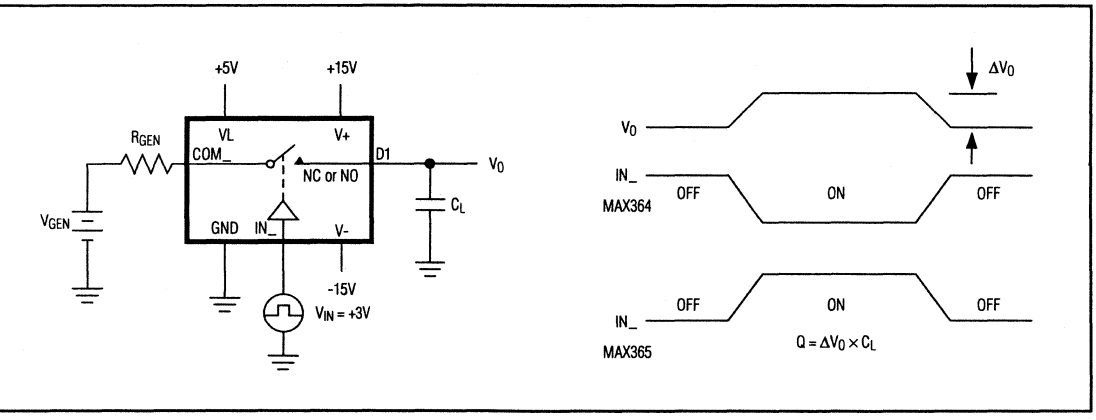


Figure 3. Charge-Injection Test Circuit

Test Circuits/Timing Diagrams (continued)

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100Hz to 13MHz	AUTOMATIC SYNTHESIZER	SPECTRUM ANALYZER

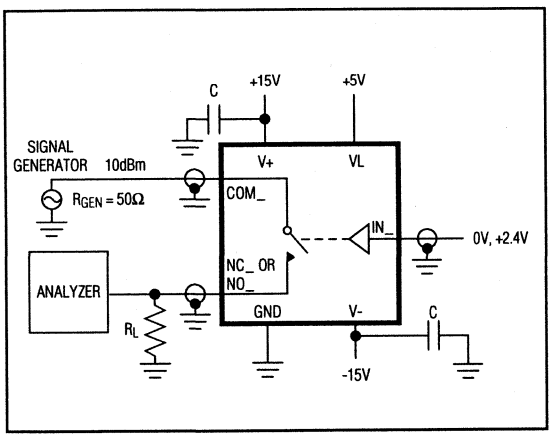


Figure 4. Off Isolation Test Circuit

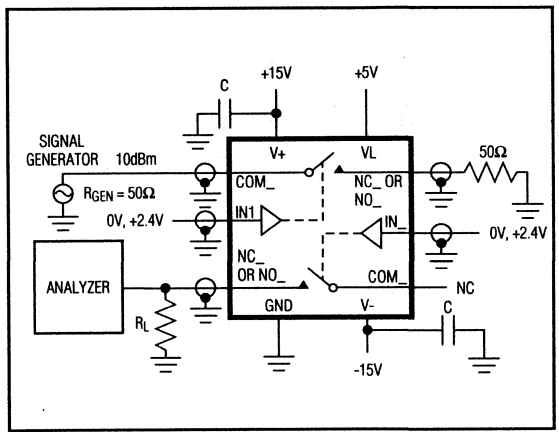


Figure 5. Crosstalk Test Circuit

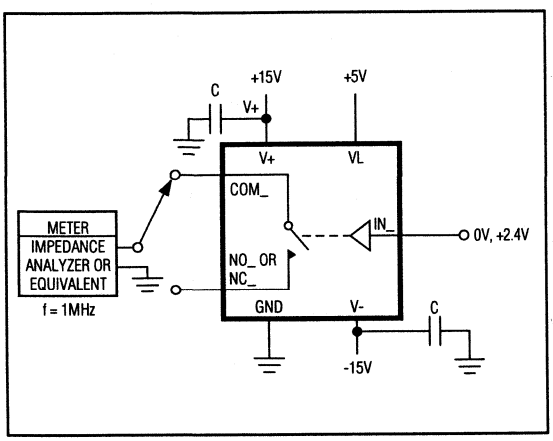


Figure 6. COM_, NC_, NO_ Off Capacitance

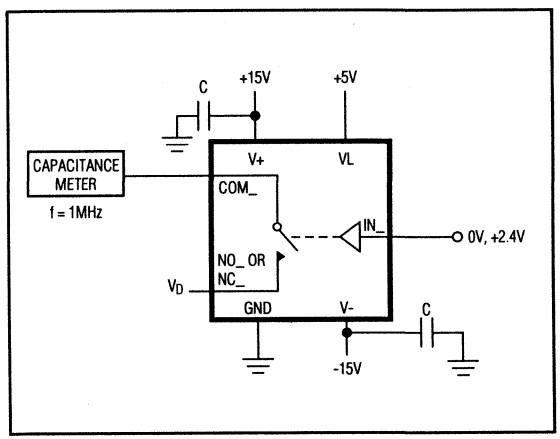
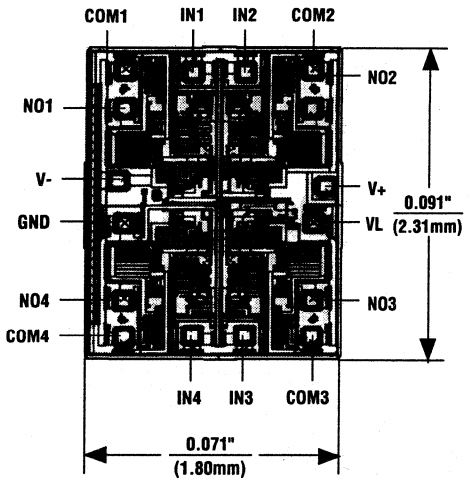


Figure 7. COM_, NC_, NO_ On Capacitance

Precision, Quad, SPST Analog Switches

Chip Topography



TRANSISTOR COUNT: 126;
SUBSTRATE CONNECTED TO V+.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Signal Line Circuit Protectors

General Description

The MAX366/MAX367 are multiple, two-terminal circuit protectors. Placed in series with signal lines, each two-terminal device protects sensitive circuit components from damaging voltages near and beyond the normal supply range. They are used at interfaces where sensitive circuits are connected to the external world and potentially damaging voltages (up to 35V beyond the supply rails) may be encountered during power-up, power-down, or fault conditions.

The MAX366 contains three protectors; the MAX367 contains eight protectors. They can be used to protect either analog or digital signals using unipolar (5V to 44V) or bipolar (±5V to ±22V) power supplies.

These devices are essentially fault-protected switches that are always on when power is applied. On-resistance is 100Ω max, and leakage is less than 1nA at +25°C.

When signal voltages exceed or are within 1.5V of the power-supply voltages, or when power is off, the two-terminal resistance increases dramatically, becoming a virtual open circuit. This ensures low current during fault conditions. The protected side of the switch maintains the correct polarity and clamps approximately 1.5V below the supply rail. There are no "glitches" or polarity reversals going into or coming out of a fault condition. ESD protection is greater than 2kV.

Applications

Data-Acquisition Systems
Process Control Systems
Digital Data Lines
ATE Equipment
Redundant/Backup Systems

Features

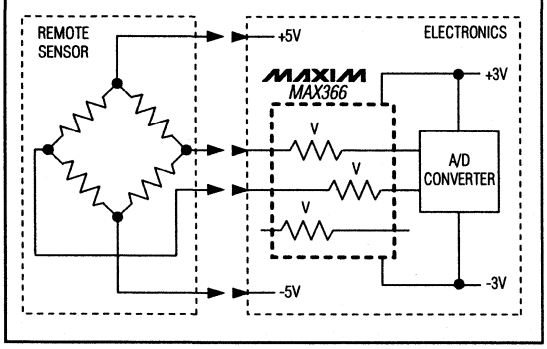
- ♦ **±35V Overvoltage Protection**
- ♦ **All Switches Off with Power Off**
- ♦ **100Ω Max On-Resistance**
- ♦ **1nA Max On-Leakage at +25°C**
- ♦ **ESD Protection Greater than 2kV per Method 3015.7**
- ♦ **44V Maximum Supply Voltage Rating**

Ordering Information

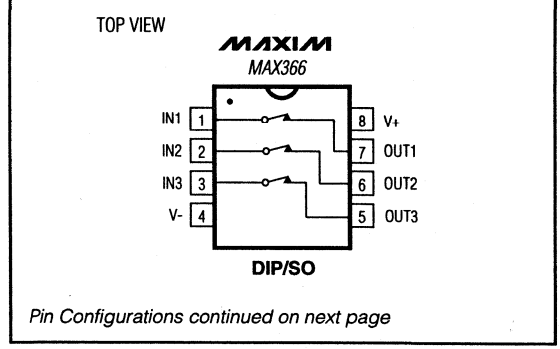
PART	TEMP. RANGE	PIN-PACKAGE
MAX366CPA	0°C to +70°C	8 Plastic DIP
MAX366CSA	0°C to +70°C	8 SO
MAX366C/D	0°C to +70°C	Dice*
MAX366EPA	-40°C to +85°C	8 Plastic DIP
MAX366ESA	-40°C to +85°C	8 SO
MAX366MJA	-55°C to +125°C	8 CERDIP**
MAX367CPN	0°C to +70°C	18 Plastic DIP
MAX367CWN	0°C to +70°C	18 Wide SO
MAX367C/D	0°C to +70°C	Dice*
MAX367EPN	-40°C to +85°C	18 Plastic DIP
MAX367EWN	-40°C to +85°C	18 Wide SO
MAX367MJN	-55°C to +125°C	18 CERDIP**

** Dice are tested at +25°C only.*
***Contact factory for availability*

Typical Operating Circuit



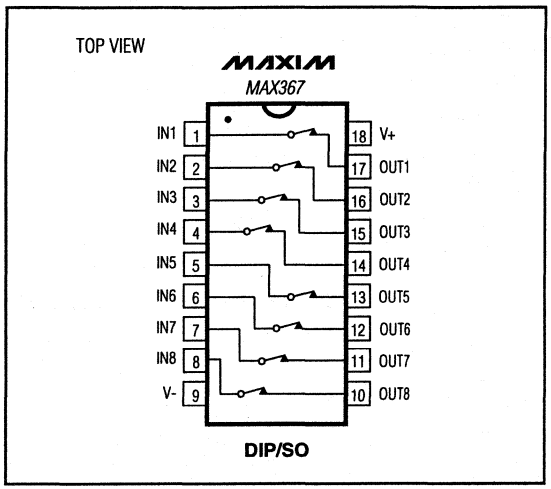
Pin Configurations



Pin Configurations continued on next page

Signal Line Circuit Protectors

Pin Configurations (continued)



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Precision, Low Voltage Analog Switches

General Description

The MAX381/MAX383/MAX385 are precision, dual, high-speed analog switches. The single-pole single-throw MAX381 and double-pole single-throw MAX385 dual switches are normally open. The single-pole double-throw MAX383 has two normally open and two normally closed poles. All three parts offer low on-resistance (less than 35Ω), guaranteed to match to within 2Ω between channels and to remain flat over the full analog signal range (Δ3Ω max). They also offer low leakage (less than 250pA at +25°C and less than 2.5nA at +85°C) and fast switching (turn-on time less than 150ns and turn-off time less than 100ns).

The MAX381/MAX383/MAX385 are fabricated with Maxim's low-voltage silicon-gate process for high system accuracy. Design improvements guarantee extremely low charge injection (10pC) and low power consumption (10μW).

These monolithic switches operate with a single positive supply (+3V to +15V) or with split supplies (±3V to ±8V) while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits
Test Equipment
Heads-Up Displays
Audio Signal Routing
Guidance and Control Systems
Military Radios
Communication Systems
Battery-Operated Systems
PBX, PABX

Features

- ♦ **Low On-Resistance, <22Ω Typical (35Ω Max)**
- ♦ **Guaranteed Matched On-Resistance Between Channels, <2Ω**
- ♦ **Guaranteed Flat On-Resistance over Specified Analog Signal Range, 4Ω Max**
- ♦ **Guaranteed Charge Injection, <10pC**
- ♦ **Guaranteed Off-Channel Leakage, <2.5nA at +85°C**
- ♦ **Single-Supply Operation (+3V to +15V) Bipolar-Supply Operation (±3V to ±8V)**
- ♦ **TTL/CMOS-Logic Compatible**
- ♦ **Rail-to-Rail Analog Signal Handling Capability**

Ordering Information

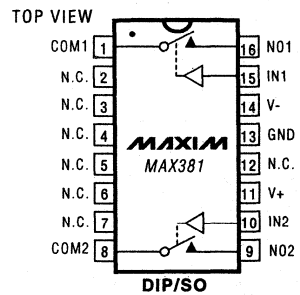
PART	TEMP. RANGE	PIN-PACKAGE
MAX381CPE	0°C to +70°C	16 Plastic DIP
MAX381CSE	0°C to +70°C	16 Narrow SO
MAX381C/D	0°C to +70°C	Dice*
MAX381EPE	-40°C to +85°C	16 Plastic DIP
MAX381ESE	-40°C to +85°C	16 Narrow SO
MAX381EJE	-40°C to +85°C	16 CERDIP**
MAX381MJE	-55°C to +125°C	16 CERDIP**
MAX381MLP	-55°C to +125°C	20 LCC**

Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C only.*

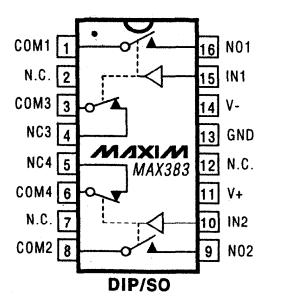
** *Contact factory for package availability.*

Pin Configurations/Block Diagrams/Truth Tables



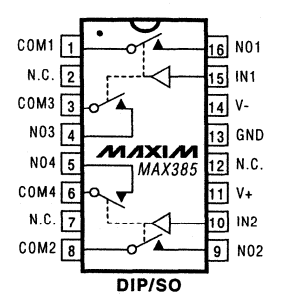
DIP/SO

MAX381	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

MAX383		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	OFF	ON
1	ON	OFF



DIP/SO

MAX385	
LOGIC	SWITCH
0	OFF
1	ON

LCC packages on last page.

SWITCHES SHOWN FOR LOGIC "0" INPUT

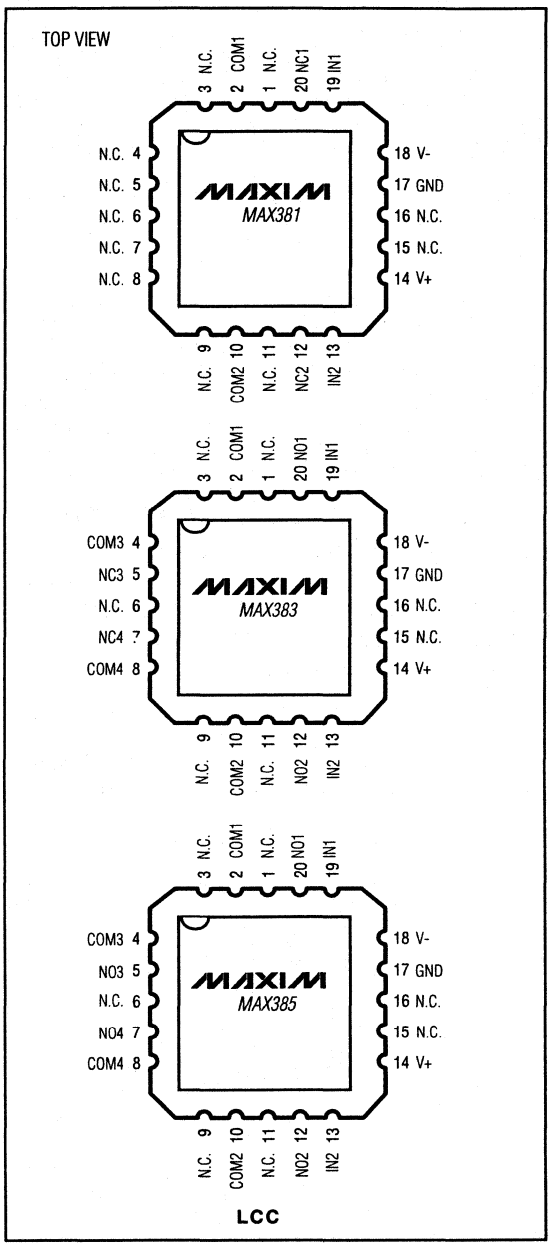
Precision, Low-Voltage Analog Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX383CPE	0°C to +70°C	16 Plastic DIP
MAX383CSE	0°C to +70°C	16 Narrow SO
MAX383C/D	0°C to +70°C	Dice*
MAX383EPE	-40°C to +85°C	16 Plastic DIP
MAX383ESE	-40°C to +85°C	16 Narrow SO
MAX383EJE	-40°C to +85°C	16 CERDIP**
MAX383MJE	-55°C to +125°C	16 CERDIP**
MAX383MLP	-55°C to +125°C	20 LCC**
MAX385CPE	0°C to +70°C	16 Plastic DIP
MAX385CSE	0°C to +70°C	16 Narrow SO
MAX385C/D	0°C to +70°C	Dice*
MAX385EPE	-40°C to +85°C	16 Plastic DIP
MAX385ESE	-40°C to +85°C	16 Narrow SO
MAX385EJE	-40°C to +85°C	16 CERDIP**
MAX385MJE	-55°C to +125°C	16 CERDIP**
MAX385MLP	-55°C to +125°C	20 LCC**

** Dice are tested at T_A = +25°C only.*
*** Contact factory for package availability.*

Pin Configurations (continued)



19-0236; Rev 0; 3/94

MAXIM

Precision, Quad, SPST Analog Switches

General Description

The MAX391/MAX392/MAX393 are precision, quad, single-pole/single-throw (SPST) analog switches designed to operate at +3V, +5V, or ±5V. The MAX391 has four normally closed (NC) switches, and the MAX392 has four normally open (NO) switches. The MAX393 has two NO and two NC switches. All three devices offer low leakage (100pA max) and fast switching speeds ($t_{ON} \leq 130ns$, $t_{OFF} \leq 75ns$). Power consumption is just 1µW—ideal for battery-operated equipment. All devices operate from a single +3V to +15V supply or from dual ±3.0V to ±8V supplies.

With ±5V supplies, the MAX391/MAX392/MAX393 offer guaranteed 2Ω max channel-to-channel matching, 30Ω max on-resistance (R_{ON}), and 4Ω max R_{ON} flatness over the specified range.

These switches are also fully specified for single +5V operation, with 2Ω max R_{ON} match, 60Ω max R_{ON}, and 6Ω max flatness.

These low-voltage switches also offer 5pC max charge injection, and ESD protection is greater than 2000V, per method 3015.7.

Applications

Battery-Operated Systems	Sample-and-Hold Circuits
Heads-Up Displays	Guidance and Control Systems
Audio and Video Switching	Military Radios
Test Equipment	Communications Systems
±5V DACs and ADCs	PBX, PABX

Features

- ♦ **Low On-Resistance, 20Ω Typical**
- ♦ **Guaranteed On-Resistance Match Between Channels, <2Ω**
- ♦ **Guaranteed On-Resistance Flatness Over Signal Range, 4Ω Max**
- ♦ **Guaranteed Charge Injection, <5pC**
- ♦ **Improved Leakage Over Temperature, <2.5nA at +85°C**
- ♦ **Electrostatic Discharge >2000V per Method 3015.7**
- ♦ **Single-Supply Operation (+3V to +15V) Bipolar-Supply Operation (±3V to ±8V)**
- ♦ **Low Power Consumption, <1µW**
- ♦ **TTL/CMOS-Logic Compatible**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX391CPE	0°C to +70°C	16 Plastic DIP
MAX391CSE	0°C to +70°C	16 Narrow SO
MAX391C/D	0°C to +70°C	Dice*
MAX391EPE	-40°C to +85°C	16 Plastic DIP
MAX391ESE	-40°C to +85°C	16 Narrow SO
MAX391EJE	-40°C to +85°C	16 CERDIP
MAX391MJE	-55°C to +125°C	16 CERDIP**

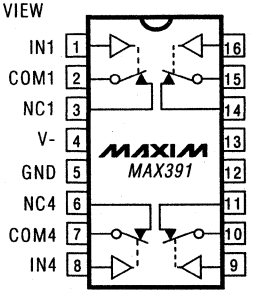
Ordering Information continued on last page.

** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations/Functional Diagrams/Truth Tables

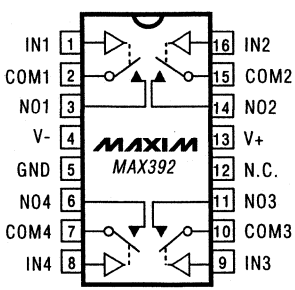
TOP VIEW



DIP/SO

MAX391	
LOGIC	SWITCH
0	ON
1	OFF

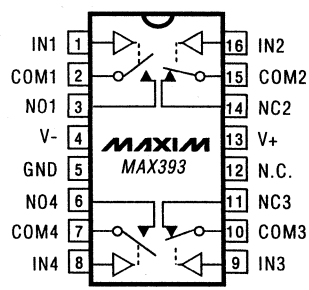
N.C. = NO CONNECT



DIP/SO

MAX392	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



DIP/SO

MAX393		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

Precision, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... -0.3V to +17V
GND ..... -0.3V to +17V
GND ..... -0.3V to (V+ + 0.3V)
V_{IN}, V_{COM}, V_{NC}, V_{NO} (Note 1) ..... V- to V+
Current (any terminal) 30mA
Peak Current, COM, NO, NC
(pulsed at 1ms, 10% duty cycle max) 100mA
ESD per Method 3015.7 ..... >2000V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above+70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX39_C_ _ ..... 0°C to +70°C
MAX39_E_ _ ..... -40°C to +85°C
MAX39_M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)			V-		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, I_{COM} = -10mA, V_{NO} or V_{NC} = ±3.5V	T_A = +25°C	C, E		20	35	Ω
				M		20	30	
			T_A = T_{MIN} to T_{MAX}				45	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, V- = -5V, I_{COM} = -10mA, V_{NO} or V_{NC} = ±3V	T_A = +25°C			0.3	2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V, V- = -5V, I_{COM} = -10mA, V_{NO} or V_{NC} = ±3V	T_A = +25°C			1	4	Ω
			T_A = T_{MIN} to T_{MAX}				6	
NO or NC Off Leakage Current (Note 6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	T_A = +25°C		-0.1	0.01	0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
				M	-5		5	
COM Off Leakage Current (Note 6)	$I_{COM(OFF)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ∓4.5V	T_A = +25°C		-0.1	0.01	0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
				M	-5		5	
COM On Leakage Current (Note 6)	$I_{COM(ON)}$	V+ = 5.5V, V- = -5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	T_A = +25°C		-0.2	0.01	0.2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5.0		5.0	
				M	-20		20	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Input Current with Input Voltage High	I_{INH}	IN = 2.4V, all others = 0.8V		-0.5	0.005	0.5	µA
Input Current with Input Voltage Low	I_{INL}	IN = 0.8V, all others = 2.4V		-0.5	0.005	0.5	µA
DYNAMIC							
Turn-On Time	t_{ON}	V_{COM} = ±3V, Figure 2	T_A = +25°C		65	130	ns
			T_A = T_{MIN} to T_{MAX}			175	
Turn-Off Time	t_{OFF}	V_{COM} = ±3V, Figure 2	T_A = +25°C		35	75	ns
			T_A = T_{MIN} to T_{MAX}			100	
Break-Before-Make Time Delay (Note 3)	t_D	MAX393 only, R_L = 300Ω, C_L = 35pF, Figure 3		5	10		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C		2	5	pC
Off Isolation (Note 7)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		72		dB
Crosstalk (Note 8)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		85		dB
NC or NO Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		22		pF
SUPPLY							
Power-Supply Range				-8.0		+8.0	V
Positive Supply Current	I+	V+ = 5.5V, V- = -5.5V, V_{IN} = 0V or V+, All channels on or off	T_A = T_{MIN} to T_{MAX}	-1		1	µA
Negative Supply Current	I-	V+ = 5.5V, V- = -5.5V, V_{IN} = 0V or V+, All channels on or off	T_A = T_{MIN} to T_{MAX}	-1		1	µA

Precision, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, I_{COM} = -10mA, V_{NO} or V_{NC} = 3.5V	T_A = +25°C			30	60	Ω
			T_A = T_{MIN} to T_{MAX}				75	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, I_{COM} = -1.0mA, V_{NO} or V_{NC} = 3V	T_A = +25°C			0.8	2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
On-Resistance Flatness (Notes 3, 5)	$R_{FLAT(ON)}$	V+ = 5V, I_{COM} = -1.0mA, V_{NO} or V_{NC} = 1V, 3V	T_A = +25°C			2	6	Ω
			T_A = T_{MIN} to T_{MAX}				8	
NO or NC Off Leakage Current (Note 9)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-0.25	0.01	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-0.1		0.1	
				M	-2.5		2.5	
COM Off Leakage Current (Note 9)	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = 0V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-0.1		0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-2.5		2.5	
				M	-5.0		5.0	
COM On Leakage Current (Note 9)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 5V, V_{NO} or V_{NC} = 4.5V	T_A = +25°C		-0.2		0.2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5.0		5.0	
				M	-20		20	
DYNAMIC								
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3V	T_A = +25°C			85	170	ns
			T_A = T_{MIN} to T_{MAX}				240	
Turn-Off Time	t_{OFF}	V_{NO} or V_{NC} = 3V	T_A = +25°C			25	50	ns
			T_A = T_{MIN} to T_{MAX}				100	
Break-Before-Make Time Delay (Note 3)	t_D	MAX393 only, R_L = 300Ω, C_L = 35pF			10			ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 4	T_A = +25°C			1	5	pC
SUPPLY								
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off			-1		1	µA
Negative Supply Current	I-	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off			-1		1	µA

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = +3.0V to +3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)		0		V+	V
Channel On-Resistance	R_{ON}	V+ = 3V, I_{COM} = -1.0mA, V_{NO} or V_{NC} = 1.5V	T_A = +25°C		83	175	Ω
			T_A = T_{MIN} to T_{MAX}			275	
DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	V_{NO} or V_{NC} = 1.5V	T_A = +25°C		160	400	ns
			T_A = T_{MIN} to T_{MAX}			500	
Turn-Off Time (Note 3)	t_{OFF}	V_{NO} or V_{NC} = 1.5V	T_A = +25°C		40	125	ns
			T_A = T_{MIN} to T_{MAX}			175	
Break-Before-Make Time Delay (Note 3)	t_D	MAX393 only, R_L = 300Ω, C_L = 35pF	T_A = +25°C	20			ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V	T_A = +25°C		1	5	pC
SUPPLY							
Positive Supply Current	I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off		-1		1	µA
Negative Supply Current	I-	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off		-1		1	µA

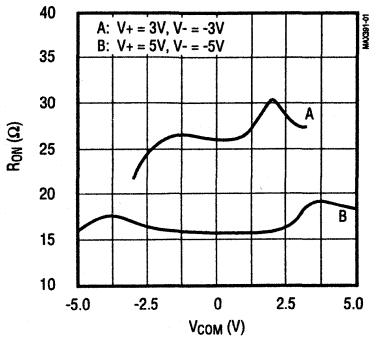
Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: ΔR_{ON} = ΔR_{ON} max - ΔR_{ON} min.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off Isolation = 20 $\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between any two switches.
Note 9: Leakage testing at single supply is guaranteed by testing with dual singles.

Precision, Quad, SPST Analog Switches

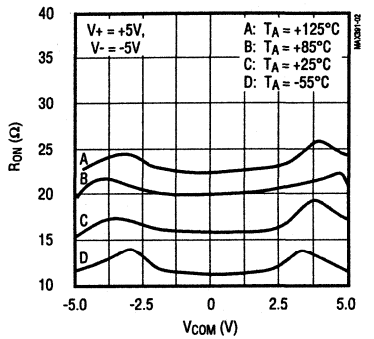
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

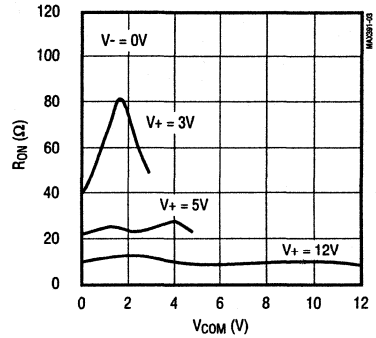
RON vs. VCOM (DUAL SUPPLIES)



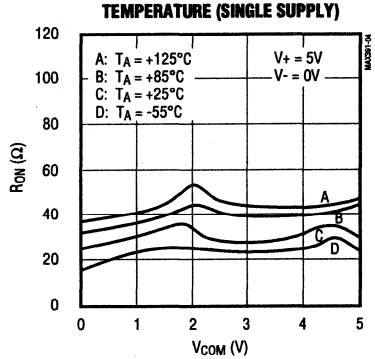
RON vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



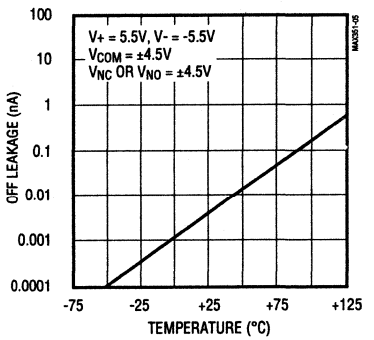
RON vs. VCOM (SINGLE SUPPLY)



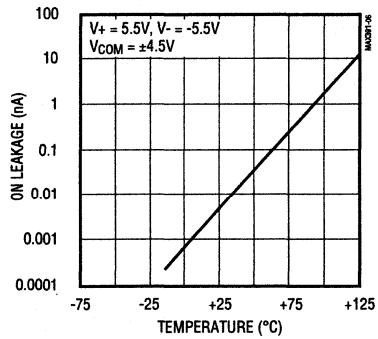
RON vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



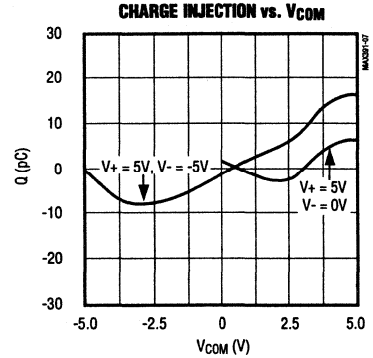
OFF LEAKAGE CURRENT vs. TEMPERATURE



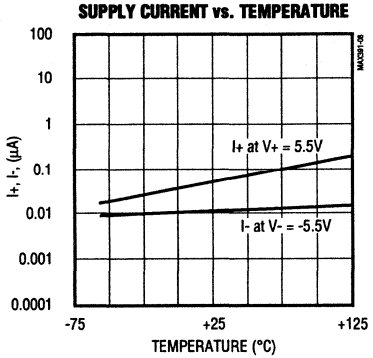
ON LEAKAGE CURRENT vs. TEMPERATURE



CHARGE INJECTION vs. VCOM



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 16, 9, 8	IN1–IN4	Inputs
2, 15, 10, 7	COM1–COM4	Analog Switch Common Terminal
3, 14, 11, 6	NO1–NO4 or NC1–NC4	Switch Inputs
4	V-	Negative Supply-Voltage Input
5	GND	Ground
12	N.C.	No Connect–not internally connected
13	V+	Positive Supply-Voltage Input—connected to substrate

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V-, and then logic inputs. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed 17V.

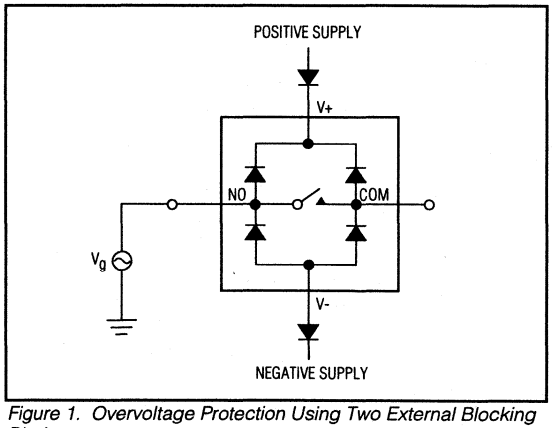


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Precision, Quad, SPST Analog Switches

Test Circuits/Timing Diagrams

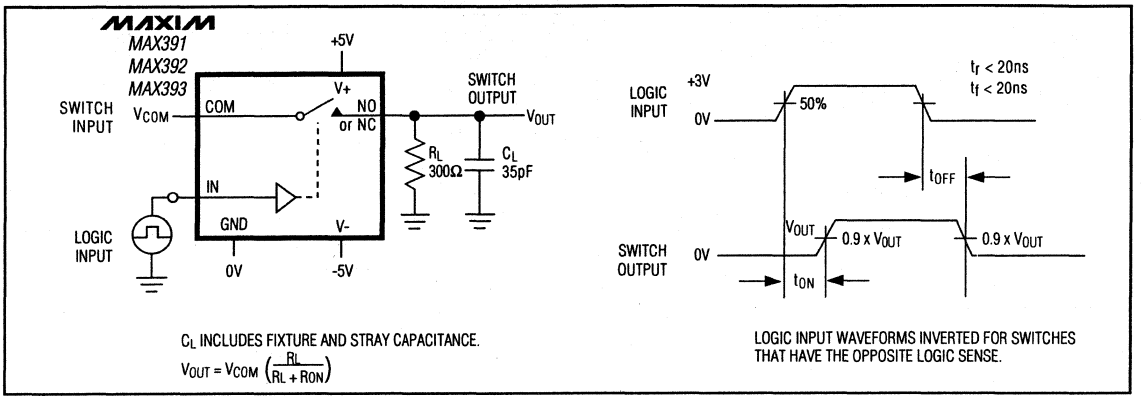


Figure 2. Switching Time

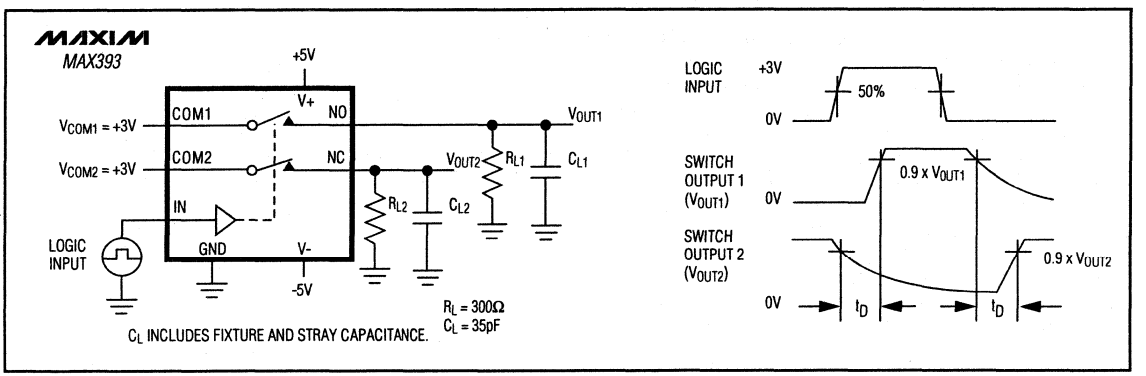


Figure 3. Break-Before-Make Interval (MAX393 only)

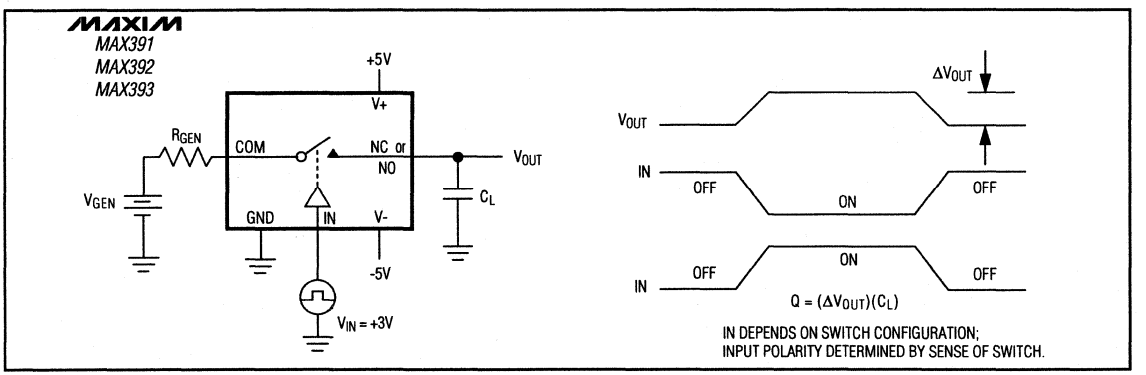


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

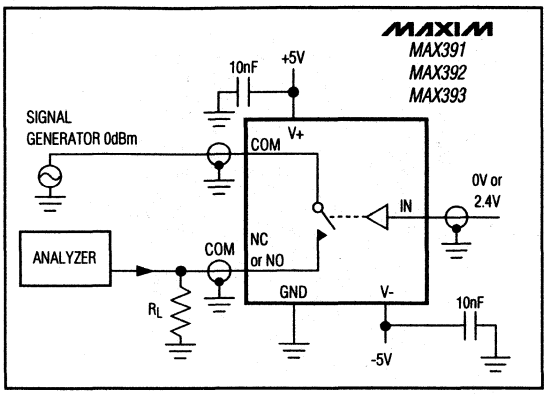


Figure 5. Off Isolation

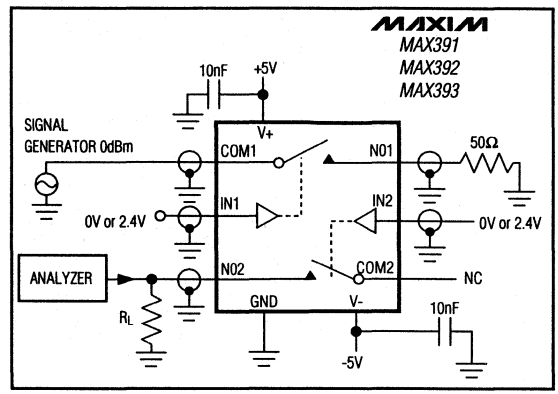


Figure 6. Crosstalk

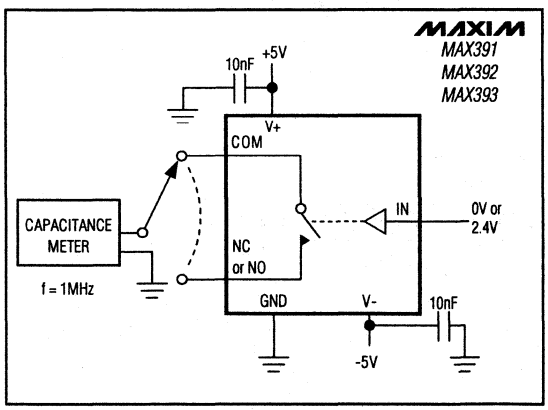


Figure 7. Channel-Off Capacitance

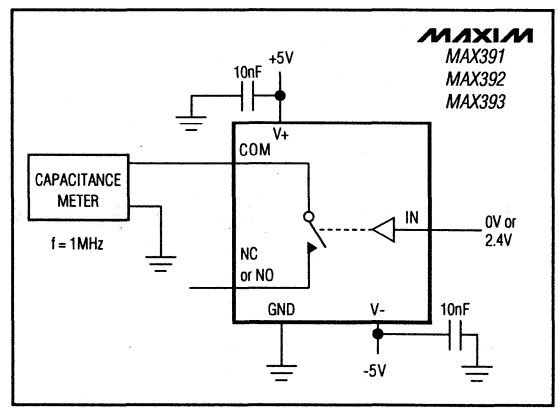


Figure 8. Channel-On Capacitance

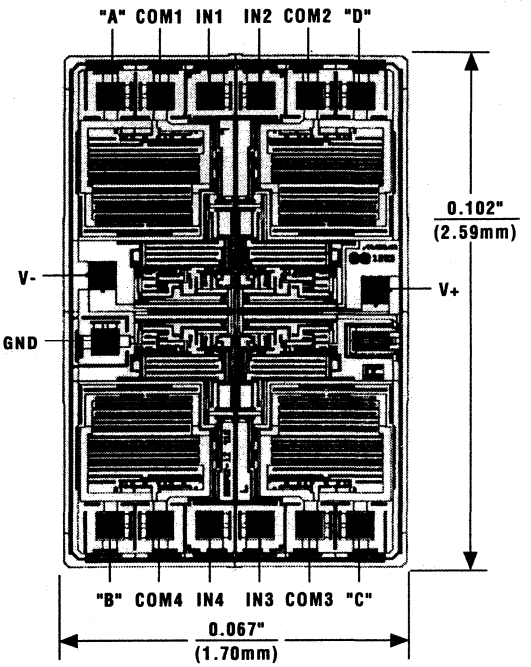
Precision, Quad, SPST Analog Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX392CPE	0°C to +70°C	16 Plastic DIP
MAX392CSE	0°C to +70°C	16 Narrow SO
MAX392C/D	0°C to +70°C	Dice*
MAX392EPE	-40°C to +85°C	16 Plastic DIP
MAX392ESE	-40°C to +85°C	16 Narrow SO
MAX392EJE	-40°C to +85°C	16 CERDIP
MAX392MJE	-55°C to +125°C	16 CERDIP**
MAX393CPE	0°C to +70°C	16 Plastic DIP
MAX393CSE	0°C to +70°C	16 Narrow SO
MAX393C/D	0°C to +70°C	Dice*
MAX393EPE	-40°C to +85°C	16 Plastic DIP
MAX393ESE	-40°C to +85°C	16 Narrow SO
MAX393EJE	-40°C to +85°C	16 CERDIP
MAX393MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883B.*

Chip Topography



MAX391		MAX392		MAX393	
PIN	NAME	PIN	NAME	PIN	NAME
A	NC1	A	NO1	A	NO1
B	NC4	B	NO4	B	NO4
C	NC3	C	NO3	C	NC3
D	NC2	D	NO2	D	NC2

TRANSISTOR COUNT: 76
SUBSTRATE CONNECTED TO V+

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

General Description

The MAX398/MAX399 precision, monolithic, CMOS analog multiplexers (muxes) offer low on-resistance (less than 100Ω), which is matched to within 5Ω between channels and remains flat over the specified analog signal range (7Ω max). They also offer low leakage over temperature (NO-off leakage current less than 2.5nA at +85°C) and fast switching speeds (transition time less than 250ns). The MAX398 is a single-ended 1-of-8 device, and the MAX399 is a differential 2-of-4 device.

The MAX398/MAX399 are fabricated with Maxim's low-voltage silicon-gate process. Design improvements yield extremely low charge injection (less than 10pC) and guarantee electrostatic discharge protection greater than 2000V.

These muxes operate with a single +3V to +15V supply or bipolar ±3V to ±8V supplies, while retaining CMOS-logic input compatibility and fast switching. CMOS inputs provide reduced input loading. The MAX398/MAX399 are pin compatible with the industry-standard DG408, DG409, DG508A, and DG509A.

Applications

Sample-and-Hold Circuits
Automatic Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing
Low-Voltage Data Acquisition Systems

Features

- **Pin Compatible with Industry-Standard DG408/DG409/DG508A/DG509A**
- **Guaranteed On-Resistance Match Between Channels (<5Ω max)**
- **Low On-Resistance (<100Ω max)**
- **Guaranteed Flat On-Resistance over Signal Range (7Ω max)**
- **Guaranteed Low Charge Injection (<10pC)**
- **NO-Off Leakage Current <2.5nA at +85°C**
- **COM-Off Leakage Current <5nA at +85°C**
- **Electrostatic Discharge Protection >2000V**
- **Single-Supply Operation (+3V to +15V) Bipolar-Supply Operation (±3V to ±8V)**
- **Low Power Consumption (<300µW)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Ordering Information

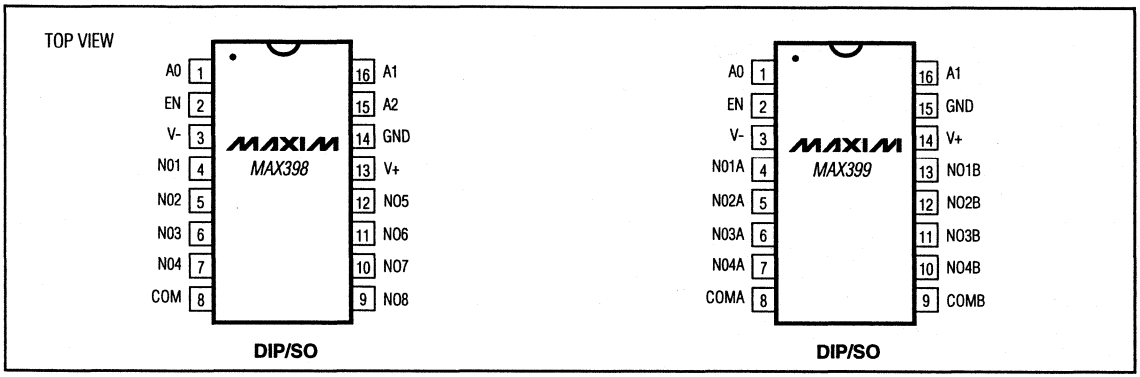
PART	TEMP. RANGE	PIN-PACKAGE
MAX398CPE	0°C to +70°C	16 Plastic DIP
MAX398CSE	0°C to +70°C	16 Narrow SO
MAX398C/D	0°C to +70°C	Dice*
MAX398EPE	-40°C to +85°C	16 Plastic DIP
MAX398ESE	-40°C to +85°C	16 Narrow SO
MAX398EJE	-40°C to +85°C	16 CERDIP**
MAX398MJE	-55°C to +125°C	16 CERDIP**

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for package availability.*

Pin Configurations

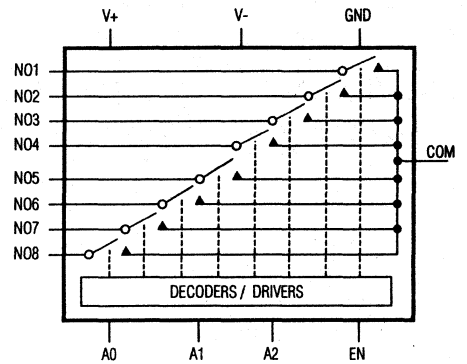


Precision, 8-Channel/Dual 4-Channel, Low-Voltage, CMOS Analog Multiplexers

Functional Diagrams

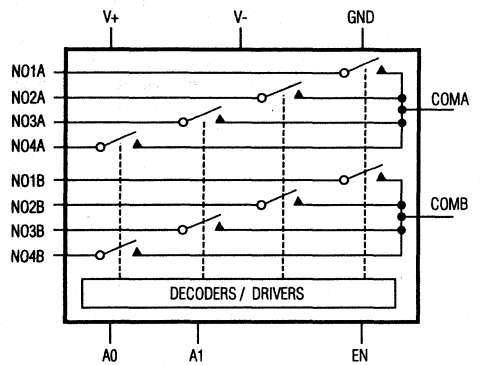
MAXIM

MAX398



MAXIM

MAX399



A0	A1	A2	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A0	A1	A2	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LOGIC "0" $V_{AL} \leq +0.8$ V, LOGIC "1" $V_{AH} \geq +2.4$ V

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX399CPE	0°C to +70°C	16 Plastic DIP
MAX399CSE	0°C to +70°C	16 Narrow SO
MAX399C/D	0°C to +70°C	Dice*
MAX399EPE	-40°C to +85°C	16 Plastic DIP
MAX399ESE	-40°C to +85°C	16 Narrow SO
MAX399EJE	-40°C to +85°C	16 CERDIP**
MAX399MJE	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications .*

*** Contact factory for package availability.*

19-4727; Rev 1; 3/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Improved, Dual, High-Speed Analog Switches

General Description

Maxim's redesigned DG401/DG403/DG405 analog switches now feature guaranteed low on-resistance matching between switches (2Ω max) and guaranteed on-resistance flatness over the signal range (3Ω max). These low on-resistance switches (20Ω typ) conduct equally well in either direction and are guaranteed to have low charge injection (15pC max). The new design offers lower off leakage current over temperature (less than 5nA at +85°C).

The DG401/DG403/DG405 are dual, high-speed switches. The single-pole/single-throw DG401 and double-pole/single-throw DG405 are normally open dual switches. The dual, single-pole/double-throw DG403 has two normally open and two normally closed switches. Switching times are 150ns max for t_{ON} and 100ns max for t_{OFF}, with a maximum power consumption of 35µW. These devices operate from a single +10V to +30V supply, or bipolar supplies of ±4.5V to ±20V. Maxim's improved DG401/DG403/DG405 are fabricated with a 44V silicon-gate process.

New Features

- **Plug-In Upgrade for Industry-Standard DG401/DG403/DG405**
- **Improved $r_{DS(ON)}$ Match Between Channels (2Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (3Ω max)**
- **Improved Charge Injection (15pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**

Existing Features

- **Low $r_{DS(ON)}$ (30Ω max)**
- **Single-Supply Operation +10V to +30V**
  Bipolar-Supply Operation ±4.5V to ±20V
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling Capability**
- **TTL/CMOS-Logic Compatible**

Applications

Sample-and-Hold Circuits	Test Equipment
Guidance and Control Systems	Heads-Up Displays
Communications Systems	PBX, PABX
Battery-Operated Systems	Audio Signal Routing
Military Radios	

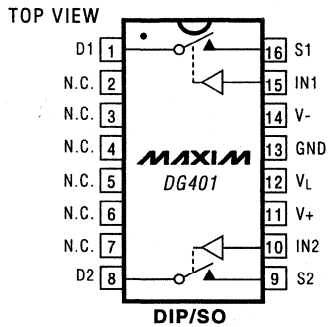
Ordering Information

PART	TEMP. RANGE	PIN PACKAGE
DG401CJ	0°C to +70°C	16 Plastic DIP
DG401CY	0°C to +70°C	16 Narrow SO
DG401C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

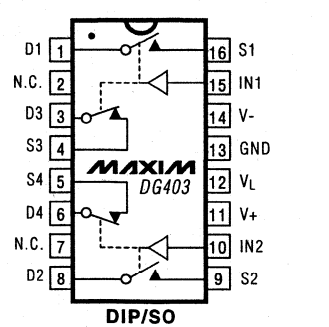
**Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams/Truth Tables



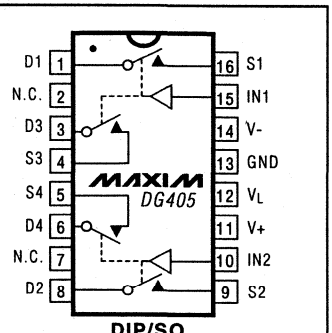
DIP/SO

DG401	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG403		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	OFF	ON
1	ON	OFF



DIP/SO

DG405	
LOGIC	SWITCH
0	OFF
1	ON

LCC packages on last page.

SWITCHES SHOWN FOR LOGIC "0" INPUT

N.C. = NOT INTERNALLY CONNECTED

Improved, Dual, High-Speed Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
- V+ 44V
- GND 25V
- V_L ..... (GND - 0.3V) to (V+ + 0.3V)

Digital Inputs, V_S, V_D (Note 1) ..... (V- - 2V) to (V+ + 2V) or 20mA (whichever occurs first)

Continuous Current (any terminal) 30mA

Continuous Current, S or D 20mA

Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
- 16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
- 16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ... 696mW
- 16-Pin CERDIP (derate 10.00mW/°C above 70°C) 800mW
- 20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges
- DG40_C_ ..... 0°C to +70°C
- DG40_D_ ..... -40°C to +85°C
- DG40_A_ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP. RANGE	MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			-15		+15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = ±10V, V_{INH} = 2.4V, V_{INL} = 0.8V	T_A = +25°C	C,D		20	45	V
				A		20	30	
			T_A = T_{MIN} to T_{MAX}	C,D			55	
				A			45	
Drain-Source On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, I_S = -10mA, V_D = ±10V	T_A = +25°C	C, D, A		0.5	2	Ω
			T_A = T_{MIN} to T_{MAX}				3	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, I_S = -10mA, V_D = ±5V, 0V	T_A = +25°C	C, D, A			3	Ω
			T_A = T_{MIN} to T_{MAX}				6	
Source-Off Leakage Current (Note 7)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ∓15.5V, V_S = ±15.5V,	T_A = +25°C	C, D	-0.50	-0.01	0.50	nA
				A	-0.25	-0.01	0.25	
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-Off Leakage Current (Note 7)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D	-0.50	-0.01	0.50	nA
				A	-0.25	-0.01	0.25	
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-On Leakage Current (Note 7)	$I_{D(ON)}$ or $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C	C, D	-1.0	-0.04	1.0	nA
				A	-0.4	-0.04	0.4	
			T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
				A	-20		20	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		-1.0	0.005	1.0	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-1.0	0.005	1.0	µA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2	T_A = +25°C		100	150	ns
Turn-Off Time	t_{OFF}	Figure 2	T_A = +25°C		60	100	ns
Break-Before-Make Delay (Note 3)	t_D	DG403 only, Figure 3	T_A = +25°C	10	20		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C		10	15	pC
Off Isolation (Note 5)	OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		72		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		90		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		12		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		12		pF
Channel-On Capacitance	$C_{D(ON)}$ or $C_{S(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		39		pF

Note 2: This data sheet uses the algebraic convention, where the most negative value is a minimum and the most positive value is a maximum.

Note 3: Guaranteed by design.

Note 4: $\Delta r_{ON} = \Delta r_{ON}(max) - \Delta r_{ON}(min)$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Off isolation = 20log (V_S/V_D), V_D = output, V_S = input to off switch.

Note 6: Between any two switches.

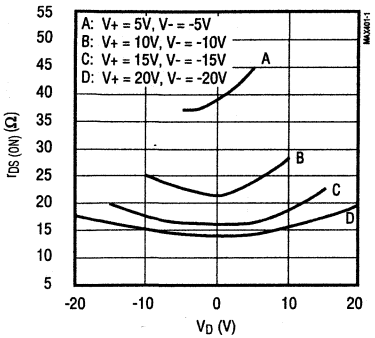
Note 7: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

Improved, Dual, High-Speed Analog Switches

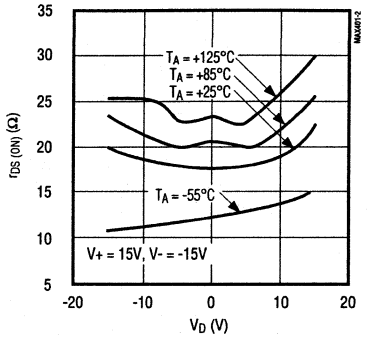
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

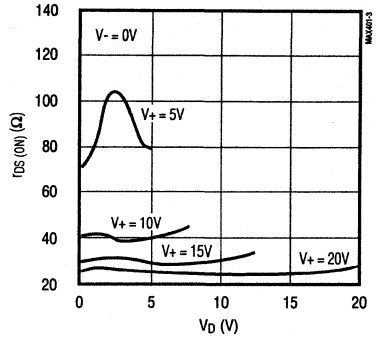
ON-RESISTANCE vs. V_D (DUAL SUPPLIES)



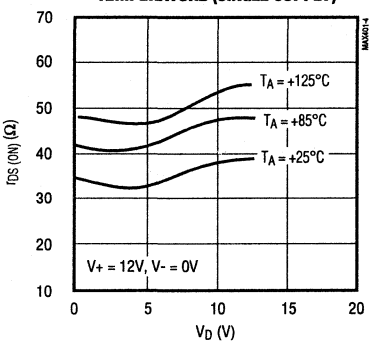
ON-RESISTANCE vs. V_D AND TEMPERATURE (DUAL SUPPLIES)



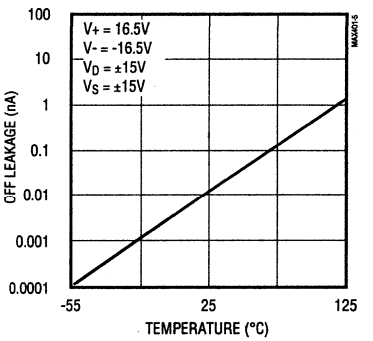
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



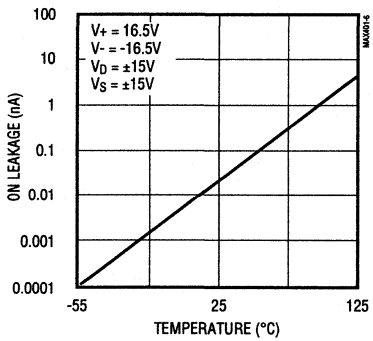
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



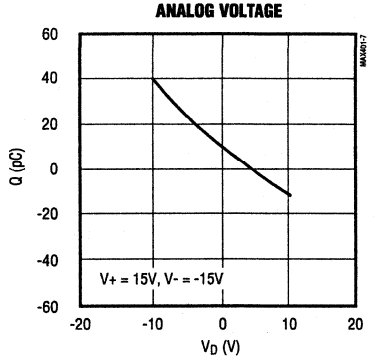
OFF LEAKAGE CURRENTS vs. TEMPERATURE



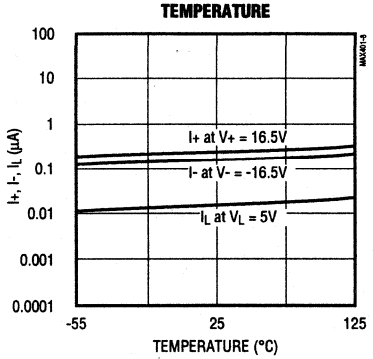
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



19-4729; Rev 1; 5/93

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

General Description

The DG406/DG407 are monolithic CMOS analog multiplexers (muxes). The DG406 is a single-ended 1-of-16 device, and the DG407 is a differential 2-of-8 device. Both are pin and functionally compatible with the industry-standard DG506A/DG507A.

The DG406/DG407 are fabricated with Maxim's new improved silicon gate process. Both parts offer low on resistance (100Ω max), improved leakage over temperature, low power consumption (I_{SUPPLY} = 75µA max) and fast switching speeds (t_{TRANS} = 250ns max). The 44V maximum breakdown voltage allows switch-off blocking capability rail-to-rail.

These muxes can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Features

- ◆ **$r_{DS(ON)}$: 100Ω Max, $\Delta r_{DS(ON)}$: 15Ω Max**
- ◆ **t_{TRANS}: 250ns Max**
- ◆ **Leakage - $T_A = T_{MIN}$ to T_{MAX}**
  $I_{S(OFF)}$: 50nA Max
  $I_{D(OFF)}$: 100nA Max (DG407), 200nA Max (DG406)
  $I_{-(ON)}$: 100nA Max (DG407), 200nA Max (DG406)
- ◆ **Q: 20pC Typ**
- ◆ **I_{SUPPLY}: 75µA Max**
- ◆ **Single- or Bipolar-Supply Operation**
- ◆ **TTL/CMOS Logic Compatible**

Ordering Information

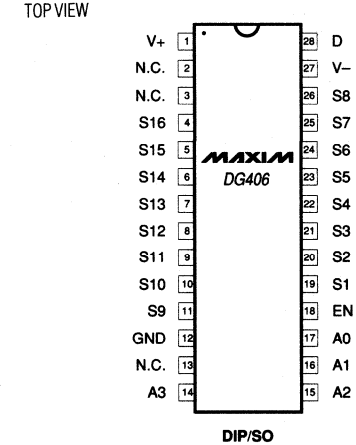
PART	TEMP. RANGE	PIN-PACKAGE
DG406CWI	0°C to +70°C	28 Wide SO
DG406C/D	0°C to +70°C	Dice*
DG406EWI	-40°C to +85°C	28 Wide SO
DG406DJ	-40°C to +85°C	28 Plastic DIP
DG406DN	-40°C to +85°C	28 PLCC
DG406DK	-40°C to +85°C	28 CERDIP
DG406AK	-55°C to +125°C	28 CERDIP**

Ordering Information continued on last page.

** Contact factory for dice specifications.*

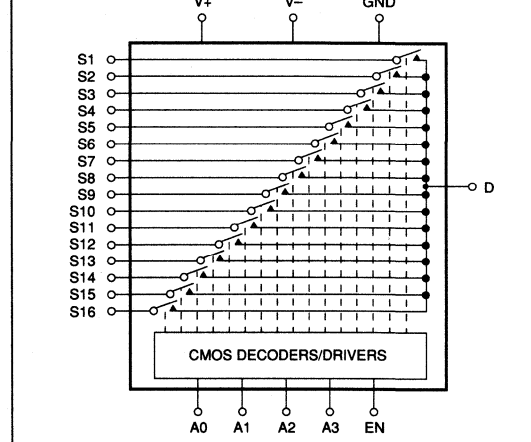
***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



DG407 on last page

Functional Diagrams



DG406 16-CHANNEL SINGLE-ENDED MULTIPLEXER

DG407 on last page

16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
Digital Inputs V_S, V_D ... (Note 1) (V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA

Continuous Power Dissipation (T_A = +25°C) (Note 2)
28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
28-Pin Wide SO (derate 12.5mW/°C above +70°C) ... 1000m
28-Pin PLCC (derate 10.53mW/°C above +70°C) 842mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C) . 1333mW
Operating Temperature Ranges:
DG406/407C_ _ ..... 0°C to +70°C
DG406/407D_ _/E_ _ ..... -40°C to +85°C
DG406/407AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.
Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 4)			-15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA, V_D = ±10V		T_A = +25°C		50	100	Ω
				T_A = T_{MIN} to T_{MAX}			125	
$r_{DS(ON)}$ Matching Between Channels	$\Delta r_{DS(ON)}$	V_D = ±10V (Note 5)		T_A = +25°C			15	Ω
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ±10V, V_S = ∓10V, V_{EN} = 0V		T_A = +25°C	-0.5		0.5	nA
				T_A = T_{MIN} to T_{MAX}	-50		50	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = ±10V, V_D = ∓10V, V_{EN} = 0V	DG406	T_A = +25°C	-2		2	nA
				T_A = T_{MIN} to T_{MAX}	-200		200	
			DG407	T_A = +25°C	-2		2	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±10V, V_S = ±10V, sequence each switch on	DG406	T_A = +25°C	-2		2	nA
				T_A = T_{MIN} to T_{MAX}	-200		200	
			DG407	T_A = +25°C	-2		2	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	

19-4725; Rev. 0; 12/91

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

General Description

The DG408 and DG409 are monolithic CMOS analog multiplexers (muxes). The DG408 is a single-ended 1-of-8 device, and the DG409 is a differential 2-of-4 device. Both devices are pin and functionally compatible with the industry standard DG508A/DG509A.

The DG408/DG409 are fabricated with Maxim's new improved silicon gate process. These muxes offer low on resistance (100Ω max), low leakage over temperature, low power consumption (I_{SUPPLY} = 75µA), and fast switching speeds (t_{TRANS} = 250ns max). The 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

The DG408/DG409 can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Features

- ◆ $r_{DS(ON)}$: 100Ω Max
- ◆ t_{TRANS}: 250ns Max
- ◆ $\Delta r_{DS(ON)}$: 15Ω Max
- ◆ Leakage - $T_A = T_{MIN}$ to T_{MAX}
  $I_{S(OFF)}$: 50nA Max
  $I_{D(OFF)}$: 100nA Max (DG409), 200nA Max (DG408)
  $I_{D(ON)}$: 100nA Max (DG409), 200nA Max (DG408)
- ◆ Q: 20pC Typ
- ◆ Single-Supply Operation (+12V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ◆ TTL/CMOS Logic Compatible
- ◆ Rail-to-Rail Switch-Off Blocking Capability

Ordering Information

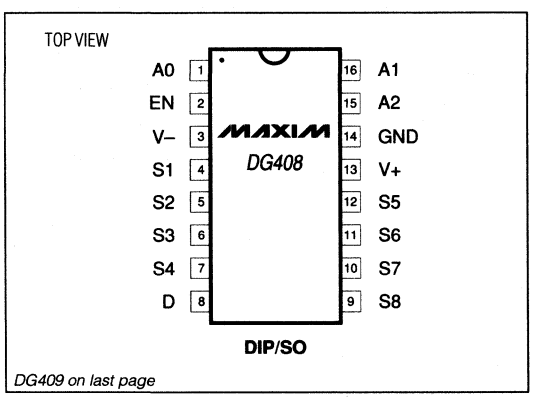
PART	TEMP. RANGE	PIN-PACKAGE
DG408C/D	0°C to +70°C	Dice*
DG408DJ	-40°C to +85°C	16 Plastic DIP
DG408DY	-40°C to +85°C	16 Narrow SO
DG408DK	-40°C to +85°C	16 CERDIP
DG408AK	-55°C to +125°C	16 CERDIP**
DG409C/D	0°C to +70°C	Dice*
DG409DJ	-40°C to +85°C	16 Plastic DIP
DG409DY	-40°C to +85°C	16 Narrow SO
DG409DK	-40°C to +85°C	16 CERDIP
DG409AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Applications

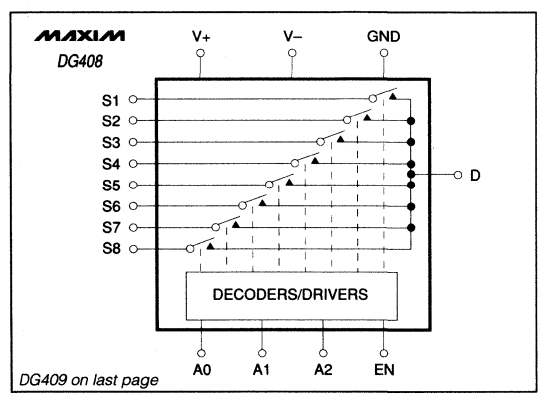
Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Pin Configurations



DG409 on last page

Functional Diagrams



DG409 on last page

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) ..... V- -2V to V+ +2V or 30mA (whichever occurs first)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(pulsed at 1 ms, 10% duty cycle max) 40mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP (derate 7.5 mW/°C above +70°C) .. 470mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) .. 696mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 900mW
Operating Temperature Ranges:
DG408/DG409C_ ..... 0°C to +70°C
DG408/DG409D_ ..... -40°C to +85°C
DG408/DG409AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 4)			-15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA, V_D = ±10V		T_A = +25°C		40	100	Ω
				T_A = T_{MIN} to T_{MAX}			125	
$r_{DS(ON)}$ Matching Between Channels	$\Delta r_{DS(ON)}$	V_D = ±10V (Note 5)		T_A = +25°C			15	Ω
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ∓10V, V_S = ±10V, V_{EN} = 0V		T_A = +25°C	-0.5		0.5	nA
				T_A = T_{MIN} to T_{MAX}	-50		50	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = ±10V, V_D = ∓10V, V_{EN} = 0V	DG408	T_A = +25°C	-1		1	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
		V_S = ∓10V, V_D = ±10V, V_{EN} = 0V	DG409	T_A = +25°C	-1		1	
				T_A = T_{MIN} to T_{MAX}	-50		50	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±10V, V_S = ±10V, sequence each switch on	DG408	T_A = +25°C	-1		1	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
			DG409	T_A = +25°C	-1		1	
				T_A = T_{MIN} to T_{MAX}	-50		50	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
INPUT								
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V, 15V			-10		10	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V, 2.4V V_A = 0V			-10		10	µA
SUPPLY								
Power-Supply Range					±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V					75	µA
Negative Supply Current	I-	V_{EN} = V_A = 0V				-75		µA
Positive Supply Current	I+	V_{EN} = 2.4V, V_A = 0V		T_A = +25°C			0.5	mA
				T_A = T_{MIN} to T_{MAX}			2	mA
Negative Supply Current	I-	V_{EN} = 2.4V, V_A = 0V			-500			µA
DYNAMIC								
Transition Time	t_{TRANS}	Figure 1					250	ns
Break-Before-Make Interval	t_{OPEN}	Figure 2		T_A = +25°C	10			ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		T_A = +25°C			150	ns
				T_A = T_{MIN} to T_{MAX}			225	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		T_A = +25°C			150	ns
Charge Injection	Q	C_L = 10nF, V_S = 0V, R_S = 0Ω		T_A = +25°C		20		pC
Off Isolation (Note 6)		V_{EN} = 0V, R_L = 1kΩ, f = 100kHz		T_A = +25°C		-75		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		8		pF
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, V_{EN} = V_S = 0V		T_A = +25°C		11		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, V_{EN} = V_D = 0V	DG408	T_A = +25°C		40		pF
			DG409			20		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, V_{EN} = V_D = 0V	DG408	T_A = +25°C		54		pF
			DG409			34		pF

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (Single Supply)

(V+ = 12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN TYP MAX (Note 3)	UNITS
SWITCH						
Analog Signal Range	V_{ANALOG}	(Note 3)			0 12	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -1mA, V_D = 3V, 10V		T_A = +25°C	90	Ω
DYNAMIC						
Transition Time	t_{TRANS}	Figure 1, V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V		T_A = +25°C	180	ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V		T_A = +25°C	180	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V		T_A = +25°C	120	ns
Charge Injection	Q	C_L = 10nF, V_S = 0V, R_S = 0Ω		T_A = +25°C	5	pC

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: Guaranteed by design.

Note 5: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}MAX - \Delta r_{DS(ON)}MIN$

Note 6: Worst-case isolation is on channel 4 because of its proximity to the drain pin. Off isolation = $20\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.

Pin Description

DG408 PIN	NAME	FUNCTION
1,16,15	A0, A1, A2	Address Inputs
2	EN	Enable Input
3	V-	Negative Supply Voltage Input
4-7, 12-9	S1-S8	Source Outputs
8	D	Drain Output
13	V+	Positive Supply Voltage Input
14	GND	Ground

DG409 PIN	NAME	FUNCTION
1,16	A0, A1	Address Inputs
2	EN	Enable Input
3	V-	Negative Supply Voltage Input
4-7	S1a-S4a	Source Outputs
8,9	Da, Db	Drain Outputs
13-10	S1b-S4b	Source Outputs
14	V+	Positive Supply Voltage Input
15	GND	Ground

19-4728; Rev 1; 3/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's redesigned DG411/DG412/DG413 analog switches now feature low on-resistance matching between switches (3Ω max) and guaranteed on-resistance flatness over the signal range (Δ4Ω max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off leakage current over temperature (less than 5nA at +85°C).

The DG411/DG412/DG413 are quad, single-pole/single-throw (SPST) analog switches. The DG411 is normally closed (NC), and the DG412 is normally open (NO). The DG413 has two NC switches and two NO switches. Switching times are less than 150ns max for t_{ON} and less than 100ns max for t_{OFF}. These devices operate from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG411/DG412/DG413 are fabricated with a 44V silicon-gate process.

New Features

- **Plug-In Upgrade for Industry-Standard DG411/DG412/DG413**
- **Improved $r_{DS(ON)}$ Match Between Channels (3Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (Δ4Ω)**
- **Improved Charge Injection (10pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (35Ω max)**
- **Single-Supply Operation +10V to +30V**
- **Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Applications

- Sample-and-Hold Circuits
- Test Equipment
- Heads-Up Displays
- Guidance & Control Systems
- Military Radios
- Communication Systems
- Battery-Operated Systems
- PBX, PABX
- Audio Signal Routing

Ordering Information

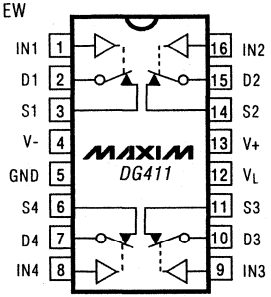
PART	TEMP. RANGE	PIN-PACKAGE
DG411CJ	0°C to +70°C	16 Plastic DIP
DG411CY	0°C to +70°C	16 Narrow SO
DG411C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

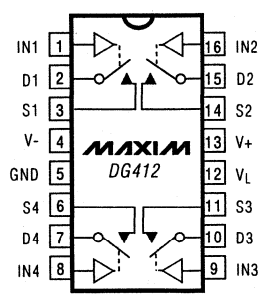
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

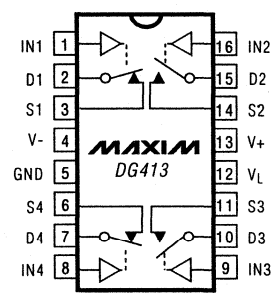
DG411	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG412	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT



DIP/SO

DG413		
LOGIC	SWITCHES 1, 2	SWITCHES 3, 4
0	ON	OFF
1	OFF	ON

Improved, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+ +0.3V)
Digital Inputs, V_S, V_D (Note 1) ..... (V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
DG41_C_ ..... 0°C to +70°C
DG41_D_ ..... -40°C to +85°C
DG41_AK_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, V_D = ±8.5V, I_S = -10mA	T_A = +25°C	C, D		17	45	Ω
				A		17	30	
			T_A = T_{MIN} to T_{MAX}				45	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, V_D = ±10V, I_S = -10mA	T_A = +25°C				3	Ω
			T_A = T_{MIN} to T_{MAX}				5	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, V_D = ±5V, 0V, I_S = -10mA	T_A = +25°C				4	Ω
			T_A = T_{MIN} to T_{MAX}				6	
Source-Off Leakage Current (Note 7)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D, A	-0.25	-0.10	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-Off Leakage Current (Note 7)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D, A	-0.25	-0.10	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-On Leakage Current (Note 7)	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D, A	-0.4	-0.1	0.4	nA
			T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
				A	-20		20	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	IN = 2.4V, all others = 0.8V		-0.500	0.005	0.500	µA
Input Current with Input Voltage Low	I_{INL}	IN = 0.8V, all others = 2.4V		-0.500	0.005	0.500	µA
SUPPLY							
Power-Supply Range				±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_D = ±10V, Figure 2	T_A = +25°C		110	175	ns
			T_A = T_{MIN} to T_{MAX}			220	
Turn-Off Time	t_{OFF}	V_D = ±10V, Figure 2	T_A = +25°C		100	145	ns
			T_A = T_{MIN} to T_{MAX}			160	
Break-Before-Make Time Delay	t_D	DG413 only, R_L = 300Ω, C_L = 35pF, Figure 3	T_A = +25°C		25		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C		5	10	pC
Off Isolation (Note 5)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		68		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		85		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
Drain-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		35		pF

Improved, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On Resistance	$r_{DS(ON)}$	V+ = 10.8V, V_D = 3.8V, I_S = -10mA	T_A = +25°C		40	80	Ω
			T_A = T_{MIN} to T_{MAX}			100	
SUPPLY							
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_S = 8V, Figure 2	T_A = +25°C		175	250	ns
			T_A = T_{MIN} to T_{MAX}			315	
Turn-Off Time	t_{OFF}	V_S = 8V, Figure 2	T_A = +25°C		95	125	ns
			T_A = T_{MIN} to T_{MAX}			140	
Break-Before-Make Time Delay	t_D	DG413 only, R_L = 300Ω, C_L = 35pF, Figure 3	T_A = +25°C		25		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 8	T_A = +25°C		5	10	pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: ΔR_{ON} = ΔR_{ON} max - ΔR_{ON} min. On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured at the extremes of the specified analog signal range.

Note 5: Off Isolation = 20 log (V_D/V_S), V_D = output, V_S = input to off switch. See Figure 5.

Note 6: Between any two switches. See Figure 6.

Note 7: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

19-0114; Rev 1; 3/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Improved, SPST/SPDT Analog Switches

General Description

Maxim's redesigned DG417/DG418/DG419 precision, CMOS, monolithic analog switches now feature guaranteed on-resistance matching (3Ω max) between switches and guaranteed on-resistance flatness over the signal range (4Ω max). These switches conduct equally well in either direction and guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers low off leakage current over temperature (less than 5nA at +85°C).

The DG417/DG418 are single-pole/single-throw (SPST) switches. The DG417 is normally closed, and the DG418 is normally open. The DG419 is single-pole/double-throw (SPDT) with one normally closed switch and one normally open switch. Switching times are less than 175ns max for t_{ON} and less than 145ns max for t_{OFF}. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. The improved DG417/DG418/DG419 are fabricated with a 44V silicon-gate process.

New Features

- **Plug-In Upgrades for Industry-Standard DG417/DG418/DG419**
- **Improved $r_{DS(ON)}$ Match Between Channels (3Ω max - DG419 only)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (4Ω max)**
- **Improved Charge Injection (10pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (35Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Applications

Sample-and-Hold Circuits	Communications Systems
Test Equipment	Battery-Operated Systems
Modems	Fax Machines
Guidance and Control Systems	PBX, PABX
Audio Signal Routing	Military Radios

Ordering Information

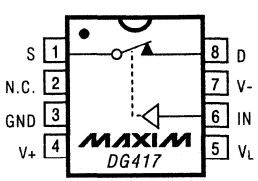
PART	TEMP. RANGE	PIN-PACKAGE
DG417CJ	0°C to +70°C	8 Plastic DIP
DG417CY	0°C to +70°C	8 SO
DG417C/D	0°C to +70°C	Dice*
DG417DJ	-40°C to +85°C	8 Plastic DIP
DG417DY	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

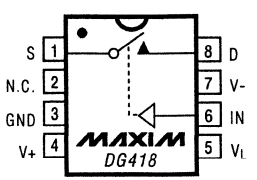
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



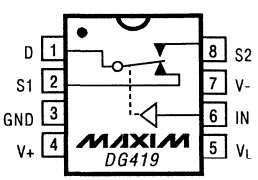
DIP/SO

DG417	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG418	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG419		
LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

N.C. = No Internal Connection

SWITCHES SHOWN FOR LOGIC "0" INPUT

Improved, SPST/SPDT Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+ +0.3V)
Digital Inputs V_S, V_D (Note 1) ..... (V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) (Note 1) 30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) .. 100mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C..) 640mW
Operating Temperature Ranges
DG41_C_ ..... 0°C to +70°C
DG41_D_ ..... -40°C to +85°C
DG41_AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{ANALOG}	(Note 3)				-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, V_D = ±10V, I_S = -10mA		T_A = +25°C	C, D		20	35	Ω
					A		20	30	
				T_A = T_{MIN} to T_{MAX}				45	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, V_D = ±10V, I_S = -10mA		T_A = +25°C				3	Ω
				T_A = T_{MIN} to T_{MAX}				4	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, V_D = ±5V, I_S = -10mA		T_A = +25°C				4	Ω
				T_A = T_{MIN} to T_{MAX}				6	
Source-Off Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V		T_A = +25°C		-0.25		0.25	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
					A	-10		10	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	DG417 DG418	T_A = +25°C		-0.25	0.1	0.25	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
					A	-10		10	
			DG419	T_A = +25°C		-0.75	-0.1	0.75	
				T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
					A	-20		20	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	DG417 DG418	T_A = +25°C		-0.4		0.4	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
					A	-20		20	
			DG419	T_A = +25°C		-0.75		0.75	
				T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
					A	-20		20	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Logic Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V		-0.5	0.005	0.5	µA
Logic Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V		-0.5	0.005	0.5	µA
DYNAMIC							
Turn-On Time	t_{ON}	DG417, DG418, V_D = ±10V, Figure 2	T_A = +25°C		100	175	ns
			T_A = T_{MIN} to T_{MAX}			250	
Turn-Off Time	t_{OFF}	DG417, DG418, V_D = ±10V, Figure 2	T_A = +25°C		60	145	ns
			T_A = T_{MIN} to T_{MAX}			210	
Transition Time	t_{TRANS}	DG419, V_S = ±10V, Figure 3	T_A = +25°C			175	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_D	DG419, V_{S1} = V_{S2} = ±10V, Figure 4	T_A = +25°C	5	13		ns
Charge Injection (Note 3)	Q	V_{GEN} = 0V, Figure 5	T_A = +25°C		3	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		68		dB
Crosstalk (Note 7)		DG419, R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 7	T_A = +25°C		85		dB
Drain-Off Capacitance	$C_{D(OFF)}$	V_D = 0V, f = 1MHz, Figure 8	T_A = +25°C		8		pF
Source-Off Capacitance	$C_{S(OFF)}$	V_D = 0V, f = 1MHz, Figure 8	T_A = +25°C		8		pF
Drain/Source-On Capacitance	$C_{D(ON)}$ or $C_{S(ON)}$	V_S = 0V, f = 1MHz, Figure 9	DG417 DG418	T_A = +25°C	30		pF
			DG419		35		
SUPPLY							
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	

Improved, SPST/SPDT Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog Signal Range	V_{ANALOG}	(Note 3)	0		12	V
Drain-Source On-Resistance	$r_{DS(ON)}$	I_S = -10mA, V_D = 3.8V, V+ = 10.8V		40	100	Ω
DYNAMIC						
Turn-On Time	t_{ON}	DG417/DG418, V_D = 8V, Figure 2		110		ns
Turn-Off Time	t_{OFF}	DG417/DG418, V_D = 8V, Figure 2		40		ns
Break-Before-Make Interval	t_D	DG419, R_L = 1000Ω, C_L = 35pF, Figure 4		60		ns
Charge Injection (Note 3)	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 5		2	10	pC
SUPPLY						
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA
Logic Supply Current	I_L	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA
Ground Current	I_{GND}	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA

Note 2: Typical values are for **design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention where the most negative value is a minimum and the most positive value a maximum, is used in this data data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.

Note 7: Between any two switches.

19-0137; Rev 1; 3/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Improved Low-Power, CMOS Analog Switches with Latches

General Description

Maxim's redesigned DG421/DG423/DG425 monolithic analog switches now feature guaranteed on-resistance matching (3Ω max) between switches and on-resistance flatness over the signal range (4Ω max). These low on-resistance switches (20Ω typ) conduct equally well in both directions. They guarantee a low charge injection of 15pC maximum and an ESD tolerance of 2000V minimum per Method 3015.7. Off leakage current over temperature has also been reduced (less than 5nA at +85°C).

The DG421/DG423/DG425 are precision, dual CMOS switches with latchable logic inputs that simplify interfacing with microprocessors (µPs). The single-pole/single-throw DG421 and double-pole/single-throw DG425 are normally open dual switches. The dual, single-pole/double-throw DG423 has two normally open and two normally closed switches. Fast switching times (175ns for t_{ON} and 145ns for t_{OFF}) and low power consumption (35µW max) make these parts ideal for battery-powered applications requiring µP-compatible switches. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Fabricated with the same 44V silicon-gate process, these switches have rail-to-rail signal handling capabilities.

Applications

- Sample-and-Hold Circuits
- Fax Machines
- Battery-Operated Systems
- Guidance and Control Systems
- Audio Signal Routing
- Modems
- Test Equipment
- PBX, PABX
- Military Radios
- Communication Systems

New Features

- **Plug-In Upgrades for Industry-Standard DG421/DG423/DG425**
- **Improved $r_{(DS)ON}$ Match Between Channels (3Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (4Ω max)**
- **Improved Charge Injection (15pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstands Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (35Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling Capability**
- **TTL/CMOS-Logic Compatible**

Ordering Information

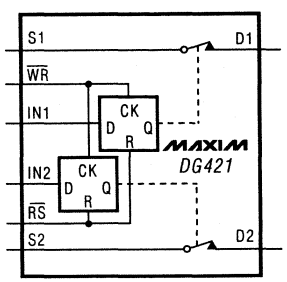
PART	TEMP. RANGE	PIN-PACKAGE
DG421CJ	0°C to +70°C	16 Plastic DIP
DG421CY	0°C to +70°C	16 SO
DG421C/D	0°C to +70°C	Dice*
DG421DJ	-40°C to +85°C	16 Plastic DIP
DG421DY	-40°C to +85°C	16 SO
DG421DK	-40°C to +85°C	16 CERDIP
DG421AK	-55°C to +125°C	16 CERDIP**

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883B.*

Functional Diagrams/Truth Tables



TWO SPST SWITCHES PER PACKAGE

DG421 TRUTH TABLE

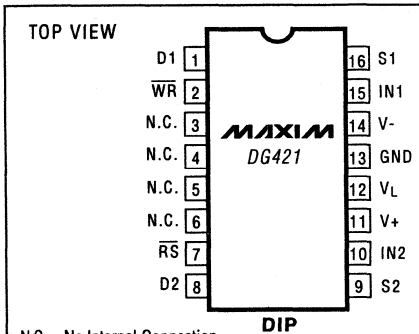
WR	RS	IN	SWITCH
0	1	0	Off
		1	On

LOGIC "0" ≤ 0.8V
LOGIC "1" ≥ 2.4V

SWITCHES SHOWN FOR LOGIC "1" INPUT

Functional Diagrams/Truth Tables continued at end of data sheet.

Pin Configurations



N.C. = No Internal Connection

Pin Configurations continued at end of data sheet.

Improved Low-Power, CMOS Analog Switches with Latches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND - 0.3V) to (V+ + 0.3V)
Digital Inputs, V_S, V_D (Note 1) ..... (V- - 2V) to (V+ + 2V)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ... 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
20-Pin PLCC (derate 10.00mW/°C above +70°C) 800mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) ... 800mW
Operating Temperature Ranges
DG42_C_ ..... 0°C to +70°C
DG42_D_ ..... -40°C to +85°C
DG42_A_ ..... -55°C to +125°C
Storage Temperature Ranges
DG42_C_/DG42_D_ ..... -65°C to +125°C
DG42_A_ ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		DG42_C, DG42_D MIN	DG42_C, DG42_D TYP	DG42_C, DG42_D MAX (Note 2)	DG42_A MIN	DG42_A TYP	DG42_A MAX (Note 2)	UNITS
SWITCH										
Analog Signal Range	V_{ANALOG}	(Note 3)		-15		15	-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = ±10V	T_A = +25°C		20	45		20	35	Ω
			T_A = T_{MIN} to T_{MAX}			45			45	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = ±10V	T_A = +25°C			3			3	Ω
			T_A = T_{MIN} to T_{MAX}			4			4	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, I_S = -10mA, V_D = ±5V	T_A = +25°C			4			4	Ω
			T_A = T_{MIN} to T_{MAX}			5			5	
Source-Off Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	-0.50	-0.01	0.50	-0.25	-0.01	0.25	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	-10		10	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	-0.50	-0.01	0.50	-0.25	-0.01	0.25	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	-10		10	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C	-1.0	-0.04	1.0	-0.40	-0.04	0.40	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	-20		20	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	IN = 2.4V, all others = 0.8V		-0.50	0.005	0.50	µA
Input Current with Input Voltage Low	I_{INL}	IN = 0.8V, all others = 2.4V		-0.50	0.005	0.50	µA
SUPPLY							
Power Supply Range	V+, V-	(Note 3)		±4.5		±20	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	-0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	-0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	-0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2	T_A = +25°C		150	250	ns
			T_A = T_{MIN} to T_{MAX}			300	
Turn-Off Time	t_{OFF}	Figure 2				200	ns
Latch Timing	t_{WW}	V_S = ±10V, R_L = 300Ω, C_L = 35pF, Figure 3	T_A = +25°C	200			ns
			T_A = -55°C to +125°C	200			
	t_{DW}		T_A = +25°C	100			
			T_A = -55°C to +125°C	100			
	t_{WD}		T_A = +25°C	60			
			T_A = -55°C to +125°C	100			
Break-Before-Make Interval (Note 3)	t_D	DG423, Figure 4	T_A = +25°C	5	25		ns
Charge Injection (Note 3)	Q	C_L = 10nF, V_G = 0V, R_G = 0Ω, Figure 5	T_A = +25°C		10	15	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		72		dB
Crosstalk (Note 7)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 7	T_A = +25°C		90		dB
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 8	T_A = +25°C		12		pF
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 8	T_A = +25°C		12		pF
Drain-On Capacitance	$C_{D(ON)}$	f = 1MHz, Figure 9	T_A = +25°C		39		pF
Source-On Capacitance	$C_{S(ON)}$	f = 1MHz, Figure 9	T_A = +25°C		39		pF

Note 2: Typical values are **for design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.

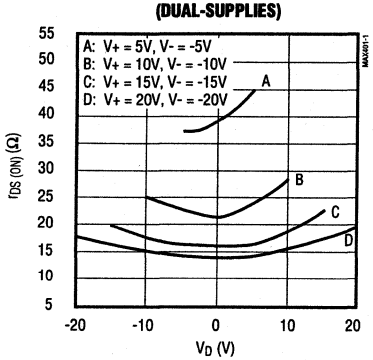
Note 7: Between any two switches.

Improved Low-Power, CMOS Analog Switches with Latches

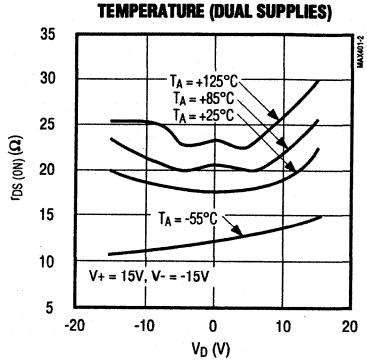
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

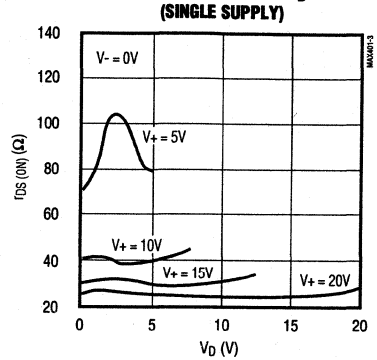
ON-RESISTANCE vs. V_D (DUAL-SUPPLIES)



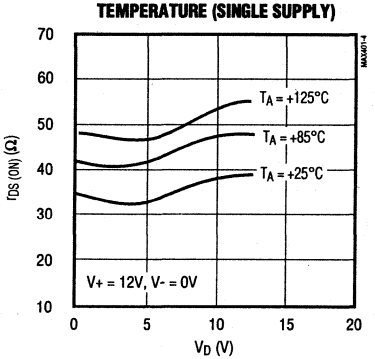
ON-RESISTANCE vs. V_D AND TEMPERATURE (DUAL SUPPLIES)



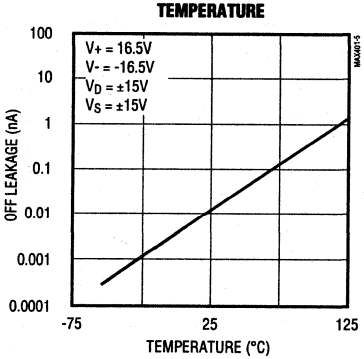
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



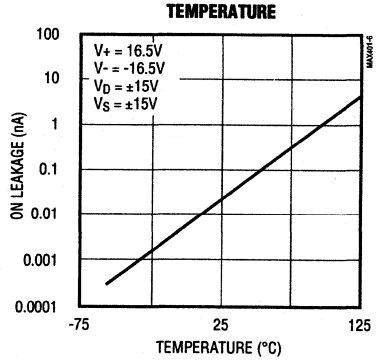
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



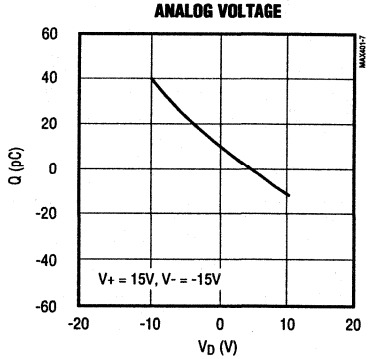
OFF LEAKAGE CURRENTS vs. TEMPERATURE



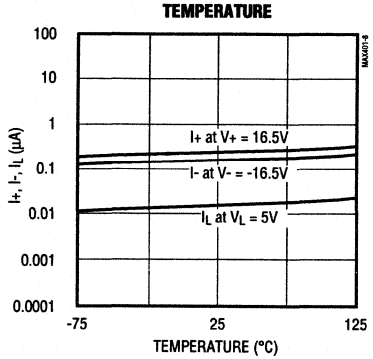
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



19-4611; Rev 1; 4/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's redesigned DG441/DG442 analog switches now feature on-resistance matching (4Ω max) between switches and guaranteed on-resistance flatness over the signal range (9Ω max). These low on-resistance switches conduct equally well in either direction and are guaranteed to have low charge injection (10pC max) and low power consumption 1.65mW. They guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off leakage current over temperature (less than 5nA at +85°C).

The DG441/DG442 are quad, single-pole/single-throw (SPST) analog switches. The DG441 has 4 normally closed switches and the DG442 has 4 normally open switches. Switching times are less than 250ns for t_{ON} and less than 70ns for t_{OFF}. These devices operate from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG441/DG442 continue to be fabricated with a 44V silicon-gate process.

New Features

- **Plug-In Upgrades for Industry-Standard DG441/DG442**
- **Improved $r_{DS(ON)}$ Match Between Channels (4Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (9Ω max)**
- **Improved Charge Injection (10pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (85Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (1.65mW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Applications

- Sample-and-Hold Circuits
- Communication Systems
- Test Equipment
- Battery-Operated Systems
- Heads-Up Displays
- Fax Machines
- PBX, PABX
- Guidance and Control Systems
- Audio Signal Routing
- Military Radios
- Modems

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG441CJ	0°C to +70°C	16 Plastic DIP
DG441CY	0°C to +70°C	16 Narrow SO
DG441C/D	0°C to +70°C	Dice*
DG441DJ	-40°C to +85°C	16 Plastic DIP
DG441DY	-40°C to +85°C	16 Narrow SO
DG441DK	-40°C to +85°C	16 CERDIP
DG441AK	-55°C to +125°C	16 CERDIP**

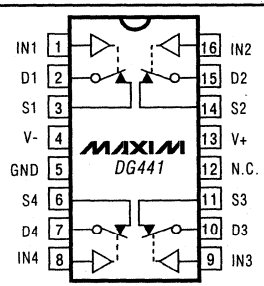
Ordering Information continued on last page.

** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883B.*

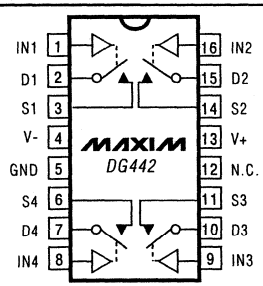
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

DG441	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG442	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

N.C. = Not Internally Connected

Improved, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+ +0.3V)
Digital Inputs, V_S, V_D (Note 1) ..... (V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) .100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
DG441C/DG442C ..... 0°C to +70°C
DG441D/DG442D ..... -40°C to +85°C
DG441AK/DG442AK ..... -65°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = 8.5V or -8.5V	T_A = +25°C			50	85	Ω
			T_A = T_{MIN} to T_{MAX}				100	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, V_D = ±10V, I_S = -10mA	T_A = +25°C				4	Ω
			T_A = T_{MIN} to T_{MAX}				5	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, V_D = 5V or -5V, I_S = -10mA	T_A = +25°C				9	Ω
			T_A = T_{MIN} to T_{MAX}				15	
Source-Off Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ∓15.5V, V_S = ±15.5V	T_A = +25°C		-0.50	0.01	0.50	nA
			T_A = T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ∓15.5V, V_S = ±15.5V	T_A = +25°C		-.0.50	0.01	0.50	nA
			T_A = T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$ or $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C		-0.50	0.08	0.50	nA
			T_A = T_{MAX}	C, D	-10		10	
				A	-20		20	
DIGITAL								
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V			-500	0.01	500	nA
Input Current with Input Voltage Low	I_{INH}	V_{IN} = 0.8V			-500	0.01	500	nA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SUPPLY							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V			15	100	µA
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V		-100	-15		µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S = ±10V, R_L = 1kΩ, Figure 2	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	DG441, V_D = ±10V, Figure 2	T_A = +25°C		90	120	ns
		DG442, V_D = ±10V, Figure 2	T_A = +25°C		110	170	
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		5	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		60		dB
Crosstalk (Note 7)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		-100		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Drain-On Capacitance	$C_{D(ON)}$	f = 1MHz, Figure 6	T_A = +25°C		16		pF

Improved, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 10.8V, V_D = 3V, 8V, I_S = 1.0mA	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range	V+			10		30	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V			15	100	µA
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V		-100	-15		µA
DYNAMIC							
Turn-On Time	t_{ON}	V_S = 8V, Figure 2	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	V_S = 8V, Figure 2	T_A = +25°C		60	200	ns
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0V	T_A = +25°C		5	10	pC

Note 2: Typical values are for **design aid only** are not guaranteed and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

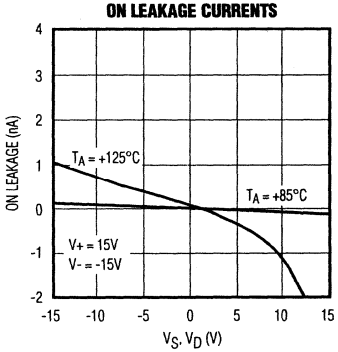
Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

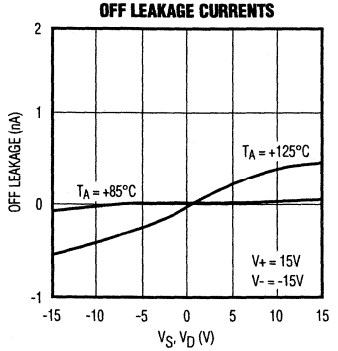
Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.

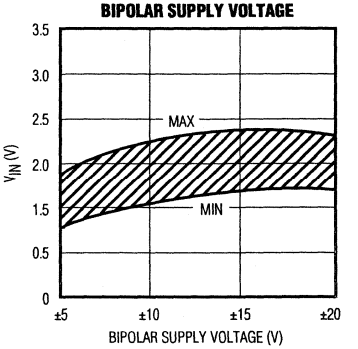
Note 7: Between any two switches.

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)







19-4705; Rev 1; 4/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's redesigned DG444/DG445 analog switches now feature on-resistance matching (4Ω max) between switches and guaranteed on-resistance flatness over the signal range (9Ω max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection (10pC max), low power consumption (35µW max), and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off leakage current over temperature (less than 5nA at +85°C).

The DG444/DG445 are quad, single-pole/single-throw (SPST) analog switches. The DG444 has 4 normally closed switches and the DG445 has 4 normally open switches. Switching times are less than 250ns for t_{ON} and less than 70ns for t_{OFF}. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG444/DG445 continue to be fabricated with a 44V silicon-gate process.

New Features

- **Plug-In Upgrades for Industry-Standard DG444/DG445**
- **Improved r_{ON} Match Between Channels (4Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (9Ω max)**
- **Improved Charge Injection (10pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (85Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Applications

Sample-and-Hold Circuits
Test Equipment
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communication Systems
Battery-Operated Systems
PBX, PABX
Audio Signal Routing
Modems/Faxes

Ordering Information

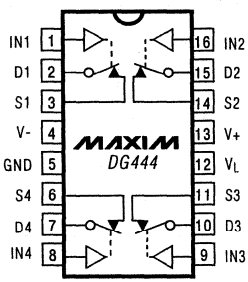
PART	TEMP. RANGE	PIN-PACKAGE
DG444CJ	0°C to +70°C	16 Plastic DIP
DG444DY	0°C to +70°C	16 Narrow SO
DG444C/D	0°C to +70°C	Dice*
DG444DJ	-40°C to +85°C	16 Plastic DIP
DG444DY	-40°C to +85°C	16 Narrow SO

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

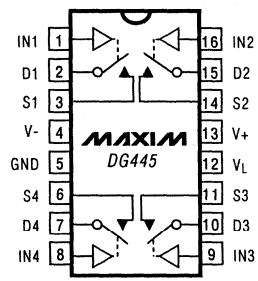
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



DIP/SO

DG444	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG445	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

Improved, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+ +0.3V)
Digital Inputs V_S, V_D (Note 1) ..... (V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) .100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ..696mW
Operating Temperature Ranges
DG444C/DG445C ..... 0°C to +70°C
DG444D/DG445D ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, V_D = ±8.5V, I_S = -10mA	T_A = +25°C		50	85	Ω
			T_A = T_{MIN} to T_{MAX}			100	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V_D = ±10V, I_S = -10mA	T_A = +25°C			4	Ω
			T_A = T_{MIN} to T_{MAX}			5	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V_D = ±5V, I_S = -10mA	T_A = +25°C			9	Ω
			T_A = T_{MIN} to T_{MAX}			15	
Source Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	-0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	-0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$ or $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C	-0.50	0.08	0.50	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
INPUT							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V, all others = 0.8V		-0.5	-0.00001	0.5	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V, all others = 2.4V		-0.5	-0.00001	0.5	µA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SUPPLY							
Power-Supply Range	V+, V-			±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_S = ±10V, Figure 2	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	DG444, V_S = ±10V, Figure 2	T_A = +25°C		90	120	ns
		DG445, V_S = ±10V, Figure 2	T_A = +25°C		110	170	ns
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		5	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		60		dB
Crosstalk (Note 7)		R_L - 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		100		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		4		pF
Source-On Capacitance	$C_{S(ON)}$	f = 1MHz, Figure 7	T_A = +25°C		16		pF
Drain-On Capacitance	$C_{D(ON)}$	f = 1MHz, Figure 7	T_A = +25°C		16		pF

Improved, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

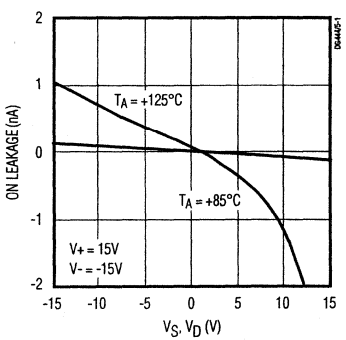
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 10.8V, V_L = 5.25V, V_D = 3V, 8V, I_S = -10mA	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range	V+, V-			10.8		24.0	V
Power-Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_S = 8V, Figure 2	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	V_S = 8V, Figure 2	T_A = +25°C		60	200	ns
Charge Injection (Note 3)	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3	T_A = +25°C		5	10	pC

Note 2: Typical values are for **design aid only,** are not guaranteed and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog signal range.
Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, $I_{D(ON)}$, and $I_{S(ON)}$, are100% tested at the maximum rated hot temperature and guaranteed at +25°C.
Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.
Note 7: Between any two switches.

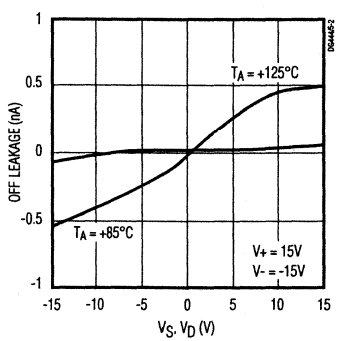
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

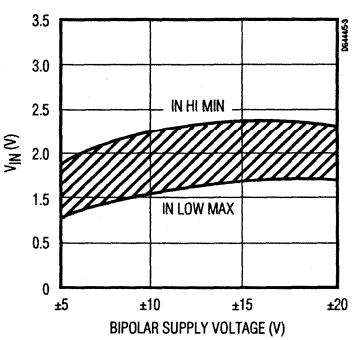
ON LEAKAGE CURRENTS



OFF LEAKAGE CURRENTS



SWITCHING THRESHOLD vs. BIPOLAR SUPPLY VOLTAGE



MAXIM

Interface Products

*Advance Information–first page of data sheet in preparation.

LINE DRIVERS/RECEIVERS

AppleTalk™

MAX216 (1 single-ended driver/2-single-ended receivers, 1 differential driver/1 differential receiver)

RS-232

+3V POWERED

4 DRVRS, 5 RCVRS

MAX560
(2 receivers active in shutdown)

MAX561 (shutdown)

3 DRVRS, 5 RCVRS

☆ **MAX212**
(true RS-232, 3mA I_{CC} max)

★ **MAX3241**
(true RS-232, 0.1µF caps, 1mA I_{CC} max)

MAX562
(2.7V to 5.25V operation)

2 DRVRS, 2 RCVRS

★ **MAX218**
(1.8V to 4.25V V_{CC} in, true RS-232 out)

† **MAX3222**
(true RS-232, 0.1µF caps, 2 receivers active in shutdown)

† **MAX3232**
(true RS-232, 0.1µF caps)

MAX563
(120kbps data rate, 2 receivers active in shutdown)

1µA SUPPLY CURRENT

† **MAX3212**
3Tx, 5Rx, 2.7V to 3.6V operation

† **MAX3218**
2Tx, 2Rx, 1.8V to 4.25V operation

† **MAX3223**
2Tx, 2Rx, 3.0V to 5.5V operation 0.1µF caps

† **MAX3243**
3Tx, 5Rx, 3.0V to 5.5V operation 0.1µF caps

+5V, 4 EXT. CAPS

2 DRVRS, 2 RCVRS

MAX202 (0.1µF caps, low cost)
MAX220 (ultra-low power)
MAX222 (I_Q = 10µA in shutdown)
MAX232 (industry standard)
MAX232A (116kbits/sec data rate, 0.1µF caps)
MAX242 (receivers active in shutdown)
MAX243 (simplified cabling)

COMPLETE PC SERIAL PORTS

MAX211 (pin compatible with MAX241, 0.1µF caps)
MAX213 (2 receivers active in shutdown, 0.1µF caps)
MAX214 (programmable DTE/DCE port)
MAX223 (2 receivers active in shutdown)
MAX241 (industry standard)

HIGH DRVR/RCVR COUNT

MAX200 (5 drivers, 0 receivers, 0.1µF caps)
MAX204 (4 drivers, 0 receivers, 0.1µF caps)
MAX206 (4 drivers, 3 receivers, 0.1µF caps)
MAX207 (5 drivers, 3 receivers, 0.1µF caps)
MAX208 (4 drivers, 4 receivers, 0.1µF caps)
MAX230 (5 drivers, 0 receivers)
MAX234 (4 drivers, 0 receivers)
MAX236 (4 drivers, 3 receivers)
MAX237 (5 drivers, 3 receivers)
MAX238 (4 drivers, 4 receivers)
MAX240 (5 drivers, 5 receivers)
MAX244 (8 drivers, 10 receivers)
MAX248 (8 drivers, 8 receivers)
MAX249 (8 drivers, 10 receivers)

+5V, INTERNAL CAPS

2 DRVRS, 2 RCVRS

MAX203 (available in SO)
MAX233
MAX233A (116kbits/sec)

HIGH DRVR/RCVR COUNT

MAX205 (5 drivers, 5 receivers)
MAX225 (5 drivers, 5 receivers, SO package)
MAX235 (5 drivers, 5 receivers)
MAX245 (8 drivers, 10 receivers)
MAX246 (8 drivers, 10 receivers)
MAX247 (8 drivers, 9 receivers)

ISOLATION PRODUCTS

2-CHIP SET

MAX250
MAX251

COMPLETE MODULE

MAX252A (UL recognized)
MAX252B (500V isolation)

+5V/+12V OR BATTERY POWER, 2 EXT. CAPS

2 DRVRS, 2 RCVRS

MAX201 (0.1µF caps)
MAX231

COMPLETE PC SERIAL PORTS

MAX209
(3 drivers, 5 receivers, 0.1µF caps)

MAX239
(3 drivers, 5 receivers)

±15kV ESD PROTECTION

★ **MAX202E** (2Tx/2Rx, ±15kV ESD per human body model & IEC 801-2)
MAX211E (4Tx/5Rx, ±15kV ESD per human body model & IEC 801-2)
★ **MAX213E** (4Tx/5Rx, ±15kV ESD per human body model & IEC 801-2)
★ **MAX232E** (2Tx/2Rx, ±15kV ESD per human body model & IEC 801-2)
★ **MAX241E** (4Tx/5Rx, ±15kV ESD per human body model & IEC 801-2)

RS-485

1 DRVR, 1 RCVR FULL DUPLEX

★ **MAX488**
(250kbps, reduces EMI by 100x)

★ **MAX489**
(MAX488 plus driver/receiver enables)

★ **MAX490**
(direct LTC490 replacement)

★ **MAX491**
(direct LTC491 replacement)

1 DRVR, 1 RCVR 1/2 DUPLEX

MAX481
(MAX485 plus 1µA shutdown)

MAX483
(250kbps, reduces EMI by 100x)

MAX485
(direct LTC485 replacement)

★ **MAX487**
(MAX483 plus 1/4-unit load)

ISOLATION PRODUCTS

★ **MAX253**
(isolated power for MAX48X family)

† **MAX1480A**
(complete 2.5Mbps isolated RS-485 in one package)

★ **MAX1480B**
(complete 250kbps isolated RS-485 in one package)

★ **New product**
☆ **Evaluation kit available**
† **Future product**
™ **AppleTalk is a trademark of Apple Computer, Inc.**

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
+3V RS-232 PRODUCTS										
MAX212	+3.0 to +3.6	3/5	1.5	2	0.33/0.68	Yes	✔	Yes	250	5 receivers active in shutdown, I_{CC} = 1.5mA, chip inductor
MAX218	+1.8 to +4.25	2/2	1.9	2	0.33/0.68	Yes	✔	Yes	250	True RS-232 performance from 1.8V to 4.25V input
MAX3212†	+2.7 to 3.6	3/5	1.0µA	2	0.33/0.68	Yes	✔	Yes	230	AutoShutdown reduces supply current to 1µA
MAX3218†	+1.8 to +4.25	2/2	1.0µA	2	0.33/0.68	Yes	✔	Yes	230	AutoShutdown reduces supply current to 1µA
MAX3222†	+3.0 to +5.5	2/2	250µA	4	0.1	Yes	✔	Yes	230	2 receivers active in shutdown, 0.5mA I_{CC}, true RS-232
MAX3223†	+3.0 to +3.6	2/2	1.0µA	4	0.1	Yes	✔	Yes	230	AutoShutdown reduces supply current to 1µA
MAX3232†	+3.0 to +5.5	2/2	250µA	4	0.1	No		Yes	230	Industry-standard MAX232 pinout, true RS-232
MAX3241	+3.0 to +5.5	2/2	500µA	4	0.1	Yes	✔	Yes	230	Mouse driveability, 2 spare receivers active in shutdown, true RS-232
MAX3243†	+3.0 to +3.6	3/5	1.0µA	4	0.1	Yes	✔	Yes	230	AutoShutdown reduces supply current to 1µA
MAX560	+3.0 to +3.6	4/5	5	4	1.0	Yes	✔	No	120	+3V, MAX561 with receivers active in shutdown
MAX561	+3.0 to +3.6	4/5	5	4	1.0	Yes		No	120	+3V, complete IBM PC serial port
MAX562	+2.7 to +5.25	3/5	20	5	0.33/0.68	Yes	✔	No	250	+2.7V to +5.25V operation, 230kbps guaranteed data rate
MAX563	+3.0 to +3.6	2/2	4	4	0.1	Yes	✔	No	200	2 receivers active in shutdown
+5V RS-232 PRODUCTS										
MAX214	+5	3/5	9	4	1.0	Yes		Yes	120	Programmable DTE/DCE port
MAX220	+5	2/2	500µA	4	4.7/10	No		Yes	22	Ultra-low power, industry-standard pinout
MAX222	+5	2/2	4	4	0.1	Yes		Yes	200	+5V IBM PC serial port with receivers active in shutdown
MAX223(MAX213)	+5	4/5	7	4	1.0(0.1)	Yes	✔	Yes	120	MAX241 + receivers active in shutdown
MAX225	+5	5/5	11	0	–	Yes		Yes	120	Available in 28-pin SO package
MAX230(MAX200)	+5	5/0	7	4	1.0(0.1)	Yes		Yes	120	5 drivers with shutdown
MAX231(MAX201)	+5 and +7.5 to +13.2	2/2	400µA	2	1.0(0.1)	No		Yes	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232(MAX202)	+5	2/2	5	4	1.0(0.1)	No		Yes	120(64)	Industry standard
MAX232A	+5	2/2	4	4	0.1	No		Yes	200	High slew rate, small caps, guaranteed 120kbps data rate
MAX233(MAX203)	+5	2/2	5	0	–	No		Yes	120	No external caps, MAX203 available in SOIC
MAX233A	+5	2/2	4	0	–	No		Yes	200	No external caps, high slew rate
MAX234(MAX204)	+5	4/0	7	4	1.0(0.1)	No		Yes	120	Replaces 1488
MAX235(MAX205)	+5	5/5	7	0	–	Yes		Yes	120	No external caps
MAX236(MAX206)	+5	4/3	7	4	1.0(0.1)	Yes		Yes	120	Shutdown, three-state
MAX237(MAX207)	+5	5/3	7	4	1.0(0.1)	No		Yes	120	Complements IBM PC serial port
MAX238(MAX208)	+5	4/4	7	4	1.0(0.1)	No		Yes	120	Replaces 1488 and 1489
MAX239(MAX209)	+5 and +7.5 to +13.2	3/5	7	2	1.0(0.1)	No		Yes	120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5/5	7	4	1.0	Yes		Yes	120	DIP or flatpak package
MAX241(MAX211)	+5	4/5	7	4	1.0(0.1)	Yes		Yes	120	Complete IBM PC serial port, industry standard
MAX242	+5	2/2	4	4	0.1	Yes	✔	Yes	200	Separate shutdown and enable
MAX243	+5	2/2	4	4	0.1	No		Yes	200	Open-line detection simplifies cabling
MAX244	+5	8/10	11	4	1.0	No		Yes	120	High slew rate
MAX245	+5	8/10	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	11	4	1.0	Yes	✔	Yes	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	11	4	1.0	Yes	✔	Yes	120	Available in quad flatpack package

† Future product—contact factory for availability. Specifications are preliminary.

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
RS-232 ISOLATION PRODUCTS										
MAX250	+5	2/2	100µA	–	–	Yes		Yes	120	Isolated RS-232 chip set
MAX251	+5	2/2	100µA	–	–	Yes		Yes	120	Isolated RS-232 chip set
MAX252A	+5	2/2	130	0	–	Yes		Yes	20	UL recognized, 1500V isolation
MAX252B	+5	2/2	130	0	–	Yes		Yes	20	Economical 500V isolation

Part Number	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	Supply Current (µA)	Shutdown Supply Current (µA)	Full Duplex	No. of Rx/Tx On Bus	Features
RS-485 PRODUCTS								
MAX481	+5	2.5	1/1	500	1	No	32	MAX485 + 1µA shutdown mode
MAX483	+5	0.25	1/1	350	1	No	32	Reduced slew rate reduces EMI and reflections
MAX485	+5	2.5	1/1	500	300	No	32	Direct LTC485 replacement
MAX487	+5	0.25	1/1	250	1	No	128	MAX483 plus 1/4 unit load
MAX488	+5	0.25	1/1	350	–	Yes	32	Reduced slew rate reduces EMI and reflections
MAX489	+5	0.25	1/1	350	1	Yes	32	MAX488 plus driver/receiver enable
MAX490	+5	2.50	1/1	500	300	Yes	32	Direct LTC490 replacement
MAX491	+5	2.50	1/1	500	300	Yes	32	Direct LTC491 replacement

Part Number	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	Supply Current (mA)	Isolated Power (mW)	Isolation Voltage (V)	Shutdown Supply Current (µA)	Full Duplex	Features
RS-485 ISOLATION PRODUCTS									
MAX1480A†	+5	2.5	1/1	10	–	1500	1	No	Complete isolated RS-485 in one package
MAX1480B	+5	0.25	1/1	10	–	1500	1	No	Complete isolated RS-485 in one package
MAX253	+5	–	–	5	750	–	1	–	Isolated power driver for RS-485

Part Number	Power Supply (V)	No. of Single-Ended Drivers/Receivers	No. of Differential Drivers/Receivers	Shutdown	Single-Ended Data Rate (kbps)	Differential Data Rate (Mbps)	Description
APPLETALK™ TRANSCEIVER							
MAX216	±5	1/2	1/1	Yes	120	1	Complete AppleTalk™ interface

Part Number	Power Supply (V)	No. of RS-232 Drivers/ Receivers	ESD Voltage (kV)	Ext. Caps	Shutdown & Three-State	Rx Active in Shutdown	Data Rate (kbps)	Features
HIGH ESD RS-232 PRODUCTS								
MAX202E	+5	2/2	±15	4 x 0.1µF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX211E	+5	4/5	±15	4 x 0.1µF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX213E	+5	4/5	±15	4 x 0.1µF	Yes	✔	120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX232E	+5	2/2	±15	4 x 1.0µF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2
MAX241E	+5	4/5	±15	4 x 1.0µF	Yes		120	±15kV ESD per human body model and ±15kV per IEC 801-2

™ AppleTalk is a trademark of Apple Computer, Inc.
† Future product—contact factory for availability. Specifications are preliminary.

19-0259; Rev 0; 5/94

MAXIM

Complete, Isolated, RS-485/RS-422 Data Interface

General Description

The MAX1480A/MAX1480B are complete, electrically isolated, RS-485/RS-422 data-communications interface solutions. Transceivers, optocouplers, and a transformer provide a complete interface in one low-cost, 28-pin DIP package. A single +5V supply on the logic side powers both sides of the interface.

The MAX1480B features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The MAX1480A's driver slew rate is not limited, allowing transmission rates up to 2.5Mbps.

These devices typically draw 28mA of quiescent supply current. The MAX1480B provides a low-power shutdown mode in which it consumes only 0.2µA.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX1480A/MAX1480B typically withstand 1600V_{RMS} (1 minute) or 2000V_{RMS} (1 second). Their isolated outputs meet all RS-485/RS-422 specifications.

Applications

Isolated RS-485/RS-422 Data Interface

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Automatic Test Equipment

HVAC/Building Control Networks

Features

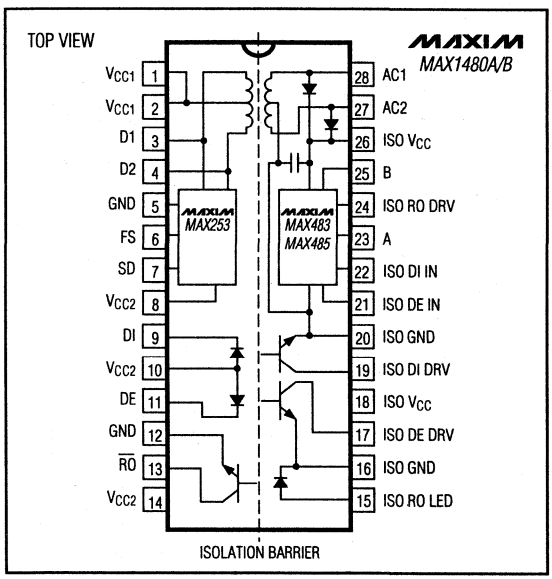
- ♦ **Isolated Data Interface, Typically to 1600V_{RMS} (1 minute)**
- ♦ **Slew-Rate Limited for Errorless Data Transmission (MAX1480B)**
- ♦ **High-Speed, Isolated, 2.5Mbps RS-485 Interface (MAX1480A)**
- ♦ **-7V to +12V Common-Mode Input Voltage Range with Respect to Isolated Ground**
- ♦ **Single +5V Supply**
- ♦ **1µW Low-Power Shutdown Mode**
- ♦ **Current Limiting and Thermal Shutdown for Driver Overload Protection**
- ♦ **Standard 28-Pin DIP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	DATA RATE (kbps)
MAX1480ACPI*	0°C to +70°C	28 Plastic DIP	2500
MAX1480BCPI	0°C to +70°C	28 Plastic DIP	250
MAX1480AEPI*	-40°C to +85°C	28 Plastic DIP	2500
MAX1480BEPI	-40°C to +85°C	28 Plastic DIP	250

** MAX1480A available in July 1994.*

Pin Configuration



Typical Operating Circuit appears on last page.

Complete, Isolated, RS-485/RS-422 Data Interface

ABSOLUTE MAXIMUM RATINGS

With Respect to GND:
- Supply Voltage (V_{CC}_) .....-0.3V to +6.0V
- Control Input Voltages (SD, FS) .....-0.3V to (V_{CC} + 0.3V)
- Receiver Output Voltages ($\overline{RO}$).....-0.3V to (V_{CC} + 0.3V)
- Output Switch Voltage (D1, D2).....+12V

With Respect to ISO GND:
- Control Input Voltages (ISO DE __).....-0.3V to (ISO V_{CC} + 0.3V)
- Driver Input Voltages (ISO DI __) .....-0.3V to (ISO V_{CC} + 0.3V)
- Receiver Output Voltages (ISO RO __) ..-0.3V to (ISO V_{CC} + 0.3V)
- Driver Output Voltages (A, B).....-8V to +12.5V
- Receiver Input Voltages (A, B).....-8V to +12.5V

LED Forward Current (DI, DE, ISO RO LED) 50mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges
- MAX1480_CPI.....0°C to +70°C
- MAX1480_EPI.....-40°C to +85°C

Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX1480B ONLY

(V_{CC} = V_{CC1} = V_{CC2} = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_S	FS = 0V	4.5	5.0	5.5	V
		FS = V_{CC} or open	4.75	5.0	5.25	
Switch Frequency	F_{SWL}	FS = 0V		200		kHz
	F_{SWH}	FS = V_{CC} or open		350		
Operating Supply Current	I_{CC}	DE´ = V_{CC} or open, R_L = ∞		28	45	mA
		DE´ = V_{CC} or open, R_L = 54Ω		86		
Shutdown Supply Current (Note 4)	I_{SD}	SD = V_{CC}		0.2		µA
Shutdown Input Threshold	V_{SDH}	High	2.4			V
	V_{SDL}	Low			0.8	
Shutdown Input Leakage Current				10		pA
FS Input Threshold	V_{FSH}	High	2.4			V
	V_{FSL}	Low			0.8	
FS Input Pull-Up Current		FS low			50	µA
FS Input Leakage Current		FS high		10		pA
Input High Voltage	V_{IH}	DE´, DI´	4.2			V
Input Low Voltage	V_{IL}	DE´, DI´			0.4	V
Isolation Resistance	R_{ISO}	T_A = +25°C, V_{ISO} = 50V_{DC}	100	10,000		MΩ
Isolation Capacitance	C_{ISO}	T_A = +25°C, V_{ISO} = 50V_{DC}		10		pF
Differential Driver Output (no load)	V_{OD1}				8	V
Differential Driver Output (with load)	V_{OD1}	R = 50Ω (RS-422)	2			V
		R = 27Ω (RS-485), Figure 3	1.5		5	
Change in Magnitude of Driver Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 3 — Differential			0.3	V
		R = 27Ω or 50Ω, Figure 3 — Common mode			0.3	
Driver Common-Mode Output	V_{OC}	R = 27Ω or 50Ω, Figure 3			4	V

ELECTRICAL CHARACTERISTICS—MAX1480B ONLY (continued)

(V_{CC} = V_{CC1} = V_{CC2} = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current (A, B)	ISO I_{IN}	DE′ = 0V, V_{CC} = 0V or 5.5V, V_{IN} = 12V			1.0	mA
		DE′ = 0V, V_{CC} = 0V or 5.5V, V_{IN} = -7V			0.8	
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	12			kΩ
Receiver Differential Threhold	V_{TH}	-7V ≤ V_{CM} ≤ 12V	-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		70		mV
$\overline{\text{Receiver Output}}$ Low Voltage	V_{OL}	I_{OUT} = 2mA, DI′ = V_{CC}			0.4	V
$\overline{\text{Receiver Output}}$ High Current	I_{OH}	V_{OUT} = 5.5V, DI′ = 0V			250	µA
Driver Short-Circuit Current	ISO I_{OSD}	-7V ≤ V_O ≤ 12V (Note 5)	35		400	mA

SWITCHING CHARACTERISTICS—MAX1480B ONLY

(V_{CC} = V_{CC1}= V_{CC2} = 5V ±10%, FS = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output Propagation Delay	t_{PLH}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
	t_{PHL}			1.0	2.0	
Driver Output Skew	t_{SKEW}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		1.0	2.0	µs
Driver Enable to Output High	t_{ZH}	Figures 6 and 8, C_L = 100pF, S2 closed		35	100	µs
Driver Enable to Output Low	t_{ZL}	Figures 6 and 8, C_L = 100pF, S1 closed		35	100	µs
Driver Disable Time from Low	t_{LZ}	Figures 6 and 8, C_L = 15pF, S1 closed		13	50	µs
Driver Disable Time from High	t_{HZ}	Figures 6 and 8, C_L = 15pF, S2 closed		13	50	µs
Receiver Input to Output Propagation Delay	t_{PLH}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		0.8	2.0	µs
	t_{PHL}			0.8	2.0	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 5 and 7, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		50		ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	0.25			Mbps
Time to Shutdown	t_{SHDN}			20	50	µs
Driver Enable from Shutdown to Output High/Low	$t_{ZH(SHDN)}$	Figures 6 and 8, C_L = 100pF, S2 closed		35	100	µs

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to logic-side ground (GND) unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = V_{CC1} = V_{CC2} = 5V and T_A = +25°C.

Note 3: See application circuit (Figure 2) for DE′ and DI′ pin descriptions.

Note 4: Shutdown supply current is the current at V_{CC1} when shutdown is enabled.

Note 5: Applies to peak current. See *Typical Operating Characteristics.*

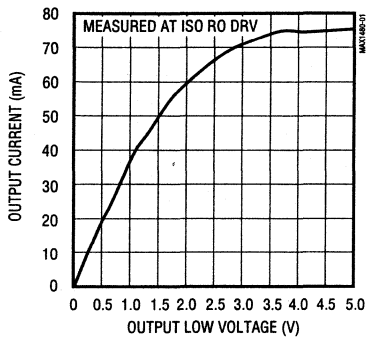
Complete, Isolated, RS-485/RS-422 Data Interface

Typical Operating Characteristics

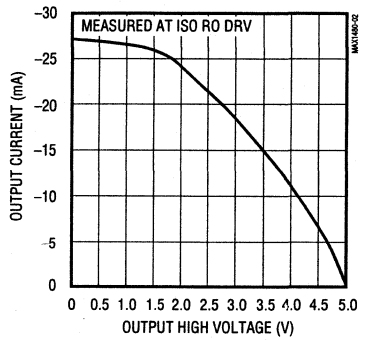
(V_{CC} = V_{CC1} = V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

MAX1480B ONLY

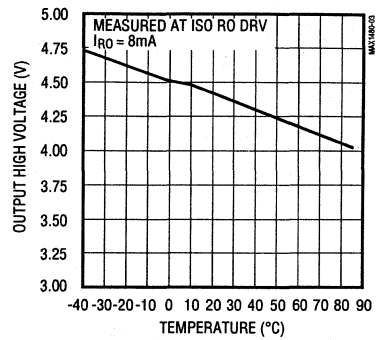
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



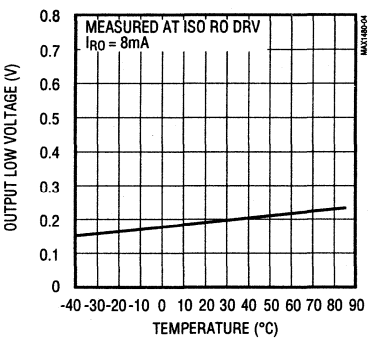
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



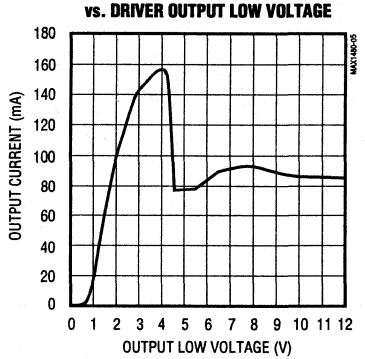
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



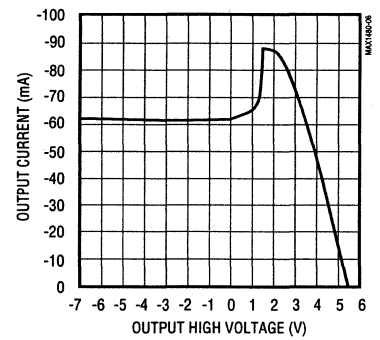
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



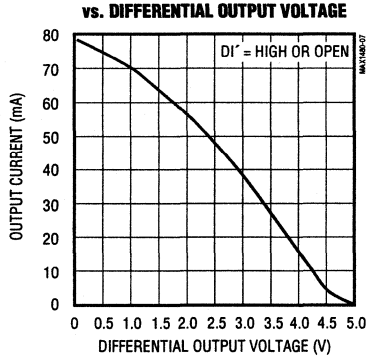
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



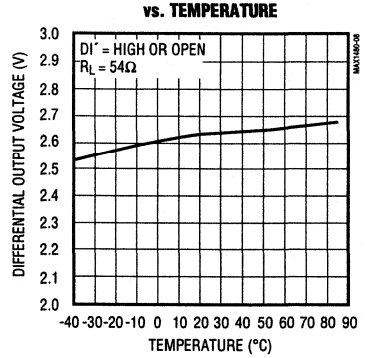
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



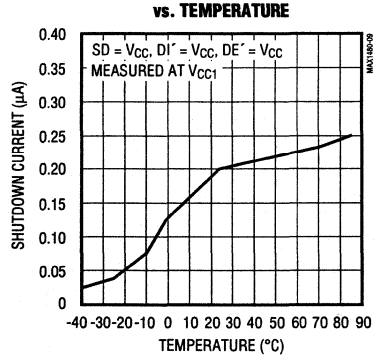
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



SHUTDOWN CURRENT vs. TEMPERATURE

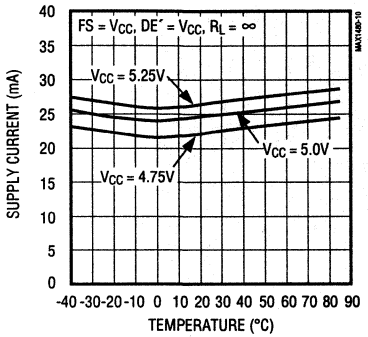


Typical Operating Characteristics (continued)

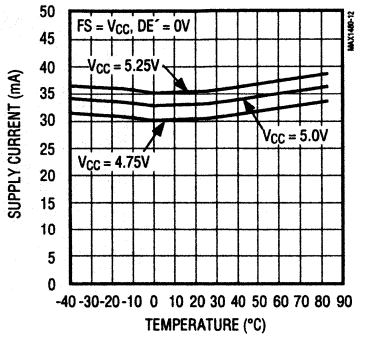
(V_{CC} = V_{CC1} = V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

MAX1480B ONLY

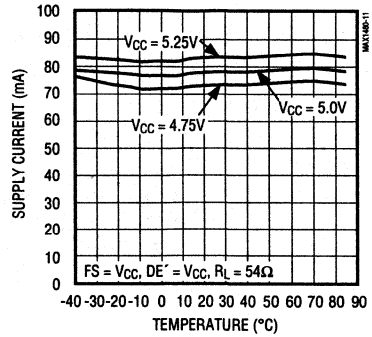
SUPPLY CURRENT vs. TEMPERATURE



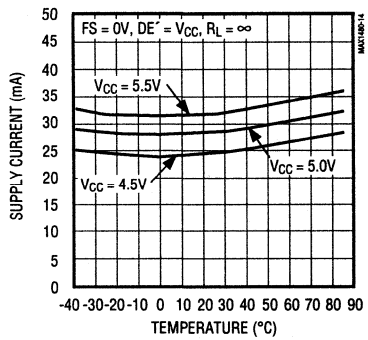
SUPPLY CURRENT vs. TEMPERATURE



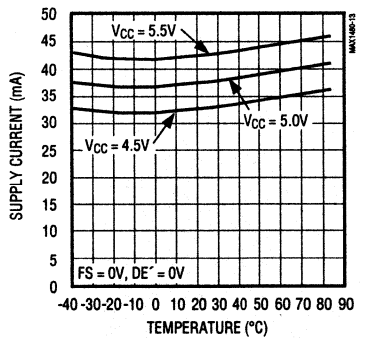
SUPPLY CURRENT vs. TEMPERATURE



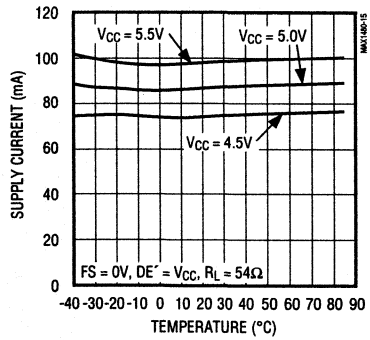
SUPPLY CURRENT vs. TEMPERATURE



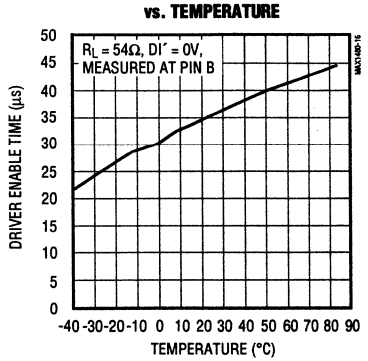
SUPPLY CURRENT vs. TEMPERATURE



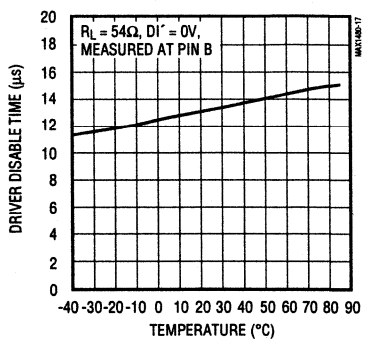
SUPPLY CURRENT vs. TEMPERATURE



DRIVER ENABLE TIME vs. TEMPERATURE



DRIVER DISABLE TIME vs. TEMPERATURE



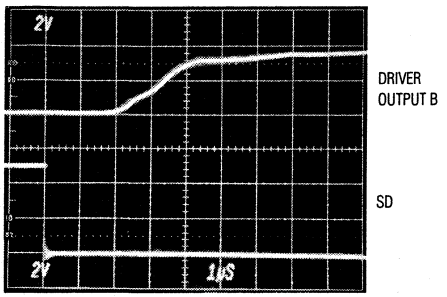
Complete, Isolated, RS-485/RS-422 Data Interface

Typical Operating Characteristics (continued)

(V_{CC} = V_{CC1} = V_{CC2} = 5V, T_A = +25°C, unless otherwise noted.)

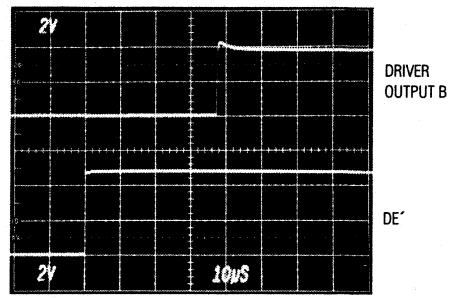
MAX1480B ONLY

POWER-UP DELAY TO TRANSMITTER OUTPUTS



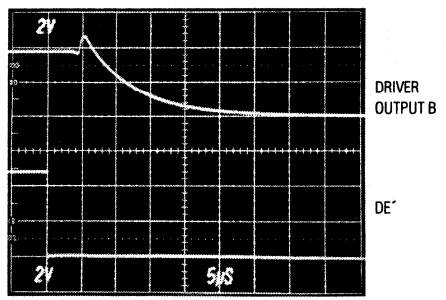
V_{CC} = 5.0V, DI´= 0V
SD = 5V TO 0V AT 1kHz

DRIVER ENABLE TIME



V_{CC} = 5.0V, DI´= 0V
DE´ TOGGLED 0V TO 5V AT 5kHz

DRIVER DISABLE TIME



V_{CC} = 5.0V, DI´= 0V
DE´ TOGGLED 0V TO 5V AT 5kHz

Pin Description

PIN	NAME	FUNCTION
1, 2	V_{CC1}	Logic-Side (non-isolated side) +5V Supply Voltage. Internally connected. Tie to V_{CC2} for normal operation.
8, 10, 14	V_{CC2}	Logic-Side (non-isolated side) +5V Supply Voltages. Must be connected together, not internally connected. Tie to V_{CC1} for normal operation.
3, 4	D1, D2	Internal Connections. Leave these pins unconnected.
5, 12	GND	Logic-Side Grounds. Must be tied together; not internally connected.
6	FS	Frequency Switch. If FS = V_{CC} or open, switch frequency = 350kHz; if FS = 0V, switch frequency = 200kHz.
7	SD	Shutdown. Ground for normal operation. When high, the power oscillator is disabled.
9	DI	Driver Input. With DE´ high, a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Drives internal LED cathode through a resistor. (See Table 1 of Figure 2.)
11	DE	Driver Enable. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the parts function as line drivers. While the driver outputs are high impedance, the chips can function as line receivers. Drives internal LED cathode through a resistor. (See Table 1 of Figure 2.)
13	$\overline{RO}$	$\overline{\text{Receiver Output}}$. If A > B by 200mV, $\overline{RO}$ will be low; if A < B by 200mV, $\overline{RO}$ will be high. Open collector; must have pull-up to V_{CC}.
15	ISO RO LED	Isolated Receiver Output LED. If A > B by 20mV, ISO RO LED will be high; if A < B by 200mV, ISO RO LED will be low. Drives internal LED anode through a resistor. (See Table 1 of Figure 2.)
16, 20	ISO GND	Isolated Grounds. Must be tied together; not internally connected.
17	ISO DE DRV	Isolated Driver-Enable Drive. The driver outputs, A and B, are enabled by bringing DE´ high. The driver outputs are high impedance when DE´ is low. If the driver outputs are enabled, the parts function as line drivers. While the driver outputs are high impedance, the chips can function as line receivers. Open-collector output; must have pull-up to ISO V_{CC} and be tied to ISO DE IN for normal operation.
18, 26	ISO V_{CC}	Isolated Supply Voltages. Must be tied together; not internally connected.
19	ISO DI DRV	Isolated Driver-Input Drive. With DE´ high, a low on DI´ forces output A low and output B high. Similarly, a high on DI´ forces output A high and output B low. Open-collector output; must have pull-up to ISO V_{CC} and be tied to ISO DI IN for normal operation.
21	ISO DE IN	Isolated Driver-Enable Input. Tie to ISO DE DRV for normal operation.
22	ISO DI IN	Isolated Driver-Input Input. Tie to ISO DI DRV for normal operation.
23	A	Noninverting Driver Output and Noninverting Receiver Input
24	ISO RO DRV	Isolated Receiver-Output Drive. Tie to ISO RO LED through a resistor for normal operation. (See Table 1 of Figure 2.)
25	B	Inverting Driver Output and Inverting Receiver Input
27, 28	AC2, AC1	Internal Connections; leave these pins unconnected.

Note: See Typical Application Circuit (Figure 2) for DE´ and DI´ pin descriptions.

Complete, Isolated, RS-485/RS-422 Data Interface

Detailed Description

The MAX1480A/MAX1480B are complete, electrically isolated, RS-485/RS-422 data-communications interface solutions. Transceivers, optocouplers, a power driver, and a transformer in one standard 28-pin DIP package provide a complete interface. Signals and power are internally transported across the isolation barrier (Figure 1). Power is transferred from the logic side (non-isolated side) to the isolated side of the barrier through a center-tapped transformer. Signals cross the barrier through high-speed optocouplers. A single +5V supply on the logic side powers both sides of the interface.

The MAX1480B features reduced-slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission at data rates up to 250kbps. The MAX1480A's driver slew rates are not limited, allowing transmission rates up to 2.5Mbps.

These devices typically draw 28mA of no-load supply current. Additionally, the MAX1480B provides a low-power shutdown mode that consumes only 0.2µA, provided DI´ and DE´ are also held high or left floating. Ground SD for normal operation. When high, SD disables the oscillator and both power switches. Pulling DI´ and DE´ high eliminates current draw through the optocouplers.

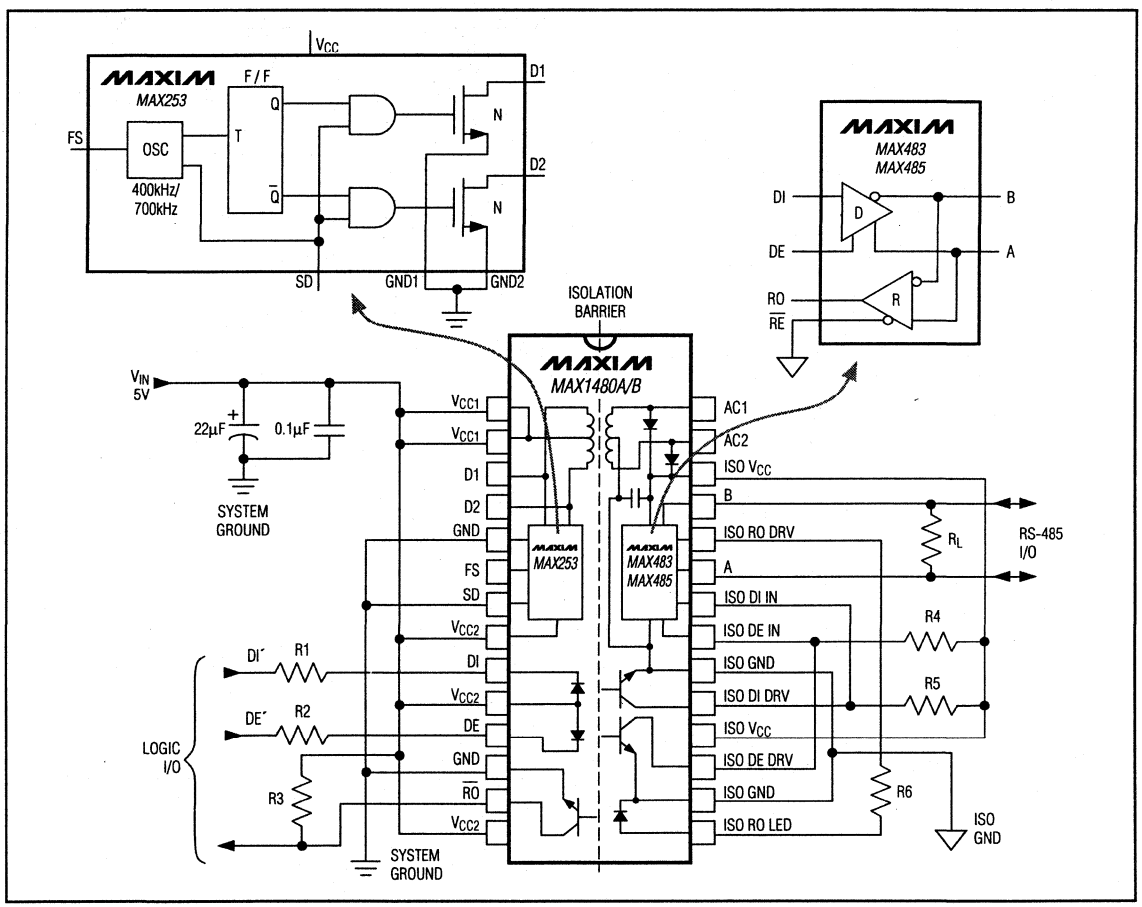


Figure 1. Detailed Block Diagram

To lower the switching frequency, pull FS low; this also increases the devices' operating voltage range from 5V ±5% to 5V ±10%. FS includes a weak pull-up, so it will switch to the high-frequency state if left floating. With FS high or open, no-load supply current is reduced by approximately 4mA and by up to 8mA when fully loaded.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that puts the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The driver outputs are enabled by bringing DE´ high. Driver-enable times are typically 1µs for the MAX1480A and 35µs for the MAX1480B. Allow time for the devices to be enabled before sending data (see the Driver Enable Time vs. Temperature graph in the *Typical Operating Characteristics*). When enabled, driver outputs function as line drivers. Driver outputs are high impedance when DE´ is low. While outputs are high impedance, they function as line receivers.

The MAX1480A/MAX1480B typically withstand 1600V_{RMS} (1 minute) or 2000V_{RMS} (1 second). The isolated outputs of these devices meet all RS-485/RS-422 specifications. The logic inputs can be driven from any TTL/CMOS-logic family with a series resistor, and the received data output can directly drive any of the TTL- or CMOS-logic families with only a resistive pull-up.

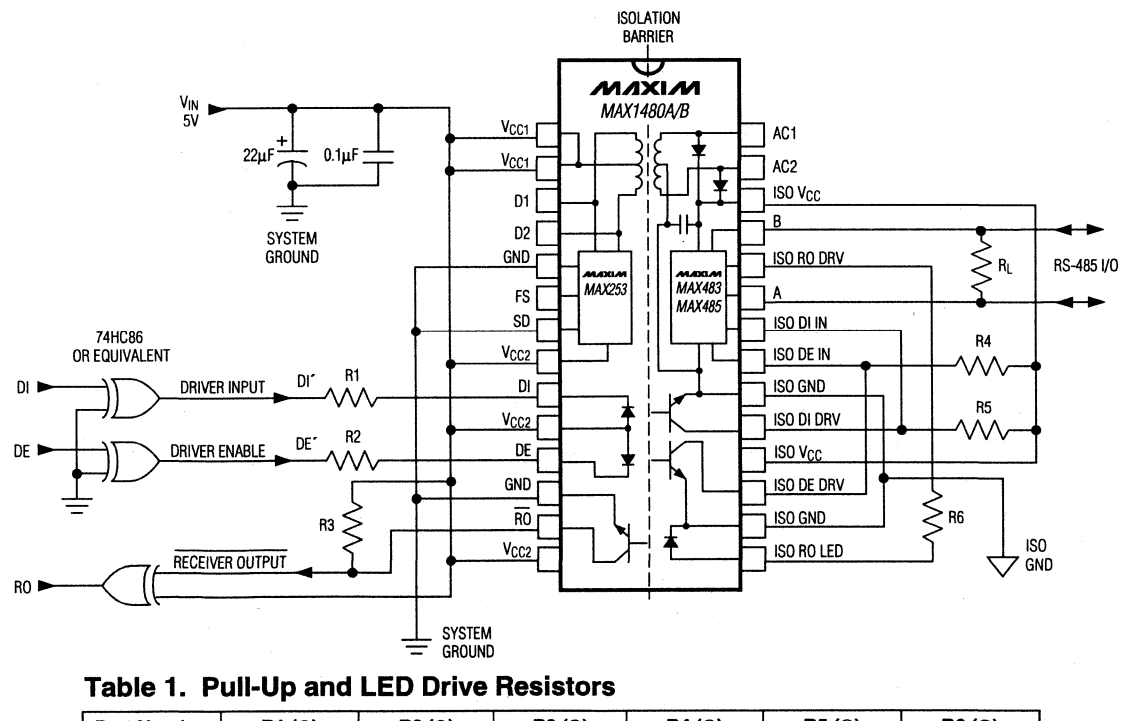


Table 1. Pull-Up and LED Drive Resistors

Part Number	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)
MAX1480A	200	200	360	3k	360	200
MAX1480B	200	510	3k	2.2k	3k	200

Figure 2. Typical Application Circuit

Complete, Isolated, RS-485/RS-422 Data Interface

Test Circuits

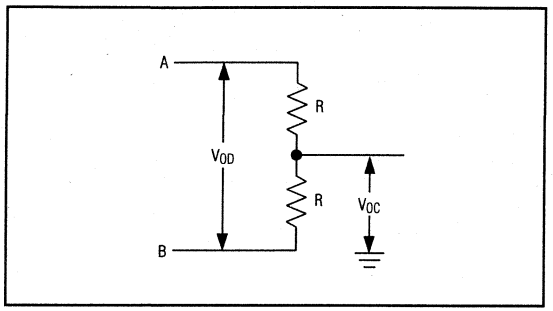


Figure 3. Driver DC Test Load

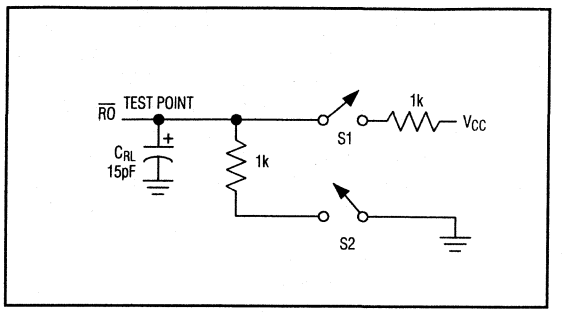


Figure 4. Receiver Timing Test Load

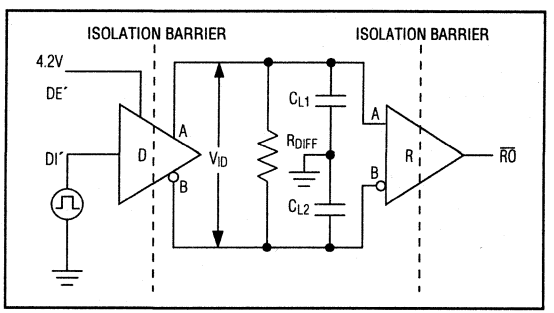


Figure 5. Driver/Receiver Timing Test Circuit

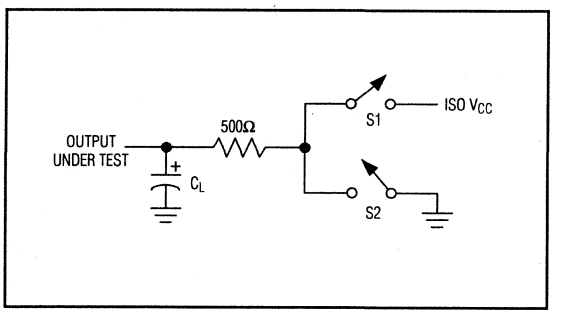


Figure 6. Driver Timing Test Load

Switching Waveforms

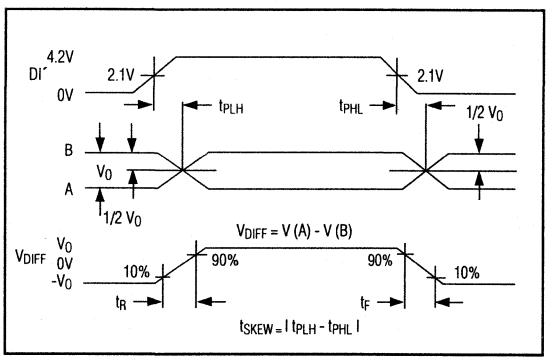


Figure 7. Driver Propagation Delays

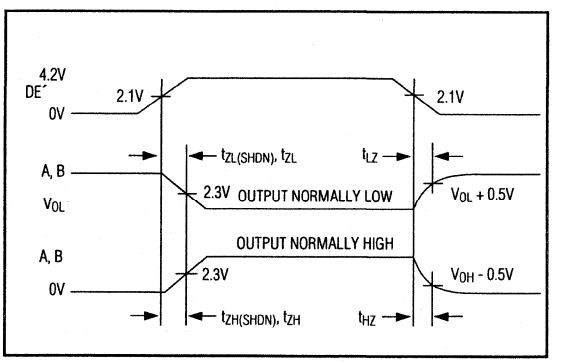


Figure 8. Driver Enable and Disable Times

Switching Waveforms (continued)

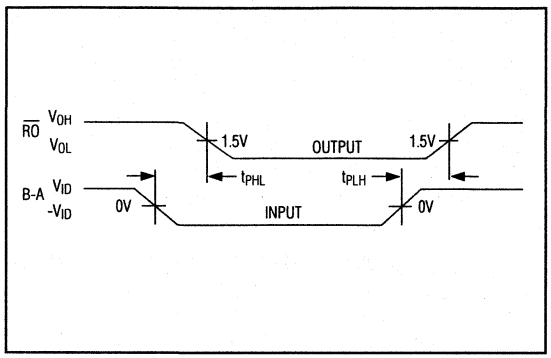


Figure 9. Receiver Propagation Delays

Function Tables

Table 2. Transmitting

INPUTS		OUTPUTS	
DE´	DI´	B	A
1	1	0	1
1	0	1	0
0	X	High-Z	High-Z

X = Don't care
High-Z = High impedance

Table 3. Receiving

INPUTS		OUTPUT
DE´	A-B	$\overline{RO}$
0	≥ +0.2V	1
0	≤ -0.2V	0
0	Inputs open	1

MAX1480B: Reduced EMI and Reflections

The MAX1480B is slew-rate-limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 10 shows the driver-output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX1480A. High-frequency harmonics with larger amplitudes are evident. Figure 11 shows the same information displayed for a MAX1480B transmitting under the same conditions. Figure 11's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

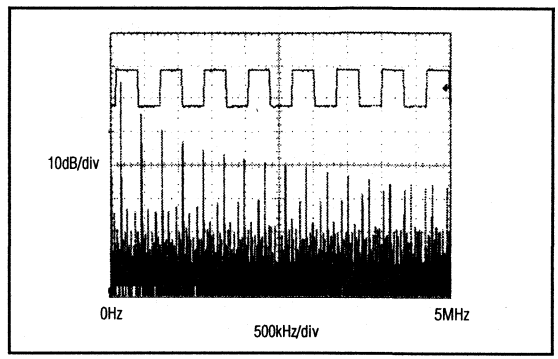


Figure 10. Driver Output Waveform and FFT Plot of MAX1480A Transmitting a 150kHz Signal

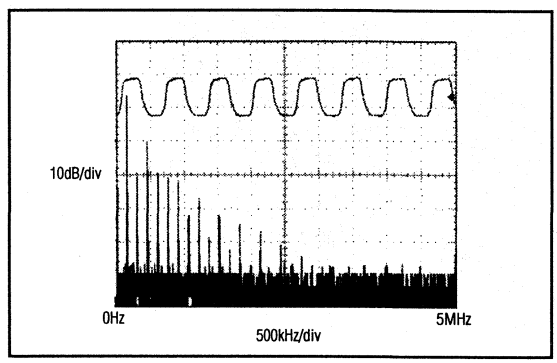


Figure 11. Driver Output Waveform and FFT Plot of MAX1480B Transmitting a 150kHz Signal

Complete, Isolated, RS-485/RS-422 Data Interface

Driver Output Protection

There are two mechanisms to prevent excessive output current and power dissipation caused by faults or by bus contention. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

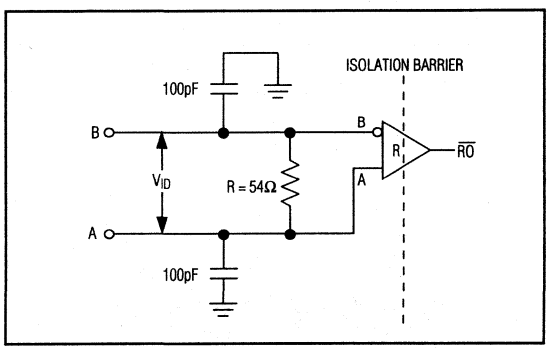


Figure 12. Receiver Propagation-Delay Test Circuit

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation-delay times. Typical propagation delays are shown in Figures 13 and 14, using the test circuit of Figure 12.

The difference in receiver propagation-delay times, $|t_{PLH} - t_{PHL}|$, is typically under 100ns for the MAX1480A and typically less than 1µs for the MAX1480B.

The driver skew times are typically 10ns for the MAX1480A and typically 100ns for the MAX1480B.

Applications Information

The MAX1480A and MAX1480B are designed for bidirectional data communications on multipoint bus-transmission lines. Figure 15 shows a typical network application circuit. To minimize reflections, terminate the line at both ends with its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX1480B is more tolerant of imperfect termination and stubs off the main line.

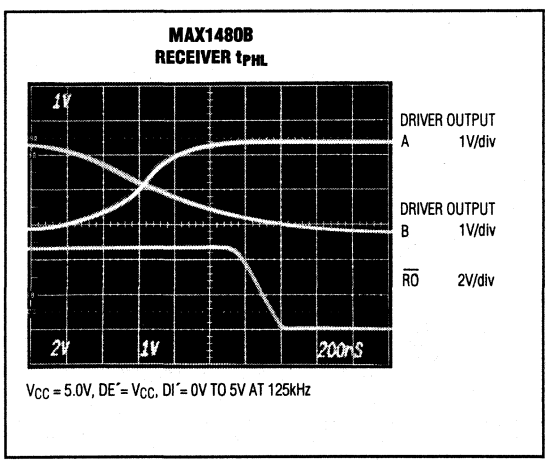


Figure 13. MAX1480B Receiver t_{PHL}

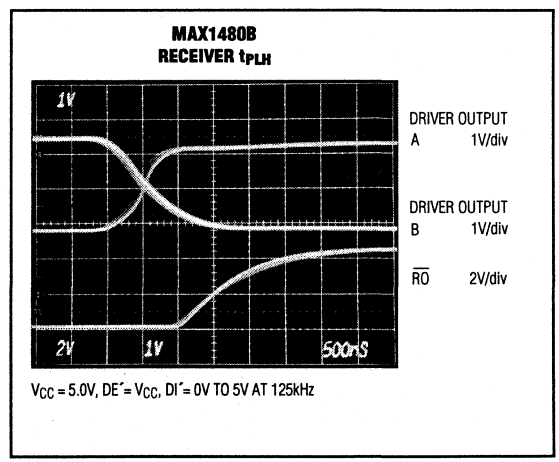


Figure 14. MAX1480B Receiver t_{PLH}

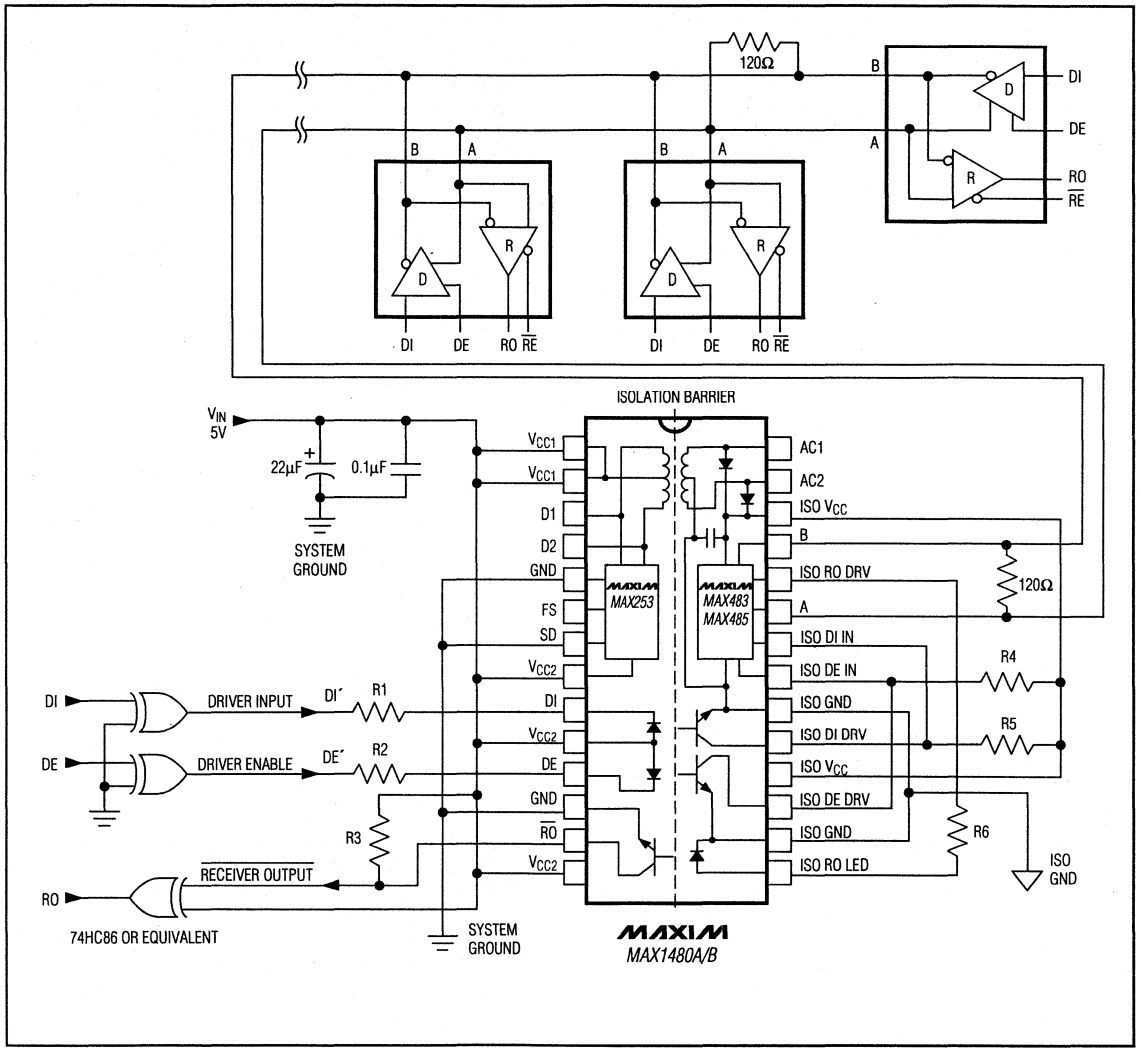


Figure 15. Typical RS-485/RS-422 Network

Complete, Isolated, RS-485/RS-422 Data Interface

Layout Considerations

The MAX1480A/MAX1480B pinouts enable optimal printed circuit board layout by minimizing interconnect lengths and crossovers. Figures 16 and 17 show the preferred layout, which is strongly recommended. You may modify it for individual designs, but always consider the following factors:

- For maximum isolation, the "isolation barrier" should not be breached except by the MAX1480A/MAX1480B. Connections and components from one side should not be located near those of the other side.
- A shield trace connected to the ground on each side of the barrier can help intercept capacitive currents that might otherwise couple into the signal path (Figure 17). In a double-sided or multi-layer board, these shield traces should be present on all conductor layers.
- Try to maximize the width of the isolation barrier wherever possible; a clear space of at least 0.25 inches between ground and isolated ground is suggested.

Pull-Up and LED Drive Resistors

The MAX1480A/MAX1480B are specified and characterized using the resistor values shown in Table 1 of Figure 2. Altering the recommended values can degrade performance.

The DI and DE inputs are the cathodes of LEDs whose anodes are connected to V_{CC}. These points are best driven by a CMOS-logic gate with a series resistor to limit the current. The resistor values shown in Table 1 are recommended when the 74HC86 gate or equivalent is used. These values may need to be adjusted if a driving gate with dissimilar series resistance is used.

The LED forward voltage is approximately 1.5V, so the voltage at DI will be about 3V with the LED on and V_{CC} = 4.5V (worst-case supply voltage). Ideally, 9mA should be allowed to flow under those conditions, so the total resistance to ground must be 3V/9mA = 333Ω. Since a typical HCMOS gate has an output resistance of approximately 120Ω, make R1 = 200Ω the closest standard value to 213Ω.

For the MAX1480A, the DE input is very similar to DI, so R2 is the same as R1. For the MAX1480B, the optimum drive current for the LED used for the DE input is 4.75mA, so R2 must be 3V/4.75mA = 632Ω. Make R2 510Ω to account for the 120Ω typical gate output resistance. Note that the gate outputs driving these LED points should not be used to drive other parts of a logic system. The output voltage will not go completely to ground, due to the IR drop from the LED current.

The value of R6 is similarly found, except the LED's cathode is referred to isolated ground. The LED forward voltage is again about 1.5V, so for an 9mA optimum LED current from a 4.5V source (the isolated V_{CC}), 3V/9mA = 333Ω is needed. The output resistance of ISO RO DRV is about 120Ω, so choose R6 = 200Ω, the closest standard value.

The pull-up resistors R3–R5 were chosen to optimize the devices' data-transfer rates, using the optocoupler specifications.

Network Protection

Many applications will need little, if any, protection from transients on the RS-485 I/O lines; some protection may be needed if the RS-485 bus represents an extended network. The first line of defense should be the four-diode bridge rectifier into zener-diode clamps, as shown in Figures 16 and 17. This will prevent a line transient from pulling A and B outside the receiver common-mode range. These "zener" diodes may be ordinary zener diodes or any of the Transzorb™ or MOV type diodes.

If a prolonged short of an RS-485 I/O line to a power source is possible, 5Ω positive temperature coefficient (PTC) resistors should be used between the MAX1480A/MAX1480B and the network, as shown in Figures 16 and 17. The normal 5Ω resistance will have little effect on the data transmission. In the event of a fault condition, a high current will flow in the diode bridge, causing the PTC resistors to heat up and dramatically increase resistance, effectively isolating the MAX1480A/MAX1480B from the fault.

The MAX1480A/MAX1480B are typically capable of isolating peaks of several thousand volts. Contact the factory if an isolation rating higher than 50V is needed.

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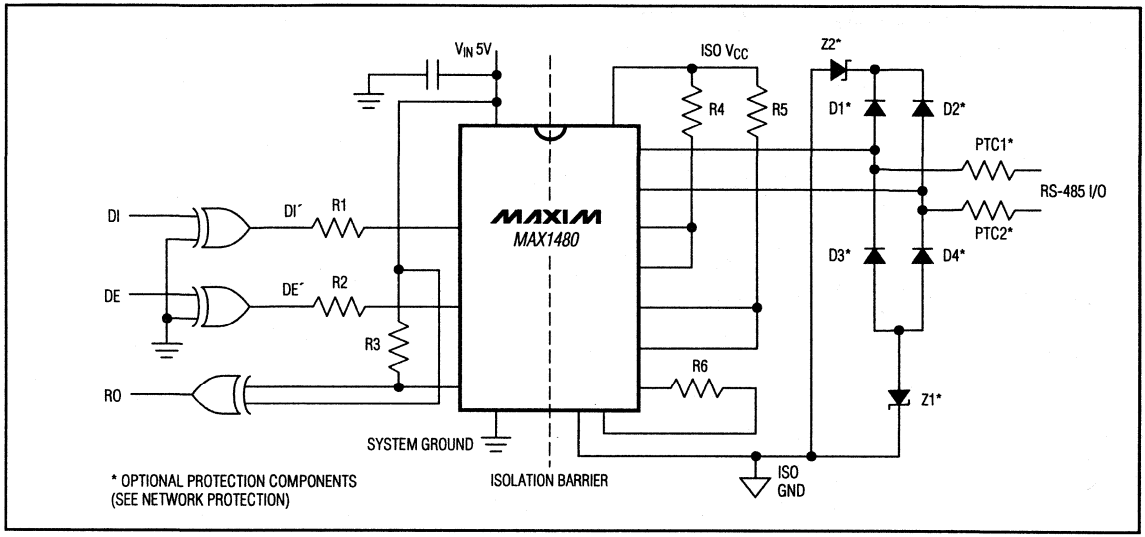


Figure 16. Typical Layout Schematic

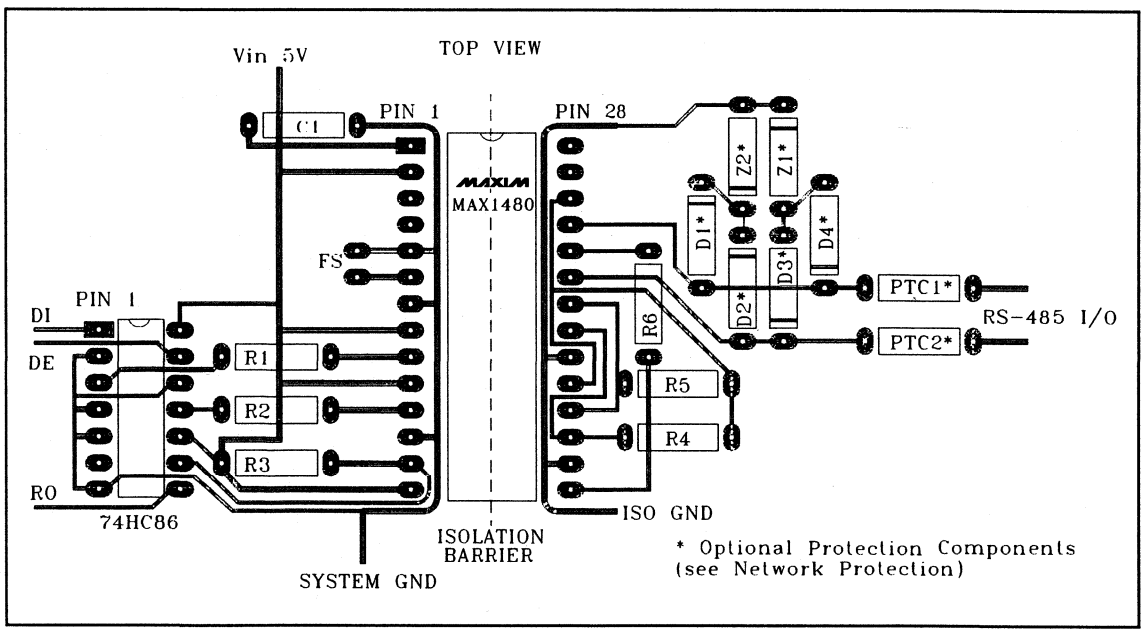
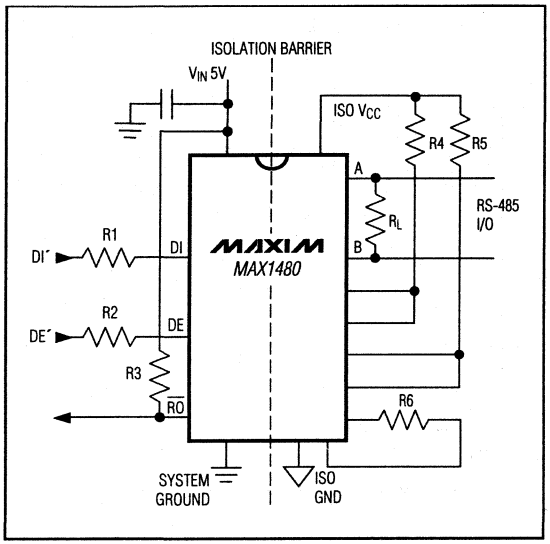


Figure 17. Typical Layout

Complete, Isolated, RS-485/RS-422 Data Interface

Typical Operating Circuit



19-0065; Rev 4; 8/93

MAXIM

+5V RS-232 Transceivers with 0.1µF External Capacitors

General Description

The MAX200-MAX211/MAX213 transceivers are designed for RS-232 and V.28 communication interfaces where ±12V supplies are not available. On-board charge pumps convert the +5V input to the ±10V needed for RS-232 output levels. The MAX201 and MAX209 operate from +5V and +12V, and contain a +12V to -12V charge-pump voltage converter.

The MAX200-MAX211/MAX213 drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at a data rate of 20kbits/sec. The drivers (all except MAX202/MAX203) maintain the ±5V EIA/TIA-232E output signal levels at data rates in excess of 120kbits/sec when loaded in accordance with the EIA/TIA-232E specification.

The 5µW shutdown mode of the MAX200, MAX205, MAX206, and MAX211 conserves energy in battery-powered systems. The MAX213 has an active-low shutdown and an active-high receiver enable control. Two receivers of the MAX213 are active, allowing ring indicator (RI) to be monitored easily using only 75µW power.

The MAX211 and MAX213 are available in a 28-pin wide small-outline (SO) package, and a 28-pin shrink small-outline package (SSOP), which occupies only 40% the area of the SO. The MAX207 is now available in a 24-pin SO package and a 24-pin SSOP. The MAX203 and MAX205 use no external components, and are recommended for applications with limited circuit board space.

Applications

Computers
Laptops, Palmtops, Notebooks
Battery-Powered Equipment
Hand-Held Equipment

Features

Superior to Bipolar:

- **0.1µF to 10µF External Capacitors**
- **120kbits/sec Data Rate (all except MAX202/MAX203)**
- **2 Receivers Active in Shutdown Mode (MAX213)**
- **Small 28-Pin SSOP Package - 40% the Area of SO Package**
- **Low-Power Shutdown Current: 1µA**
- **Designed for RS-232 and V.28 Applications**
- **Three-State TTL/CMOS Receiver Outputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX200CPP	0°C to +70°C	20 Plastic DIP
MAX200CWP	0°C to +70°C	20 Wide SO
MAX200EPP	-40°C to +85°C	20 Plastic DIP
MAX200EWP	-40 °C to +85°C	20 Wide SO
MAX201CPD	0°C to +70°C	14 Plastic DIP
MAX201CWE	0°C to +70°C	16 Wide SO
MAX201C/D	0°C to +70°C	Dice*
MAX201EPD	-40 °C to +85°C	14 Plastic DIP
MAX201EWE	-40 °C to +85°C	16 Wide SO

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Selection Table

Part Number	Power-Supply Voltage (V)	No. of RS-232 Drivers	No. of RS-232 Receivers	No. of Receivers Active in Shutdown	No. of External Capacitors (0.1µF)	Low-Power Shutdown/ TTL Three-State
MAX200	+5	5	0	0	4	Yes/No
MAX201	+5 and +9.0 to +13.2	2	2	0	2	No/No
MAX202	+5	2	2	0	4	No/No
MAX203	+5	2	2	0	None	No/No
MAX204	+5	4	0	0	4	No/No
MAX205	+5	5	5	0	None	Yes/Yes
MAX206	+5	4	3	0	4	Yes/Yes
MAX207	+5	5	3	0	4	No/No
MAX208	+5	4	4	0	4	No/No
MAX209	+5 and +9.0 to +13.2	3	5	0	2	No/Yes
MAX211	+5	4	5	0	4	Yes/Yes
MAX213	+5	4	5	2	4	Yes/Yes

+5V RS-232 Transceivers with 0.1µF External Capacitors

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) .. 889mW
24-Pin Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
24-Pin Wide Plastic DIP (derate 9.09mW/°C above+70°C) 727mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) .. 941mW
24-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
24-Pin CERDIP (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX2_ _C_ _ ..... 0°C to +70°C
MAX2_ _E_ _ ..... -40°C to +85°C
MAX2_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX202/204/206/208/211/213 V_{CC} = 5V ±10%, MAX200/203/205/207 V_{CC} = 5V ±5%, C1–C4 = 0.1µF, MAX201/MAX209 V_{CC} = 5V ±10%, V+ = 9.0V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5	±8		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX202, MAX203		8	15	mA
		MAX200, MAX204-MAX208, MAX211, MAX213		11	20	
		MAX201, MAX209		0.4	1	
V+ Power-Supply Current	No load	MAX201		5	10	mA
		MAX209		7	15	
Shutdown Supply Current	Figure 1, T_A = +25°C	MAX200, MAX205, MAX206, MAX211		1	10	µA
		MAX213		15	50	
Input Logic Threshold Low	T_{IN}, $\overline{EN}$, SHDN, EN, $\overline{SHDN}$				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	$\overline{EN}$, SHDN, EN, $\overline{SHDN}$		2.4			
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
RS-232 Input Voltage Operating Range			-30		+30	V
Receiver Input Threshold Low	V_{CC} = 5V, T_A = +25°C	Active mode	0.8	1.2		V
		Shutdown mode, MAX213, R4, R5	0.6	1.5		
Receiver Input Threshold High	V_{CC} = 5V, T_A = +25°C	Active mode		1.7	2.4	V
		Shutdown mode, MAX213, R4, R5		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	V_{CC} = 5V, T_A = +25°C		3	5	7	kΩ

ELECTRICAL CHARACTERISTICS (continued)

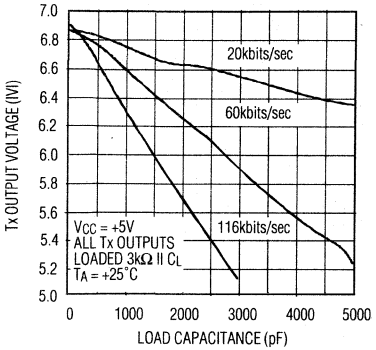
(MAX202/204/206/208/211/213 V_{CC} = 5V ±10%, MAX200/203/205/207 V_{CC} = 5V ±5%, C1–C4 = 0.1µF, MAX201/MAX209 V_{CC} = 5V ±10%, V+ = 9.0V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA (MAX201, MAX202, MAX203), I_{OUT} = 1.6mA (all others)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, EN = 0V, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
Output Enable Time (Figure 2)	MAX205, MAX206, MAX209, MAX211, MAX213			600		ns
Output Disable Time (Figure 2)	MAX205, MAX206, MAX209, MAX211, MAX213			200		ns
Receiver Propagation Delay	MAX213	$\overline{SHDN}$ = 0V, R4, R5		4	40	µs
		$\overline{SHDN}$ = V_{CC}		0.5	10	
	MAX200-MAX211			0.5	10	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Transition Region Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C measured from +3V to -3V or -3V to +3V	MAX200, MAX204-MAX211, MAX213	3	5.5	30	V/µs
		MAX201, MAX202, MAX203		4	30	
RS-232 Output Short-Circuit Current				±10	±60	mA

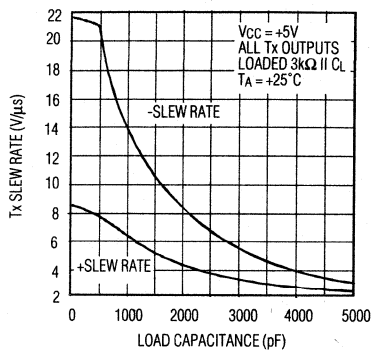
+5V RS-232 Transceivers with 0.1μF External Capacitors

Typical Operating Characteristics

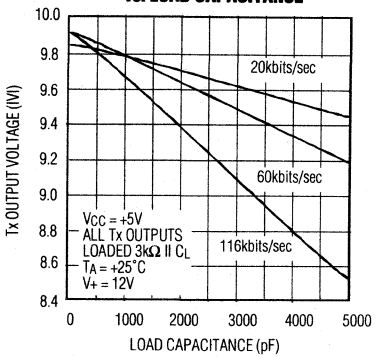
MAX200/204/205/206/207/208/211/213
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



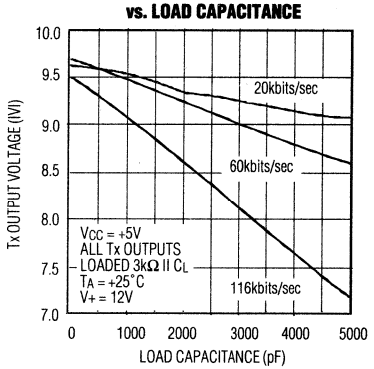
MAX200/204/205/206/207/208/211/213
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



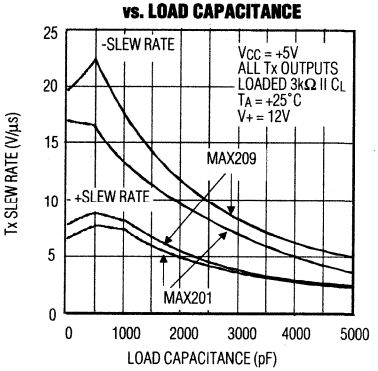
MAX209
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX201
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX201/MAX209
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



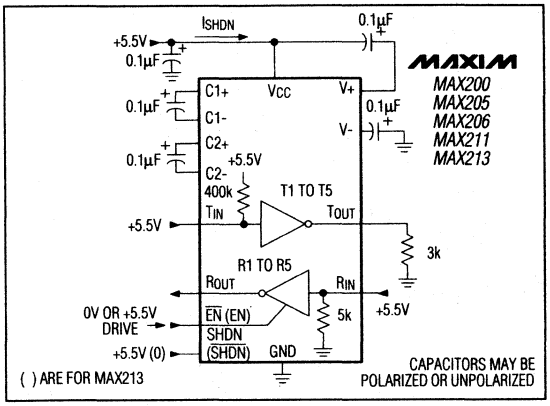


Figure 1. Shutdown Current Test Circuit

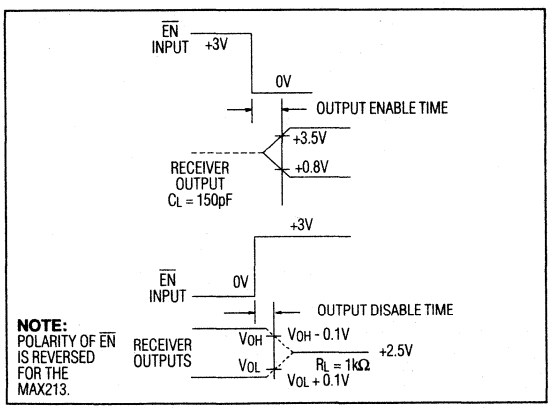


Figure 2. Receiver Output Enable and Disable Timing

Detailed Description

The MAX200–MAX211/MAX213 consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. Each section is described in detail below.

+5V to ±10V Dual Charge-Pump Voltage Converter

+5V to ±10V conversion is performed by two charge-pump voltage converters (Figure 4). The first uses capacitor C1 to double +5V to +10V, storing +10V on the V+ output filter capacitor, C3. The second charge-pump voltage converter uses capacitor C2 to invert +10V to -10V, storing -10V on the V- output filter capacitor, C4.

The MAX201 and MAX209 include only the V+ to V- charge-pump, and are intended for applications that have a VCC = +5V supply and a V+ supply in the +9V to +13.2V range.

In shutdown mode, V+ is internally connected to VCC by a 1kΩ pull-down resistor and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With VCC = 5V, the typical driver-output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet the EIA/TIA-232E and V.28 specifications which call for ±5V minimum output levels under worst-case conditions. These include a minimum 3kΩ load, VCC = 4.5V, and maximum operating temperature. The open-circuit output voltage swing ranges from (V+ - 0.6V) to V-.

Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers can be left unconnected, since 400kΩ pull-up resistors to VCC are included on-

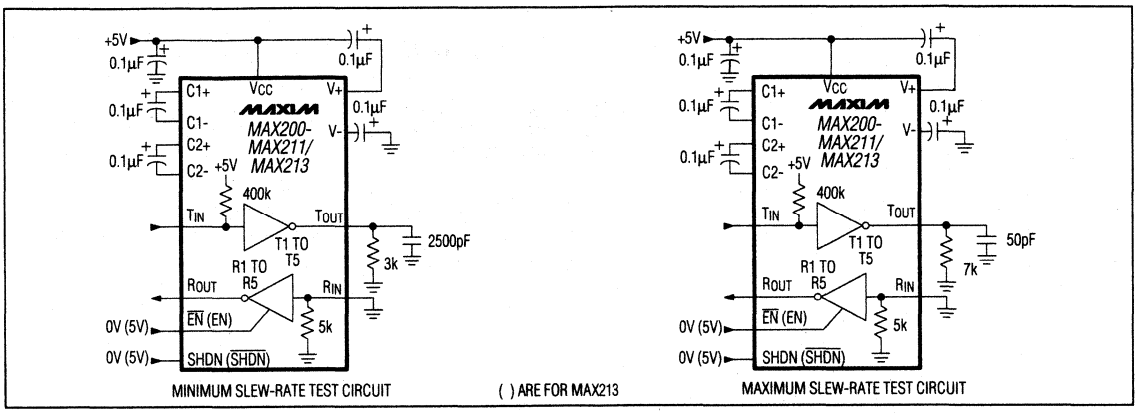


Figure 3. Transition Slew-Rate Test Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

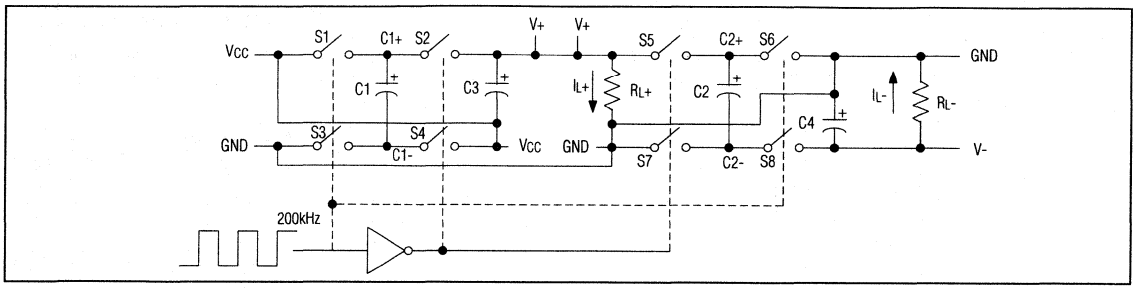


Figure 4. Dual Charge-Pump Diagram

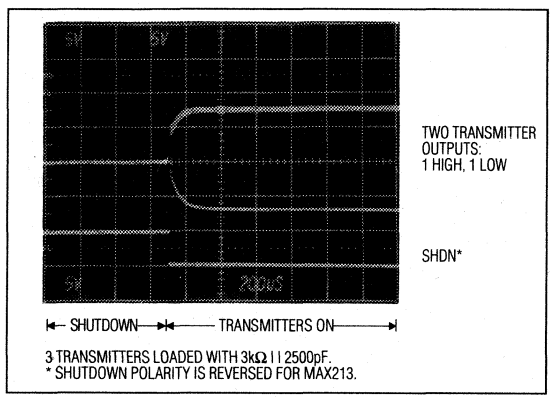


Figure 5. Transmitter Outputs When Exiting Shutdown

chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. The input pull-up resistors typically source 15µA; therefore, the driver inputs should be driven high or open circuited to minimize power-supply current in shutdown mode.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA, even if the transmitter output is backdriven between 0V and (VCC + 6V). Below -0.5V, the transmitter output is diode clamped to ground with a 1kΩ series impedance. The transmitter output is also zener clamped to approximately (VCC + 6V), with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert RS-232 signals to CMOS logic output levels. Receiver outputs are inverting, maintaining compatibility with driver outputs. The guaranteed receiver input thresholds of 0.8V and 2.4V are significantly tighter than the ±3.0V thresholds required by the EIA/TIA-232E specification. This allows receiver inputs to respond to TTL/CMOS logic levels, and improves noise margin for RS-232 levels.

The MAX200–MAX211/MAX213's guaranteed 0.8V threshold (0.6V in shutdown for the MAX213) ensures that receivers shorted to ground will have a logic 1 output. Also, the 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. In shutdown, the MAX213 receivers R4 and R5 have no hysteresis.

Shutdown and Enable Control

In shutdown mode, the MAX200/MAX205/MAX206/MAX211/MAX213 charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213). The time required to exit shutdown is 1ms, as shown in Figure 5.

All receivers except R4 and R5 on the MAX213 are put into a high-impedance state in shutdown mode. The MAX213's R4 and R5 receivers still function in shutdown mode. These two receivers are useful for monitoring external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, so that the receivers can be connected directly to a three-state bus. It has no effect on the RS-232 drivers or on the charge pumps.

MAX213 Receiver Operation in Shutdown

During normal operation, the MAX213's receiver propagation delay is typically 1µs. When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. In shutdown mode, propagation delays increase to 4µs for a high-to-low or a low-to-high transition.

When exiting shutdown, all receiver outputs are invalid until the charge pumps reach nominal values (<2ms when using 0.1µF capacitors).

Table 1a. MAX200 Control Pin Configurations

SHDN	OPERATION STATUS	TRANSMITTERS T1-T5
0	Normal Operation	All Active
1	Shutdown	All High-Z

Table 1b. MAX205/MAX206/MAX211 Control Pin Configurations

SHDN	$\overline{EN}$	OPERATION STATUS	TRANSMITTERS T1-T5	RECEIVERS R1-R5
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	0	Shutdown	All High-Z	All High-Z

Table 1c. MAX213 Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	TRANSMITTERS	RECEIVERS	
			T1-T4	R1-R3	R4, R5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

* Active = active with reduced performance.

+5V RS-232 Transceivers with 0.1µF External Capacitors

Applications Information

Capacitor Selection

The type of capacitor used is not critical for proper operation. Ceramic capacitors are suggested. To ensure proper RS-232 signal levels over temperature when using 0.1µF capacitors, make sure the capacitance value does not degrade excessively as the temperature varies. If in doubt, use capacitors with a larger nominal value. Also observe the capacitors' ESR (effective series resistance) value over temperature, since it will influence the amount of ripple on V+ and V-. To reduce the output impedance at V+ and V-, use larger capacitors (up to 10µF). If polarized capacitors are used, obey the polarities shown in Figure 1 and the Pin Configuration diagrams.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

Figure 5 shows two driver outputs exiting shutdown. As they become active, the two driver outputs are shown going to opposite RS-232 levels (one driver input is high, the other is low). Each driver is loaded with 3kΩ in parallel with 2500pF. The driver outputs display no ringing or undesirable transients as they come out of shutdown.

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitors.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce noise margins.

Power Supplies for MAX201/MAX209

If at power-up, the V+ supply rises after the V_{CC} supply, place a diode (e.g. 1N914) in series with the V+ supply.

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER	CONDITION	EIA/TIA-232E, V.28 SPECIFICATION
Driver Output Voltage 0 Level 1 Level Output Level, Max	 3kΩ to 7kΩ load 3kΩ to 7kΩ load No load	 +5.0V to +15V -5.0V to -15V ±25V
Data Rate	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbits/sec
Receiver Input Voltage 0 Level 1 Level Input Level, Max		 +3.0V to +15V -3.0V to -15V ±25V
Instantaneous Slew Rate, Max	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max		100mA
Transition Rate on Driver Output	V.28	1ms or 3% of the period
	EIA/TIA-232E	4% of the period
Driver Output Resistance	-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIA-232E and V.24 Asynchronous Interfaces

PIN	CONNECTION	
1	Received Line Signal Detector, sometimes called Carrier Detect (DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

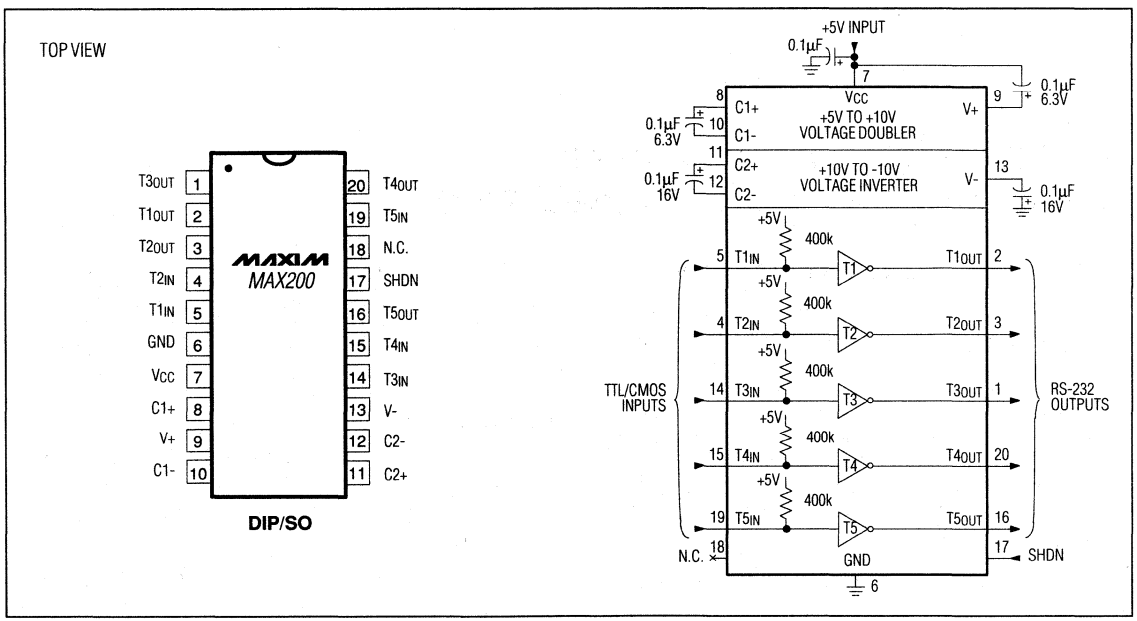


Figure 6. MAX200 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

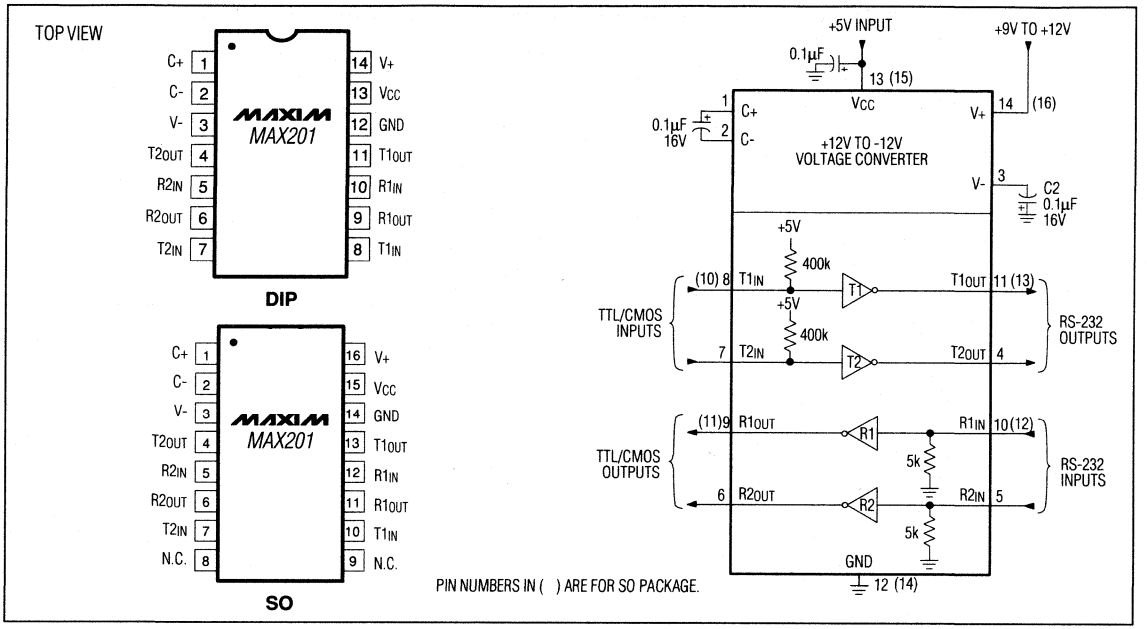


Figure 7. MAX201 Pin Configurations and Typical Operating Circuit

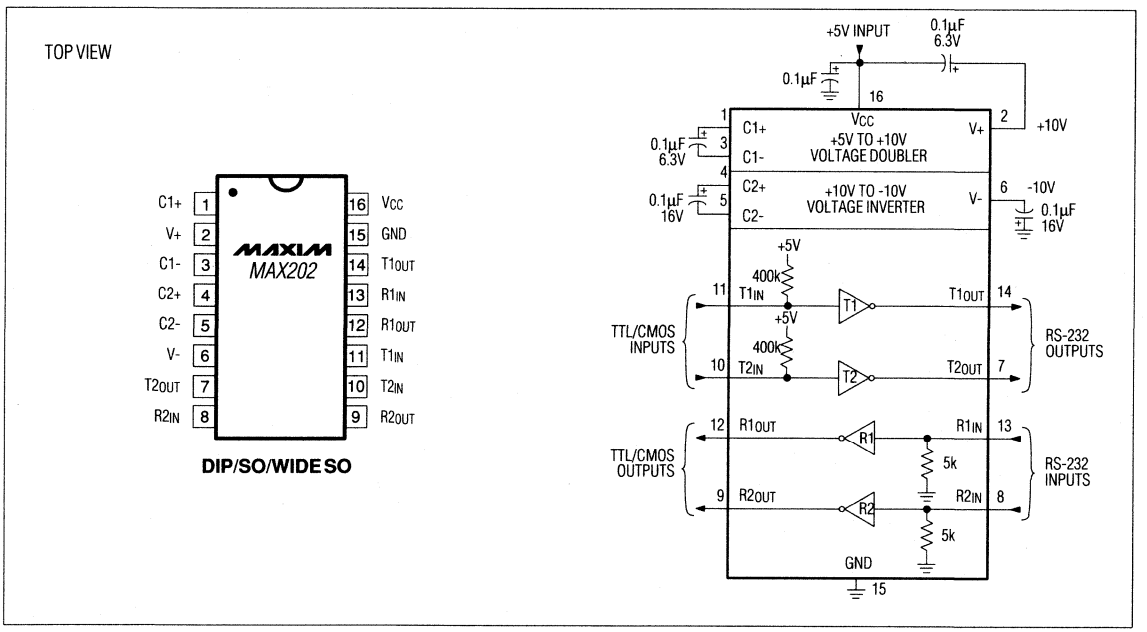


Figure 8. MAX202 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

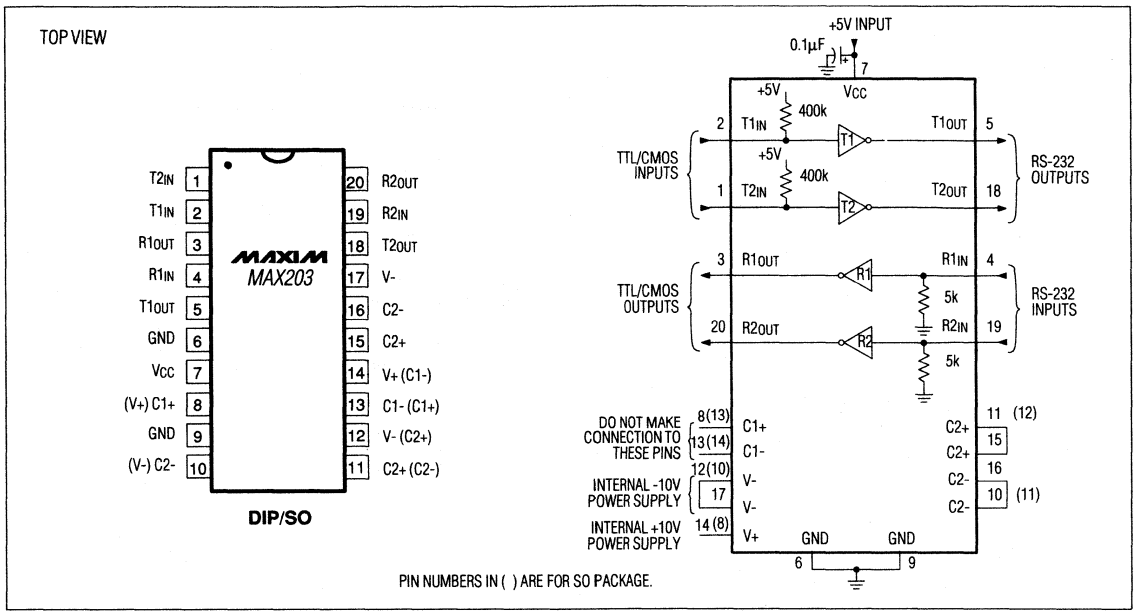


Figure 9. MAX203 Pin Configuration and Typical Operating Circuit

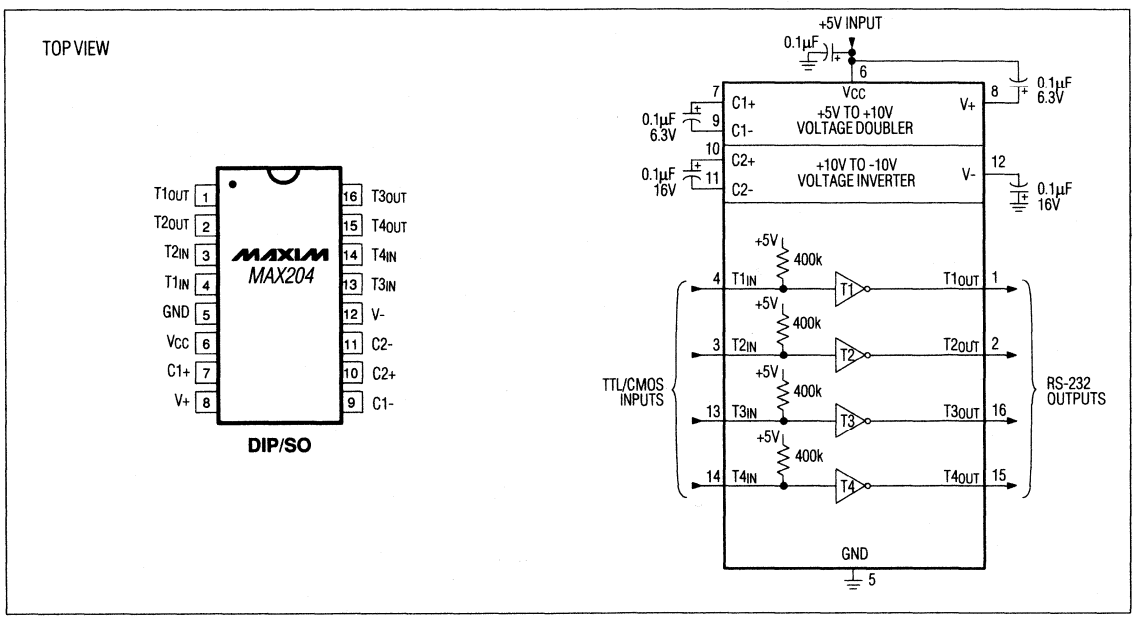


Figure 10. MAX204 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

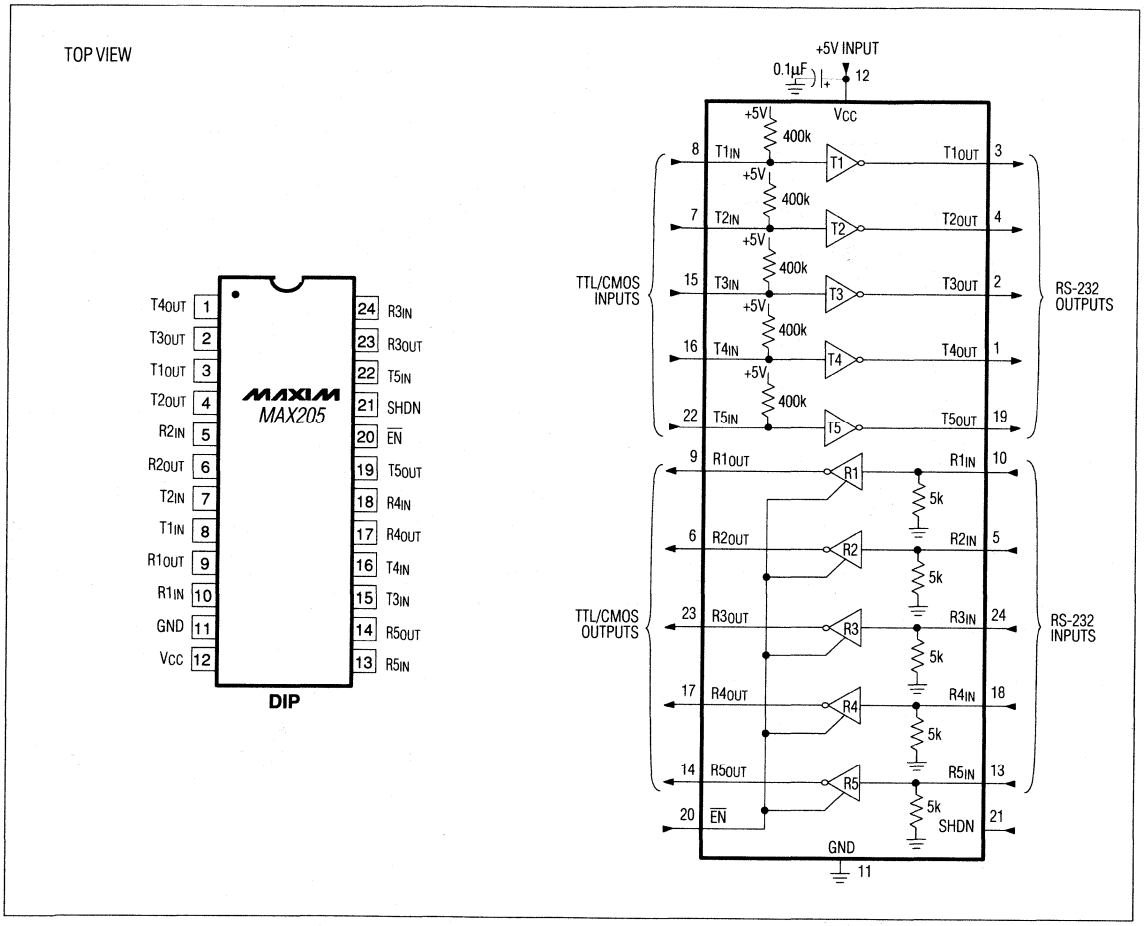


Figure 11. MAX205 Pin Configuration and Typical Operating Circuit

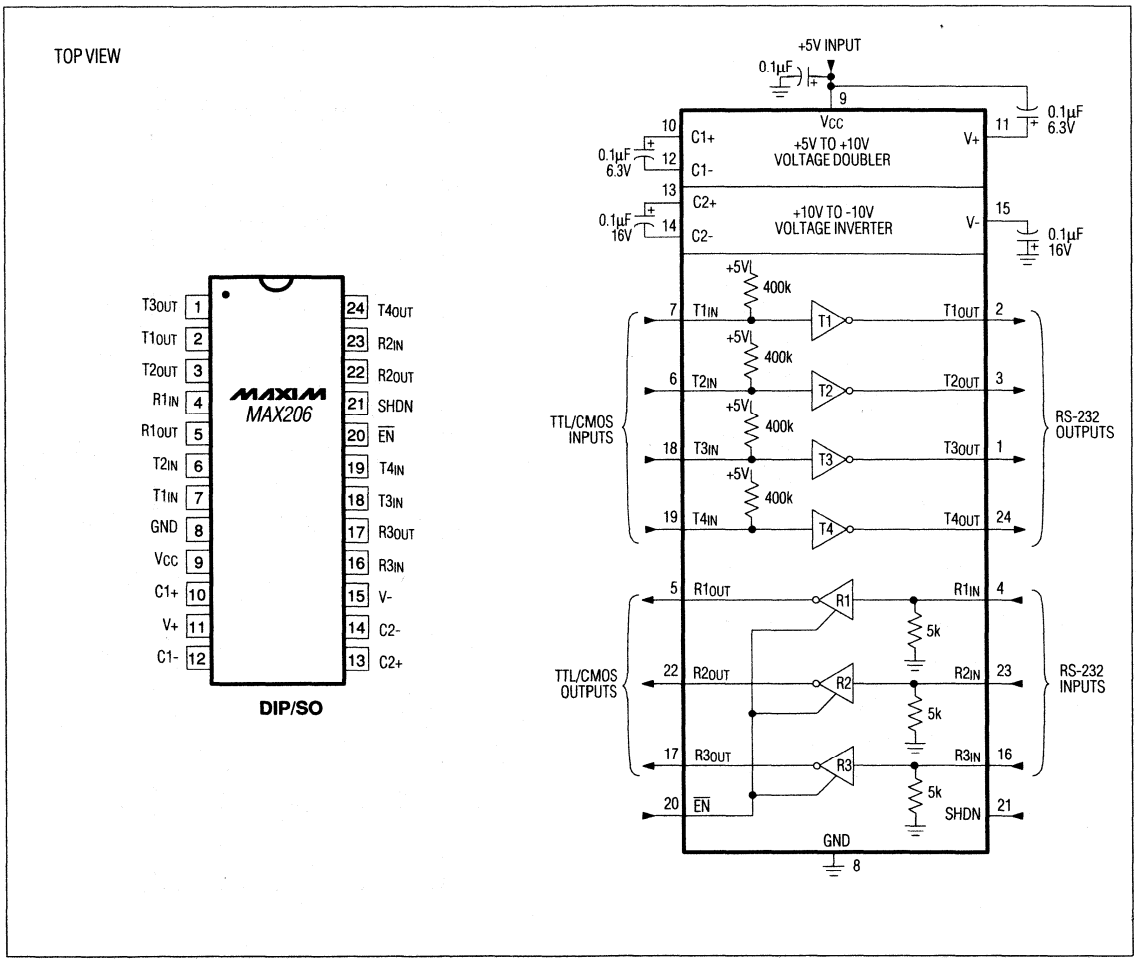


Figure 12. MAX206 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

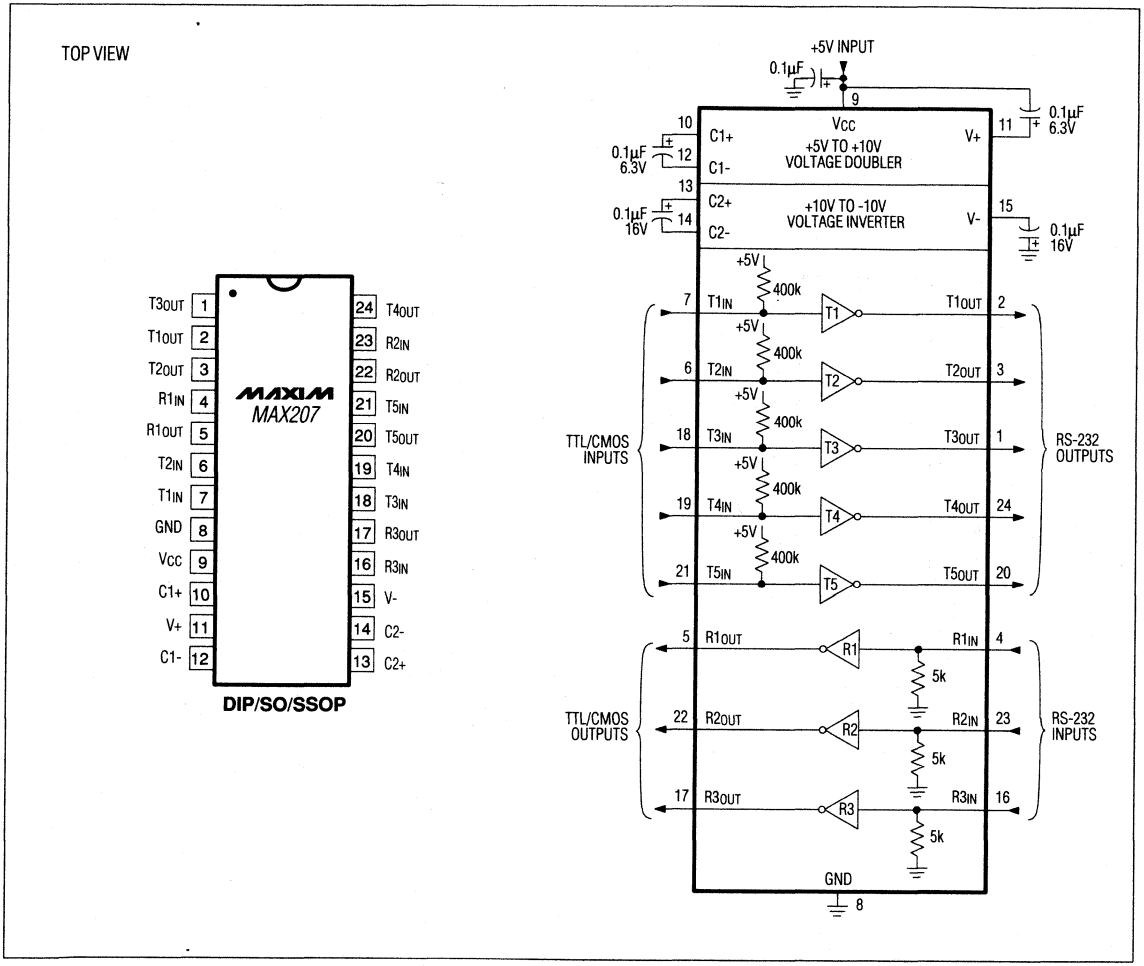


Figure 13. MAX207 Pin Configuration and Typical Operating Circuit

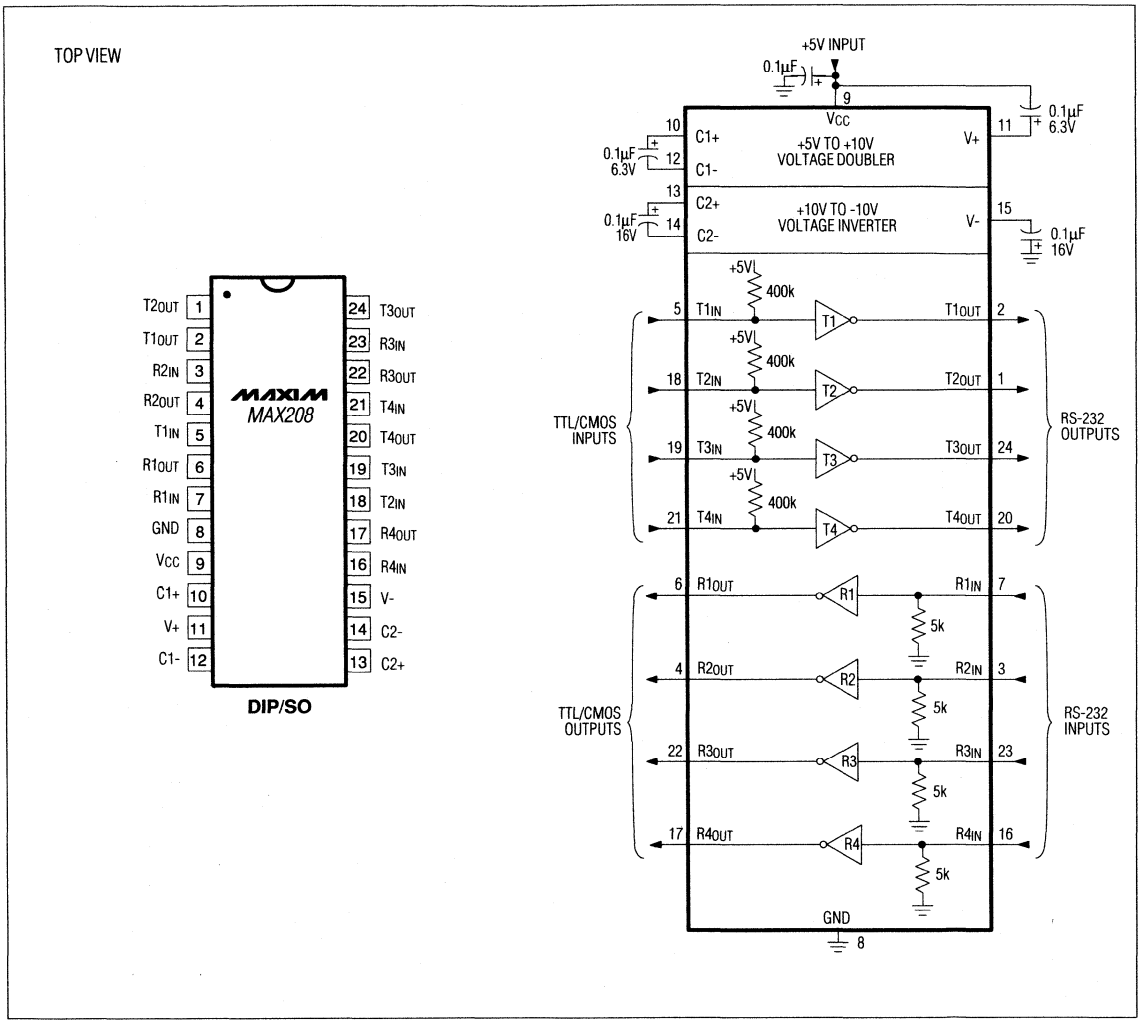


Figure 14. MAX208 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

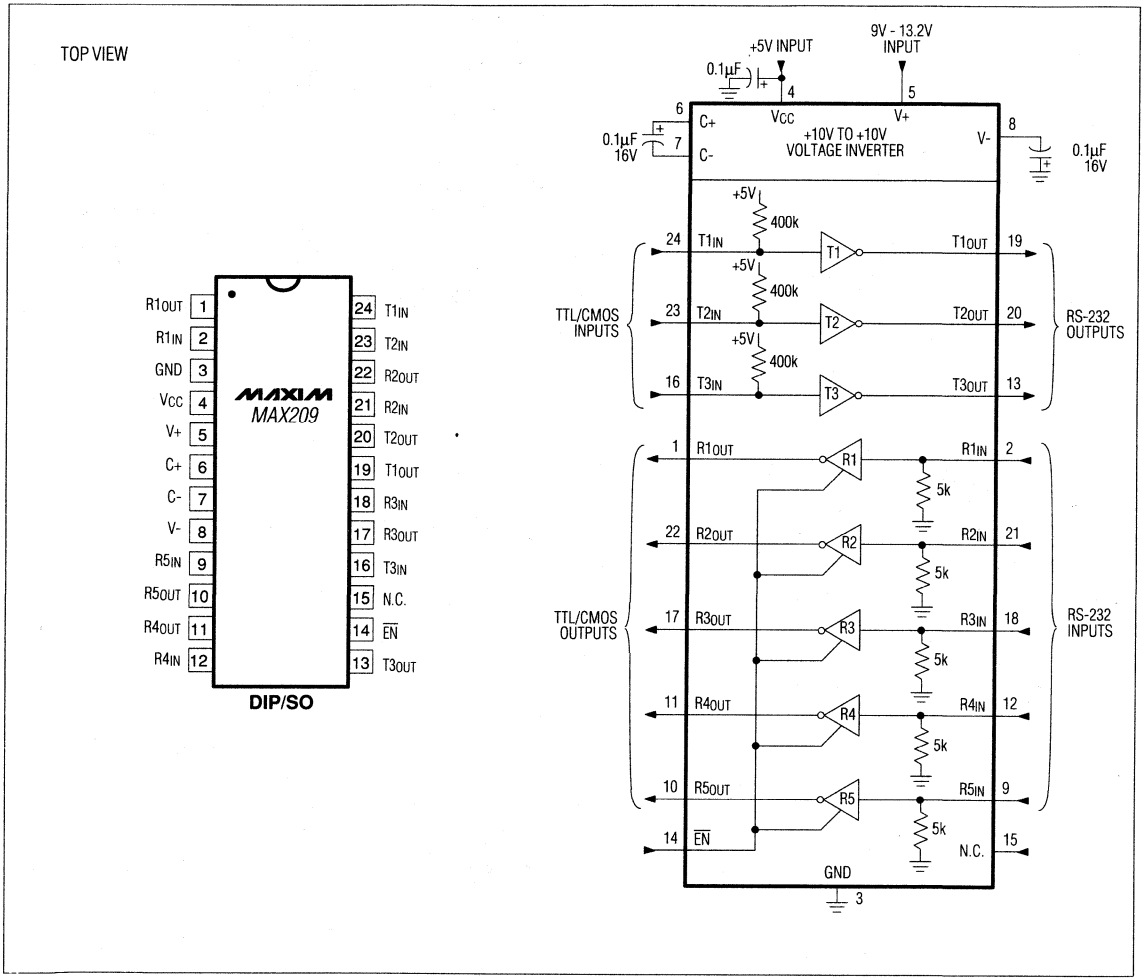


Figure 15. MAX209 Pin Configuration and Typical Operating Circuit

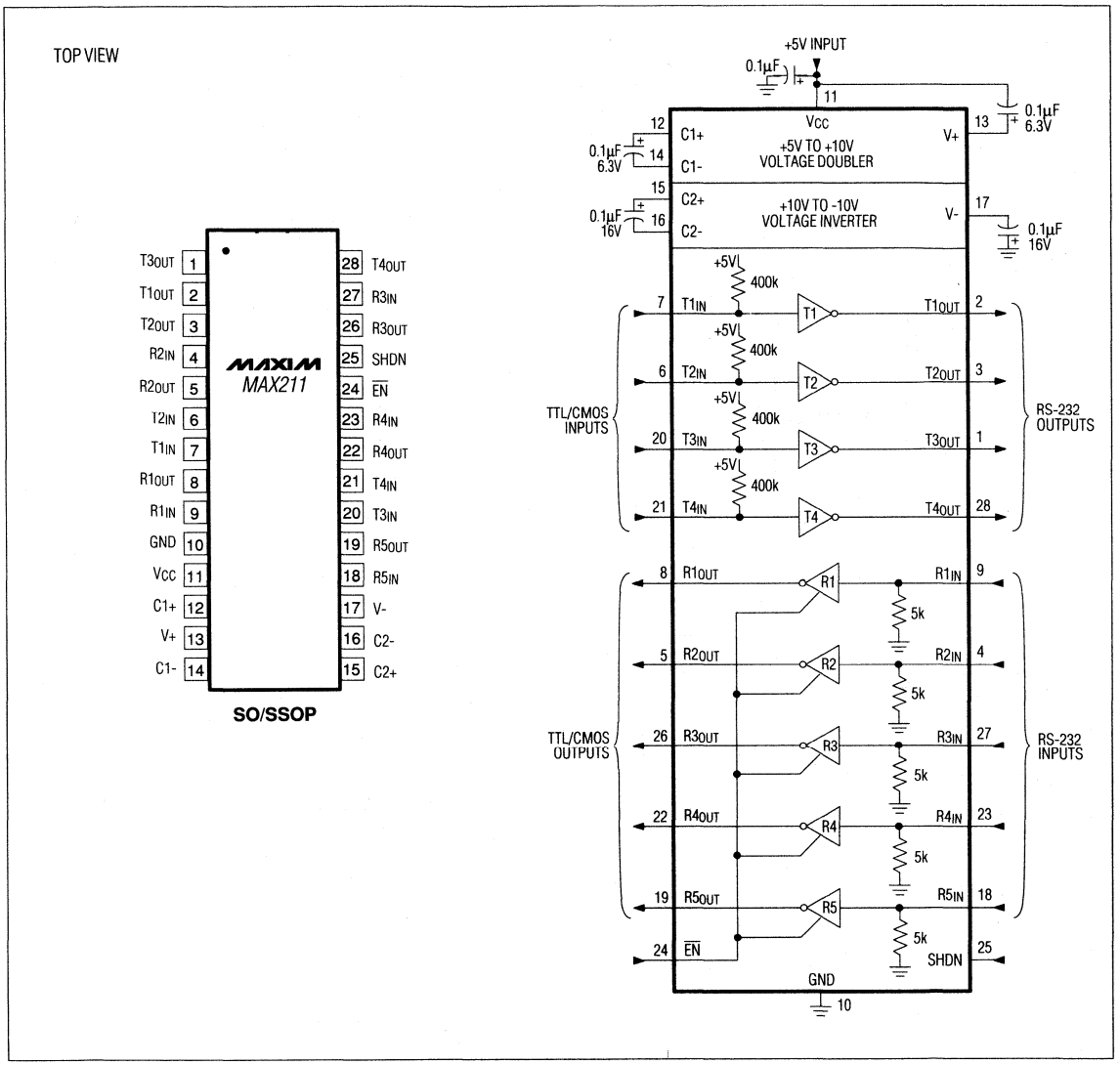
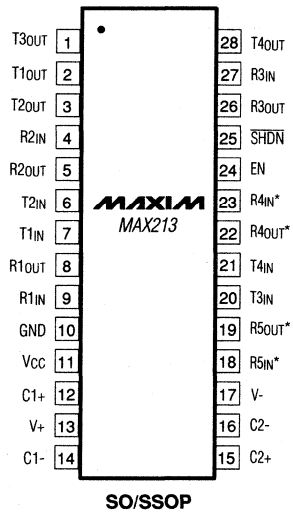


Figure 16. MAX211 Pin Configuration and Typical Operating Circuit

+5V RS-232 Transceivers with 0.1µF External Capacitors

TOP VIEW



SO/SSOP

*ACTIVE IN SHUTDOWN

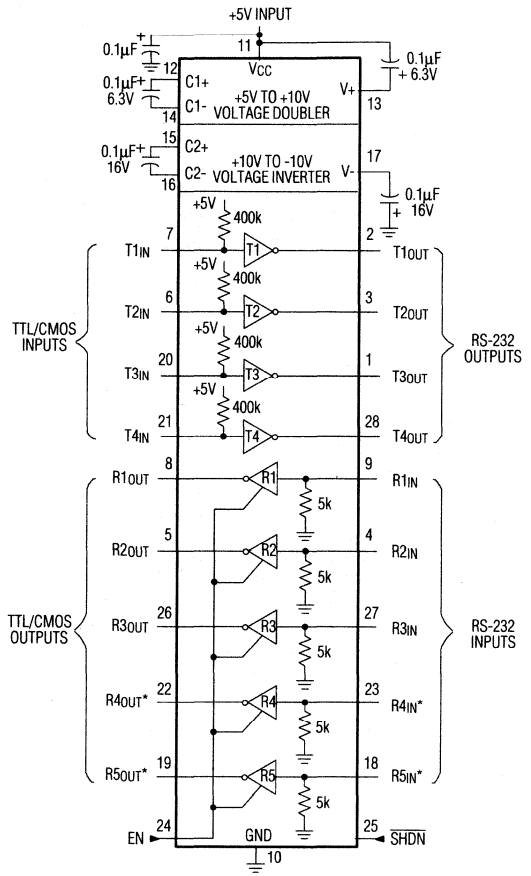


Figure 17. MAX213 Pin Configuration and Typical Operating Circuit

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX202CPE	0°C to +70°C	16 Plastic DIP
MAX202CSE	0°C to +70°C	16 Narrow SO
MAX202CWE	0°C to +70°C	16 Wide SO
MAX202C/D	0°C to +70°C	Dice*
MAX202EPE	-40 °C to +85°C	16 Plastic DIP
MAX202ESE	-40 °C to +85°C	16 Narrow SO
MAX202EWE	-40 °C to +85°C	16 Wide SO
MAX203CPP	0°C to +70°C	20 Plastic DIP
MAX203CWP	0°C to +70°C	20 Wide SO
MAX203EPP	-40°C to +85°C	20 Plastic DIP
MAX203EWP	-40°C to +85°C	20 Wide SO
MAX204CPE	0°C to +70°C	16 Plastic DIP
MAX204CWE	0°C to +70°C	16 Wide SO
MAX204C/D	0°C to +70°C	Dice*
MAX204EPE	-40°C to +85°C	16 Plastic Dip
MAX204EWE	-40°C to +85°C	16 Wide SO
MAX205CPG	0°C to +70°C	24 Wide Plastic DIP
MAX205EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX206CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX206CWG	0°C to +70°C	24 Wide SO
MAX206CAG	0°C to +70°C	24 SSOP
MAX206ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX206EWG	-40°C to +85°C	24 Wide SO
MAX206EAG	-40°C to +85°C	24 SSOP
MAX207CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX207CWG	0°C to +70°C	24 Wide SO
MAX207CAG	0°C to +70°C	24 SSOP
MAX207ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX207EWG	-40°C to +85°C	24 Wide SO
MAX207EAG	-40°C to +85°C	24 SSOP
MAX208CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX208CWG	0°C to +70°C	24 Wide SO
MAX208CAG	0°C to +70°C	24 SSOP
MAX208C/D	0°C to +70°C	Dice*
MAX208ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX208EWG	-40°C to +85°C	24 Wide SO
MAX208EAG	-40°C to +85°C	24 SSOP
MAX209CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX209CWG	0°C to +70°C	24 Wide SO
MAX209C/D	0°C to +70°C	Dice*
MAX209ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX209EWG	-40°C to +85°C	24 Wide SO
MAX211CWI	0°C to +70°C	28 Wide SO
MAX211CAI	0°C to +70°C	28 SSOP
MAX211C/D	0°C to +70°C	Dice*
MAX211EWI	-40°C to +85°C	28 Wide SO
MAX211EAI	-40°C to +85°C	28 SSOP
MAX213CWI	0°C to +70°C	28 Wide SO
MAX213CAI	0°C to +70°C	28 SSOP
MAX213C/D	0°C to +70°C	Dice*
MAX213EWI	-40°C to +85°C	28 Wide SO
MAX213EAI	-40°C to +85°C	28 SSOP

** Contact factory for dice specifications.*

19-0175; Rev 1; 6/94

MAXIM

±15kV ESD-Protected, +5V RS-232 Transceivers

General Description

The MAX202E/MAX232E/MAX211E/MAX213E/MAX241E line drivers/receivers are designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The MAX211E/MAX213E/MAX241E comprise four line drivers and five receivers; they also feature a shutdown mode and a receiver-enable input. The MAX202E and MAX232E have two drivers and two receivers. The drivers and receivers for all five devices meet all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps when loaded in accordance with the EIA/TIA-232E specification.

The MAX211E/MAX213E/MAX241E are available in a 28-pin wide SO package, as well as a 28-pin SSOP package that requires 60% less board space. The MAX202E and MAX232E come in 16-pin narrow SO, wide SO, DIP and CERDIP packages, as well as a 20-pin ceramic LCC package. The MAX232E and MAX241E operate with four 1µF capacitors, while the MAX202E/MAX211E/MAX213E operate with four 0.1µF capacitors, further reducing cost and board space.

Applications

Notebook, Subnotebook and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment

Selection Table

Part Number	No. of RS-232 Drivers	No. of RS-232 Receivers	Receiver Three-State Output Shutdown	External Capacitor Value (µF)	ESD Protection (kV)
MAX202E	2	2	No	No	0.1	±15
MAX211E	4	5	Yes	Yes	0.1	±15
MAX213E	4	5	Yes*	Yes	0.1	±15
MAX232E	2	2	No	No	1.0	±15
MAX241E	4	5	Yes	Yes	1.0	±15

*Two receivers active

™ *LapLink is a registered trademark of Traveling Software, Inc.*

Features

Better than Bipolar!

- **ESD Protection:**
  ±15kV—Human Body Model
  ±8kV—IEC801-2, Contact Discharge
  ±15kV—IEC801-2, Air-Gap Discharge
- **Latchup Free (unlike bipolar equivalents)**
- **2 Drivers, 2 Receivers (MAX202E/232E)**
  4 Drivers, 5 Receivers (MAX211E/213E/241E)
- **Guaranteed 120kbps Data Rate—**
  LapLink™ Compatible
- **Guaranteed 3V/µs Min Slew Rate**
- **Operate from Single +5V Power Supply**

Ordering Information

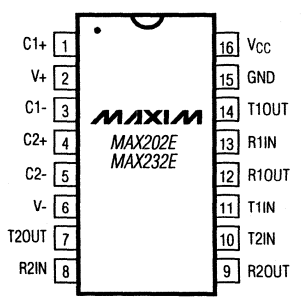
PART	TEMP. RANGE	PIN-PACKAGE
MAX202ECPE	0°C to +70°C	16 Plastic DIP
MAX202ECSE	0°C to +70°C	16 Narrow SO
MAX202ECWE	0°C to +70°C	16 Wide SO
MAX202EC/D	0°C to +70°C	Dice*
MAX202EEPE	-40°C to +85°C	16 Plastic DIP
MAX202EESE	-40°C to +85°C	16 Narrow SO
MAX202EEWE	-40°C to +85°C	16 Wide SO

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C.*

Pin Configurations

TOP VIEW



DIP/SO

Pin Configurations and Typical Operating Circuits continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... -14V to +0.3V
Input Voltages
T_IN ..... -0.3V to (V_{CC} + 0.3V)
R_IN ..... ±30V
Output Voltages
T_OUT ..... (V- - 0.3V) to (V+ + 0.3V)
R_OUT ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_OUT ..... Continuous
Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ..1000mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX2_ _EC_ _ ..... 0°C to +70°C
MAX2_ _EE_ _ ..... -40°C to +85°C
MAX232EM_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C1–C4 = 0.1µF for MAX202E/MAX211E/MAX213E, C1–C4 = 1.0µF for MAX232E/MAX241E, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Operating Voltage Range	V_{CC}			4.5		5.5	V
V_{CC} Supply Current	I_{CC}	No load, T_A = +25°C	MAX202E		8	15	mA
			MAX211E/MAX213E		14	20	
			MAX232E		5	10	
			MAX241E		7	15	
Shutdown Supply Current		T_A = +25°C, Figure 1	MAX211E/MAX241E		1	10	µA
			MAX213E		15	50	
LOGIC							
Input Pull-Up Current		T_IN = 0V (MAX211E/MAX213E/MAX241E)			15	200	µA
Input Leakage Current		T_IN = 0V to V_{CC} (MAX202E/MAX232E)				±10	µA
Input Threshold Low	V_{IL}	T_IN; EN, $\overline{SHDN}$ (MAX213E) or $\overline{EN}$, SHDN (MAX211E/MAX241E)				0.8	V
Input Threshold High	V_{IH}	T_IN		2.0			V
		EN, $\overline{SHDN}$ (MAX213) or $\overline{EN}$, SHDN (MAX211E/MAX241E)		2.4			
Output Voltage Low	V_{OL}	R_OUT; I_{OUT} = 3.2mA (MAX202E/MAX232E) or I_{OUT} = 1.6mA (MAX211E/MAX213E/MAX241E)				0.4	V
Output Voltage High	V_{OH}	R_OUT; I_{OUT} = -1.0mA		3.5	V_{CC} - 0.4		V
Output Leakage Current		0V ≤ R_{OUT} ≤ V_{CC}, MAX211E/MAX213E/MAX241E outputs disabled			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C1–C4 = 0.1µF for MAX202E/MAX211E/MAX213E, C1–C4 = 1.0µF for MAX232E/MAX241E, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

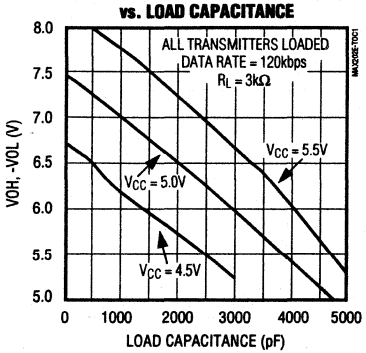
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-232E RECEIVER INPUTS							
Input Voltage Range				-30		+30	V
Input Threshold Low		T_A = +25°C, V_{CC} = 5V	All parts, normal operation	0.8	1.2		V
			MAX213E in shutdown	0.6	1.5		
Input Threshold High		T_A = +25°C, V_{CC} = 5V	All parts, normal operation		1.7	2.4	V
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		1.5	2.4	
Input Hysteresis		V_{CC} = 5V, no hysteresis for the MAX211E/MAX213E/MAX241E in shutdown		0.2	0.5	1.0	V
Input Resistance		T_A = +25°C, V_{CC} =5V		3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS							
Output Voltage Swing		All driver inputs loaded with 3kΩ to ground (Note 1)		±5.0	±9		V
Output Resistance		V_{CC} = V+ =V- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current					±10	±60	mA
TIMING CHARACTERISTICS							
Maximum Data Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF, one transmitter switching		120			kbps
Receiver Propagation Delay	t_{PLHR}, t_{PHLR}	C_L = 150pF	All parts, normal operation		0.5	10	µs
			MAX213E (R4, R5), $\overline{SHDN}$ = 0V, EN = V_{CC}		4	40	
Receiver Output Enable Time		MAX211E/MAX213E/MAX241E, normal operation, Figure 2			600		ns
Receiver Output Disable Time		MAX211E/MAX213E/MAX241E, normal operation, Figure 2			200		ns
Transmitter Propagation Delay	t_{PLHT}, t_{PHLT}	R_L = 3kΩ, C_L = 2500pF, all transmitters loaded			2		µs
Transition-Region Slew Rate		T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from -3V to +3V or +3V to -3V, Figure 3		3	6	30	V/µs

Note 1: MAX211EE_ _ and MAX213EE_ _ tested with V_{CC} = 5V ±5%.

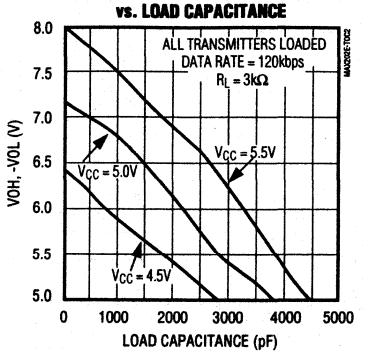
Typical Operating Characteristics

(Typical Operating Circuits, V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

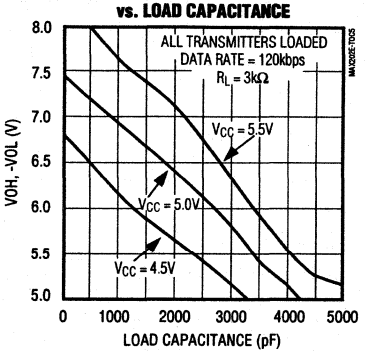
MAX232E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



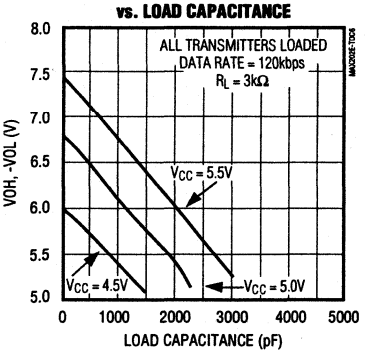
MAX202E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



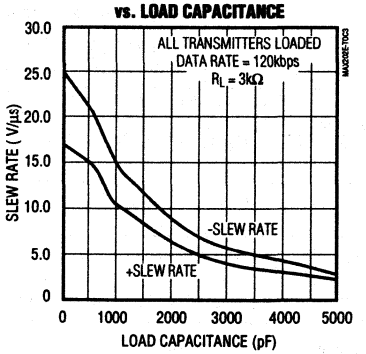
MAX241E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



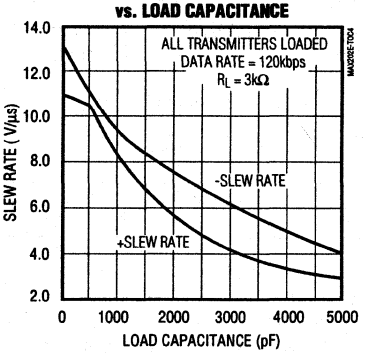
MAX211E/MAX213E
TRANSMITTER OUTPUT VOLTAGE
vs. LOAD CAPACITANCE



MAX211E/MAX213E/MAX241E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



MAX202E/MAX232E
TRANSMITTER SLEW RATE
vs. LOAD CAPACITANCE



Pin Descriptions

MAX202E/MAX232E

PIN		NAME	FUNCTION
DIP/SO	LCC		
1, 3	2, 4	C1+, C1-	Terminals for positive charge-pump capacitor
2	3	V+	+2V_{CC} voltage generated by the charge pump
4, 5	5, 7	C2+, C2-	Terminals for negative charge-pump capacitor
6	8	V-	-2V_{CC} voltage generated by the charge pump
7, 14	9, 18	T_OUT	RS-232 Driver Outputs
8, 13	10, 17	R_IN	RS-232 Receiver Inputs
9, 12	12, 15	R_OUT	RS-232 Receiver Outputs
10, 11	13, 14	T_IN	RS-232 Driver Inputs
15	19	GND	Ground
16	20	V_{CC}	+4.5V to +5.5V Supply Voltage Input
—	1, 6, 11, 16	N.C.	No Connect—not internally connected

MAX211E/MAX213E/MAX241E

PIN	NAME	FUNCTION
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX213E, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX211E and MAX241E, all receivers are inactive in shutdown.
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs. Only the MAX211E, MAX213E, and MAX241E have internal pull-ups to V_{CC}.
10	GND	Ground
11	V_{CC}	+4.5V to +5.5V Supply Voltage
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor
13	V+	+2V_{CC} voltage generated by the charge pump
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor
17	V-	-2V_{CC} voltage generated by the charge pump
24	$\overline{EN}$	Receiver Enable—active low (MAX211E, MAX241E)
	EN	Receiver Enable—active high (MAX213E)
25	SHDN	Shutdown Control—active high (MAX211E, MAX241E)
	$\overline{SHDN}$	Shutdown Control—active low (MAX213E)

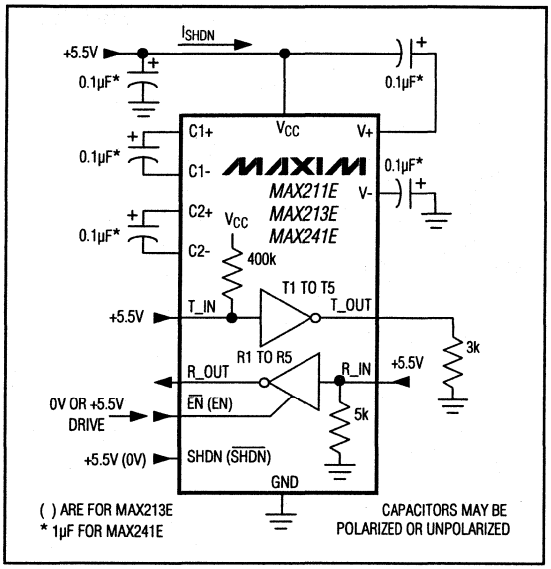


Figure 1. Shutdown-Current Test Circuit (MAX211E/MAX213E/MAX241E)

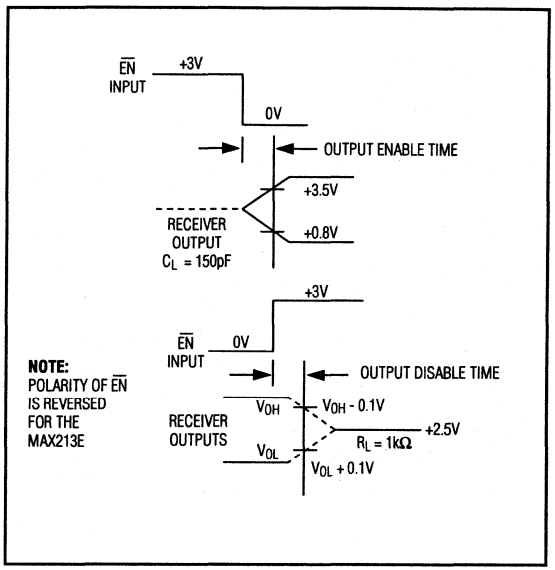


Figure 2. Receiver Output Enable and Disable Timing (MAX211E/MAX213E/MAX241E)

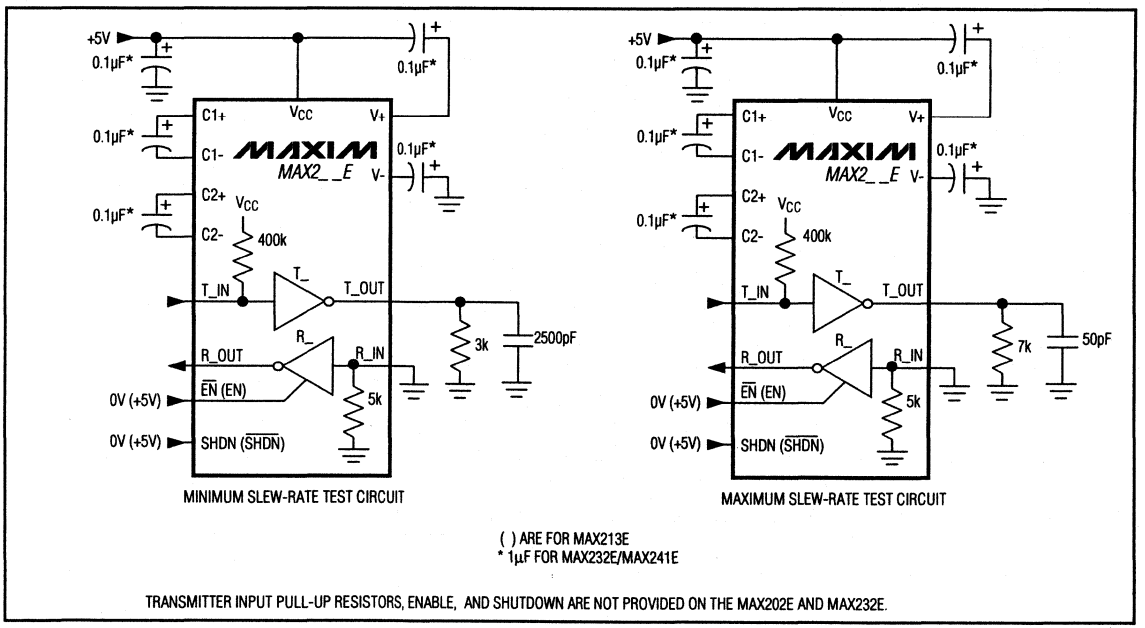


Figure 3. Transition Slew-Rate Circuit

Detailed Description

The MAX202E/MAX232E/MAX211E/MAX213E/MAX241E consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. These E versions of the MAX202, MAX211, MAX213, MAX232 and MAX241 provide extra protection against ESD. They survive ±15kV discharges to the RS-232 inputs and outputs, tested using the Human Body Model. When tested according to IEC801-2, they survive ±8kV contact-discharges and ±15kV air-gap discharges. The rugged MAX202E/MAX211E/MAX213E/MAX232E/MAX241E are intended for use in harsh environments, or applications where the RS-232 connection is frequently changed (such as notebook computers). The standard (non-"E") MAX202, MAX211, MAX213, MAX232 and MAX241 are recommended for applications where cost is critical.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by dual charge-pump voltage converters (Figure 4). The first charge-pump converter uses capacitor C1 to double the +5V into +10V, storing the +10V on the output filter capacitor, C3. The second uses C2 to invert the +10V into -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to V_{CC} by a 1kΩ pull-down resistor and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

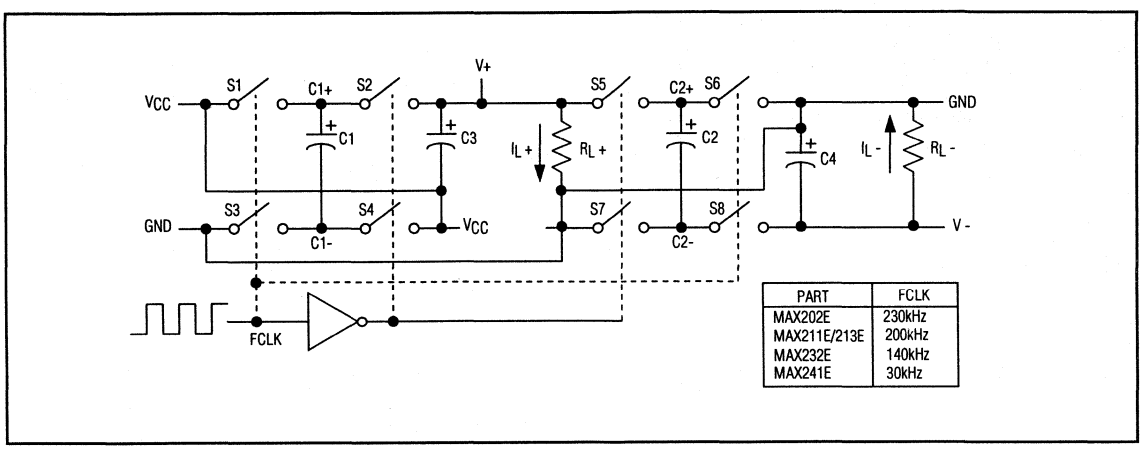
With V_{CC} = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet EIA/TIA-232E and V.28 specifications that call for ±5V minimum output levels under worst-case conditions. These include a 3kΩ load, minimum V_{CC}, and maximum operating temperature. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers on the MAX211E, MAX213E, and MAX241E can be left unconnected because 400kΩ pull-up resistors to V_{CC} are included on-chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. The MAX202E and MAX232E do not have pull-up resistors on the transmitter inputs.

When in low-power shutdown mode, the MAX211E/MAX213E/MAX241E driver outputs are turned off and draw only leakage currents—even if they are back-driven with voltages between 0V and 12V. Below -0.5V in shutdown, the transmitter output is diode-clamped to ground with a 1kΩ series impedance.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic output levels. The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS-logic levels, as well as RS-232 levels.



PART	FCLK
MAX202E	230kHz
MAX211E/213E	200kHz
MAX232E	140kHz
MAX241E	30kHz

Figure 4. Charge-Pump Diagram

The guaranteed 0.8V input low threshold ensures that receivers shorted to ground have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

Receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise- and fall-time signals with moderate amounts of noise and ringing.

In shutdown, the MAX213E's R4 and R5 receivers have no hysteresis.

Shutdown and Enable Control (MAX211E/MAX213E/MAX241E)

In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 1µA (15µA for the MAX213E). The time required to exit shutdown is under 1ms, as shown in Figure 5.

Receivers

All MAX213E receivers, except R4 and R5, are put into a high-impedance state in shutdown mode (see Tables 1a and 1b). The MAX213E's R4 and R5 receivers still function in shutdown mode. These two awake-in-shutdown receivers can monitor external activity while maintaining minimal power consumption.

The enable control is used to put the receiver outputs into a high-impedance state, to allow wire-OR connection of two EIA/TIA-232E ports (or ports of different types) at the UART. It has no effect on the RS-232 drivers or the charge pumps.

Note: The enable control pin is active low for the MAX211E and the MAX241E ($\overline{EN}$) but is active high for the MAX213E (EN). The shutdown control pin is active high for the MAX211E and the MAX241E ($\overline{SHDN}$), but is active low for the MAX213E ($\overline{SHDN}$).

The MAX213E's receiver propagation delay is typically 0.5µs in normal operation. In shutdown mode, propagation delay increases to 4µs for both rising and falling transitions. The MAX213E's receiver inputs have approximately 0.5V hysteresis, except in shutdown when receivers R4 and R5 have no hysteresis.

When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. When coming out of shutdown, all receiver outputs are invalid until the charge pumps reach nominal values (less than 2ms when using 0.1µF capacitors).

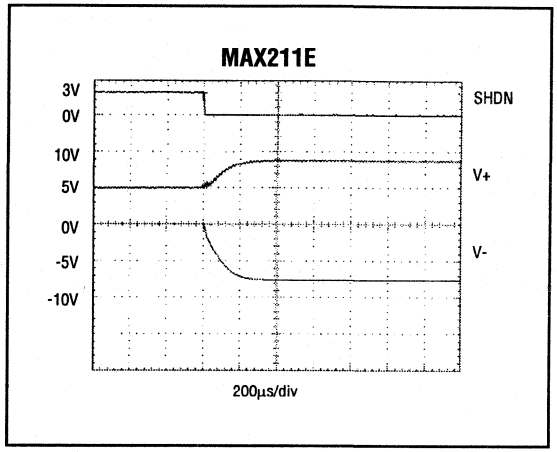


Figure 5. MAX211E V+ and V- when Exiting Shutdown (0.1µF capacitors)

Table 1a. MAX211E/MAX241E Control Pin Configurations

SHDN	$\overline{EN}$	OPERATION STATUS	Tx 1–4	Rx 1–5
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All High-Z
1	X	Shutdown	All High-Z	All High-Z

X = Don't Care

Table 1b. MAX213E Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	Tx 1–4	Rx	
				1–3	4, 5
0	0	Shutdown	All High-Z	High-Z	High-Z
0	1	Shutdown	All High-Z	High-Z	Active*
1	0	Normal Operation	All Active	High-Z	High-Z
1	1	Normal Operation	All Active	Active	Active

**Active = active with reduced performance*

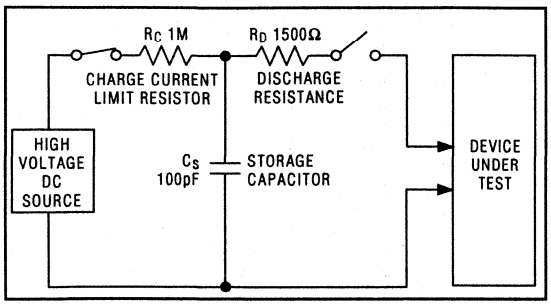


Figure 6a. Human Body ESD Test Model

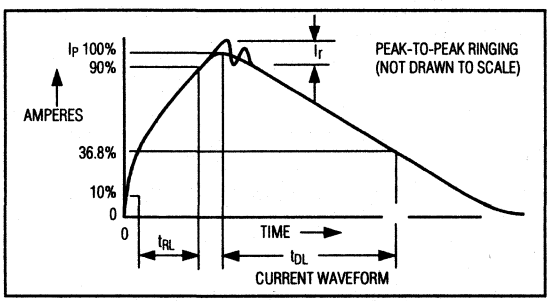


Figure 6b. Human Body Model Current Waveform

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX202E/MAX211E/MAX213E/MAX232E/MAX241E keep working without latchup, whereas competing RS-232 products can latch and must be powered down to remove latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to the following limits:

1) ±15kV using the Human Body Model
2) ±8kV using the contact discharge method specified in IEC801-2
3) ±15kV using IEC801-2's air-gap method.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 6a shows the Human Body Model, and Figure 6b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC801-2

The IEC801-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX202E/MAX211E/MAX213E/MAX232E/MAX241E help you design equipment that meets level 4 (the highest level) of IEC801-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC801-2 is higher peak current in IEC801-2, because series resistance is lower in the IEC801-2 model. Hence, the ESD withstand voltage measured to IEC801-2 is generally lower than that measured using the Human Body Model. Figure 7b shows the current waveform for the 8kV IEC801-2 level-four ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just RS-232 inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX202E, MAX211E and MAX213E require 0.1µF capacitors, and the MAX232E and MAX241E require 1µF capacitors, although in all cases capacitors up to 10µF can be used without harm. Ceramic, aluminum-electrolytic, or tantalum capacitors are suggested for the 1µF capacitors, and ceramic

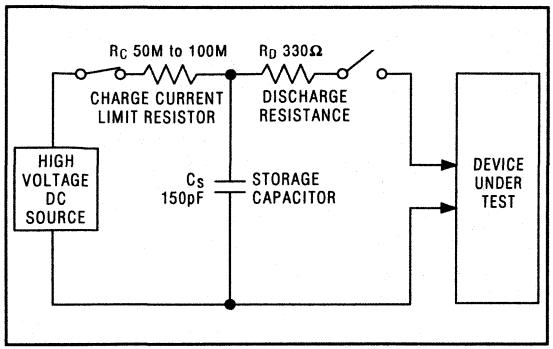


Figure 7a. IEC801-2 ESD Test Model

dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2x) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

To reduce the output impedance at V+ and V-, use larger capacitors (up to 10µF). This can be useful when "stealing" power from V+ or from V-.

Bypass VCC to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple VCC to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce both driver output swing and noise margins. Increasing the value of the charge-pump capacitors (up to 10µF) helps maintain performance when power is drawn from V+ or V-.

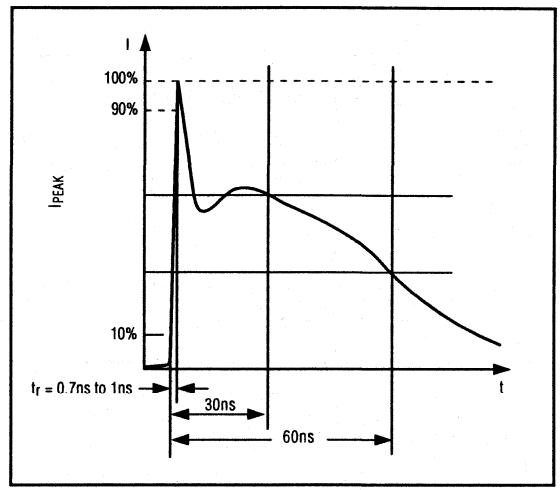


Figure 7b. IEC801-2 ESD Generator Current Waveform

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

The driver outputs display no ringing or undesirable transients as they come out of shutdown.

High Data Rates

These transceivers maintain the RS-232 ±5.0V minimum driver output voltages at data rates of over 120kbps. Communication at these high rates is made easier if the capacitive loads on the transmitters are small; i.e., short cables are best.

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

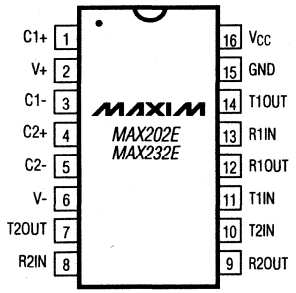
PARAMETER	CONDITION	EIA/TIA-232E, V.28 SPECIFICATION
Driver Output Voltage		
0 Level	3kΩ to 7kΩ load	+5.0V to +15V
1 Level	3kΩ to 7kΩ load	-5.0V to -15V
Output Level, Max	No load	±25V
Data Rate	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbps
Receiver Input Voltage		
0 Level		+3.0V to +15V
1 Level		-3.0V to -15V
Input Level		±25V
Instantaneous Slew Rate, Max	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max		100mA
Transition Rate on Driver Output	V.28	1ms or 3% of the period
	EIA/TIA-232E	4% of the period
Driver Output Resistance	-2V < V_{OUT} < +2V	300Ω

Table 3. DB9 Cable Connections Commonly Used for EIA/TIAE-232E and V.24 Asynchronous Interfaces

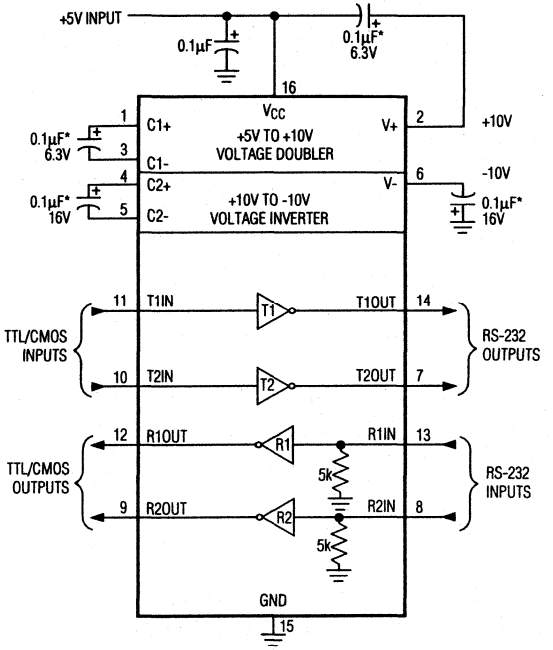
PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

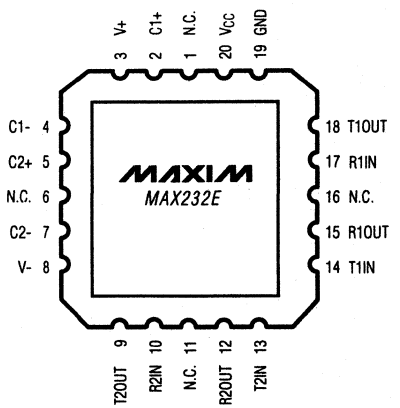
Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



DIP/SO



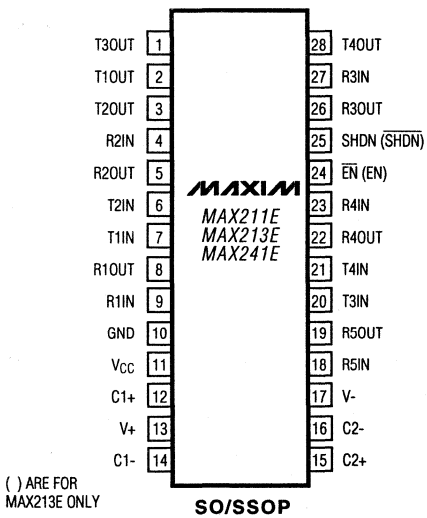


LCC

NOTE: PIN NUMBERS ON TYPICAL OPERATING CIRCUIT REFER TO DIP/SO PACKAGE, NOT LCC.
* 1.0µF CAPACITORS, MAX232E ONLY.

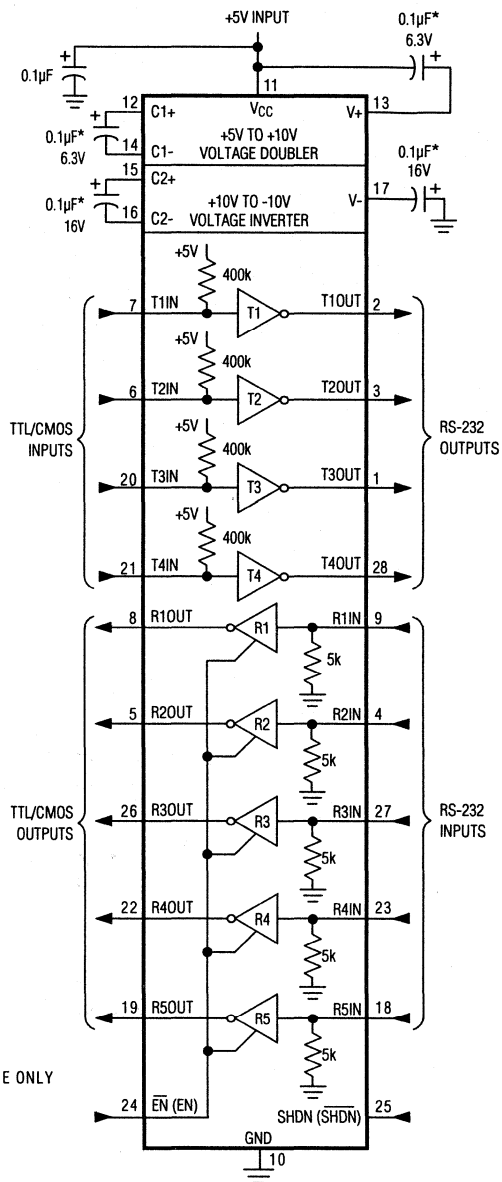
Pin Configurations and Typical Operating Circuits (continued)

TOP VIEW



( ) ARE FOR MAX213E ONLY

SO/SSOP



NOTES:
( ) ARE FOR MAX213E ONLY
* 1.0µF CAPACITORS, MAX241E ONLY

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX211ECWI	0°C to +70°C	28 Wide SO
MAX211ECAI	0°C to +70°C	28 SSOP
MAX211EC/D	0°C to +70°C	Dice*
MAX211EEWI	-40°C to +85°C	28 Wide SO
MAX211EEAI	-40°C to +85°C	28 SSOP
MAX213ECWI	0°C to +70°C	28 Wide SO
MAX213ECAI	0°C to +70°C	28 SSOP
MAX213EC/D	0°C to +70°C	Dice*
MAX213EEWI	-40°C to +85°C	28 Wide SO
MAX213EEAI	-40°C to +85°C	28 SSOP
MAX232ECPE	0°C to +70°C	16 Plastic DIP
MAX232ECSE	0°C to +70°C	16 Narrow SO
MAX232ECWE	0°C to +70°C	16 Wide SO
MAX232EC/D	0°C to +70°C	Dice*
MAX232EEPE	-40°C to +85°C	16 Plastic DIP
MAX232EESE	-40°C to +85°C	16 Narrow SO
MAX232EEWE	-40°C to +85°C	16 Wide SO
MAX232EMLP	-55°C to +125°C	20 LCC
MAX232EMJE	-55°C to +125°C	16 CERDIP
MAX241ECWI	0°C to +70°C	28 Wide SO
MAX241ECAI	0°C to +70°C	28 SSOP
MAX241EC/D	0°C to +70°C	Dice*
MAX241EEWI	-40°C to +85°C	28 Wide SO
MAX241EEAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C.

19-0162; Rev 2; 2/94

EVALUATION KIT AVAILABLE

MAXIM

+3V-Powered, Low-Power, True RS-232 Transceiver

General Description

The MAX212 RS-232 transceiver is intended for 3V-powered EIA/TIA-232E and V.28/V.24 communication interfaces where 3 drivers and 5 receivers are needed with minimum power consumption. The operating voltage range extends from 3.6V down to 3.0V while still maintaining true RS-232 and EIA/TIA-562 voltage levels.

A 1µA typical shutdown mode reduces power consumption, extending battery life in portable systems. While shut down, all receivers can remain active or can be disabled under logic control. This enables a system incorporating the CMOS MAX212 to be in low-power shutdown mode and monitor incoming RS-232 activity.

A guaranteed data rate of 120kbps provides compatibility with popular software for communicating with personal computers.

Three-state drivers on all receiver outputs are provided so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART.

The MAX212 is available in both small-outline (SO) and shrink-small-outline (SSOP) packages. The SSOP package occupies less than half of the board area required by the equivalent SO package.

Applications

Computers
Notebooks/Palmtops/Subnotebooks
Printers
Peripherals
Instruments

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX212CWG	0°C to +70°C	24 Wide SO
MAX212CAG	0°C to +70°C	24 SSOP
MAX212C/D	0°C to +70°C	Dice*
MAX212EWG	-40°C to +85°C	24 Wide SO
MAX212EAG	-40°C to +85°C	24 SSOP

** Dice are tested at T_A = +25°C only.*

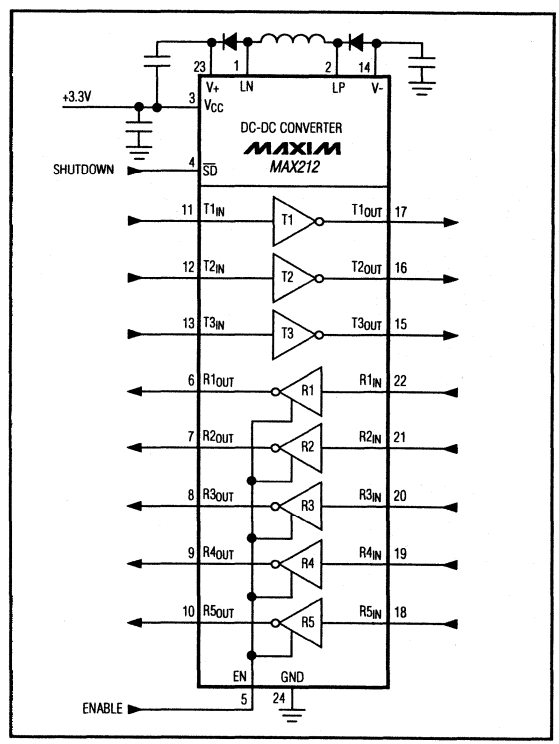
EV KIT	TEMP. RANGE	BOARD TYPE
MAX212EVKIT-SSOP	0°C to +70°C	Surface Mount

Features

SUPERIOR TO BIPOLAR:

- **Operates from Single +3.0V to +3.6V Supply**
- **24-Pin SSOP or Wide SO Packages**
- **Meets All EIA/TIA-232E & EIA/TIA-562 Specifications**
- **3mA Max Supply Current (Unloaded)**
- **1µA Low-Power Shutdown Mode**
- **All Receivers Active During Low-Power Shutdown**
- **Mouse Compatible at 3.0V**
- **Low-Cost, Surface-Mount External Components**
- **120kbps Guaranteed Data Rate—LapLink™ Compatible**
- **Three-State Receiver Outputs**
- **Evaluation Kit Available**
- **Flow-Through Pinout**

Typical Operating Circuit



™LapLink is a registered trademark of Traveling Software.

+3V-Powered, Low-Power, True RS-232 Transceiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{CC} ..... -0.3V to +4.6V
- V+ ..... (V_{CC} - 0.3V) to +7.4V
- V- ..... -7.4V to +2.0V
- LN ..... -0.3V to (V+ + 1.0V)
- LP ..... (V- - 1.0V) to (V+ + 0.3V)

Input Voltages
- T_IN, $\overline{SD}$, EN ..... -0.3V to (V+ + 0.3V)
- R_IN ..... ±25V

Output Voltages
- T_OUT ..... ±15V
- R_OUT ..... -0.3V to (V+ + 0.3V)

Short-Circuit Duration, T_OUT ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
- Wide SO (derate 11.76mW/°C above +70°C) 941mW
- SSOP (derate 8.00mW/°C above +70°C) 640mW

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Operating Voltage Range	Meets or exceeds EIA/TIA-232E specifications	3.0		3.6	V
V_{CC} Supply Current	No load, V_{CC} = 3.3V		1.5	3.0	mA
Shutdown Supply Current	$\overline{SD}$ = EN = GND, R_IN = GND or V_{CC}		1	15	µA
Shutdown Supply Current with Receivers Active	$\overline{SD}$ = GND, EN = V_{CC}, R_IN = GND or V_{CC}		1	15	µA
LOGIC					
Input Logic Threshold Low	T_IN, EN, $\overline{SD}$; V_{CC} = 3.0V to 3.6V			V_{CC} / 3	V
Input Logic Threshold High	T_IN, EN, $\overline{SD}$; V_{CC} = 3.0V to 3.6V	2V_{CC} / 3			V
Input Current High	T_IN, EN, $\overline{SD}$; V_{IN} = V_{CC}			1	µA
Input Current Low	T_IN, EN, $\overline{SD}$, V_{IN} = GND			1	µA
Hysteresis	T_IN; V_{CC} = 3.3V		0.3		V
Logic Output Voltage Low	I_{OUT} = 1.0mA			0.25	V
Logic Output Voltage High	I_{OUT} = -1.0mA	V_{CC} - 0.5			V
Logic Output Leakage Current	EN = GND, 0V < R_OUT < V_{CC}			±10	µA
EIA/TIA-232E RECEIVERS					
EIA/TIA-232E Input Voltage Operating Range		-25		+25	V
EIA/TIA-232E Input Voltage Threshold Low		0.4			V
EIA/TIA-232E Input Voltage Threshold High				2.8	V
EIA/TIA-232E Input Hysteresis			0.7		V
EIA/TIA-232E Input Resistance	-15V < V_{IN} < 15V	3	5	7	kΩ
EIA/TIA-232E TRANSMITTERS					
Output Voltage Swing (V_{HIGH}, V_{LOW})	All transmitters loaded 3kΩ to GND	±5.0	±5.5		V
Output Resistance	V_{CC} = V- = V+ = 0V, -2V < T_OUT < 2V	300			Ω
EIA/TIA-232E Short-Circuit Current			28	100	mA

TIMING CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

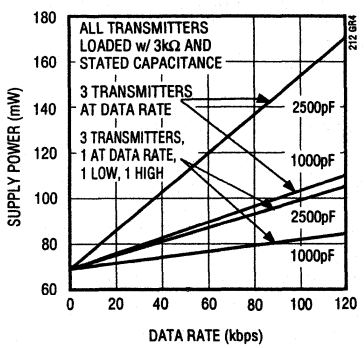
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		1000pF || 3kΩ load on each transmitter, 150pF load on each receiver	120	250		kbps
Receiver Output Enable Time	t_{ER}			70	200	ns
Receiver Output Disable Time	t_{DR}			420	700	ns
Transmitter Output Enable Time	t_{ET}	Includes power-supply start-up		250		µs
Transmitter Output Disable Time	t_{DT}			600		ns
Receiver Propagation Delay	t_{PHLR}	150pF load		300	700	ns
	t_{PLHR}			300	700	
Transmitter Propagation Delay	t_{PHLT}	2500pF || 3kΩ load		800	2000	ns
	t_{PLHT}			800	2000	
Transition-Region Slew Rate		R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V	4.0	10	30	V/µs

2

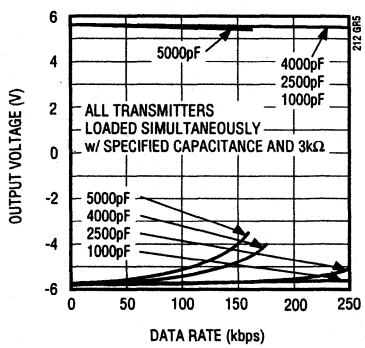
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

SUPPLY POWER vs. DATA RATE



TRANSMITTER OUTPUT VOLTAGE vs. DATA RATE

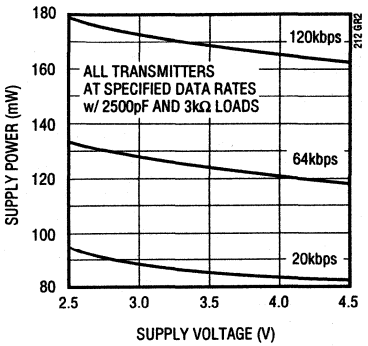


+3V-Powered, Low-Power, True RS-232 Transceiver

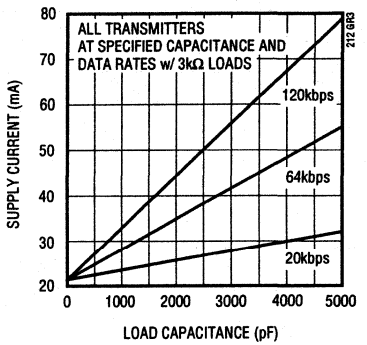
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

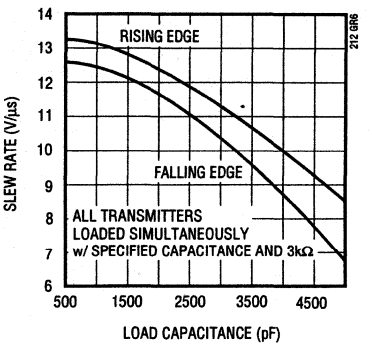
SUPPLY POWER vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. LOAD CAPACITANCE



SLEW RATE vs. LOAD CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	LN	Inductor/Diode Connection Point
2	LP	Inductor/Diode Connection Point
3	V_{CC}	Supply Voltage Input, 3.0V to 3.6V
4	$\overline{SD}$	Shutdown Control. Connect to V_{CC} for normal operation. Connect to GND to shut down the power supply and to disable the drivers. Receiver status is not changed by this control.
5	EN	Receiver Enable Control. Connect to V_{CC} for normal operation. Connect to GND to force the receiver outputs into a high-Z state.
6-10	$R1_{OUT}$-$R5_{OUT}$	Receiver Outputs, swing GND to V_{CC}
11-13	$T1_{IN}$-$T3_{IN}$	Transmitter Inputs
14	V-	Negative Supply generated on-board
15-17	$T3_{OUT}$-$T1_{OUT}$	Transmitter Outputs
18-22	$R5_{IN}$-$R1_{IN}$	Receiver Inputs
23	V+	Positive Supply generated on-board
24	GND	Ground

Detailed Description

The MAX212 line driver/receiver is intended for 3V-powered EIA/TIA-232E and V.28/V.24 communications interfaces where 3 drivers and 5 receivers are required. The operating voltage range extends from 3.6V down to 3.0V while still maintaining true RS-232 and EIA/TIA-562 transmitter output voltage levels.

The circuit comprises three sections: power supply, transmitters, and receivers. The power-supply section converts the supplied 3V to about ±6.5V, to provide the voltages necessary for the drivers to meet true RS-232 levels. External components are small and inexpensive.

The transmitters and receivers are guaranteed to operate at data rates of 120kbps.

A shutdown mode reduces current to 1µA to extend battery life in portable systems. While shut down, all receivers can remain active or can be disabled under logic control. This enables a system incorporating the MAX212 to be in low-power shutdown mode and still monitor incoming RS-232 activity.

Three-state drivers on all receiver outputs are provided so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART.

+3V-Powered, Low-Power, True RS-232 Transceiver

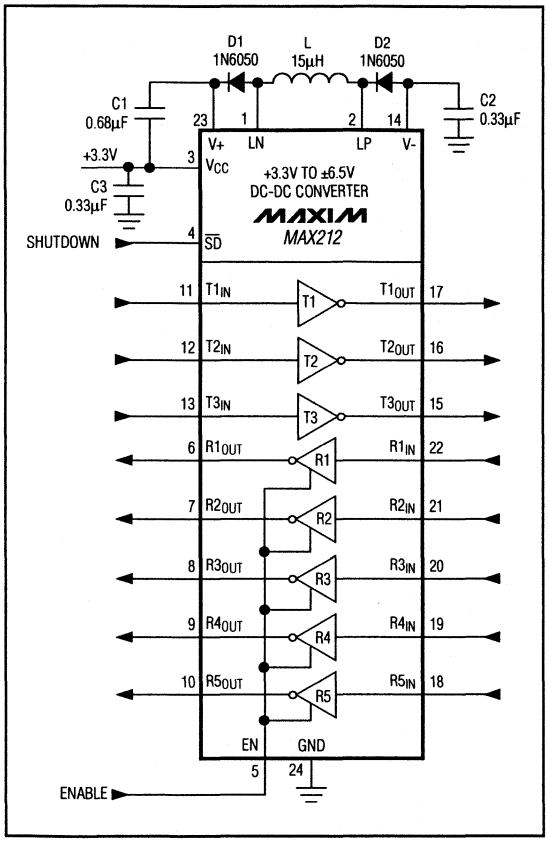


Figure 1. Typical Application Circuit

Switch-Mode Power Supply

The switch-mode power supply uses a single inductor with two inexpensive diodes and two capacitors to generate ±6.5V from the 3.0V to 3.6V input. Figure 1 shows the complete circuit for the power supply.

Use a 15µH inductor with a saturation current rating of at least 350mA and under 1Ω resistance. Sample surface-mount inductors are available from Maxim. Use 1N6050 diodes or equivalent. Surface-mount equivalents for the 1N6050 include the Motorola MMBD6050LT1, Philips PMBD6050, and Allegro (formerly Sprague) TMPD6050LT.

For C1 and C2, use ceramic capacitors with values no less than indicated in Figure 1. These capacitors determine the ripple on V+ and V-, but not the absolute voltages. Bypass V_{CC} to GND with at least 0.33µF close to the MAX212. Increase this to 4.7µF if there are no other V_{CC} supply bypass components less than 6 inches (15cm) away from the MAX212.

Component suppliers are listed in Table 1.

RS-232 Drivers

All three drivers are identical and deliver EIA/TIA-232E and EIA/TIA-562 output voltage levels when V_{CC} is between 3.0V and 3.6V. Disable the drivers by taking the $\overline{SD}$ pin to GND. The transmitter outputs are forced into a high-impedance state when $\overline{SD}$ is grounded.

RS-232 Receivers

All five receivers are identical and accept EIA/TIA-232E and EIA/TIA-562 input signals. The CMOS receiver outputs swing rail-to-rail (0V to V_{CC}). When EN is high, the receivers are active regardless of $\overline{SD}$'s status. When EN is low, the receivers' outputs are put into a high-impedance state. This allows two RS-232 ports (or two parts of different types) to be wire-ORed at the UART.

Table 1. Suggested Component Suppliers

MANUFACTURER	PART NUMBER	PHONE NUMBER	FAX NUMBER
Allegro	TMPD6050LT	USA (508) 853-5000	USA (508) 853-5049
Motorola	MMBD6050LT1	USA (408) 749-0510	USA (408) 991-7420
Murata	LQH4N150K-TA	USA (404) 831-9172 Japan (075) 951-9111	USA (404) 436-3030 Japan (075) 955-6526
Philips	PMBD6050	USA (401) 762-3800	USA (401) 767-4493
Sumida	CD43150	USA (708) 956-0666 Japan (03) 3607-5111	USA (708) 956-0702 Japan (03) 3607-5428
TDK	NLC453232T-150K	USA (708) 803-6100 Japan (03) 3278-5111	USA (708) 803-6296 Japan (03) 3278-5358

+3V-Powered, Low-Power, True RS-232 Transceiver

Operating Modes

$\overline{SD}$ and EN determine the operation of the MAX212 as follows:

$\overline{SD}$	EN	RECEIVER OUTPUTS	DRIVER OUTPUTS	DC-DC CONVERTER	SUPPLY CURRENT
L	L	High-Z	High-Z	Off	Minimum
L	H	Enabled	High-Z	Off	Minimum
H	L	High-Z	Enabled	On	Normal
H	H	Enabled	Enabled	On	Normal

Shutdown

V+ and V- are disabled and the transmitters are put into a high-impedance state when $\overline{SD}$ is taken to logic low. Receiver operation is not affected, but power consumption is dramatically reduced while in shutdown mode. Supply current is minimized when the receiver inputs are static in any of three states: floating (ground), less than GND, or greater than V_{CC}. This will be true for all static RS-232 conditions. The presence of AC signals on receiver inputs will increase V_{CC} current in shutdown.

From a low-power system perspective, powering-up with non-critical or unused sections of circuitry shut down or deselected is generally recommended. Activating these sections only when required saves power and reduces power-up current surges. Powering-up the MAX212 in shutdown mode (holding the shutdown pin, $\overline{SD}$, low until V_{CC} > 2.7V), helps to achieve this.

Driving the MAX212 from 5V Logic

The MAX212 can interface with 5V logic while it operates from a 3V supply, however a 200kΩ series resistor between $\overline{SD}$ and the +5V logic signal is required (see Figure 2). This protects the MAX212 by preventing $\overline{SD}$ from sinking current while V+ is powering up. Also, the UART must not be permitted to send a logic high to the MAX212's EN or transmitter input pins until $\overline{SD}$ is high (not shut down).

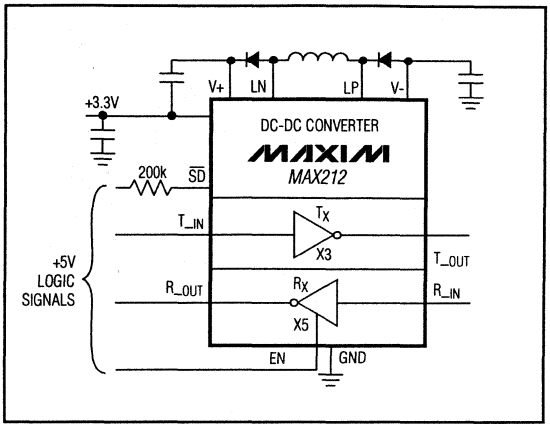


Figure 2. Connecting to +5V Logic

Mouse Driveability

The MAX212 has been specifically designed to power serial mice while operating from low-voltage power supplies. It has been tested with samples of ten major mouse models from six manufacturers, including the leading three, Logitech (5 models), Mouse Systems, and Microsoft. The MAX212 successfully drove all serial mice and met their respective current and voltage requirements (Figure 1).

Figure 3 shows the transmitter output voltages under increasing load current. The MAX212's switching regulator ensures the transmitters will supply at least ±5V during worst-case load conditions.

EIA/TIA-232E and 562 Standards

Most of the power drawn by RS-232 circuits is consumed because the EIA/TIA-232E standard demands that at least ±5V be delivered by the transmitters to impedances that can be as low as 3kΩ. For applica-

+3V Powered RS-232 Transceivers from Maxim

PART	POWER-SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/ RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	DATA RATE (kbps)	FEATURES
MAX212	3.0 to 3.6	3/5	5	250	True RS-232 from +3V
MAX560	3.0 to 3.6	4/5	2	120	2 receivers active in shutdown
MAX561	3.0 to 3.6	4/5	0	120	Pin compatible with MAX241
MAX562	2.7 to 5.25	3/5	5	250	Wide supply range

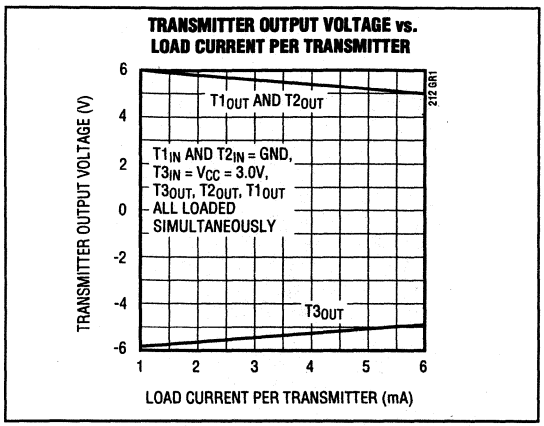


Figure 3. Mouse Emulation Circuit Current

tions where power consumption is especially critical, the EIA/TIA-562 standard provides an alternative.

EIA/TIA-562 transmitter output voltage levels need only reach ±3.7V, and because they need only drive the same 3kΩ receiver loads specified by RS-232, total power consumption is considerably reduced. Since the EIA/TIA-232E and EIA/TIA-562 receiver input voltage thresholds are the same, interoperability between the two standards is guaranteed and devices from both standards will communicate with each other successfully.

Maxim's MAX560 and MAX561 are EIA/TIA-562 transceivers that operate on a single supply from 3.0V to 3.6V, and the MAX562 transceiver operates from 2.7V to 5.25V while producing EIA/TIA-562 levels.

Evaluation Kit

The MAX212 evaluation kit (EV kit) is a fully assembled and tested, surface-mount demonstration board that provides quick and easy evaluation of the MAX212.

The MAX212 EV kit is intended for 3.3V ±300mV-powered EIA/TIA-232E and V.28/V.24 communications interfaces where 3 drivers and 5 receivers are needed with minimum power consumption.

A logic or pin-selectable shutdown mode reduces current to 1µA. While shut down, all receivers can remain active or can be disabled under logic control via the EN input.

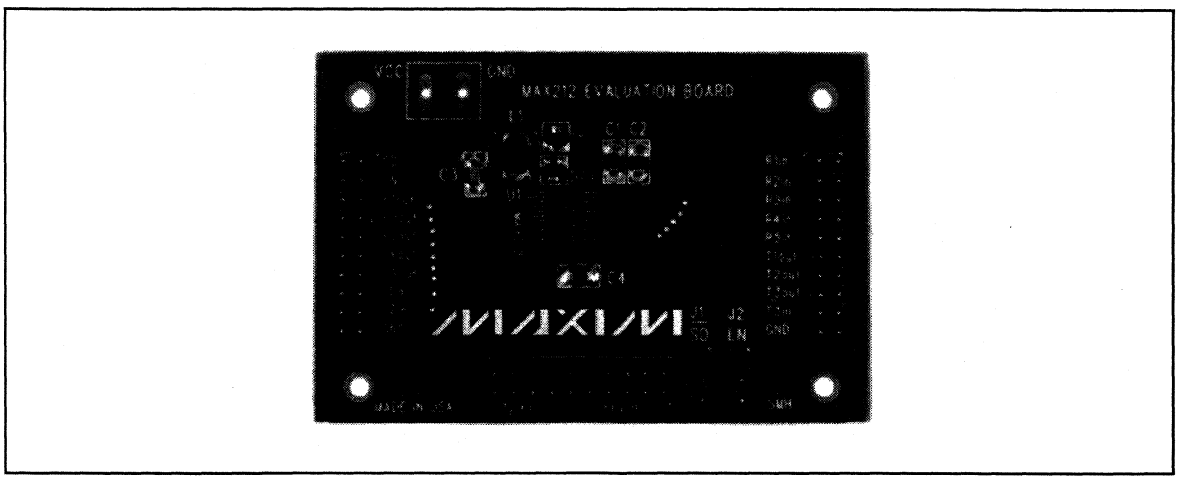
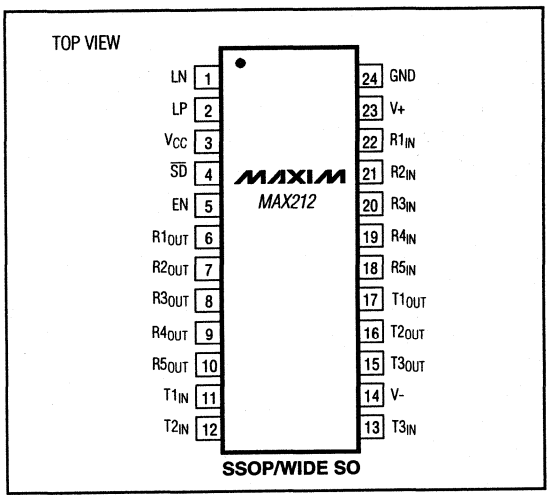


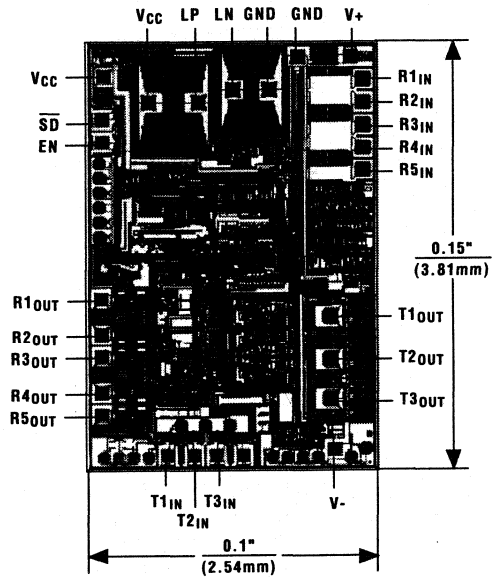
Figure 4. MAX212 Evaluation Kit

+3V-Powered, Low-Power, True RS-232 Transceiver

Pin Configuration



Chip Topography



TRANSISTOR COUNT: 1382 ;
SUBSTRATE CONNECTED TO V+.

19-0199; Rev 0; 10/93

MAXIM

Programmable DTE/DCE, +5V RS-232 Transceiver

General Description

The MAX214 +5V RS-232 transceiver provides a complete, 8-line, software-configurable, DTE or DCE port RS-232 interface. Tx, Rx, RTS, CTS, DTR, DSR, DCD, and RI circuits can be configured as either Data Terminal Equipment (DTE) or Data Circuit-Terminating Equipment (DCE) using the DTE/DCE control pin. The MAX214 eliminates the need to swap cables when switching between DTE and DCE configurations.

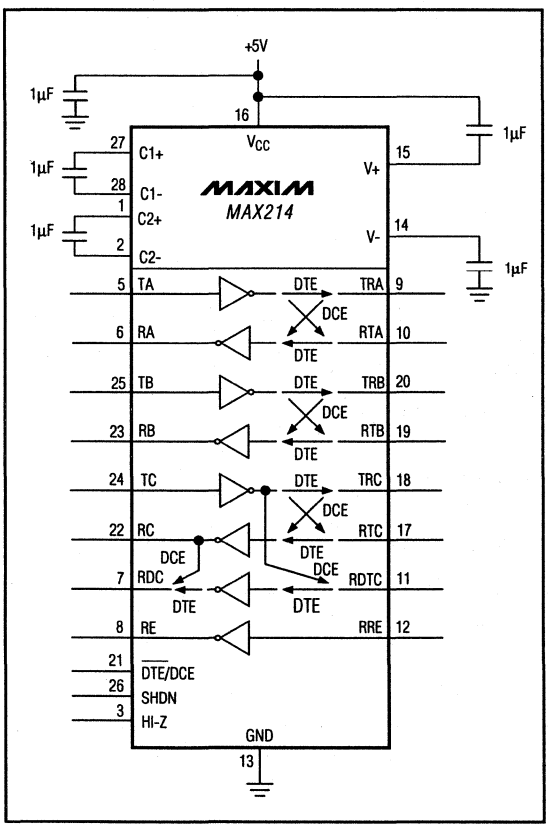
Applications

AT-Compatible Laptop Computers

AT-Compatible Desktop Computers

Modems, Printers, and Other Peripherals

Typical Operating Circuit



Features

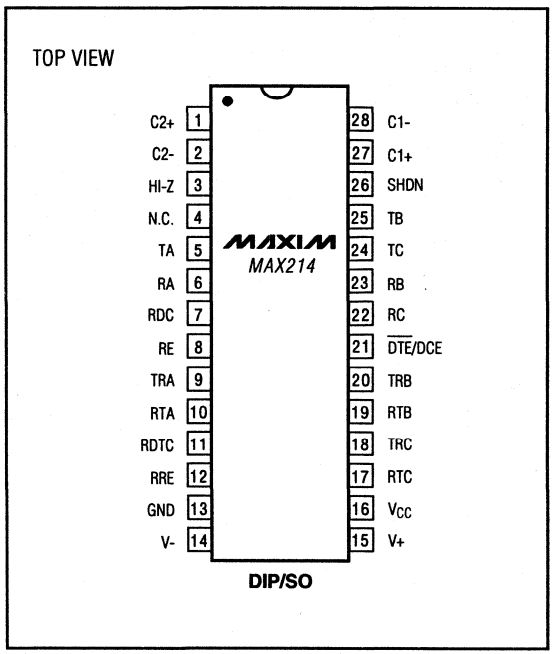
- ♦ **Eliminates Null Modem Cables**
- ♦ **Programmable DTE or DCE Serial Port**
- ♦ **1µF Charge-Pump Capacitors**
- ♦ **116kbps Data Rate—Guaranteed**
- ♦ **20µA Shutdown Mode**
- ♦ **Receivers Active in Shutdown**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX214CPI	0°C to +70°C	28 Plastic DIP
MAX214CWI	0°C to +70°C	28 Wide SO
MAX214C/D	0°C to +70°C	Dice*
MAX214EPI	-40°C to +85°C	28 Plastic DIP
MAX214EWI	-40°C to +85°C	28 Wide SO

* *Dice are specified at T_A = +25°C.*

Pin Configuration



Programmable DTE/DCE, +5V RS-232 Transceiver

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
Input Voltages
  T_{IN}, $\overline{DTE}$/DCE, SHDN HI-Z ..... -0.3V to (V_{CC} + 0.3V)
  R_{IN} ..... ±15V
Output Voltages:
  T_{OUT} ..... ±15V
  R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit (one output at a time)
  T_{OUT} to GND ..... Continuous
  R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
  Wide SO (derate 12.50mW/°C above +70°C) 1000mW
Operating Temperature Ranges:
  MAX214C_I ..... 0°C to +70°C
  MAX214E_I ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C1 to C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Logic Input Threshold Low			0.8	1.4		V
Logic Input Threshold High				1.4	2.0	V
Logic Input Pull-Up Current	Normal operation		1	10	50	µA
	Shutdown			±0.01	±1	
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.5		V
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 1)		300	300k		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±25		mA
RS-232 RECEIVERS						
Input Voltage Operating Range					±15	V
Positive Threshold Input Low	T_A = +25°C, V_{CC} = 5V, normal operation, SHDN = 0V		0.8	1.3		V
Positive Threshold Input High	T_A = +25°C, V_{CC} = 5V, normal operation, SHDN = 0V			1.8	2.4	V
Positive Threshold Input Hysteresis	V_{CC} = 5V, normal operation, SHDN = 0V (no hysteresis in shutdown)		0.2	0.5	1.0	V
Negative Threshold Input Low	T_A = +25°C, V_{CC} = 5V	Normal operation, SHDN = 0V	-2.6	-1.9		V
		Shutdown, SHDN = 5V	0.8	1.3		
Negative Threshold Input High	T_A = +25°C, V_{CC} = 5V	Normal operation, SHDN = 0V		-1.5	-0.2	V
		Shutdown, SHDN = 5V		1.3	2.4	
Negative Threshold Input Hysteresis	V_{CC} = 5V, normal operation, SHDN = 0V (no hysteresis in shutdown)		0.2	0.4	1.0	V
Input Resistance	HI-Z = 0V and SHDN = 0V		3	5	7	kΩ
	HI-Z = 5V or SHDN = 5V		100	300		
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, C1 to C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{CC} Supply Current	No load, T_A = +25°C			9	20	mA
Shutdown Supply Current	$\overline{DTE}$/DCE = 0V, SHDN = HI-Z = V_{CC}, Figure 1	T_A = +25°C		4	20	µA
		T_A = T_{MIN} to T_{MAX}			50	
CONTROL LOGIC ($\overline{DTE}$/DCE, SHDN, HI-Z)						
Logic Input Threshold Low			0.8	1.3		V
Logic Input Threshold High				1.3	2.0	V
Input Leakage Current					±1	µA
AC CHARACTERISTICS						
Data Rate	Normal operation, transmitters and receivers			200	116	kbps
	Receivers in shutdown mode			20		
Transition-Region Slew Rate	T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = to 2500pF, measured from 3V to -3V or -3V to 3V		6	12	30	V/µs
Transmitter Propagation Delay, TTL to RS-232 (Normal Operation)	t_{PHLT}			1.3	3.5	µs
	t_{PLHT}			1.4	3.5	
Transmitter + to - Propagation-Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			100		ns
Receiver Propagation Delay, RS-232 to TTL (Normal Operation)	t_{PHLR}, t_{PLHR}			0.4	1.5	µs
Receiver Propagation Delay, RS-232 to TTL (Shutdown Mode)	t_{PHLR}			0.4	10	µs
	t_{PLHR}			1.5	10	
Receiver Propagation-Delay Difference (Normal Operation)	$\lvert t_{PHLT} - t_{PLHT} \rvert$			100		ns
MODE-CHANGE TIMING (DTE/DCE)						
Transmitter Enable Time	t_{TEN} (includes charge-pump start-up time)			250		µs
Transmitter Disable Time	t_{TTR}			600		ns
Transmitter $\overline{DTE}$/DCE Switch Time	t_{TSW}			600		ns
Receiver $\overline{DTE}$/DCE Switch Time	t_{RSW}			300		ns
Receiver Termination-Resistor Connect/Disconnect Time	(SHDN = 0V)			300		ns
Receiver Termination-Resistor Connect Entering SHDN Time				250		µs
Receiver Termination-Resistor Disconnect Exiting SHDN Time				300		ns

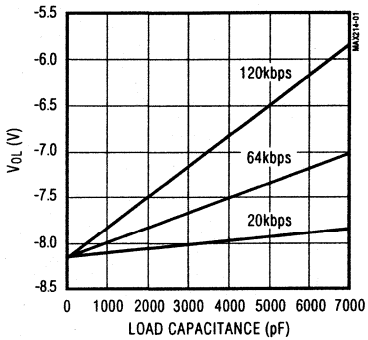
Note 1: The 300Ω minimum is the EIA/TIA-232E specification, but the actual resistance when in shutdown mode or when V_{CC} = 0V is typically 300kΩ.

Programmable DTE/DCE, +5V RS-232 Transceiver

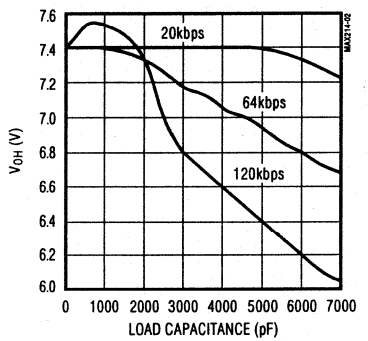
Typical Operating Characteristics

(V_{CC} = 5V, C1 to C4 = 1µF, all transmitters loaded with 3kΩ in parallel with 2.5nF, T_A = +25°C, unless otherwise noted.)

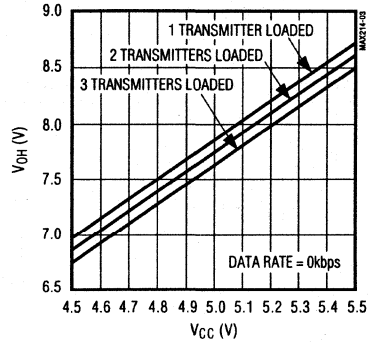
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



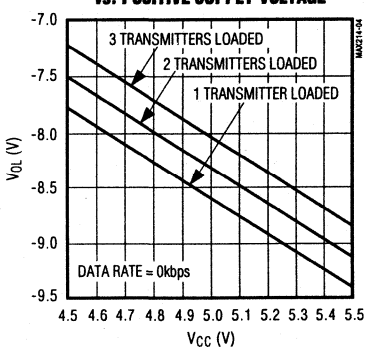
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



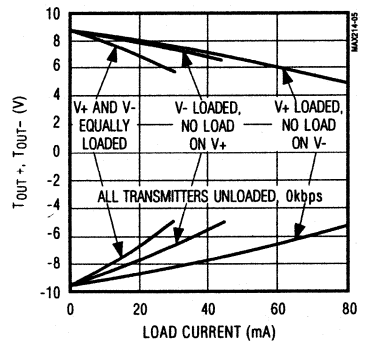
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC} POSITIVE SUPPLY VOLTAGE



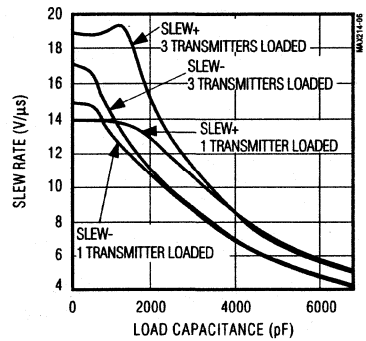
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. POSITIVE SUPPLY VOLTAGE



TRANSMITTER OUTPUT VOLTAGES vs. V+, V- LOAD CURRENT



SLEW RATE vs. LOAD CAPACITANCE



Programmable DTE/DCE, +5V RS-232 Transceiver

Pin Description

PIN	NAME	FUNCTION
1, 2	C2+, C2-	Terminals for negative charge-pump capacitor
3	HI-Z	RS-232 receiver impedance control. Take high to disconnect the termination resistor.
4	N.C.	No connect—not internally connected
5, 24, 25	TA, TC, TB	TTL/CMOS driver A, C, B inputs
6, 8, 22, 23	RA, RE, RC, RB	TTL/CMOS receiver A, E, C, B outputs
7	RDC	TTL/CMOS DTE receiver output D for $\overline{DTE}$/DCE = 0V, or TTL/CMOS DCE receiver output C for $\overline{DTE}$/DCE = +5V
9, 18, 20	TRA, TRC, TRB	RS-232 DTE driver output for $\overline{DTE}$/DCE= 0V, or RS-232 DCE receiver input for $\overline{DTE}$/DCE = +5V
10, 17, 19	RTA, RTC, RTB	RS-232 DTE receiver input for $\overline{DTE}$/DCE = 0V, or RS-232 DCE driver output for $\overline{DTE}$/DCE = +5V
11	RDTC	RS-232 DTE receiver input D for $\overline{DTE}$/DCE = 0V, or RS-232 DCE driver output C for $\overline{DTE}$/DCE = +5V
12	RRE	RS-232 receiver input
13	GND	Ground
14	V-	-2V_{CC} voltage generated by the charge pump
15	V+	+2V_{CC} voltage generated by the charge pump
16	V_{CC}	+4.5V to +5.5V supply voltage
21	$\overline{DTE}$/DCE	Data terminal equipment (DTE) and data circuit-terminating equipment (DCE) control pin. DCE active high and DTE active low.
26	SHDN	Shutdown control; shutdown high, normal operation low
27, 28	C1+, C1-	Terminals for positive charge-pump capacitor

Detailed Description

The MAX214 RS-232 transceiver provides a complete, 8-line, software-configurable, DTE or DCE port RS-232 interface. Tx, Rx, RTS, CTS, DTR, DSR, DCD, and RI circuits can be configured as either Data Terminal Equipment (DTE) or Data Circuit-Terminating Equipment (DCE) using the $\overline{DTE}$/DCE control pin. The MAX214 eliminates the need to swap cables when switching between DTE and DCE configurations. This is useful when, for example, a portable computer is required to communicate with printers, modems, and other computers without carrying multiple cables.

The MAX214 runs from a single +5V supply and incorporates a dual charge-pump voltage converter to generate the necessary voltages for the RS-232 transmitters. A shutdown mode is provided to save power when transmission is not required, but the receivers always stay active for simple detection of ring indicator signals.

$\overline{DTE}$/DCE Operation

The $\overline{DTE}$/DCE pin allows circuit configuration under software control. Tables 1a and 1b show the pin definitions of the MAX214 in both DTE and DCE modes. The Function columns show the direction of data flow from the input pin to the output pin of the MAX214, and onto the corresponding DB-25 connector's pin.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by two charge-pump voltage converters (Figure 2). The first uses capacitor C1 to double the +5V to +10V, storing the +10V on the output filter capacitor, C3. The second charge-pump voltage converter uses C2 to invert the +10V to -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is pulled to V_{CC} by an internal resistor, and V- falls to GND.

Programmable DTE/DCE, +5V RS-232 Transceiver

Table 1a. DTE-Operation Pin Configurations

TTL/CMOS I/O LABEL	MAX214 PIN	FUNCTION	MAX214 PIN	RS-232 I/O LABEL	DB-25 PIN	INPUT THRESHOLD
Transmitter (TxD)	5		9	TxD	2	
Receiver (RxD)	6		10	RxD	3	+
Request to Send (RTS)	25		20	RTS	4	
Clear to Send (CTS)	23		19	CTS	5	-
Data Terminal Ready (DTR)	24		18	DTR	6	
Data Set Ready (DSR)	22		17	DSR	20	-
Detector Carrier Data (DCD)	7		11	DCD	8	+
Ring Indicator (RI)	8		12	RI	22	+

Table 1b. DCE-Operation Pin Configurations

MAX214 PIN	FUNCTION	MAX214 PIN	RS-232 I/O LABEL	DB-25 PIN	INPUT THRESHOLD
5		10	RxD	3	
6		9	TxD	2	+
25		19	CTS	5	
23		20	RTS	4	-
24		17	DSR	20	
		11	DCD	8	
22		18	DTR	6	-
7					
8		12	RI	22	+

Programmable DTE/DCE, +5V RS-232 Transceiver

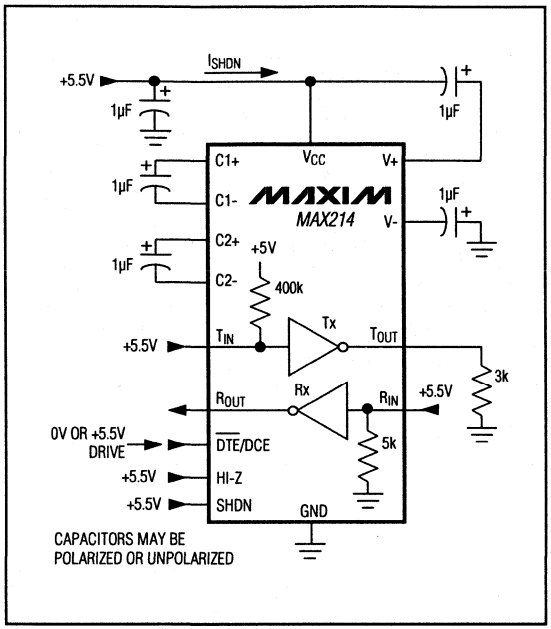


Figure 1. MAX214 Shutdown-Current Test Circuit

RS-232 Drivers

With V_{CC} = 5V, the typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. Under worst-case operating conditions (including 116kbps data rate, 3kΩ || 2500pF load, V_{CC} = 4.5V, maximum rated temperature) the output swing is guaranteed to meet the ±5V minimum specified by EIA/TIA-232 and V.28. The open-circuit output voltage swing ranges from (V+ - 0.6V) to V-.

Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers can be left unconnected because 400kΩ pull-up resistors to V_{CC} are included on-chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. The input pull-up resistors typically source 10µA; in shutdown mode, they are disconnected to reduce supply current.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA, even if the transmitter output is back-driven with voltages up to ±15V.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS-logic levels. They invert, to match the inversion of RS-232 drivers. The guaranteed receiver input thresholds are significantly tighter than the ±3V thresholds required by the EIA/TIA-232E specification,

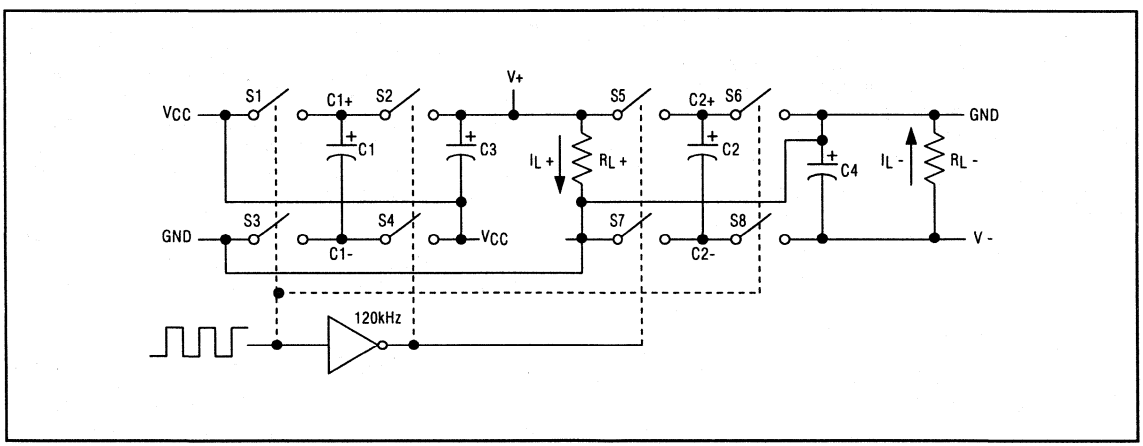


Figure 2. Charge-Pump Diagram

Programmable DTE/DCE, +5V RS-232 Transceiver

Table 2. Control Pin Configurations

CONTROL INPUTS			RS-232 PINS		
SHUTDOWN	HI-Z	DTE/DCE	TRA, TRB, TRC	RTA, RTB, RTC, RDTC	RRE
0	0	0	Transmit Mode	Receive Mode/5kΩ	Receive Mode/5kΩ
0	0	1	Receive Mode/5kΩ	Transmit Mode	Receive Mode/5kΩ
0	1	0	Transmit Mode	Receive Mode/HI-Z	Receive Mode/HI-Z
0	1	1	Receive Mode/HI-Z	Transmit Mode	Receive Mode/HI-Z
1	0	0	Disabled/HI-Z	Slow Receive/HI-Z	Slow Receive/HI-Z
1	0	1	Slow Receive/HI-Z	Disabled/HI-Z	Slow Receive/HI-Z
1	1	0	Disabled/HI-Z	Slow Receive/HI-Z	Slow Receive/HI-Z
1	1	1	Slow Receive/HI-Z	Disabled/HI-Z	Slow Receive/HI-Z

which improves noise margins. The polarity of each receiver's input threshold is shown in Tables 1a and 1b. In normal operating mode, receiver inputs are internally connected to ground with 5kΩ resistors. So unconnected receivers with positive input thresholds have high outputs, and those with negative input thresholds have low outputs.

When shut down, all receivers have positive thresholds. This allows the receiver inputs to respond to TTL-/CMOS-logic levels, as well as RS-232 levels. The guaranteed 0.8V input threshold ensures that receivers shorted to ground will have a logic 1 output. Also, the 300kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

The receiver's 0.5V of hysteresis provides clean output transitions, even with slow rise-time and fall-time signals with moderate amounts of noise and ringing. The receivers have no hysteresis in shutdown mode.

HI-Z Control

The receiver inputs are terminated with 5kΩ resistors, to comply with the requirements of EIA/TIA-232E. However, these internal resistors can be disconnected by taking the HI-Z control pin to a logic high. This makes all of the MAX214's receiver inputs high impedance, and facilitates the transmission of RS-232 data from a single transmitter to multiple receivers. In this case, all but one of the receiving ICs should be put into the high input-impedance state.

Shutdown Control

In shutdown mode, the charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled. This reduces supply current typically to 4µA. The time required to exit shutdown is about 250µs, as shown in Figure 3.

Receivers

Receiver outputs never go into a high-impedance state; they are always active, even in shutdown mode (see Table 2). These awake-in-shutdown receivers are useful for monitoring external activity (for example, on RI), while maintaining minimal power consumption. Receivers in shutdown mode are slower (20kbps) than when not shut down (116kbps), and lack the hysteresis present in normal operation.

Drivers

The driver outputs are high impedance in shutdown mode, even when back-driven with voltages up to ±15V.

Applications Information

Capacitor Selection

The type of capacitor (C1 to C4) used is not critical for proper operation. The MAX214 requires 1µF capacitors, although in all cases capacitors of up to 10µF can be used without harm. Ceramic dielectrics are suggested for the 1µF capacitors.

When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger nominal value (for example, 2 times larger). The effective series resistance (ESR) of the capacitors may vary over temperature and increase when below 0°C. ESR influences the amount of ripple on V+ and V-, so if low ripple is required over wide temperature ranges, use larger capacitors or low-ESR types.

To reduce the output impedance at V+ and V-, use larger capacitors (up to 10µF). This can be useful when "stealing" power from V+ or from V-.

Driver Outputs when Exiting Shutdown

Figure 3 shows the MAX214 driver outputs when exiting shutdown. As they become active, the two driver outputs are shown going to opposite RS-232 levels (one driver input is high, the other is low). Each driver is loaded with 3kΩ in parallel with 2.5nF.

Power-Supply Bypassing

Decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitors.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce noise margins. See the Output Voltage vs. Load Current graph in the *Typical Operating Characteristics*. Increasing the charge-pump capacitor sizes up to 10µF reduces the impedance of the V+ and V- outputs.

High Data Rates

The MAX214 maintains the RS-232 ±5.0V minimum driver output voltage even at high data rates. The *Typical Operating Characteristics* show transmitter output voltage levels driving 3kΩ in parallel with various capacitive loads at data rates up to 120kbps.

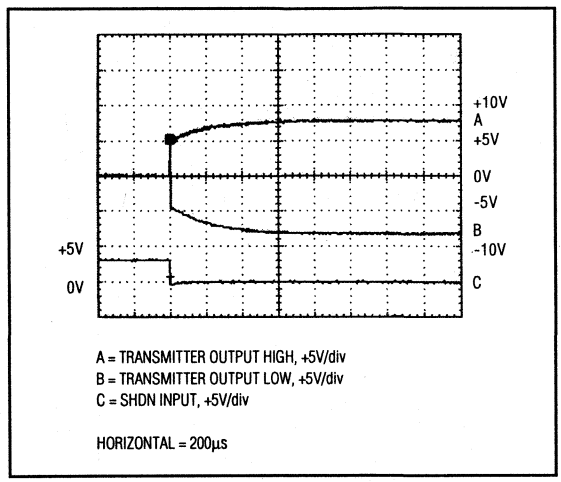


Figure 3. Transmitter Outputs When Exiting Shutdown

Programmable DTE/DCE, +5V RS-232 Transceiver

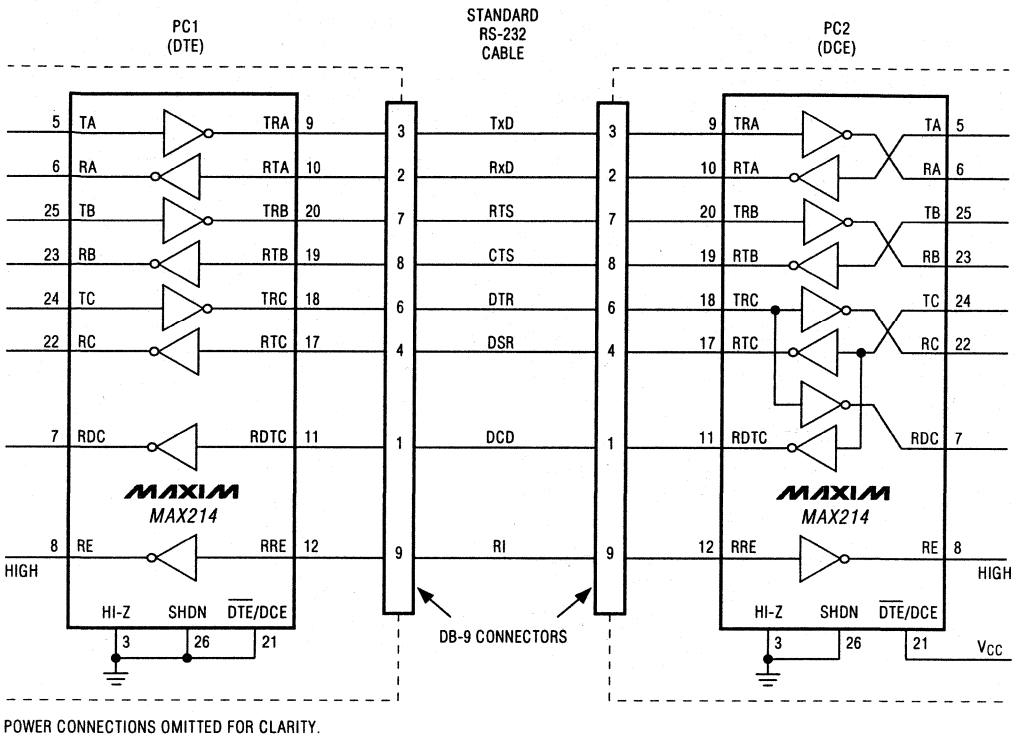
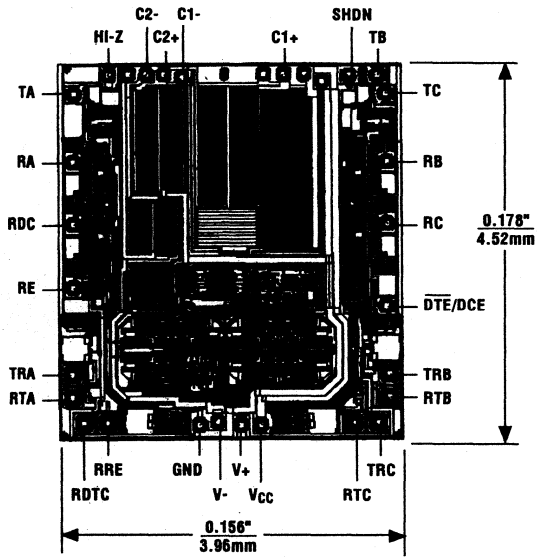


Figure 4. Typical Application Circuit Showing 2 PCs with Both DTE and DCE Operation

Table 3. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER	CONDITIONS	EIA/TIA-232E, V.28 SPECIFICATIONS
Driver Output Voltage 0 Level 1 Level Output Level, Max	3kΩ to 7kΩ load	+5.0V to +15V
	3kΩ to 7kΩ load	-5.0V to -15V
	No load	±25V
Data Rate	$3k\Omega \le R_L \le 7k\Omega$, $C_L \le 2500pF$	Up to 20kbits/sec
Receiver Input Voltage 0 Level 1 Level Input Level, Max		+3.0V to +15V
		-3.0V to -15V
		±25V
Instantaneous Slew Rate, Max	$3k\Omega \le R_L \le 7k\Omega$, $C_L \le 2500pF$	30V/µs
Driver Output Short-Circuit Current, Max		100mA
Transition Rate on Driver Output	V.28	1ms or 3% of the period
	EIA/TIA-232E	4% of the period
Driver Output Resistance	$-2V < V_{OUT} < +2V$	300Ω

Chip Topography



TRANSISTOR COUNT: 694;
SUBSTRATE CONNECTED TO V+.

Table 4. DB9/DB25 Cable Connections Commonly Used for EIA/TIA-232 and V.24 Asynchronous Interfaces

DB9 PIN	DB25 PIN	NAME	SYMBOL	FUNCTION
1	8	Received Line Signal Detector, sometimes called Data Carrier Detect	DCD	Handshake from DCE
2	3	Receive Data	RxD	Data from DCE
3	2	Transmit Data	TxD	Data from DTE
4	20	Data Terminal Ready	DTR	Handshake from DTE
5	7	Signal Ground	GND	Reference point for signals
6	6	Data Set Ready	DSR	Handshake from DCE
7	4	Request to Send	RTS	Handshake from DTE
8	5	Clear to Send	CTS	Handshake from DCE
9	22	Ring Indicator	RI	Handshake from DCE

19-0246; Rev 0; 3/94

1.8V to 4.25V-Powered, True RS-232 Dual Transceiver

General Description

The MAX218 RS-232 transceiver is intended for battery-powered EIA/TIA-232E and V.28/V.24 communications interfaces that need two drivers and two receivers with minimum power consumption. It provides a wide +1.8V to +4.25V operating voltage range while maintaining true RS-232 and EIA/TIA-562 voltage levels. The MAX218 runs from two alkaline, NiCd, or NiMH cells without any form of voltage regulator.

A shutdown mode reduces current consumption to 1µA, extending battery life in portable systems. While shut down, all receivers can remain active or can be disabled under logic control, permitting a system incorporating the CMOS MAX218 to monitor external devices while in low-power shutdown mode.

A guaranteed 120kbps data rate provides compatibility with popular software for communicating with personal computers. Three-state drivers are provided on all receiver outputs so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART. The MAX218 is available in 20-pin DIP, SO, and SSOP packages.

Applications

Battery-Powered Equipment
Computers
Printers
Peripherals
Instruments
Modems

Features

BETTER THAN BIPOLAR!

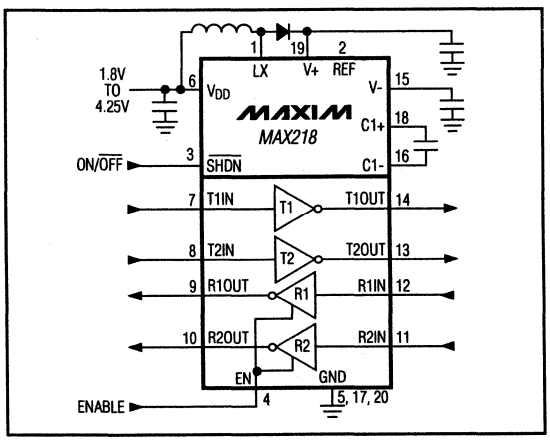
- **Operates Directly from Two Alkaline, NiCd, or NiMH Cells**
- **+1.8V to +4.25V Supply Voltage Range**
- **120kbps Data Rate**
- **Low-Cost Surface-Mount Components**
- **Meets EIA/TIA-232E Specifications**
- **1µA Low-Power Shutdown Mode**
- **Both Receivers Active During Low-Power Shutdown**
- **Three-State Receiver Outputs**
- **Flow-Through Pinout**
- **On-Board DC-DC Converters**
- **20-Pin SSOP, Wide SO, or DIP Packages**

Ordering Information

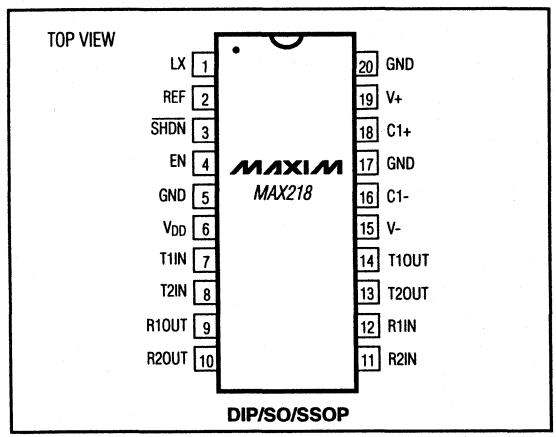
PART	TEMP. RANGE	PIN-PACKAGE
MAX218CPP	0°C to +70°C	20 Plastic DIP
MAX218CWP	0°C to +70°C	20 Wide SO
MAX218CAP	0°C to +70°C	20 SSOP
MAX218C/D	0°C to +70°C	Dice*
MAX218EPP	-40°C to +85°C	20 Plastic DIP
MAX218EWP	-40°C to +85°C	20 Wide SO
MAX218EAP	-40°C to +85°C	20 SSOP

Contact factory for dice specifications.

Typical Operating Circuit



Pin Configuration



1.8V to 4.25V-Powered, True RS-232 Dual Transceiver

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... -0.3V to +4.6V
- V+ ..... (V_{DD} - 0.3V) to +7.5V
- V- ..... +0.3V to -7.4V
- V_{DD} to V- ..... +12V
- LX ..... -0.3V to (1V + V+)

Input Voltages
- T_IN, EN, $\overline{SHDN}$ ..... -0.3V to +7V
- R_IN ..... ±25V

Output Voltages
- T_OUT ..... ±15V)
- R_OUT ..... -0.3V to (V_{DD} + 0.3V)

Short-Circuit Duration, R_OUT, T_OUT to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
- Wide SO (derate 10.00mW/°C above +70°C) 800mW
- SSOP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
- MAX218C_ P ..... 0°C to +70°C
- MAX218E_ P ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = 1.8V to 4.25V, C1 = 0.47µF, C2 = C3 = C4 = 1µF, L1 = 15µH, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.0V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Operating Voltage Range		1.8		4.25	V
Supply Current (Note 1)	No load, V_{DD} = EN = $\overline{SHDN}$ = 3.0V, T_A = +25°C		1.9	3.0	mA
Shutdown Supply Current	$\overline{SHDN}$ = EN = 0V, all R_INs static		0.04	10	µA
	$\overline{SHDN}$ = 0V, EN = V_{DD}, all R_INs static		0.04	10	
LOGIC					
Input Logic Threshold Low	T_IN, EN, $\overline{SHDN}$			0.33 x V_{DD}	V
Input Logic Threshold High	T_IN, EN, $\overline{SHDN}$	0.67 x V_{DD}			V
Input Hysteresis	T_IN		0.1		V
Input Leakage Current	T_IN, EN, $\overline{SHDN}$ = 0V or V_{DD}		0.001	±1	µA
Output Voltage Low	R_OUT, I_{OUT} = 1.0mA			0.4	V
Output Voltage High	R_OUT, I_{OUT} = -0.4mA	V_{DD} - 0.25	V_{DD} - 0.08		V
Output Leakage Current	R_OUT, 0V ≤ R_OUT ≤ V_{DD}, EN = 0V		0.05	±10	µA
Output Short-Circuit Current	R_OUT		±12		mA
EIA/TIA-232E RECEIVER INPUTS					
Input Voltage Range		-25		+25	V
Input Threshold Low	V_{DD} = 2.0V to 4.25V	0.4			V
	V_{DD} = 1.8V to 4.25V	0.3			
Input Threshold High	V_{DD} = 1.8V to 4.25V			3.0	V
	V_{DD} = 1.8V to 3.6V			2.8	
Input Hysteresis			0.7		V
Input Resistance	-15V < R_IN < +15V	3	5	7	kΩ
EIA/TIA-232E TRANSMITTER OUTPUTS					
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground	±5	±6		V
Output Resistance	V_{DD} = 0V, -2V < T_OUT < +2V	300			Ω
Output Short-Circuit Current			±24	±100	mA

Note 1: Entire supply current for the circuit of Figure 1.

TIMING CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = 1.8V to 4.25V, C1 = 0.47µF, C2 = C3 = C4 = 1µF, L1 = 15µH, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = 3.0V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate		1000pF ‖ 3kΩ load each transmitter, 150pF load each receiver	120			kbps
Receiver Output Enable Time	t_{ER}			90	300	ns
Receiver Output Disable Time	t_{DR}			200	500	ns
Transmitter Output Enable Time	t_{ET}			140	450	µs
Transmitter Output Disable Time	t_{DT}			500		ns
Receiver Propagation Delay	t_{PHLR}	150pF load		290	700	ns
	t_{PLHR}	150pF load		260	700	
Transmitter Propagation Delay	t_{PHLT}	2500pF ‖ 3kΩ load		1.9	2.7	µs
	t_{PLHT}	2500pF ‖ 3kΩ load		1.8	2.7	
Transition Region Slew Rate		T_A = +25°C, V_{DD} = 3.0V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V	3.0		30	V/µs

Pin Description

PIN	NAME	FUNCTION
1	LX	Inductor/Diode Connection Point
2	REF	Internal Reference Bypass Node. Normally left open. Bypass to GND (between pin 2 and pin 5) with 0.1µF if V_{DD} is noisy.
3	$\overline{SHDN}$	Shutdown Control. Connect to V_{DD} for normal operation. Connect to GND to shut down the power supply and to disable the drivers. Receiver status is not changed by this control.
4	EN	Receiver Output Enable Control. Connect to V_{DD} for normal operation. Connect to GND to force the receiver outputs into high-Z state.
5, 17, 20	GND	Ground. Connect all GND pins to ground.
6	V_{DD}	Supply Voltage Input; 1.8V to 4.25V. Bypass to GND with at least 1µF. See *Capacitor Selection* section.
7, 8	T1IN, T2IN	Transmitter Inputs
9, 10	R1OUT, R2OUT	Receiver Outputs; swing between GND and V_{DD}.
11, 12	R2IN, R1IN	Receiver Inputs
13, 14	T2OUT, T1OUT	Transmitter Outputs; swing between V+ and V-.
15	V-	Negative Supply generated on-board
16, 18	C1-, C1+	Terminals for Negative Charge-Pump Capacitor
19	V+	Positive Supply generated on-board

1.8V to 4.25V-Powered, True RS-232 Dual Transceiver

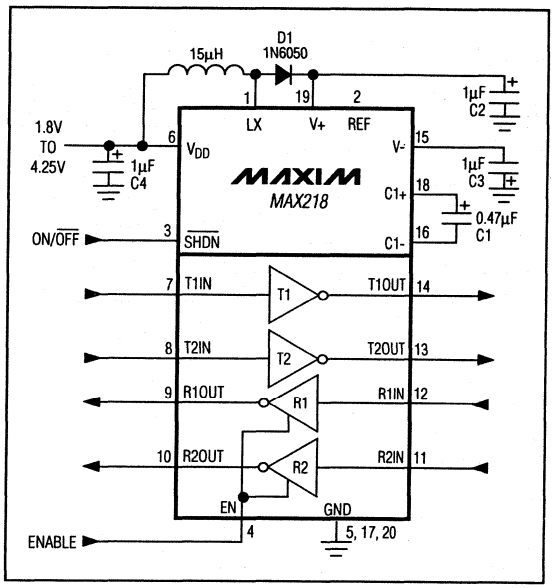


Figure 1. Single-Supply Operation

Detailed Description

The MAX218 line driver/receiver is intended for battery-powered EIA/TIA-232 and V.28/V.24 communications interfaces that require two drivers and two receivers. The operating voltage extends from 1.8V to 4.25V, yet the device maintains true RS-232 and EIA/TIA-562 transmitter output voltage levels. This wide supply voltage range permits direct operation from a variety of batteries without the need for a voltage regulator. For example, the MAX218 can be run directly from a single lithium cell or a pair of alkaline cells. It can also be run directly from two NiCd or NiMH cells from full-charge voltage down to the normal 0.9V/cell end-of-life point. The 4.25V maximum supply voltage allows the two rechargeable cells to be trickle- or fast-charged while driving the MAX218.

The circuit comprises three sections: power supply, transmitters, and receivers. The power-supply section converts the supplied input voltage to 6.5V, providing the voltages necessary for the drivers to meet true RS-232 levels. External components are small and inexpensive.

The transmitters and receivers are guaranteed to operate at 120kbps data rates, providing compatibility with LapLink™ and other high-speed communications software. A shutdown mode extends battery life by reducing supply current to 0.04µA. While shut down, all receivers can either remain active or be disabled under logic control. With this feature, the MAX218 can be in low-power shutdown mode and still monitor activity on external devices. Three-state drivers are provided on both receiver outputs.

Switch-Mode Power Supply

The switch-mode power supply uses a single inductor with one diode and three small capacitors to generate ±6.5V from an input voltage in the 1.8V to 4.25V range.

Inductor Selection

Use a 15µH inductor with a saturation current rating of at least 350mA and less than 1Ω resistance. Sample inductors are available from Maxim. Table 1 lists suppliers of inductors that meet the 15µH/350mA/1Ω specifications.

Diode Selection

Key diode specifications are fast recovery time (<10ns), average current rating (>100mA), and peak current rating (>350mA). Inexpensive fast silicon diodes, such as the 1N6050, are generally recommended. More expensive Schottky diodes improve efficiency and give slightly better performance at very low V_{DD} voltages. Table 1 lists suppliers of both surface-mount and through-hole diodes.

Capacitor Selection

Use capacitors with values at least as indicated in Figure 1. Capacitor C2 determines the ripple on V+, but not the absolute voltage. Capacitors C1 and C3 determine both the ripple and the absolute voltage of V-. Bypass V_{DD} to GND with at least 1µF (C4) placed close to pins 5 and 6. If the V_{DD} line is not bypassed elsewhere (e.g., at the power supply), increase C4 to 4.7µF.

It is not normally necessary to bypass REF. However, if the V_{DD} supply is noisy, bypass REF to GND with 0.1µF.

You may use ceramic or polarized capacitors in all locations. If you use polarized capacitors, tantalum types are preferred because of the high operating frequency of the power supplies (about 250kHz). If aluminum electrolytics are used, higher capacitance values may be required.

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Table 1. Suggested Component Suppliers

MANUFACTURER	PART NUMBER	PHONE	FAX
Inductors			
Murata	LQH4N150K-TA	USA (814) 237-1431 Japan (075) 951-9111	USA (814) 238-0490 Japan (075) 955-6526
Sumida	CD43150	USA (708) 956-0666 Japan (03) 3607-5111	USA (708) 956-0702 Japan (03) 3607-5428
TDK	NLC453232T-150K	USA (708) 803-6100 Japan (03) 3278-5111	USA (708) 803-6296 Japan (03) 3278-5358
Diodes—Surface Mount			
Central Semiconductor	CMPSH-3, Schottky	USA (516) 435-1110	USA (516) 435-1824
Motorola	MMBD6050LT1, Silicon	USA (408) 749-0510	USA (408) 991-7420
Philips	PMBD6050, Silicon	USA (401) 762-3800	USA (401) 767-4493
Diodes—Through-Hole			
Motorola	1N6050, Silicon 1N5817, Schottky	USA (408) 749-0510	USA (408) 991-7420

RS-232 Drivers

The two drivers are identical, and deliver EIA/TIA-232E and EIA/TIA-562 output voltage levels when V_{DD} is between 1.8V and 4.25V. The transmitters drive up to 3kΩ in parallel with 1000pF at up to 120kbps. Connect unused driver inputs to either GND or V_{DD}. Disable the drivers by taking $\overline{SHDN}$ low. The transmitter outputs are forced into a high-impedance state when $\overline{SHDN}$ is low.

RS-232 Receivers

The two receivers are identical, and accept both EIA/TIA-232E and EIA/TIA-562 input signals. The CMOS receiver outputs swing rail-to-rail. When EN is high, the receivers are active regardless of the state of $\overline{SHDN}$. When EN is low, the receiver outputs are put into a high-impedance state. This allows two RS-232 ports (or two ports of different types) to be wired-ORed at the UART.

Operating Modes

$\overline{SHDN}$ and EN determine the MAX218's mode of operation, as shown in Table 2.

Table 2. Operating Modes

$\overline{SHDN}$	EN	RECEIVER OUTPUT	DRIVER OUTPUT	DC-DC CONVERTER	SUPPLY CURRENT
L	L	High-Z	High-Z	OFF	Minimum
L	H	Enabled	High-Z	OFF	Minimum
H	L	High-Z	Enabled	ON	Normal
H	H	Enabled	Enabled	ON	Normal

Shutdown

When $\overline{SHDN}$ is low, the power supplies are disabled and the transmitters are put into a high-impedance state. Receiver operation is not affected by taking $\overline{SHDN}$ low. Power consumption is dramatically reduced in shutdown mode. Supply current is minimized when the receiver inputs are static in any of three states: floating (ground), GND, or V_{DD}.

Applications Information

Operation from Regulated/Unregulated Dual System Power Supplies

The MAX218 is intended for use with three different power-supply sources: it can be powered directly from a battery, from a 3.0V or 3.3V power supply, or simultaneously from both. Figure 1 shows the single-supply configuration. Figure 2 shows the circuit for operation from both a 3V supply and a raw battery supply—an ideal configuration where a regulated 3V supply is being derived from two cells. In this application, the MAX218's logic levels remain appropriate for interface with 3V logic, yet most of the power for the MAX218 is drawn directly from the battery, without suffering the efficiency losses of the DC-DC converter. This prolongs battery life.

Bypass the input supplies with 0.1µF at V_{DD} (C4) and at least 1µF at the inductor (C5). Increase C5 to 4.7µF if the power supply has no other bypass capacitor connected to it.

1.8V to 4.25V-Powered, True RS-232 Dual Transceiver

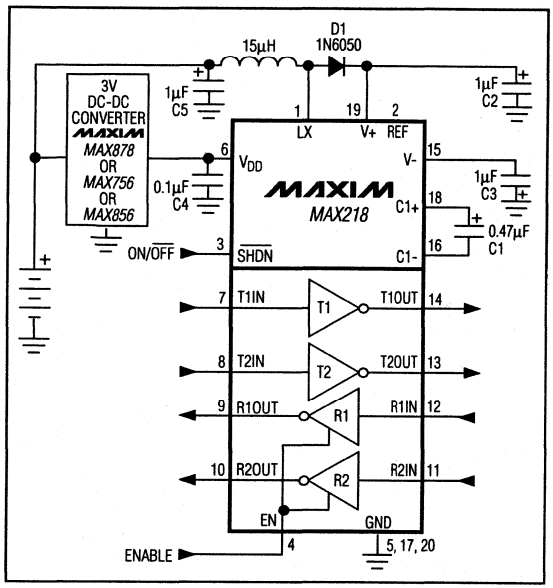


Figure 2. Operating from Unregulated and Regulated Supplies

Low-Power Operation

The following suggestions will help you get maximum life out of your batteries.

Shut the MAX218 down when it is not being used for transmission. The receivers can remain active when the MAX218 is shut down, to alert your system to external activity.

Transmit at the highest practical data rate. Although this raises the supply current while transmission is in progress, the transmission will be over sooner. As long as the MAX218 is shut down as soon as each transmission ends, this practice will save energy.

Operate your whole system from the raw battery voltage rather than suffer the losses of a regulator or DC-DC converter. If this is not possible, but your system is powered from two cells and employs a 3V DC-DC converter to generate the main logic supply, use the circuit of Figure 2. This circuit draws most of the MAX218's power straight from the battery, but still provides logic-level compatibility with the 3V logic.

Keep communications cables short to minimize capacitive loading. Lowering the capacitive loading on the transmitter outputs reduces the MAX218's power consumption. Using short, low-capacitance cable also helps transmission at the highest data rates.

Keep the $\overline{SHDN}$ pin low while power is being applied to the MAX218, and take $\overline{SHDN}$ high only after V_{DD} has risen above about 1.5V. This avoids active operation at very low voltages, where currents of up to 150mA can be drawn. This is especially important with systems powered from rechargeable cells; if $\overline{SHDN}$ is high while the cells are being trickle charged from a deep discharge, the MAX218 could draw a significant amount of the charging current until the battery voltage rises above 1.5V.

EIA/TIA-232E and EIA/TIA-562 Standards

RS-232 circuits consume much of their power because the EIA/TIA-232E standard demands that the transmitters deliver at least 5V to receivers with impedances that can be as low as 3kΩ. For applications where power consumption is critical, the EIA/TIA-562 standard provides an alternative.

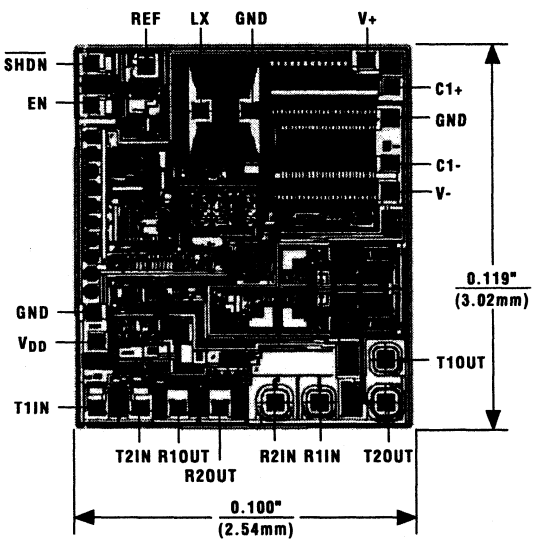
EIA/TIA-562 transmitter output voltage levels need only reach ±3.7V, and because they have to drive the same 3kΩ receiver loads, the total power consumption is considerably reduced. Since the EIA/TIA-232E and EIA/TIA-562 receiver input voltage thresholds are the same, interoperability between EIA/TIA-232E and EIA/TIA-562 devices is guaranteed. Maxim's MAX560 and MAX561 are EIA/TIA-562 transceivers that operate on a single supply from 3.0V to 3.6V, and the MAX562 transceiver operates from 2.7V to 5.25V while producing EIA/TIA-562 levels.

1.8V to 4.25V-Powered, True RS-232 Dual Transceiver

3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

PART	POWER SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/ RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	GUARANTEED DATA RATE (kbps)	EIT/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	120	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	120	232	Operates directly from batteries without a voltage regulator
MAX560	3.0 to 3.6	4/5	2	120	562	Pin compatible with MAX213
MAX561	3.0 to 3.6	4/5	0	120	562	Pin compatible with MAX241
MAX562	2.7 to 5.25	3/5	5	230	562	Wide supply range
MAX563	3.0 to 3.6	2/2	2	120	562	0.1µF capacitors

Chip Topography



TRANSISTOR COUNT: 571;
SUBSTRATE CONNECTED TO GND.

19-4323; Rev 3; 5/94

MAXIM

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

General Description

The MAX220-MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, and in particular, for those applications where ±12V is not available.

These parts are particulary useful in battery-powered systems since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225, MAX233, MAX235, and MAX245-MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

Superior to Bipolar

- **Operate from Single +5V Power Supply (+5V and +12V—MAX231 and MAX239)**
- **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- **Meet All EIA/TIA-232E and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **3-State Driver and Receiver Outputs**
- **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	4.7/10	No		120	Ultra low-power, industry-standard pinout
MAX222	+5	2/2/	4	0.1	Yes		200	+5V IBM PC serial port with receivers active in shutdown
MAX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	✔	120	MAX241 + receivers active in shutdown
MAX225	+5	5/5	0	–	Yes	✔	120	Available in SO
MAX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes		120	5 drivers with shutdown
MAX231 (MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0 (0.1)	No		120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No		120 (64)	Industry standard
MAX232A	+5	2/2	4	0.1	No		200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0	–	No		120	No external caps
MAX233A	+5	2/2	0	–	No		200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No		120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0	–	Yes		120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes		120	Shutdown, three-state
MAX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No		120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No		120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0 (0.1)	No		120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes		120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes		120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✔	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No		200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No		120	High slew rate
MAX245	+5	8/10	0	–	Yes	✔	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	–	Yes	✔	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	–	Yes	✔	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	✔	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	✔	120	Available in quad flatpack package

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
T_{OUT} (Note 1) ..... ±15V
Output Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Driver/Receiver Output Short Circuited to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _ ..... 0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ ..... -40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Normal operation			5	40	µA
	$\overline{SHDN}$ = 0V, MAX222/242, shutdown			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate	Except MAX220, normal operation			200	116	kbits/ sec
	MAX220			22	20	
Transmitter Output Resistance	V_{CC} = V+ V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	Except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	Except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	Except MAX243, V_{CC} = 5V, no hyst. in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{EN}$ Input Threshold Low	MAX242			1.4	0.8	V
$\overline{EN}$ Input Threshold High	MAX242		2.0	1.4		V
POWER SUPPLY						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5, 6, 9, 19	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both outputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0° to +70°C		2	50	
		T_A = -40° to +85°C		2	50	
		T_A = -55° to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current	MAX222/242				±1	µA
$\overline{SHDN}$ Threshold Low	MAX222/242			1.4	0.8	V
$\overline{SHDN}$ Threshold High	MAX222/242		2.0	1.4		V
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TLL to RS-232 (Normal Operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TLL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TLL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ goes High), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes Low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLR} - t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

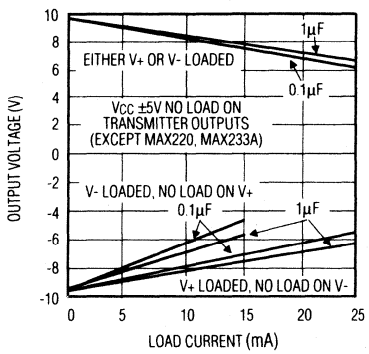
Note 2: MAX243 $R2_{OUT}$ is guaranteed to be low when $R2_{IN}$ is ≥ 0V or is floating.

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

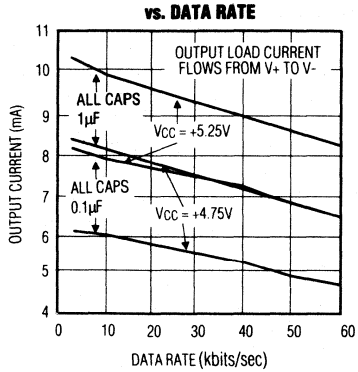
Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243

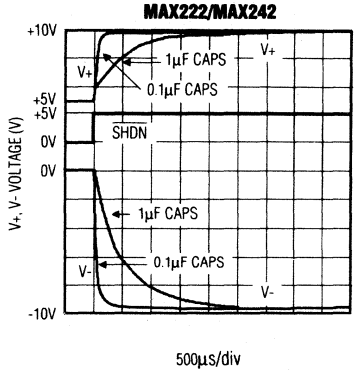
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



ON-TIME EXITING SHUTDOWN – MAX222/MAX242



ABSOLUTE MAXIMUM RATINGS—MAX223/MAX230-MAX241

V_{CC} .....-0.3V to +6V
V+ .....(V_{CC} - 0.3V) to +14V
V- .....+0.3V to -14V
Input Voltages
T_{IN} .....-0.3V to (V_{CC} + 0.3V)
R_{IN} .....±30V
Output Voltages
T_{OUT} .....(V+ + 0.3V) to (V- - 0.3V)
R_{OUT} .....-0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_{OUT} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C).....1067mW
24-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 500mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) 941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1000mW
44-Pin Plastic FP (derate 11.11mW/°C above +70°C).....889mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
24-Pin Narrow CERDIP
(derate 12.50mW/°C above +70°C).....1000mW
24-Pin Sidebraze (derate 20.0mW/°C above +70°C) 1600mW
28-Pin SSOP (derate 9.52mW/°C above +70°C).....762mW
Operating Temperature Ranges
MAX2_ _C_ _.....0°C to +70°C
MAX2_ _E_ _.....-40°C to +85°C
MAX2_ _M_ _.....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10 sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX223/MAX230-MAX241

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 30kΩ to ground		±5.0	±7.3		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX232/233		5	10	mA
		MAX232/230/234-238/240/241		7	15	
		MAX231/239		.4	1	
V+ Power-Supply Current		MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	T_A = +25°C	MAX223		15	50	µA
		MAX241		1	10	
Input Logic Threshold Low	T_{IN}; EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX230/235-241)				0.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX230/235-241)		2.4			
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
Receiver Input Voltage Operating Range			-30		+30	V

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

ELECTRICAL CHARACTERISTICS — MAX223/MAX230-MAX241 (continued)

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

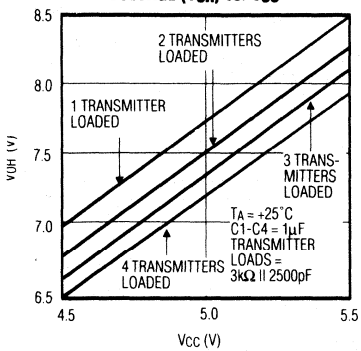
PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235-MAX241)		0.8	1.2		V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)		0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235-MAX241)			1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)			1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V; no hysteresis in shutdown			0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233 I_{OUT} = 3.2mA)					0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = 1.0mA			3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX235-241)				0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223			600		ns
		MAX235-MAX241			400		
Receiver Output Disable Time	Normal operation	MAX223			900		ns
		MAX235-MAX241			250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF	Normal operation			0.5	10	µs
		$\overline{SHDN}$ = 0V (MAX223)	tPHLS		4	40	
			tPLHS		6	40	
Transition Region Slew Rate	MAX223/MAX230/MAX234-241 T_A = +25°C, V_{CC} = 5V R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			3	5.1	30	V/µs
	MAX231/MAX232/MAX233 T_A = +25°C, V_{CC} = 5V R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V				4	30	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V			300			Ω
Receiver Out Short-Circuit Current					±10		mA

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

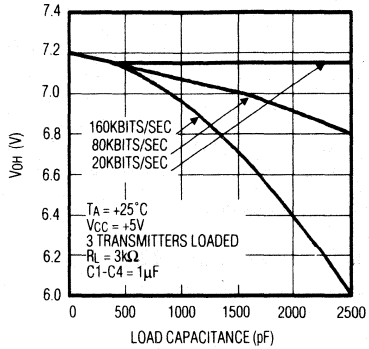
Typical Operating Characteristics

MAX223/MAX230/MAX234-241

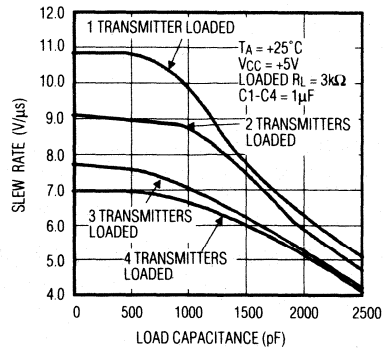
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



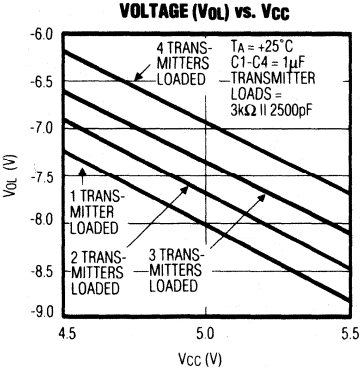
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



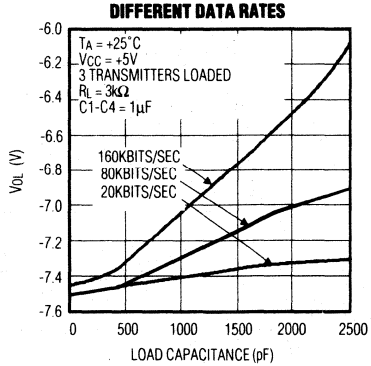
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



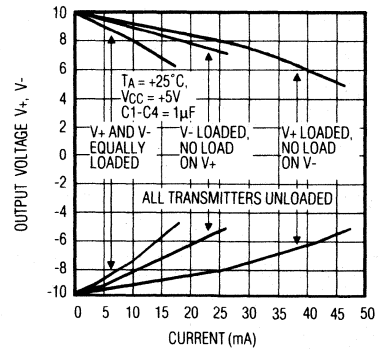
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



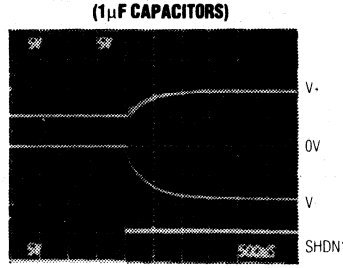
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE V+, V- vs. LOAD CURRENT



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY IS REVERSED FOR THE MAX241

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX225/MAX244-MAX249

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN}, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENR}$, $\overline{ENT}$, $\overline{ENRA}$, $\overline{ENRB}$, $\overline{ENTA}$, $\overline{ENTB}$ ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±25V
T_{OUT} (Note 3) ..... ±15V
R_{OUT} ..... -0.3V to (VCC + 0.3V)
Short Circuit (1 output at a time)
T_{OUT} to GND ..... Continuous
R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ..1000mW
40-Pin Plastic DIP (derate 11.11mW/°C above +70°C) .611mW
44-Pin PLCC (derate 13.33mW/°C above +70°C) 1067mW
Operating Temperature Ranges:
MAX225C _ _, MAX24_C_ _ ..... 0°C to +70°C
MAX225E _ _, MAX24_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 3: Input Voltage measured with transmitter output in a high-impedance state, shutdown, or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX225/MAX244-MAX249

(MAX225 V_{CC} = 5.0V ±5%; MAX244-MAX249 V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Tables1A-1D	Normal operation		10	50	µA
		Shutdown		±0.01	±1	
Data Rate	Tables1A-1D, Normal operation			120	64	kbits/sec
Output Voltage Swing	All transmitter outputs loaded with 3Ωk to GND		±5	±7.5		V
Output Leakage Current (Shutdown)	Tables1A-1D	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENT}$, $\overline{ENTA}$, $\overline{ENTB}$ = V_{CC}		±0.01	±25	µA
				±0.01	±25	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 4)		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±30		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±25	V
RS-232 Input Threshold Low	V_{CC} = 5V		0.8	1.3		V
RS-232 Input Threshold High	V_{CC} = 5V			1.8	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled, Tables 1A-1D, 0V ≤ V_{OUT} ≤ V_{CC}, $\overline{ENR\_}$ = V_{CC}			±0.05	±0.10	µA

ELECTRICAL CHARACTERISTICS—MAX225/MAX244-MAX249 (continued)

(MAX225 V_{CC} = 5.0V ±5%; MAX244-MAX249 V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

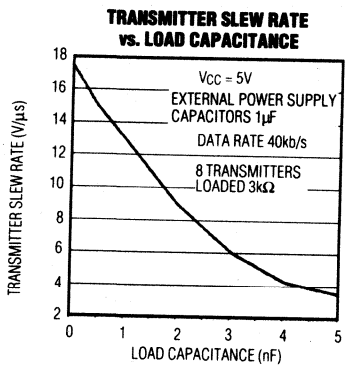
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC						
Operating Supply Voltage		MAX225	4.75		5.25	V
		MAX244-MAX249	4.5		5.5	
V_{CC} Supply Current (Normal Operation)	No Load	MAX225		10	20	mA
		MAX244-MAX249		11	30	
	3kΩ loads on all outputs	MAX225		40		
		MAX244-MAX249		57		
Shutdown Supply Current	T_A = +25°C			8	25	µA
	T_A = T_{MIN} to T_{MAX}				50	
Control Input	Leakage Current				±1	µA
	Threshold Low			1.4	0.8	V
	Threshold High		2.4	1.4		
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V		5	10	30	V/µs
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}			1.3	3.5	µs
	t_{PLHT}			1.5	3.5	
Receiver Propagation Delay TTL to RS-232 (Normal Operation), Figure 2	t_{PHLR}			0.6	1.5	µs
	t_{PLHR}			0.6	1.5	
Receiver Propagation Delay TTL to RS-232 (Low Power Mode), Figure 2	t_{PHLS}			0.6	10	µs
	t_{PLHS}			3.0	10	
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver-Output Enable Time, Figure 3	t_{ER}			100	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}			100	500	ns
Transmitter Enable Time	t_{ET}	MAX246-249 (excludes charge-pump startup)		5		µs
		MAX225/MAX245-MAX249 (includes charge-pump startup)		10		ms
Transmitter Disable Time, Figure 4	t_{DT}			100		ns

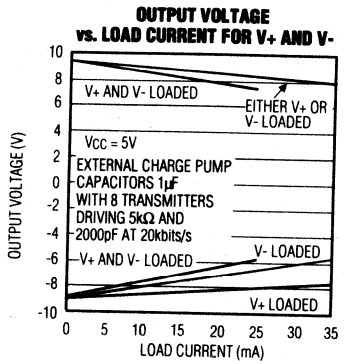
Note 4: The 300Ω minimum specification complies with EIA/TIA-232E, but the actual resistance when in shutdown mode or V_{CC} = 0 is 10MΩ as is implied by the leakage specification.

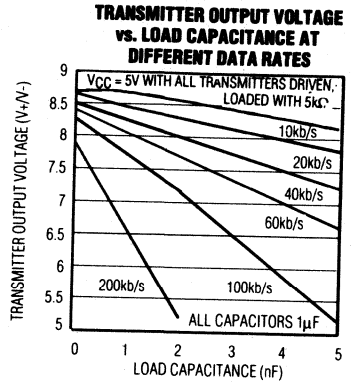
+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

Typical Operating Characteristics

MAX225/MAX244-MAX249







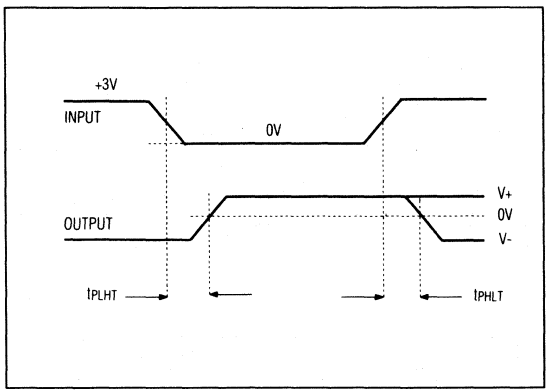


Figure 1. Transmitter Propagation Delay Timing

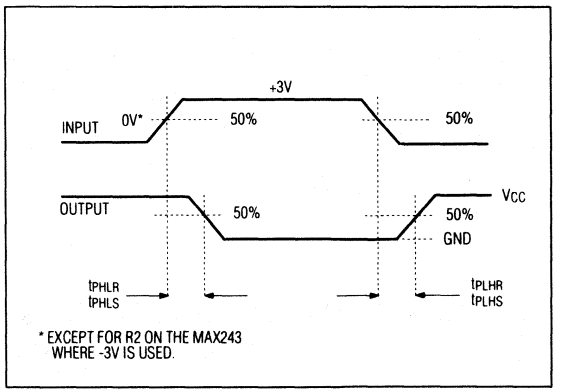


Figure 2. Receiver Propagation Delay Timing

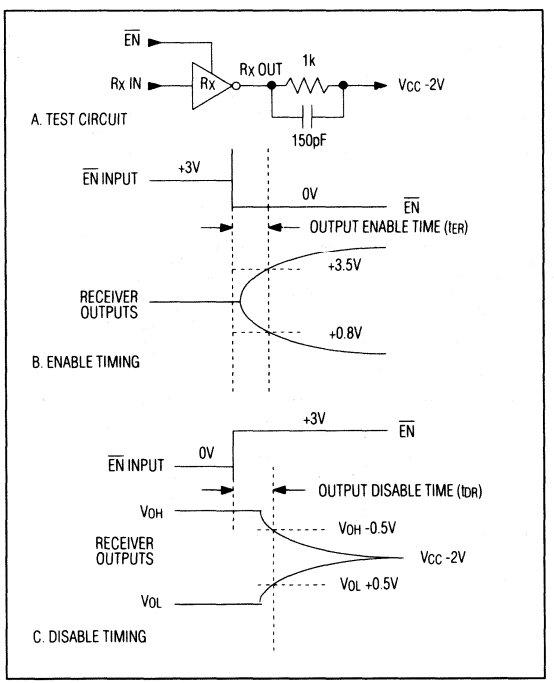


Figure 3. Receiver-Output Enable and Disable Timing

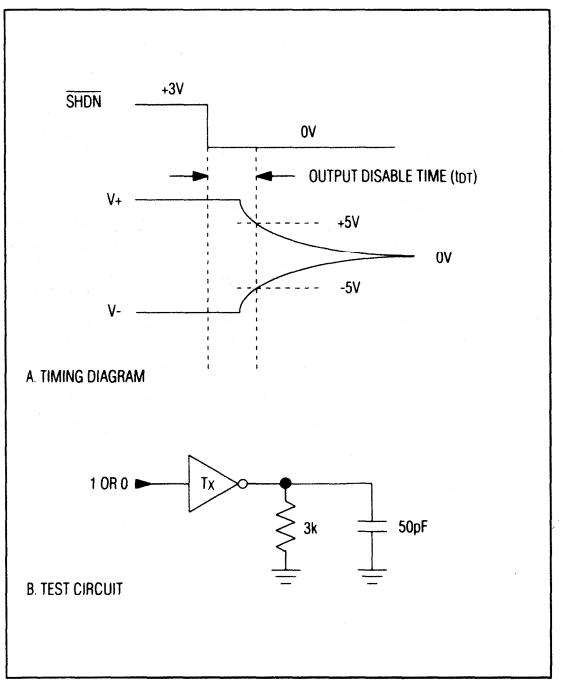


Figure 4. Transmitter-Output Disable Timing

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

Table 1a. MAX225 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS	RECEIVERS
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All 3-State
1	0	Shutdown	All 3-State	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State

Table 1b. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1-RA4 3-State RA5 Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low Power Receiver Mode	All Low Power Receiver Mode
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receiver Mode	RB1-RB4 3-State RA5 Low-Power Receiver Mode

Table 1c. MAX246 Control Pin Configurations

$\overline{ENA}$	$\overline{ENB}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All Active	RA1-RA4 3-State RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receiver Mode	RB1-RB4 3-State RA5 Low-Power Receiver Mode

Table 1d. MAX247/248/249 Control Pin Configurations

ENTA	ENTB	ENRA	ENRB	OPERATION STATUS		TRANSMITTERS		RECEIVERS	
					MAX247	TA1–TA4	TB1–TB4	RA1–RA4	RB1–RB5
					MAX248	TA1–TA4	TB1–TB4	RA1–RA4	RB1–RB4
					MAX249	TA1–TA3	TB1–TB3	RA1–RA5	RB1–RB5
0	0	0	0	Normal Operation		All Active	All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All Active	All 3-State, except RB5 stays active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State	All Active
0	0	1	1	Normal Operation		All Active	All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All Active	All 3-State, except RB5 stays active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State	All Active
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State	All 3-State, except RB5 stays active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All Active	All 3-State, except RB5 stays active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State	All Active
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	All 3-State, except RB5 stays active on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State	All 3-State, except RB5 stays active on MAX247

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

Detailed Description

The MAX220-MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX220-MAX249 have two internal charge-pumps that convert +5V to ±10V (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see *Typical Operating Characteristics*), except on the MAX225 and MAX245-MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA/TIA-232E driver output voltage when sourcing current from V+ and V- to external circuitry.

When using the shutdown feature in the MAX222, MAX225, MAX230, MAX235, MAX236, MAX240, MAX241 and MAX245-MAX249 avoid using V+ and V- to power external circuitry. When these parts are shut down, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ is internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA/TIA-232E and V.28 specification, that calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built-in. The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode.

The MAX239 has a receiver 3-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low-power shutdown control. The receiver TTL/CMOS outputs are in a high-impedance 3-state mode whenever the 3-state $\overline{EN}$able line is high, and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less then 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/µs unloaded and 10V/µs loaded with 3Ω and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA/TIA-232E.

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

The low-power receive-mode feature of the MAX223, MAX242, and MAX245-MAX249 puts the IC into shutdown mode, but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates. This operation conserves system power.

MAX243—Negative Threshold

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA/TIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Shutdown—MAX222-MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$) that allows receiver output control independent of $\overline{SHDN}$. With all other devices, $\overline{SHDN}$ also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. Both devices have separate receiver and transmitter-enable controls. The charge pumps turn off and the devices shutdown when a logic high is applied to the $\overline{ENT}$ input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the $\overline{ENR}$ input. On the MAX245, eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1-RA4 and RB1-RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

Receiver and Transmitter Enable Control Inputs

The MAX225 and MAX245-MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

Tables 1A-1D define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled, ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

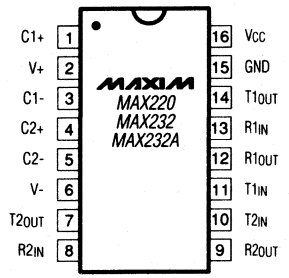
The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/s.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

TOP VIEW



DIP/SO

CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

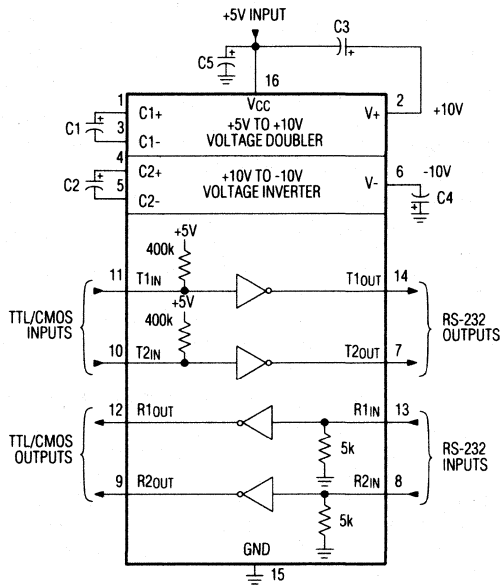
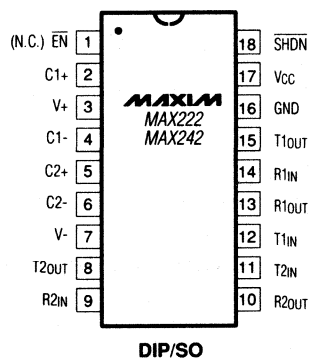


Figure 5. MAX220/232/232A Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP/SO

( ) ARE FOR MAX222 ONLY.

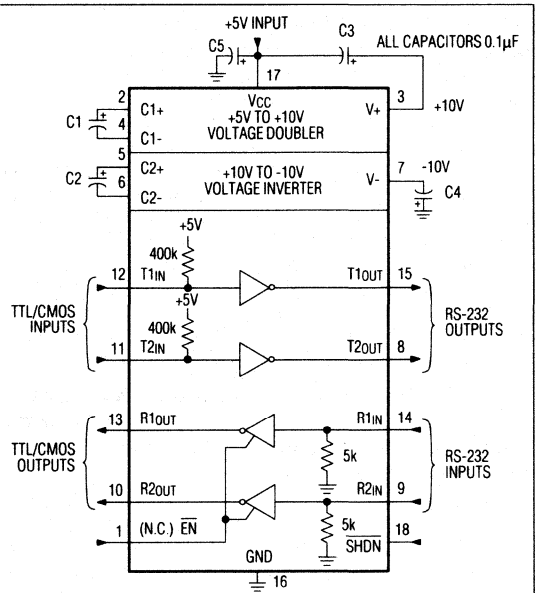


Figure 6. MAX222/MAX242 Pin Configuration and Typical Operating Circuit

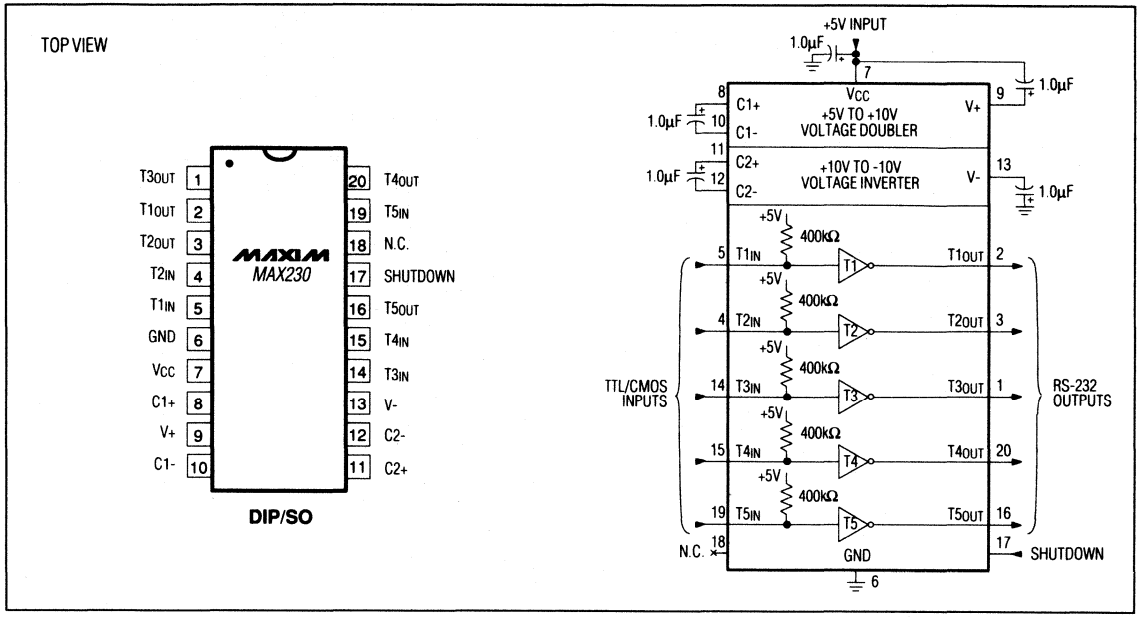


Figure 7. MAX230 Pin Configuration and Typical Operating Circuit

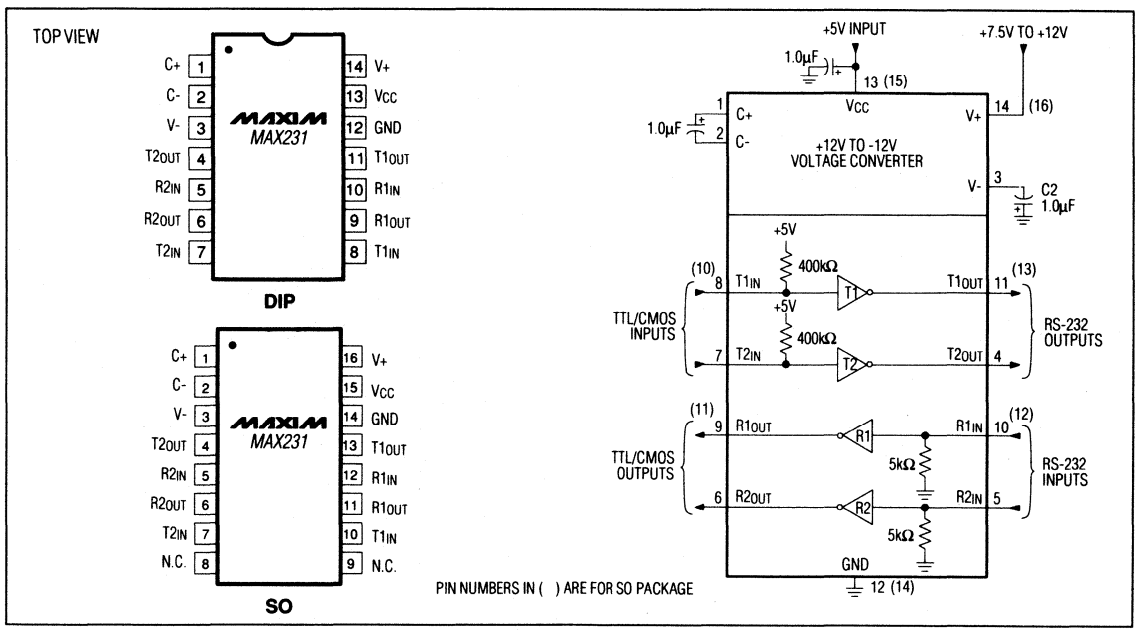


Figure 8. MAX230 Pin Configurations and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

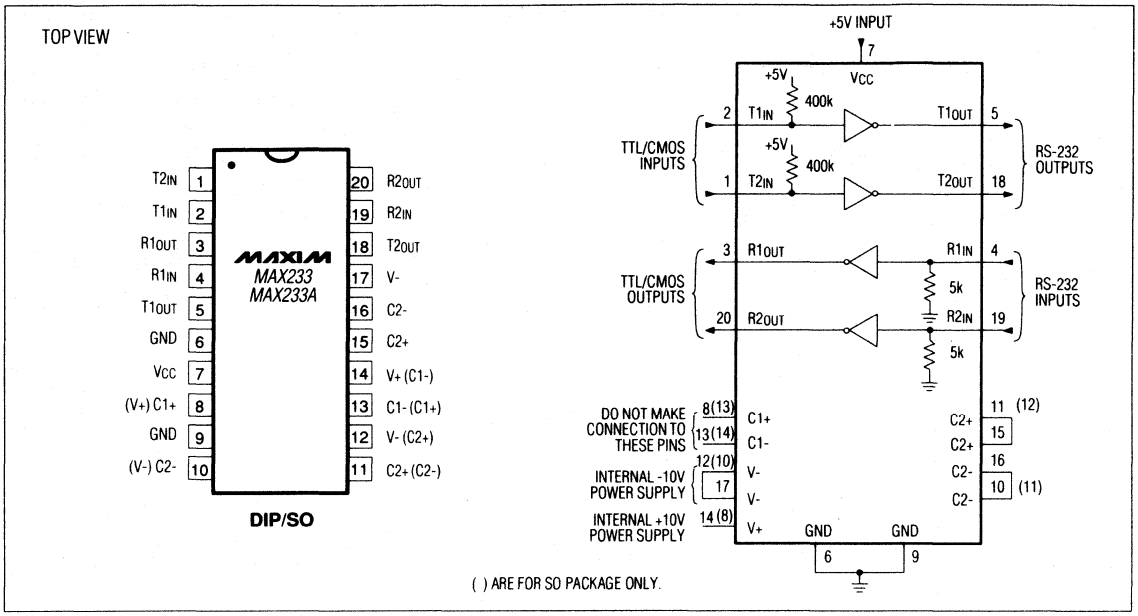


Figure 9. MAX233/MAX233A Pin Configuration and Typical Operating Circuit

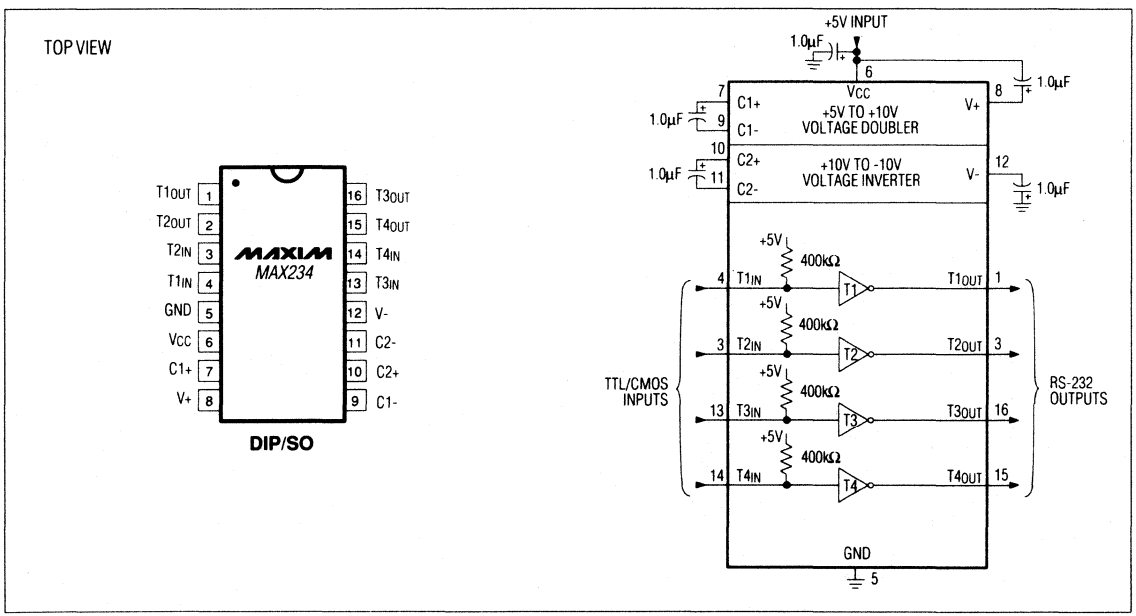
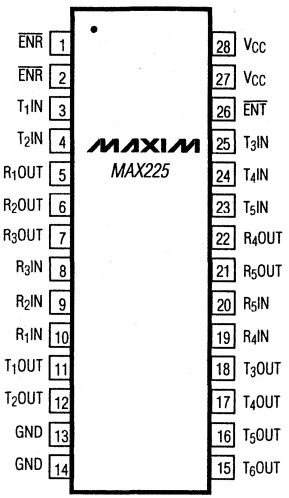


Figure 10. MAX234 Pin Configuration and Typical Operating Circuit

TOP VIEW



SO

MAX225 Functional Description

5 Receivers

5 Transmitters

2 Control Pins

1 Receiver Enable ($\overline{ENR}$)

1 Transmitter Enable ($\overline{ENT}$)

PINS ($\overline{ENR}$, GND, V_{CC}, T_5OUT) ARE INTERNALLY CONNECTED. CONNECT EITHER OR BOTH EXTERNALLY. T_5OUT IS A SINGLE DRIVER.

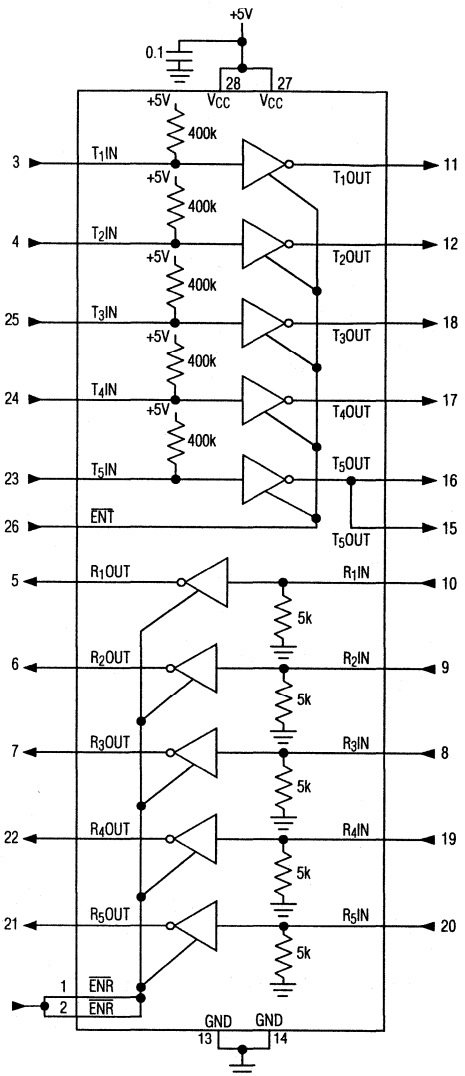


Figure 11. MAX225 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

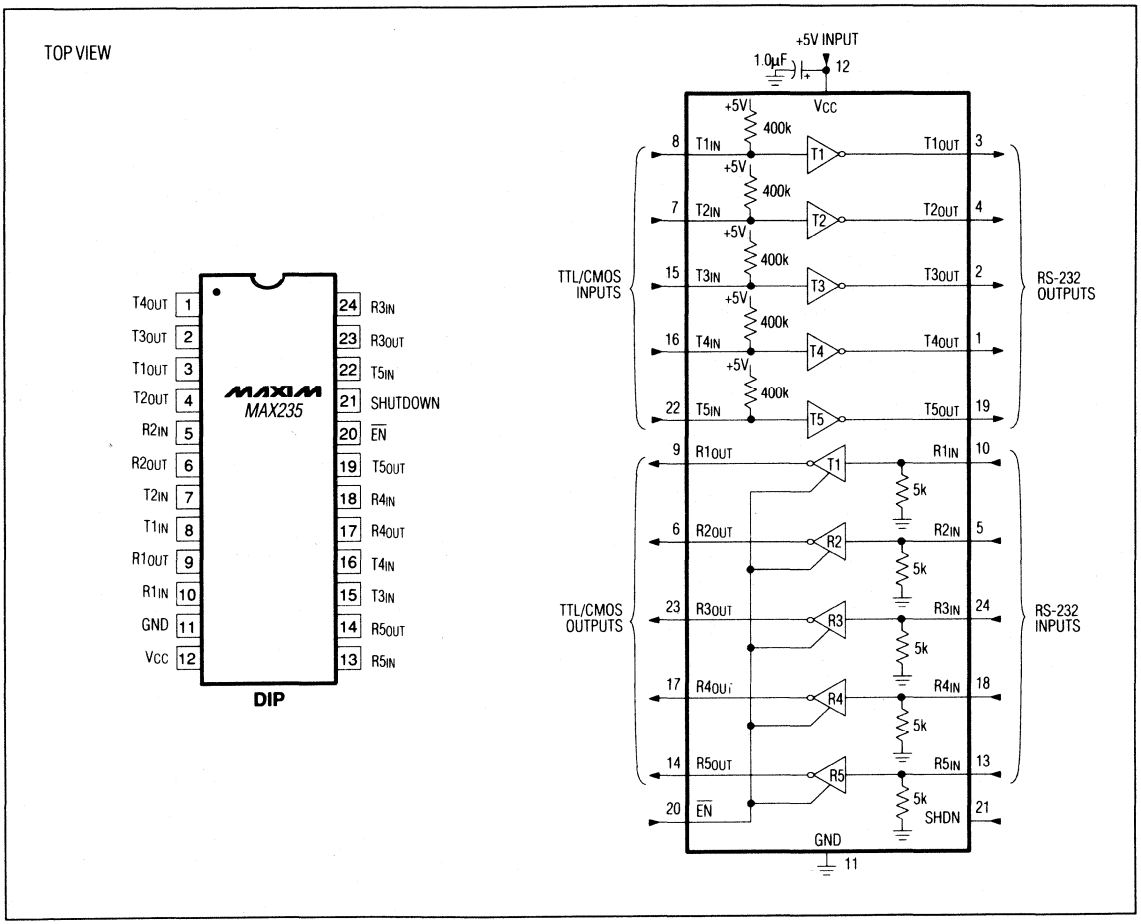


Figure 12. MAX235 Pin Configuration and Typical Operating Circuit

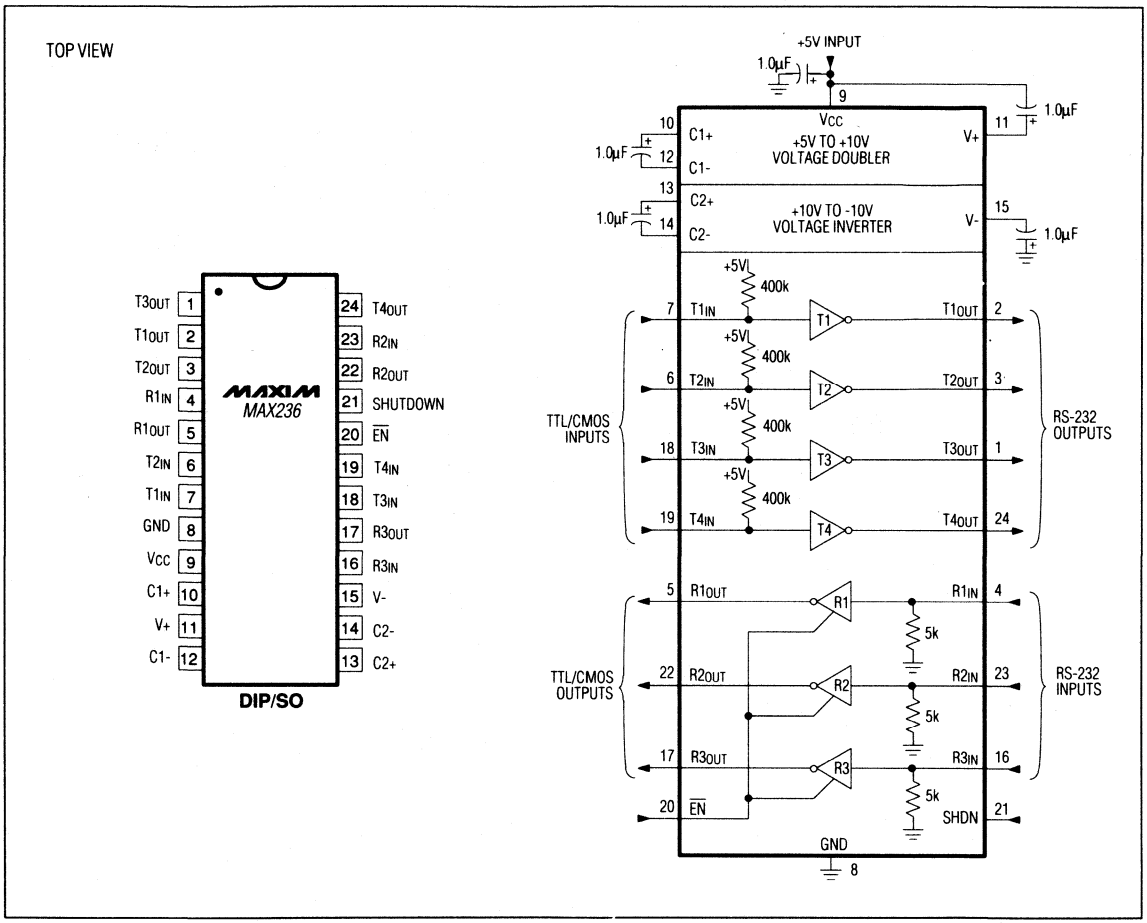


Figure 13. MAX236 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

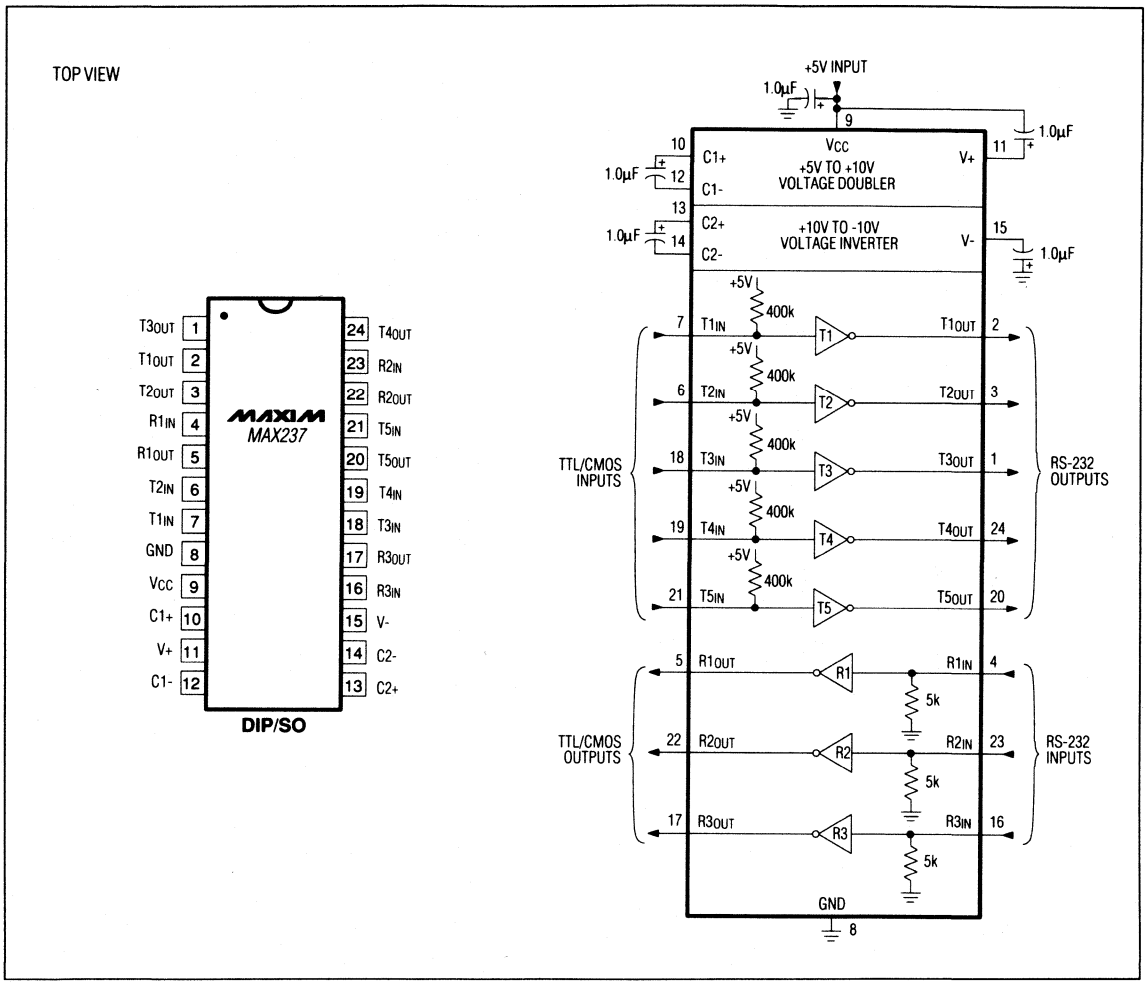


Figure 14. MAX237 Pin Configuration and Typical Operating Circuit

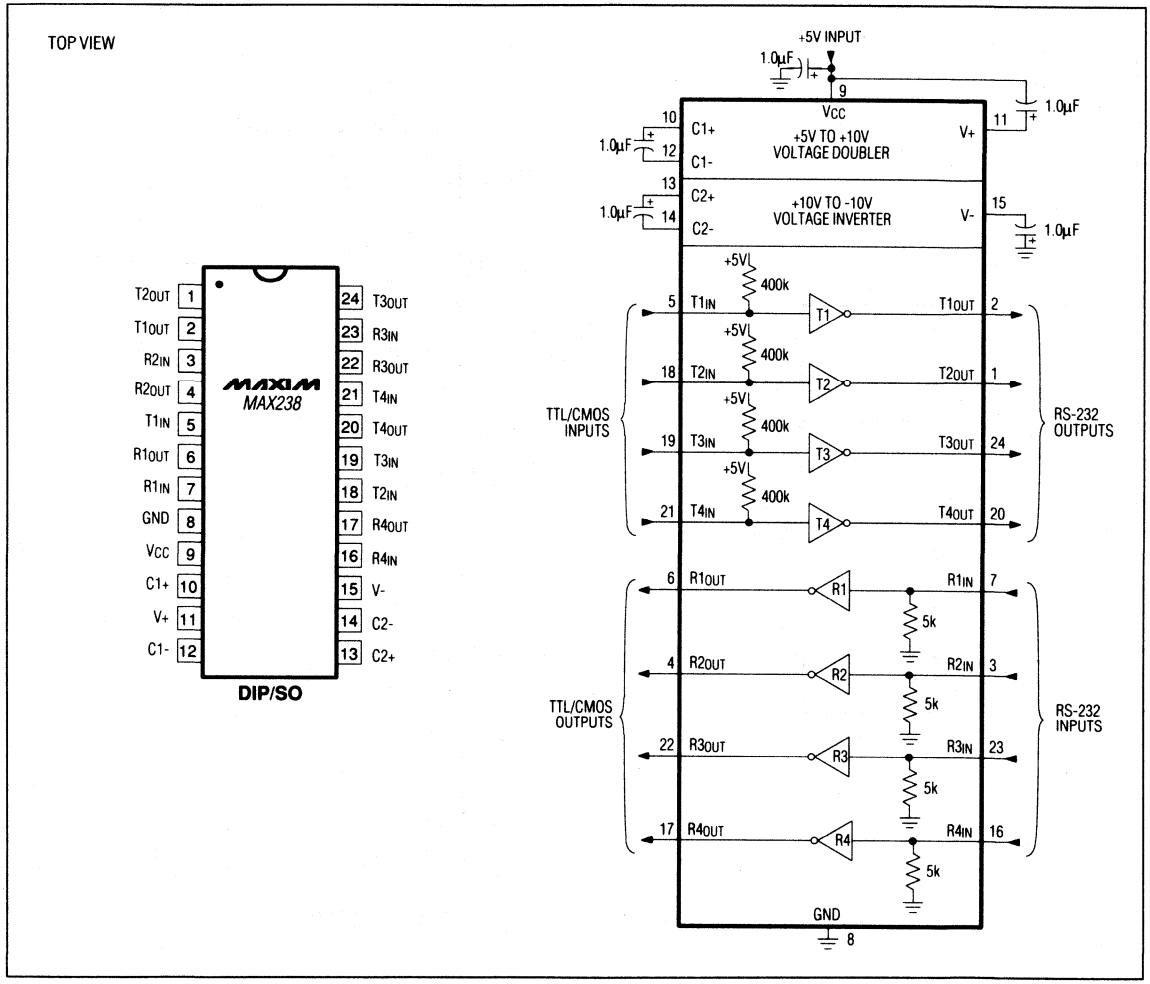


Figure 15. MAX238 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

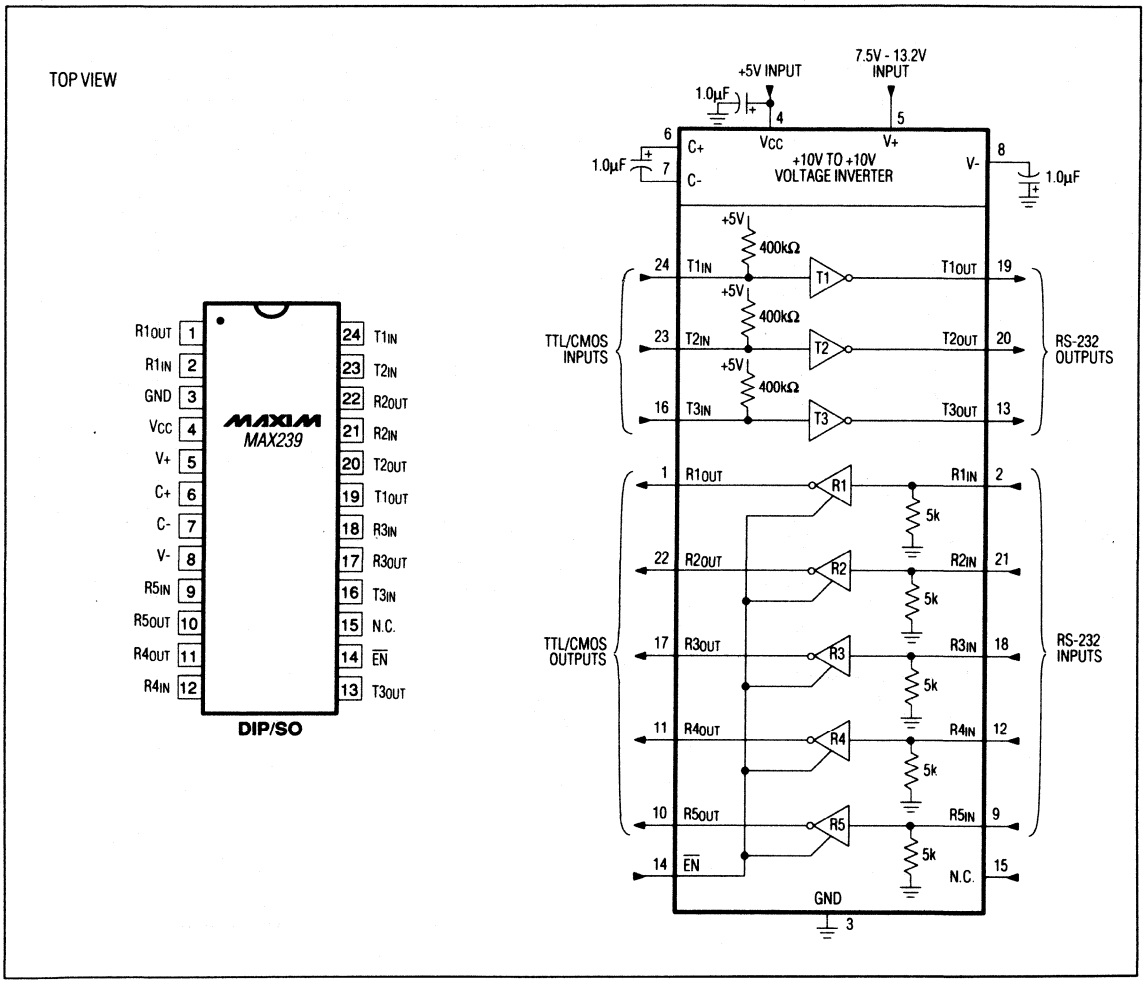


Figure 16. MAX239 Pin Configuration and Typical Operating Circuit

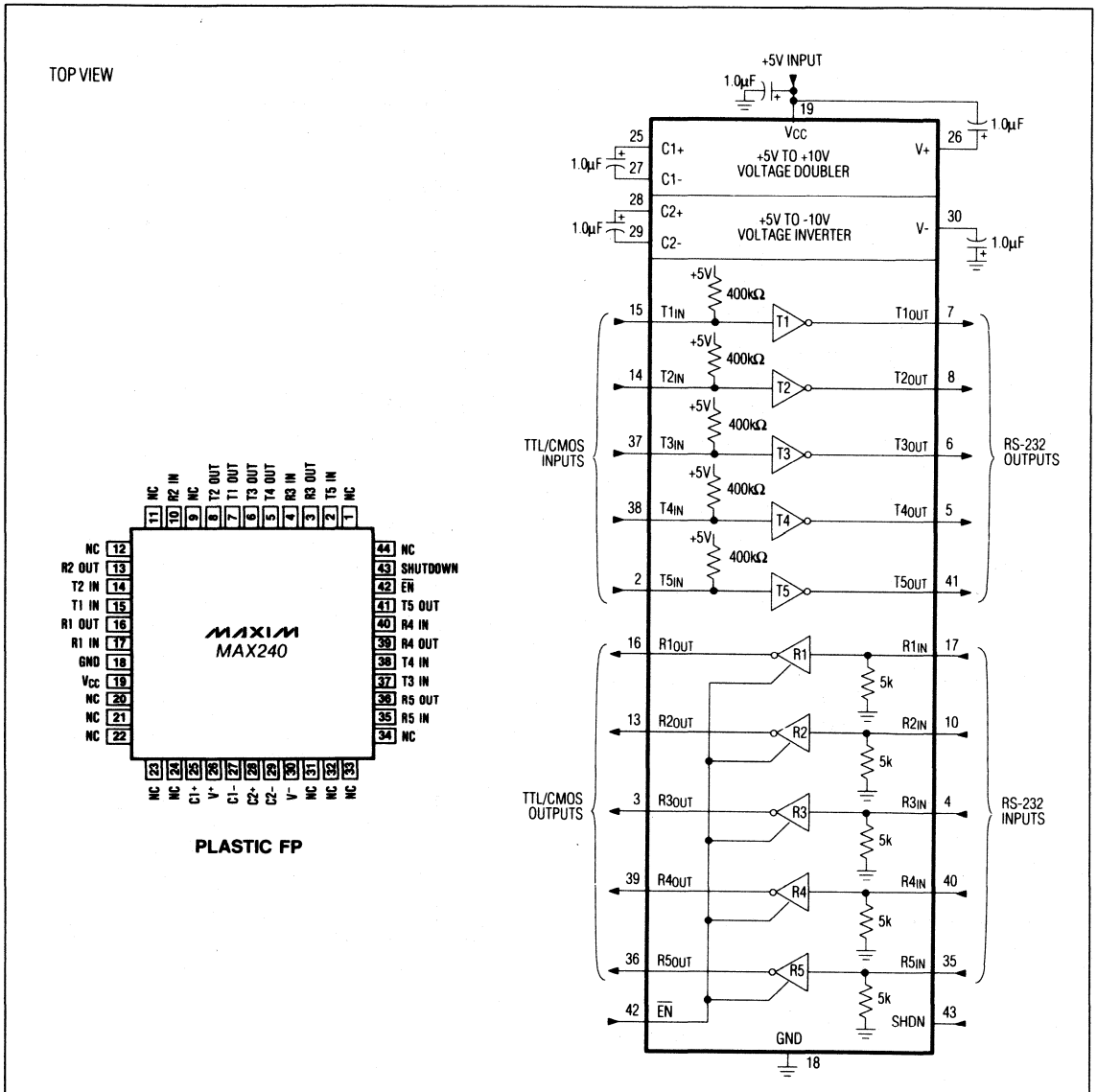


Figure 17. MAX240 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

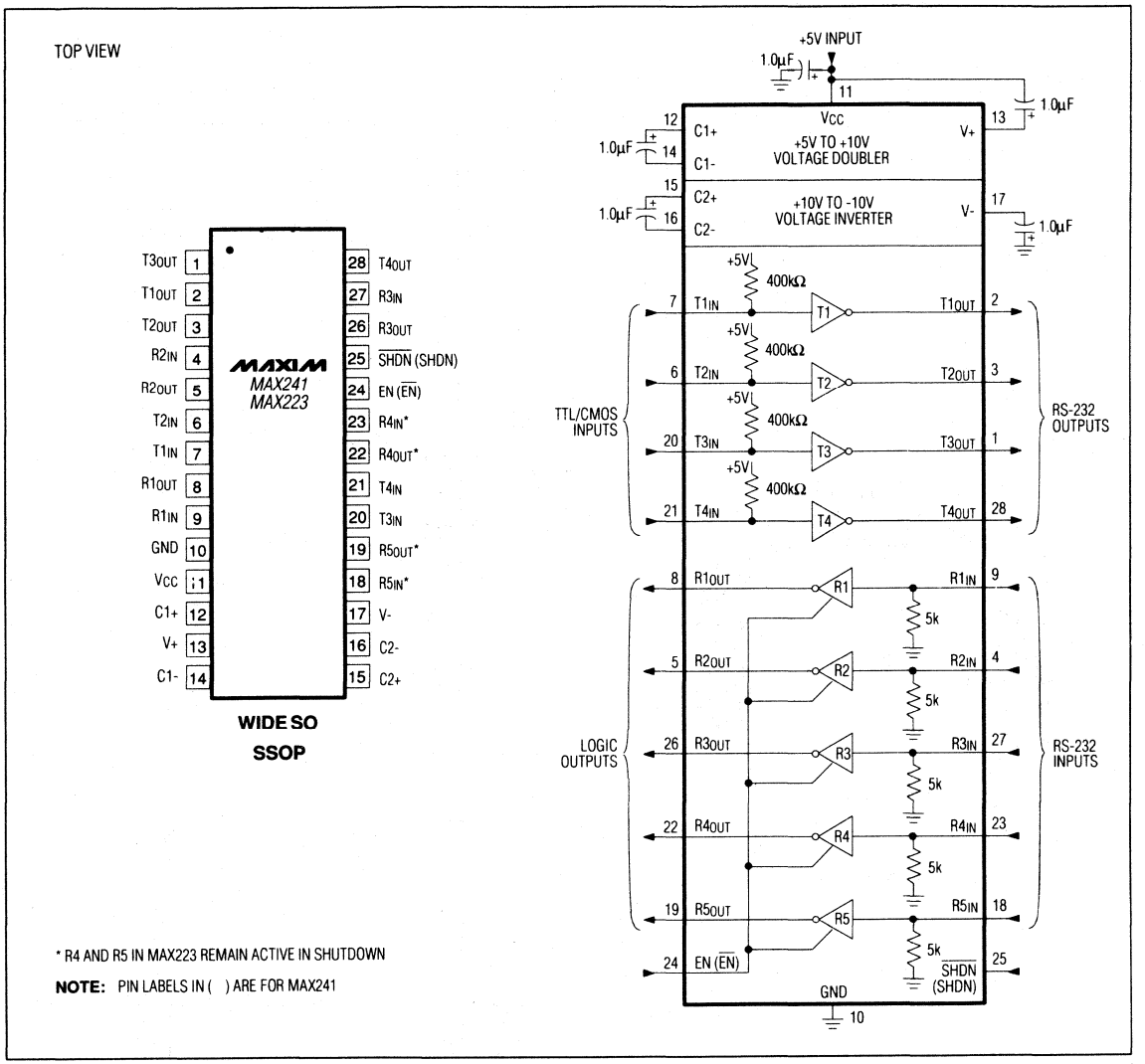
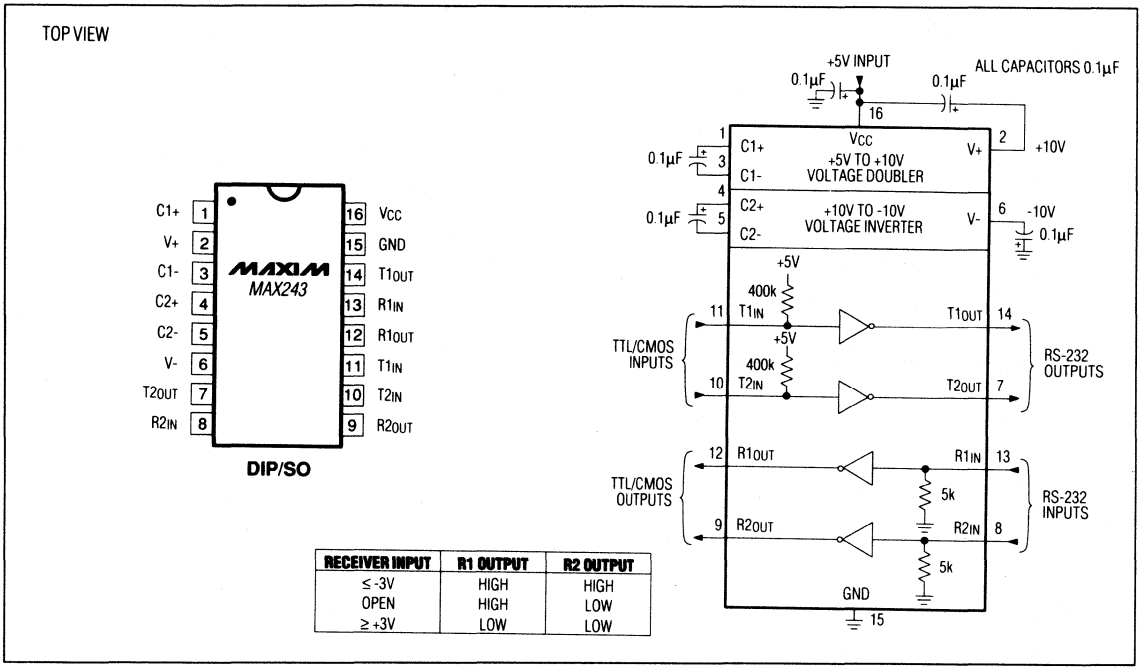


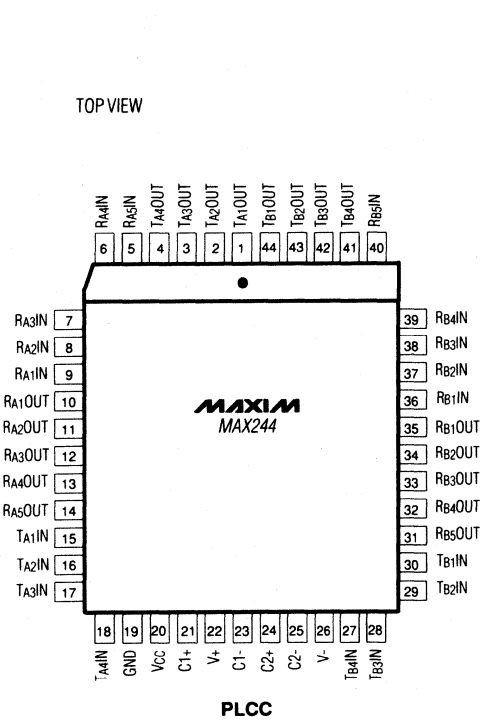
Figure 18. MAX241, MAX223 Pin Configuration and Typical Operating Circuit



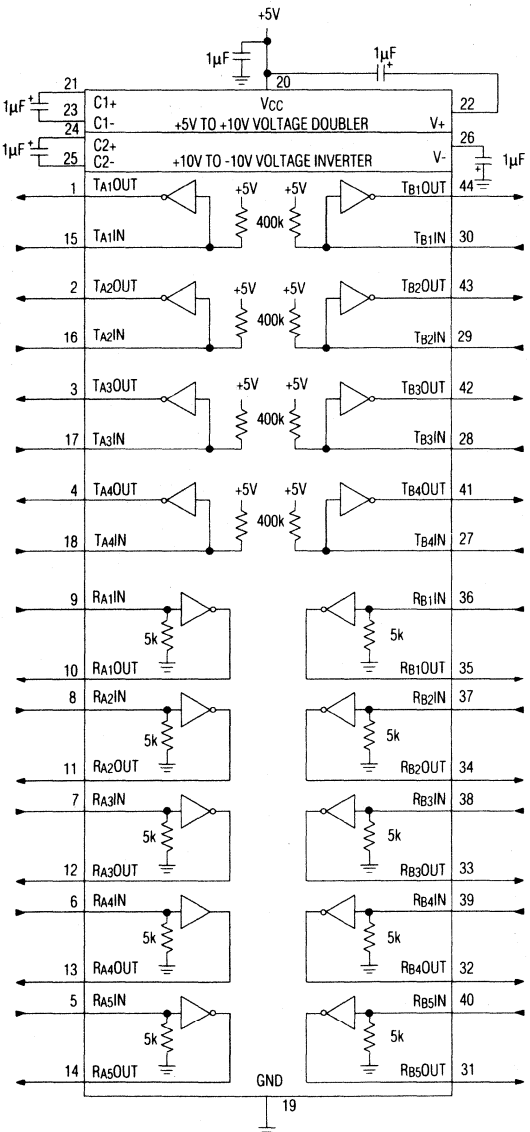
RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

Figure 19. MAX243 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers



PLCC



MAX244 Functional Description

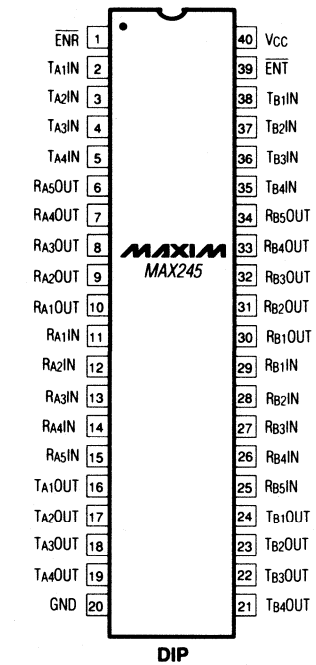
10 Receivers Always Active
- 5 A-Side Receivers
- 5 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

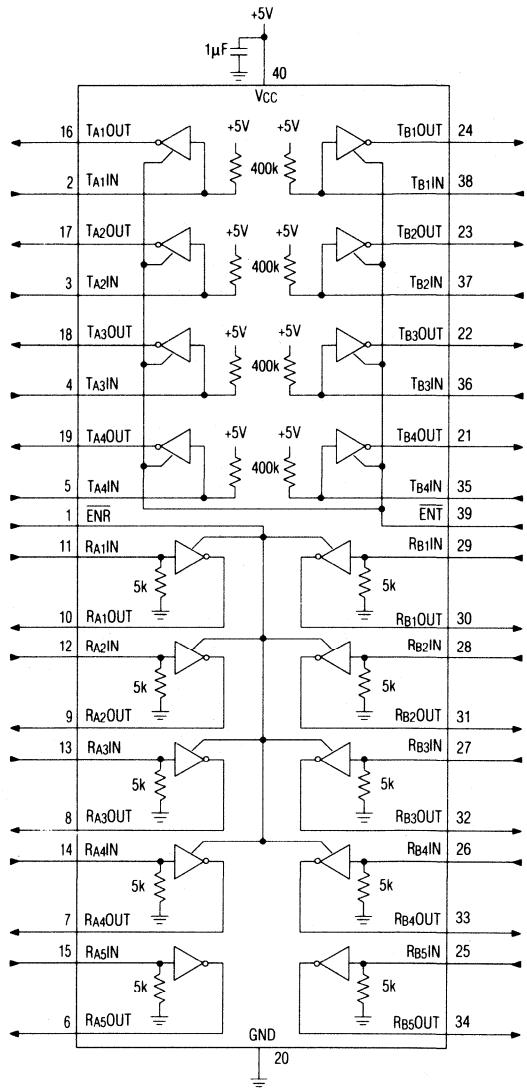
No Control Pins

Figure 20. MAX244 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP



MAX245 Functional Description

10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

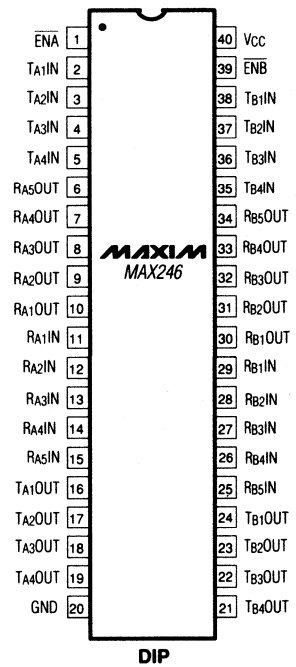
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

2 Control Pins
- 1 Receiver Enable ($\overline{ENR}$)
- 1 Transmitter Enable ($\overline{ENT}$)

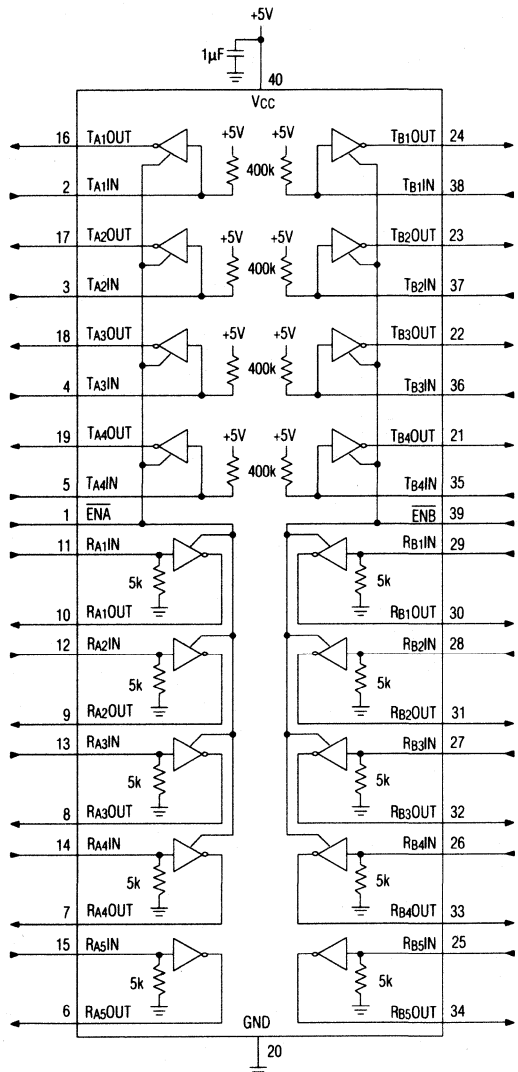
Figure 21. MAX245 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

TOP VIEW



DIP



MAX246 Functional Description

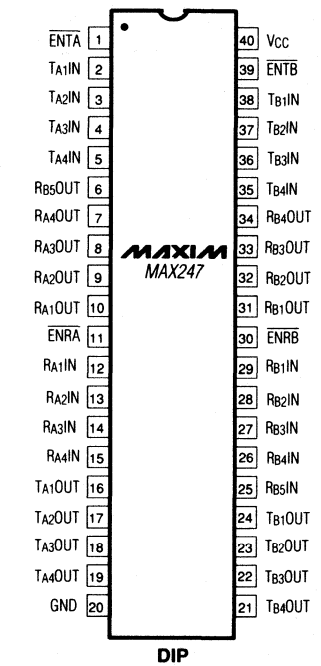
10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

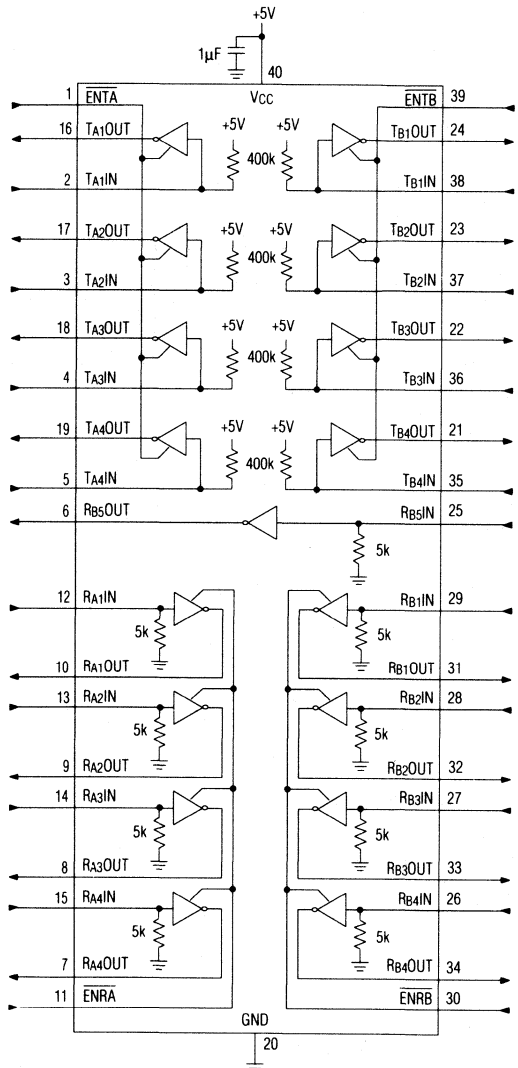
2 Control Pins
- Enable A-Side ($\overline{ENA}$)
- Enable B-Side ($\overline{ENB}$)

Figure 22. MAX246 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP



MAX247 Functional Description

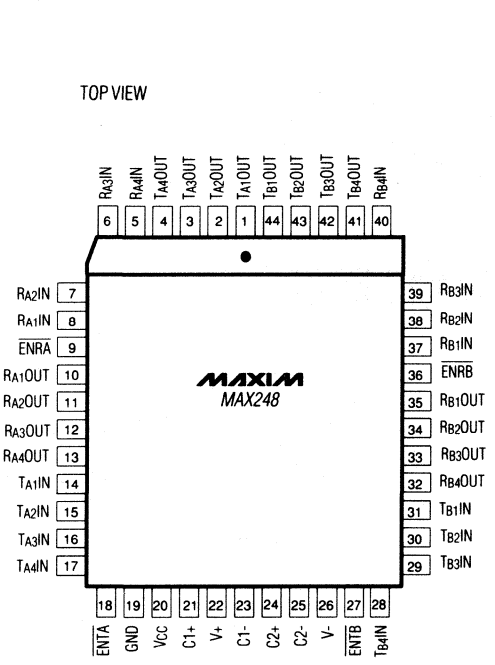
9 Receivers
- 4 A-Side Receivers
- 5 B-Side Receivers (R_{B5} always active)

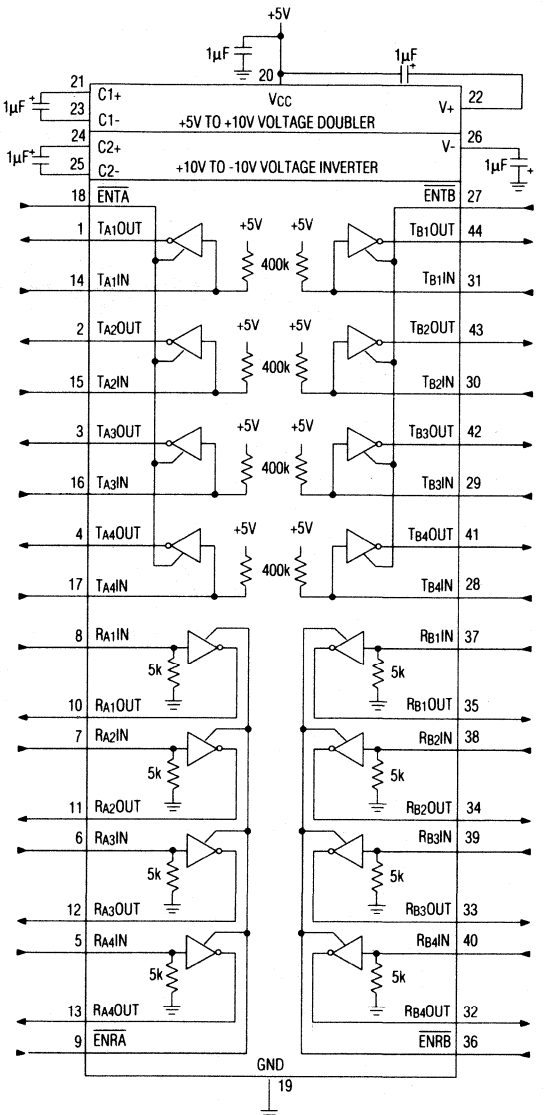
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 23. MAX247 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers





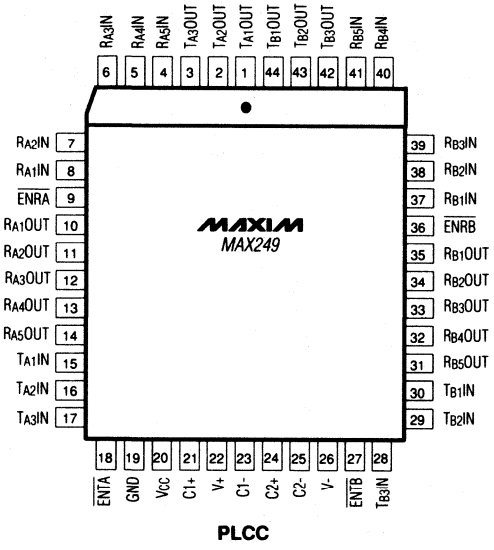
MAX248 Functional Description

8 Receivers
- 4 A-Side Receivers
- 4 B-Side Receivers

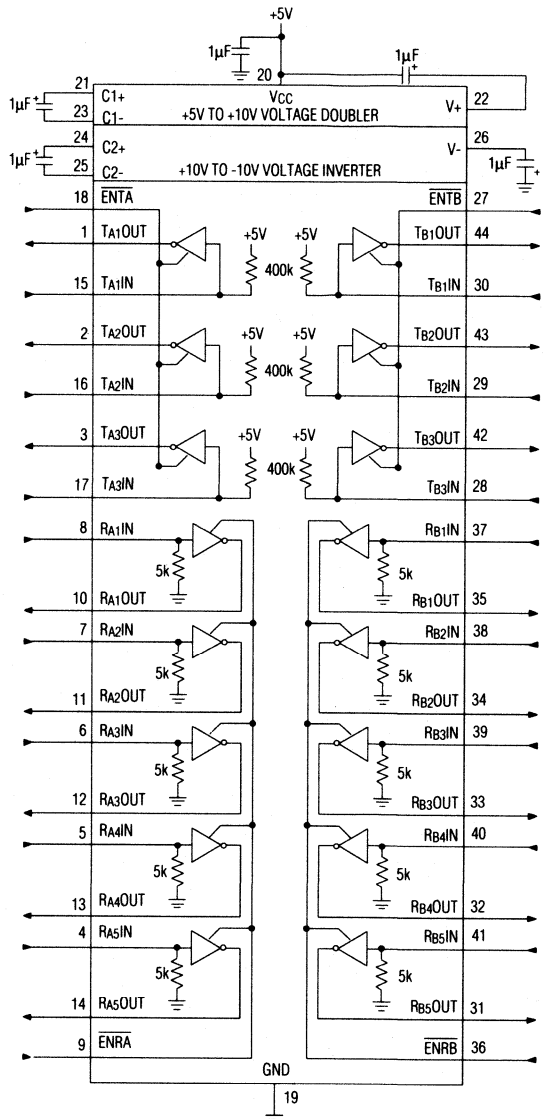
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 24. MAX248 Pin Configuration and Typical Operating Circuit



PLCC



MAX249 Functional Description

10 Receivers
- 5 A-Side Receivers
- 5 B-Side Receivers

6 Transmitters
- 3 A-Side Transmitters
- 3 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 25. MAX249 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX222CPN	0°C to +70°C	18 Plastic DIP
MAX222CWN	0°C to +70°C	18 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	18 Plastic DIP
MAX222EWN	-40°C to +85°C	18 Wide SO
MAX222EJN	-40°C to +85°C	18 CERDIP
MAX222MJN	-55°C to +125°C	18 CERDIP
MAX223CAI	0°C to +70°C	28 SSOP
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223C/D	0°C to +70°C	Dice*
MAX223EAI	-40°C to +85°C	28 SSOP
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX225CWI	0°C to +70°C	28 Wide SO
MAX225EWI	-40°C to +85°C	28 Wide SO
MAX230CPP	0°C to +70°C	20 Plastic DIP
MAX230CWP	0°C to +70°C	20 Wide SO
MAX230C/D	0°C to +70°C	Dice*
MAX230EPP	-40°C to +85°C	20 Wide SO
MAX230EWP	-40°C to +85°C	20 Wide SO
MAX230EJP	-40°C to +85°C	20 CERDIP
MAX230MJP	-55°C to +125°C	20 CERDIP
MAX231CPD	0°C to +70°C	14 Plastic DIP
MAX231CWE	0°C to +70°C	16 Wide SO
MAX231CJD	0°C to +70°C	14 CERDIP
MAX231C/D	0°C to +70°C	Dice*
MAX231EPD	-40°C to +85°C	14 Plastic DIP
MAX231EWE	-40°C to +85°C	16 Wide SO
MAX231EJD	-40°C to +85°C	14 CERDIP
MAX231MJD	-55°C to +125°C	14 CERDIP
MAX232CPE	0°C to +70°C	16 Plastic DIP
MAX232CSE	0°C to +70°C	16 Narrow SO
MAX232CWE	0°C to +70°C	16 Wide SO
MAX232C/D	0°C to +70°C	Dice*
MAX232EPE	-40°C to +85°C	16 Plastic DIP
MAX232ESE	-40°C to +85°C	16 Narrow SO
MAX232EWE	-40°C to +85°C	18 Wide SO
MAX232EJE	-40°C to +85°C	16 CERDIP
MAX232MJE	-55°C to +125°C	16 CERDIP
MAX232MLP	-55°C to +125°C	20 LCC
MAX232ACPE	0°C to +70°C	16 Plastic DIP
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic DIP
MAX232AESE	-40°C to +85°C	16 Plastic SO
MAX232AEWE	-40°C to +85°C	18 Wide SO
MAX232AEJE	-40°C to +85°C	16 CERDIP
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX232AMLP	-55°C to +125°C	20 LCC
MAX233CPP	0°C to +70°C	20 Plastic DIP
MAX233EPP	-40°C to +85°C	20 Plastic DIP
MAX233ACPP	0°C to +70°C	20 Plastic DIP
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233AEPP	-40°C to +85°C	20 Plastic DIP
MAX233AEWP	-40°C to +85°C	20 Wide SO
MAX234CPE	0°C to +70°C	16 Plastic DIP
MAX234CWE	0°C to +70°C	16 Wide SO
MAX234C/D	0°C to +70°C	Dice*
MAX234EPE	-40°C to +85°C	16 Plastic DIP
MAX234EWE	-40°C to +85°C	16 Wide SO
MAX234EJE	-40°C to +85°C	16 CERDIP
MAX234MJP	-55°C to +125°C	16 CERDIP
MAX235CPG	0°C to +70°C	24 Wide Plastic DIP
MAX235EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX235EDG	-40°C to +85°C	24 Ceramic SB
MAX235MDG	-55°C to +125°C	24 Ceramic SB
MAX236CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX236CEG	0°C to +70°C	24 Wide SO
MAX236C/D	0°C to +70°C	Dice*
MAX236ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX236EWG	-40°C to +85°C	24 Wide SO
MAX236ERG	-40°C to +85°C	24 Narrow CERDIP
MAX236MRG	-55°C to +125°C	24 CERDIP
MAX237CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX237CEG	0°C to +70°C	24 Wide SO
MAX237C/D	0°C to +70°C	Dice*
MAX237ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX237EWG	-40°C to +85°C	24 Wide SO
MAX237ERG	-40°C to +85°C	24 Narrow CERDIP
MAX237MRG	-55°C to +125°C	24 CERDIP
MAX238CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX238CEG	0°C to +70°C	24 Wide SO
MAX238C/D	0°C to +70°C	Dice*
MAX238ENG	-40°C to +85°C	24 Narrow Plastic DIP

Contact factory for dice specifications.

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

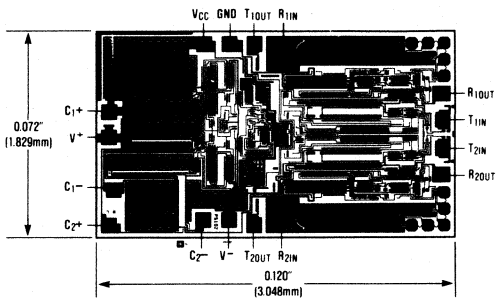
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX238EWG	-40°C to +85°C	24 Wide SO
MAX238ERG	-40°C to +85°C	24 CERDIP
MAX238MRG	-55°C to +125°C	24 CERDIP
MAX239CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX239CEG	0°C to +70°C	24 Wide SO
MAX239C/D	0°C to +70°C	Dice*
MAX239ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX239EWG	-40°C to +85°C	24 Wide SO
MAX239ERG	-40°C to +85°C	24 Narrow CERDIP
MAX239MRG	-55°C to +125°C	24 CERDIP
MAX240CMH	0°C to +70°C	44 Plastic FP
MAX240C/D	0°C to +70°C	Dice*
MAX241CAI	0°C to +70°C	28 SSOP
MAX241CWI	0°C to +70°C	28 Wide SO
MAX241C/D	0°C to +70°C	Dice*
MAX241EAI	-40°C to +85°C	28 SSOP
MAX241EWI	-40°C to +85°C	28 Wide SO
MAX242CPN	0°C to +70°C	18 Plastic DIP
MAX242CWN	0°C to +70°C	18 Wide SO
MAX242C/D	0°C to +70°C	Dice*
MAX242EPN	-40°C to +85°C	18 Plastic DIP
MAX242EWN	-40°C to +85°C	18 Wide SO
MAX242EJN	-40°C to +85°C	18 CERDIP
MAX242MJN	-55°C to +125°C	18 CERDIP
MAX243CPE	0°C to +70°C	16 Plastic DIP
MAX243CSE	0°C to +70°C	16 Narrow SO
MAX243CWE	0°C to +70°C	16 Wide SO
MAX243C/D	0°C to +70°C	Dice*
MAX243EPE	-40°C to +85°C	16 Plastic DIP
MAX243ESE	-40°C to +85°C	16 Narrow SO
MAX243EWE	-40°C to +85°C	16 Wide SO
MAX243EJE	-40°C to +85°C	16 CERDIP
MAX243MRG	-55°C to +125°C	16 CERDIP
MAX244CQH	0°C to +70°C	44 PLCC
MAX244C/D	0°C to +70°C	Dice*
MAX244EQH	-40°C to +85°C	44 PLCC
MAX245CPL	0°C to +70°C	40 Plastic DIP
MAX245C/D	0°C to +70°C	Dice*
MAX245EPE	-40°C to +85°C	40 Plastic DIP
MAX246CPL	0°C to +70°C	40 Plastic DIP
MAX246C/D	0°C to +70°C	Dice*
MAX246EPE	-40°C to +85°C	40 Plastic DIP
MAX247CPL	0°C to +70°C	40 Plastic DIP
MAX247C/D	0°C to +70°C	Dice*
MAX247EPL	-40°C to +85°C	40 Plastic DIP
MAX248CQH	0°C to +70°C	44 PLCC
MAX248C/D	0°C to +70°C	Dice*
MAX248EQH	-40°C to +85°C	44 PLCC
MAX249CQH	0°C to +70°C	44 PLCC
MAX249EQH	-40°C to +85°C	44 PLCC

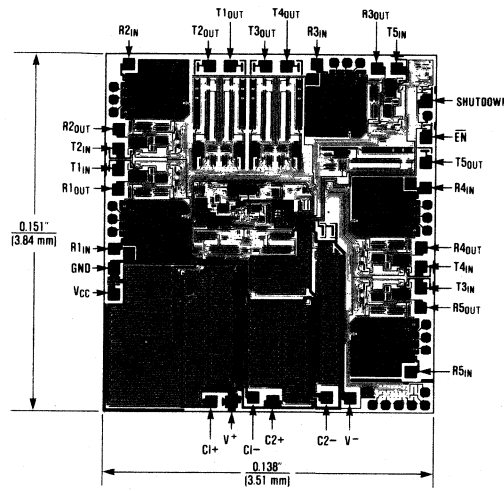
**Contact factory for dice specifications.*

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

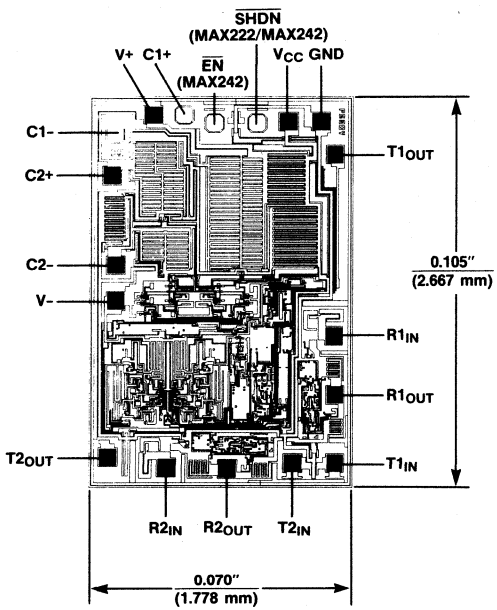
Chip Topographies



MAX231, MAX232 and MAX233



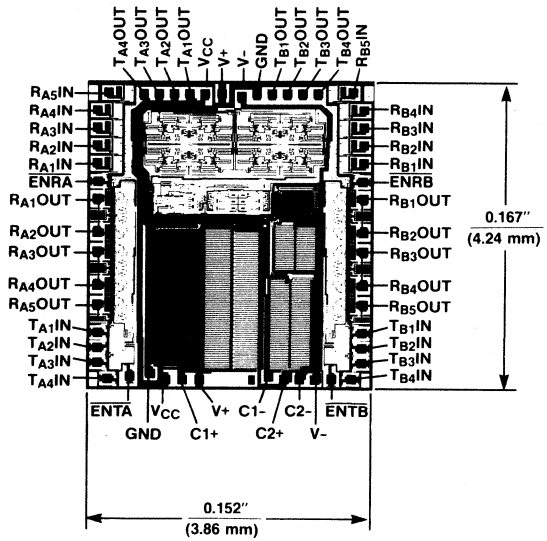
MAX230 and MAX234-239, MAX240, MAX241



MAX220/222/232A/233A/242/243

CONNECT SUBSTRATE TO V+

SHUTDOWN PIN OF MAX234, MAX237, MAX238, MAX239, MAX240 AND MAX241 ARE INTERNALLY CONNECTED TO GROUND.



MAX244/245/246/247/248/249

19-0226; Rev 0; 1/94

MAXIM

Transformer Driver for Isolated RS-485 Interface

General Description

The MAX253 is a monolithic oscillator/power-driver, specifically designed to provide isolated power for an isolated RS-485 or RS-232 data interface. It drives a center-tapped transformer primary from a 5V or 3.3V DC power supply. The secondary can be wound to provide any isolated voltage needed at power levels up to 1W.

The MAX253 consists of a CMOS oscillator driving a pair of N-channel power switches. The oscillator runs at double the output frequency, driving a toggle flip-flop to ensure 50% duty cycle to each of the switches. Internal delays are arranged to ensure break-before-make action between the two switches.

The SD pin puts the entire device into a low-power shutdown state, disabling both the power switches and oscillator.

Applications

Isolated RS-485/RS-232 Power-Supply Transformer Driver

High Noise-Immunity Communications Interface

Isolated and/or High-Voltage Power Supplies

Bridge Ground Differentials

Medical Equipment

Process Control

Features

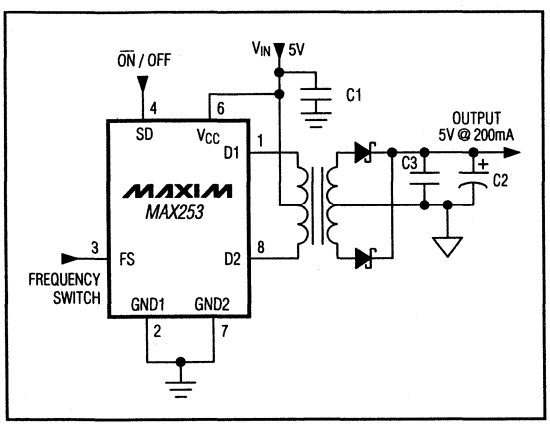
- ♦ **Power-Supply Transformer Driver for Isolated RS-485/RS-232 Data-Interface Applications**
- ♦ **Single +5V or +3.3V Supply**
- ♦ **Low-Current Shutdown Mode: 0.4µA**
- ♦ **Pin-Selectable Frequency: 350kHz or 200kHz**
- ♦ **8-Pin DIP, SO, and µMAX Packages**

Ordering Information

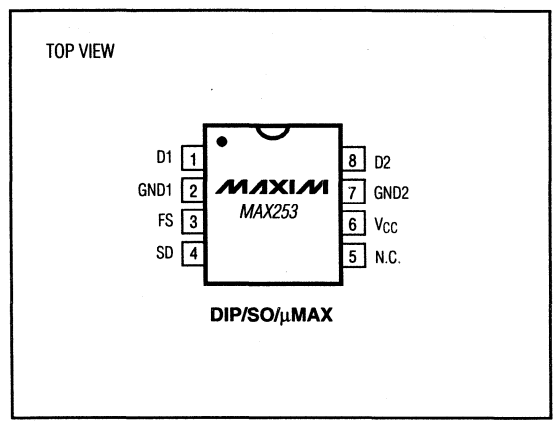
PART	TEMP. RANGE	PIN-PACKAGE
MAX253CPA	0°C to +70°C	8 Plastic DIP
MAX253CSA	0°C to +70°C	8 SO
MAX253CUA	0°C to +70°C	8 µMAX
MAX253C/D	0°C to +70°C	Dice*
MAX253EPA	-40°C to +85°C	8 Plastic DIP
MAX253ESA	-40°C to +85°C	8 SO
MAX253EUA	-40°C to +85°C	8 µMAX
MAX253MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



Transformer Driver for Isolated RS-485 Interface

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... -0.3V to +7V
Control Input Voltages (SD, FS) ..... -0.3V to (V_{CC} + 0.3V)
Output Switch Voltage (D1, D2) 12V
Peak Output Switch Current (D1, D2) 1A
Average Output Switch Current (D1, D2) 200mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX253C_ _ ..... 0°C to +70°C
MAX253E_ _ ..... -40°C to +85°C
MAX253MJA ..... -55°C to +125°C
Junction Temperatures
MAX253C_ _/E_ _ ..... +150°C
MAX253MJA ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switch On Resistance	D1, D2; 100mA		1.5	4.0	Ω
Switch Frequency	FS = V_{CC} or open	250	350	500	kHz
	FS = 0V	150	200	300	
Operating Supply Current (Note 1)	No load, SD = 0V, FS low		0.45	5.0	mA
Shutdown Supply Current (Note 2)	SD = V_{CC}		0.4		µA
Shutdown Input Threshold	High	2.4			V
	Low			0.8	µA
Shutdown Input Leakage Current			10		pA
FS Input Threshold	High	2.4			V
	Low			0.8	
FS Input Leakage Current	FS = 0V			50	µA
	FS = V_{CC}		10		pA
Start-Up Voltage		2.5	2.2		V

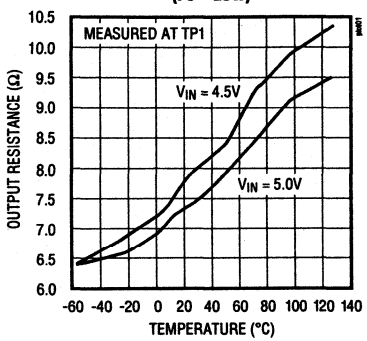
Note 1: Operating supply current is the current used by the MAX253 only, not including load current.
Note 2: Shutdown supply current includes output switch-leakage currents.

Transformer Driver for Isolated RS-485 Interface

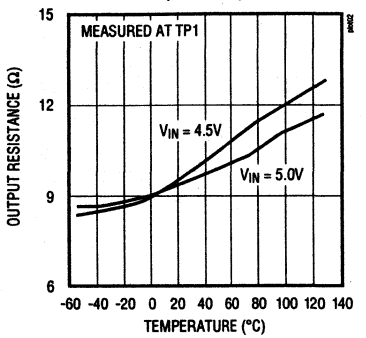
Typical Operating Characteristics

(Circuit of Figure 6, V_{IN} = 5V ±10%, T_A = +25°C, unless otherwise noted.)

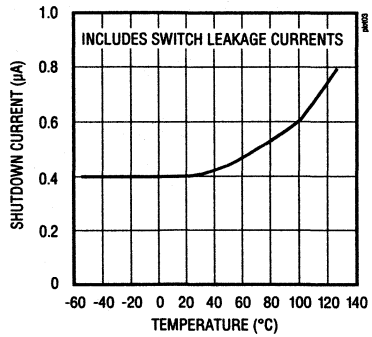
OUTPUT RESISTANCE vs. TEMPERATURE (FS = LOW)



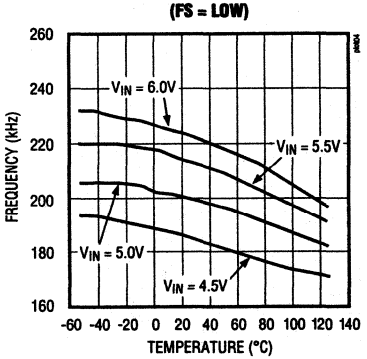
OUTPUT RESISTANCE vs. TEMPERATURE (FS = HIGH)



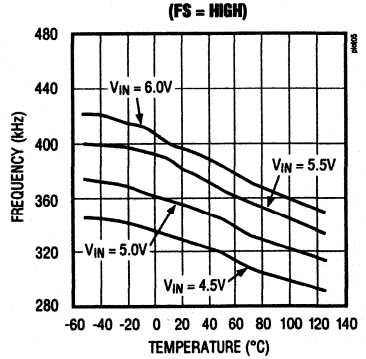
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



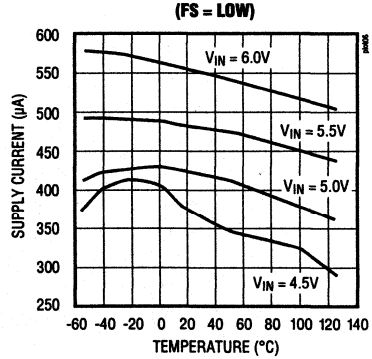
D1, D2 FREQUENCY vs. TEMPERATURE (FS = LOW)



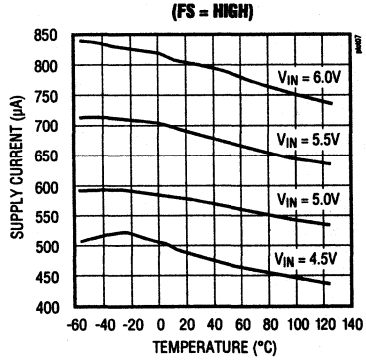
D1, D2 FREQUENCY vs. TEMPERATURE (FS = HIGH)



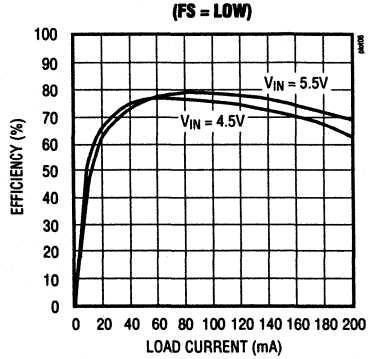
SUPPLY CURRENT vs. TEMPERATURE (FS = LOW)



SUPPLY CURRENT vs. TEMPERATURE (FS = HIGH)



EFFICIENCY vs. LOAD CURRENT (FS = LOW)

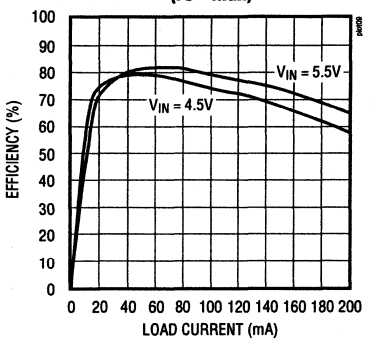


Transformer Driver for Isolated RS-485 Interface

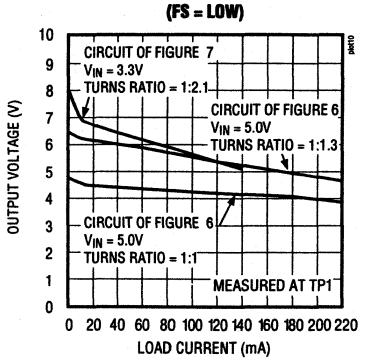
Typical Operating Characteristics (continued)

(Circuit of Figure 6, V_{IN} = 5V ± 10%, T_A = +25°C, unless otherwise noted.)

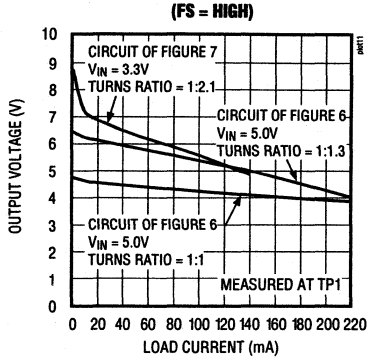
EFFICIENCY vs. LOAD CURRENT (FS = HIGH)



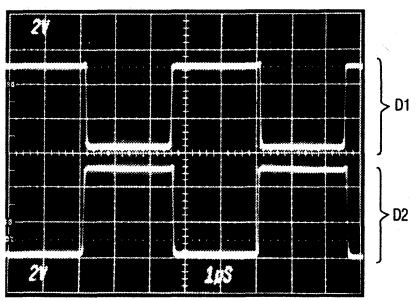
OUTPUT VOLTAGE vs. LOAD CURRENT (FS = LOW)



OUTPUT VOLTAGE vs. LOAD CURRENT (FS = HIGH)

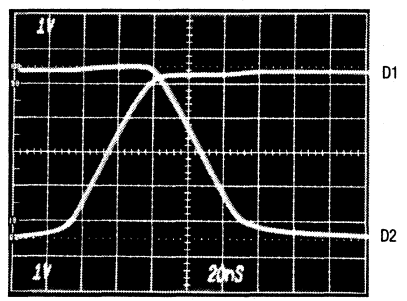


SWITCHING WAVEFORMS (TWO CYCLES)



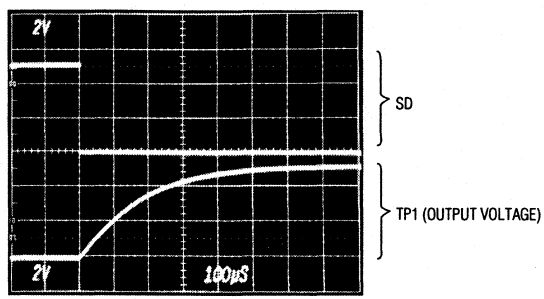
CIRCUIT OF FIGURE 1

SWITCHING WAVEFORMS (BREAK BEFORE MAKE)



CIRCUIT OF FIGURE 1

TIME FROM SHUTDOWN TO POWER-UP



CIRCUIT OF FIGURE 6

Transformer Driver for Isolated RS-485 Interface

Pin Description

PIN	NAME	FUNCTION
1	D1	Open drain of N-channel transfomer drive 1.
2	GND1	Ground. Connect both GND1 and GND2 to ground.
3	FS	Frequency switch. If FS = V_{CC} or open, switch frequency = 350kHz; if FS = 0V, switch frequency = 200kHz.
4	SD	Shutdown. Ground for normal operation, tie high for shutdown.
5	N.C.	Not internally connected.
6	V_{CC}	+5V supply voltage.
7	GND2	Ground. Connect both GND1 and GND2 to ground.
8	D2	Open drain of N-channel transformer drive 2.

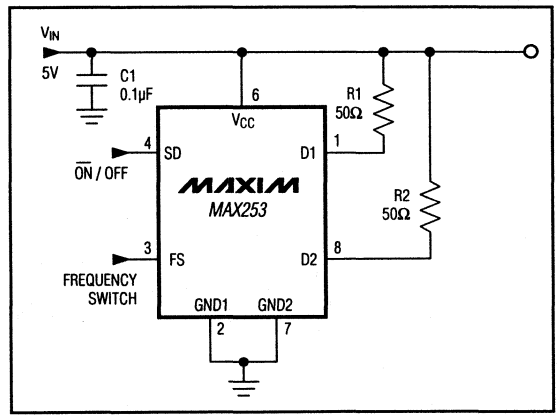


Figure 1. Test Circuit

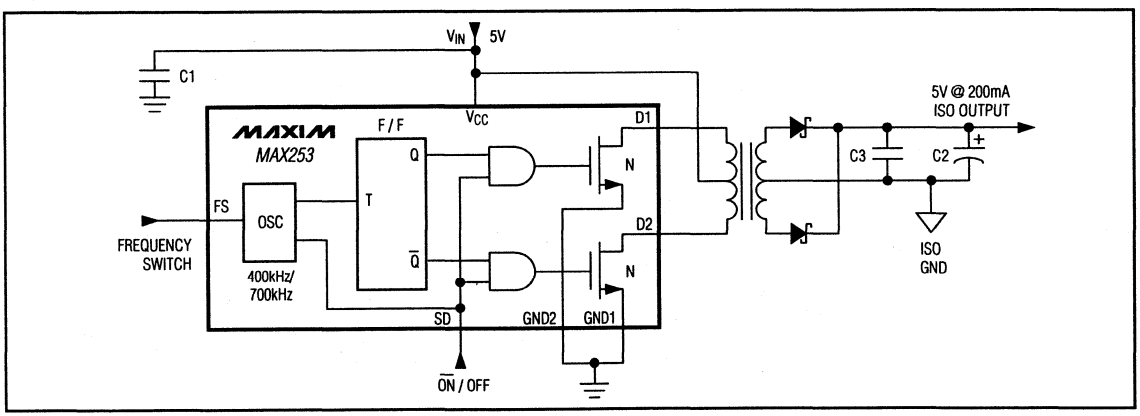


Figure 2. Block Diagram

Detailed Description

The MAX253 is an isolated power-supply transformer driver specifically designed to form the heart of a fully isolated RS-485 data interface. Completely isolated communications are obtained by combining the MAX253 with a linear regulator, a center-tapped transformer, optocouplers, and the appropriate Maxim interface product (as described in the *Isolated RS-485/RS-232 Data Interface* section).

The MAX253 consists of an RC oscillator followed by a toggle flip-flop, which generates two 50% duty-cycle square waves, out-of-phase at half the oscillator frequency (see Figure 2). These two signals drive the ground-referenced output switches. Internal delays ensure break-before-make action between the two switches.

Ground SD for normal operation. When high, SD disables all internal circuitry, including the oscillator and both power switches.

Pulling FS low reduces the oscillator frequency and lowers the supply current (see Supply Current vs. Temperature in the *Typical Operating Characteristics*). FS includes a weak pull-up, so it will float to the high-frequency state if not connected.

Transformer Driver for Isolated RS-485 Interface

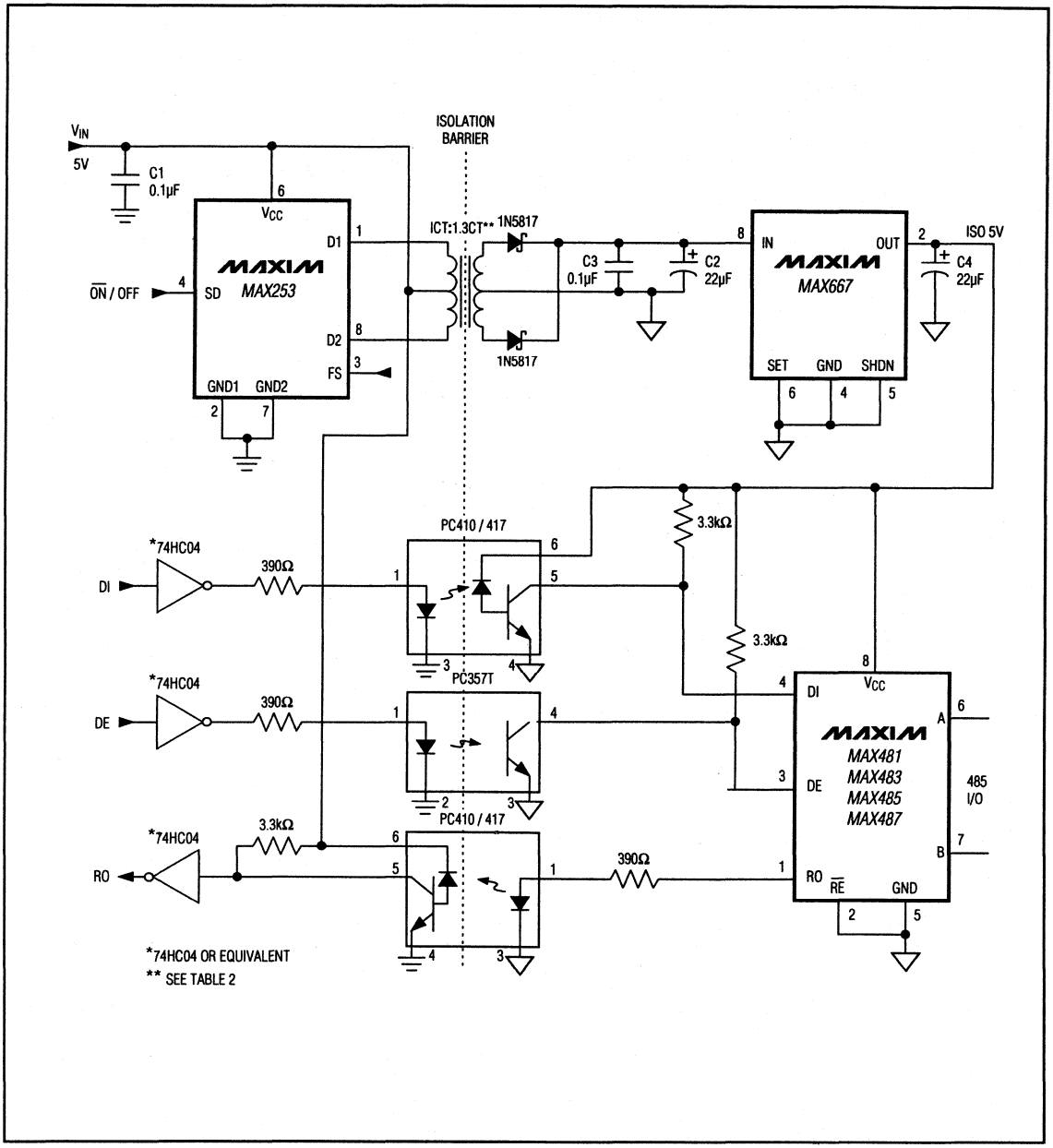


Figure 3. Typical RS-485 Application Circuit, 5V Configuration

Transformer Driver for Isolated RS-485 Interface

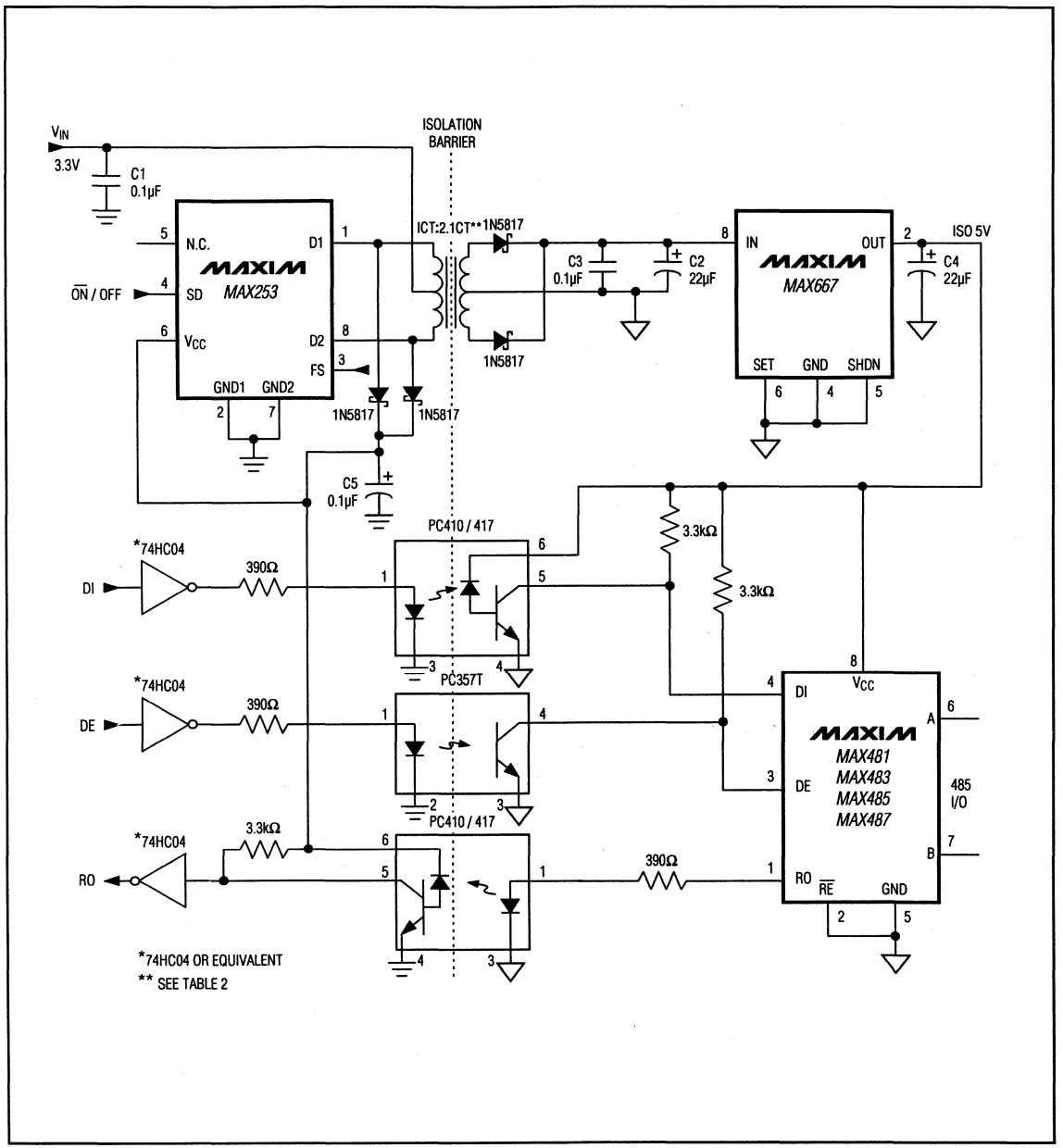


Figure 4. Typical RS-485 Application Circuit, 3.3V Configuration

Transformer Driver for Isolated RS-485 Interface

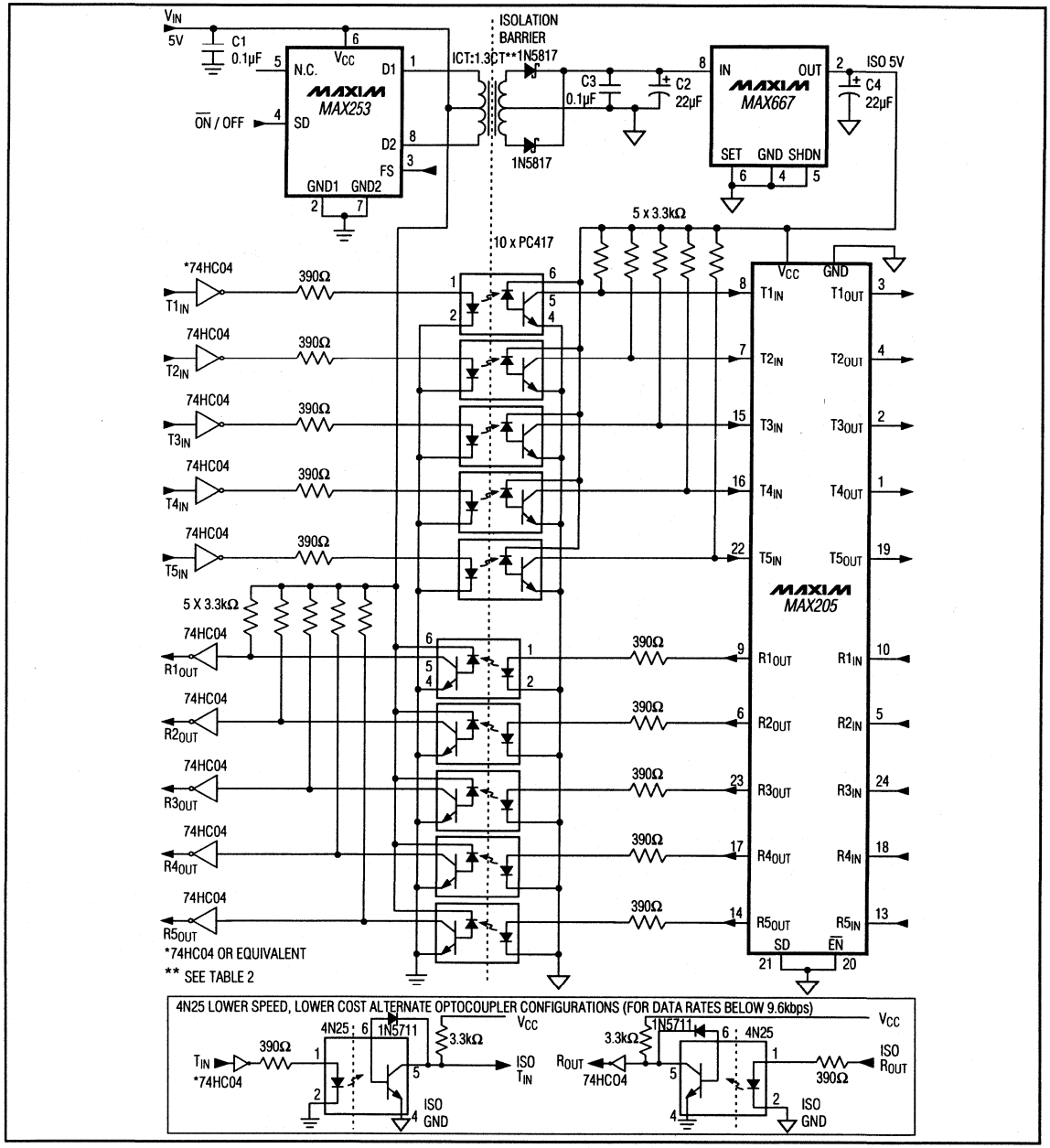


Figure 5. Typical RS-232 Application Circuit

Transformer Driver for Isolated RS-485 Interface

Applications Information

Figures 3–5 are typical isolated RS-485/RS-232 data-interface circuits. These circuits withstand 1800V_{RMS} (1sec) and are intended for industrial communications and control applications where very high voltage transients, differential ground potentials, or high noise may be encountered.

Table 2 lists transformer characteristics for the applications of Figures 3–10. Some suggested manufacturers of transformers, transformer cores, and optocouplers are listed in Table 3, along with their respective phone and fax numbers.

Important layout considerations include:

- For maximum isolation, the "isolation barrier" should not be breached. Connections and components from one side should not be located near those of the other side.
- Since the optocoupler outputs are relatively high-impedance nodes, they should be located as close as possible to the Maxim interface IC. This minimizes stray capacitance and maximizes data rate.

Refer to the µMAX package information for pin spacing and physical dimensions.

Isolated RS-485 Data Interface

The MAX253 power-supply transformer driver is designed specifically for isolated RS-485 data-interface applications. The application circuits of Figures 3 and 4 combine the MAX253 with a low-dropout linear regulator, a transformer, several high-speed optocouplers, and a Maxim RS-485 interface device. With a few modifications to these circuits, full-duplex communications can be implemented by substituting the MAX481/MAX485 with the MAX490/MAX491 (for data rates up to 2.5Mbps) or substituting the MAX483/MAX487 with the MAX488/MAX489 (for data rates up to 250kbps).

The data transfer rates of the application circuits in Figures 3 and 4 are critically limited by the optocouplers. Table 1 lists suggested optocouplers and the appropriate Maxim interface device for data-transfer rates up to 2.5Mbps.

Refer to the MAX1480 data sheet for a complete isolated RS-485 solution in one package.

Isolated RS-232 Data Interface

The MAX253 is ideal for isolated RS-232 data-interface applications requiring more than four transceivers. The 1W power output capability of the MAX253 enables it to drive more than 10 transceivers simultaneously. Figure 5 shows the typical application circuit for a complete 120kbps isolated RS-232 data interface. The figure also shows how the Sharp PC417 optocouplers can be replaced by the lower-cost 4N25 devices to achieve data-transfer rates up to 9.6kbps.

For 3.3V operation, substitute the primary portion of Figure 5 with the circuit of Figure 7.

For applications requiring two transceivers or fewer, refer to the MAX250/MAX251 or MAX252 data sheet.

Isolated Power Supplies

The MAX253 is a versatile isolated power driver, capable of driving a center-tapped transformer primary from a 5V or a 3.3V DC power supply (see Figures 6 and 7). The secondary can be wound to provide any isolated voltage needed at power levels up to 1W with a 5V supply, or 600mW with a 3.3V supply. Figure 6 shows a typical 5V to isolated 5V application circuit that delivers up to 200mA of isolated 5V power.

In Figure 7, the MAX253 is configured to operate from a 3.3V supply, deriving a "boost" V_{CC} for the MAX253 by connecting diodes to both ends of the transformer primary. This produces nearly double the input supply, and may be useful for other applications, as shown in Figure 4. The average current in each MAX253 switch must still be limited to less than 200mA, so the total power available is approximately 600mW.

Table 1. Optocouplers and RS-485 Interface ICs for Various Data Rates

DATA RATE	FULL DUPLEX RS-485 IC	HALF DUPLEX RS-485 IC	OPTOCOUPLER FOR DI / RO	OPTOCOUPLER FOR DE
250kbps	MAX488/MAX489	MAX483/MAX487	PC417*	PC357T*
2.5Mbps	MAX490/MAX491	MAX481/MAX485	PC410*	PC357T

* PC-Series Optocouplers, Sharp Electronics
USA Phone: (206) 834-2500
FAX: (206) 834-8903
Sharp Electronics, Europe GmbH
Germany Phone: (040) 2376-0
FAX: (040) 230764

Transformer Driver for Isolated RS-485 Interface

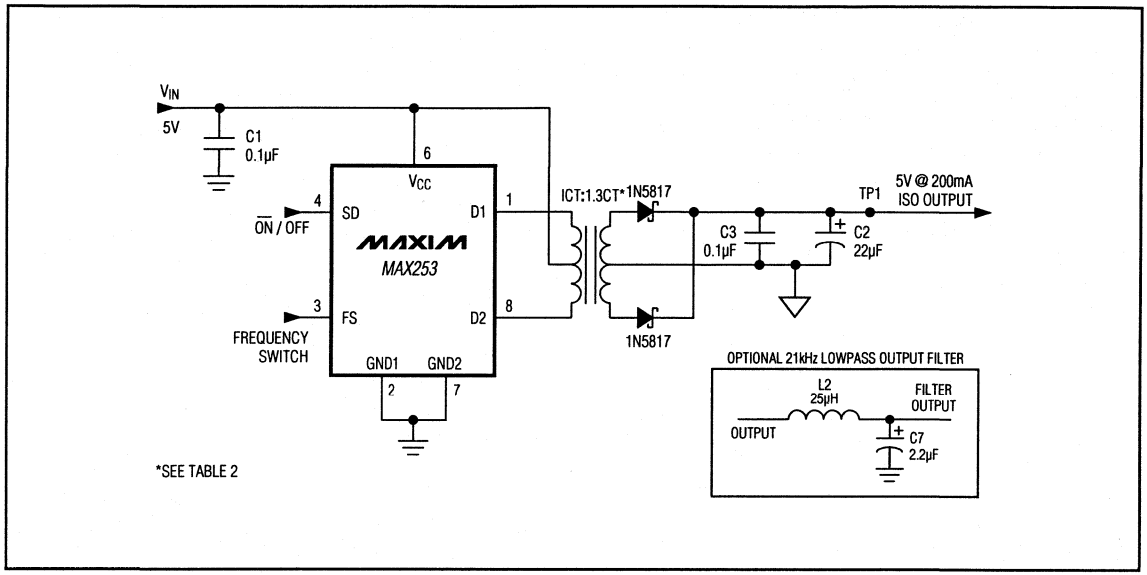


Figure 6. 5V to Isolated 5V Application Circuit

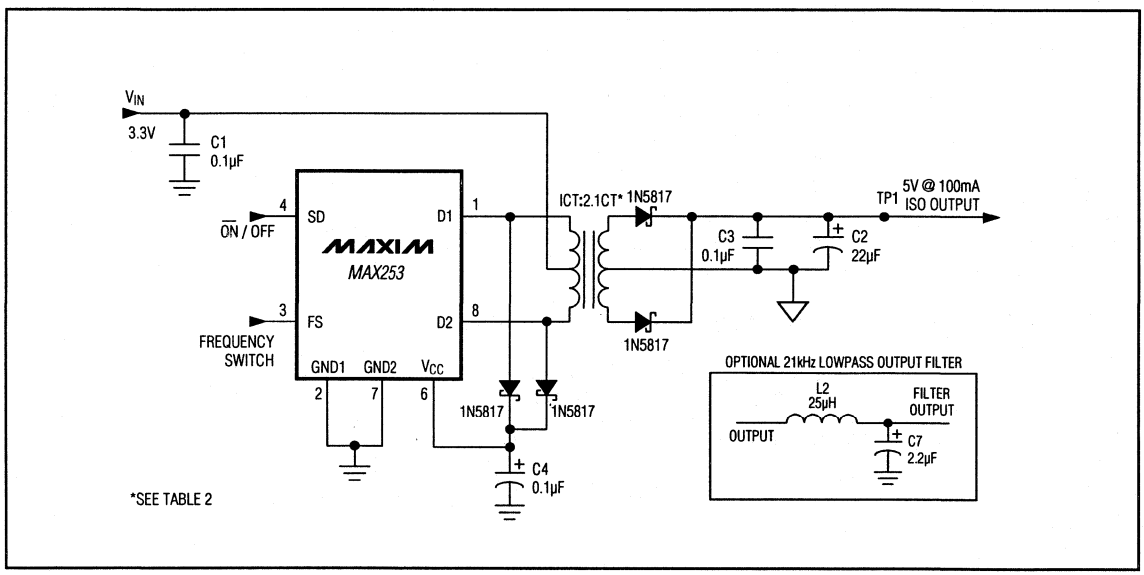


Figure 7. 3.3V to Isolated 5V Application Circuit

Transformer Driver for Isolated RS-485 Interface

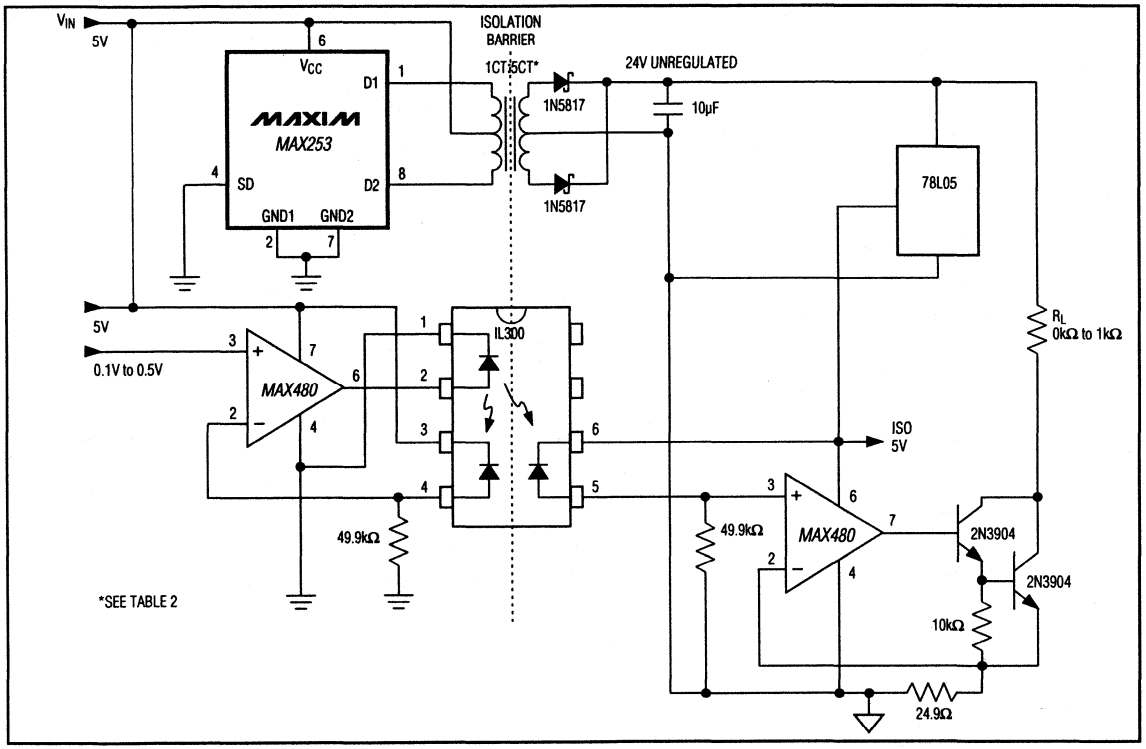


Figure 8. Typical 4mA to 20mA Application Circuit

Output-Ripple Filtering

A simple lowpass pi-filter (Figures 6 and 7) can be added to the output to reduce output ripple noise to about 10mVp-p. The cutoff frequency shown is 21kHz. Since the filter inductor is in series with the circuit output, minimize its resistance so the voltage drop across it is not excessive.

Isolated 4mA to 20mA Analog Interface

The 4mA to 20mA current loop is a standard analog signal range that is widely used in the process-control industry for transducer and actuator control signals. These signals are commonly referred to a distant ground that may be at a considerably higher voltage with respect to the local ground.

An analog signal in the range of 0.1V to 0.5V is applied to the first MAX480 to generate a signal current in the range of 20µA to 100µA. This low-level signal is transferred across the barrier by the Siemens IL300 linear optocoupler. This device is unique in that it corrects the dominant nonlinearity present in most optocouplers—the LED efficiency variation. The IL300 is really two optocouplers in the same package sharing the same LED; one detector is across the isolation barrier, the other is on the same side as the LED (Figure 8). The latter detector is used to generate a feedback signal identical to the signal on the isolated side of the barrier. The current signal transferred across the barrier is converted back to a voltage that matches the input in the 100mV to 500mV range. This voltage is then transformed to the final 4mA to 20mA current signal range by the second MAX480, Darlington stage, and the 20Ω resistor.

Isolated ADC

Almost any serial-interface device is a candidate for operation across an isolation barrier; Figure 10 illustrates one example. The MAX176 analog-to-digital converter (ADC) operates from +5V and -12V supplies, provided by the multiple-tapped secondary and linear regulators. If some additional isolated power is needed for signal conditioning, multiplexing, or possibly for a

Transformer Driver for Isolated RS-485 Interface

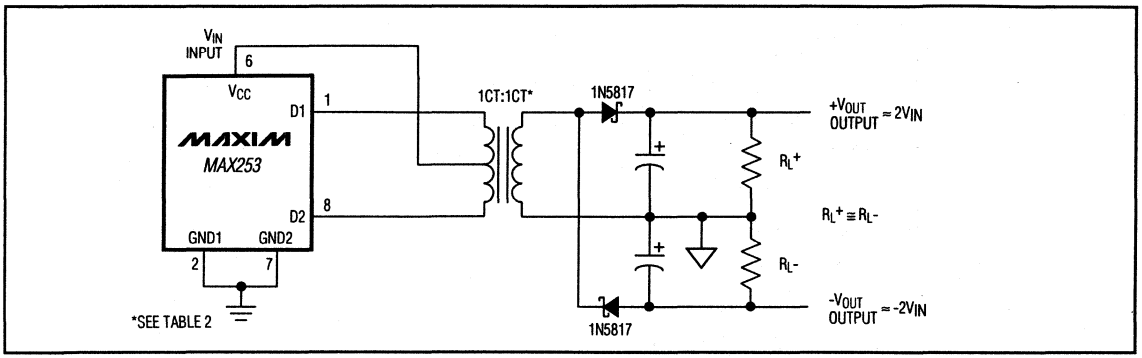


Figure 9a. Half-Wave Rectifier—Bipolar

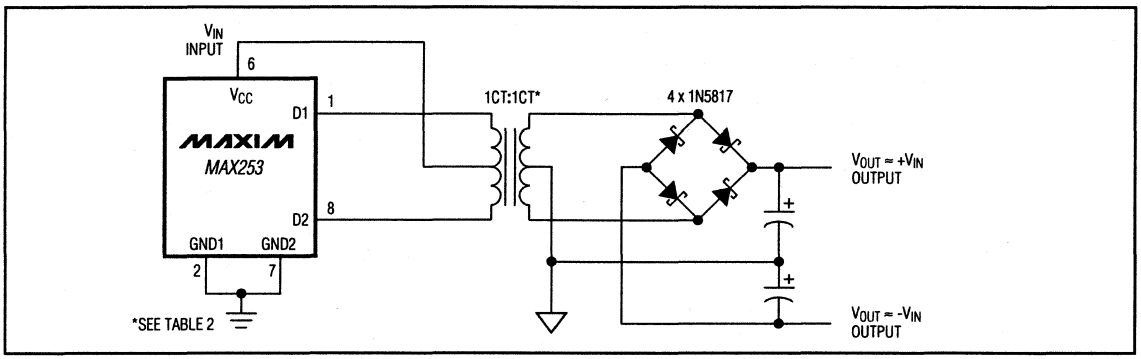


Figure 9b. Full-Wave Rectifier—Bipolar

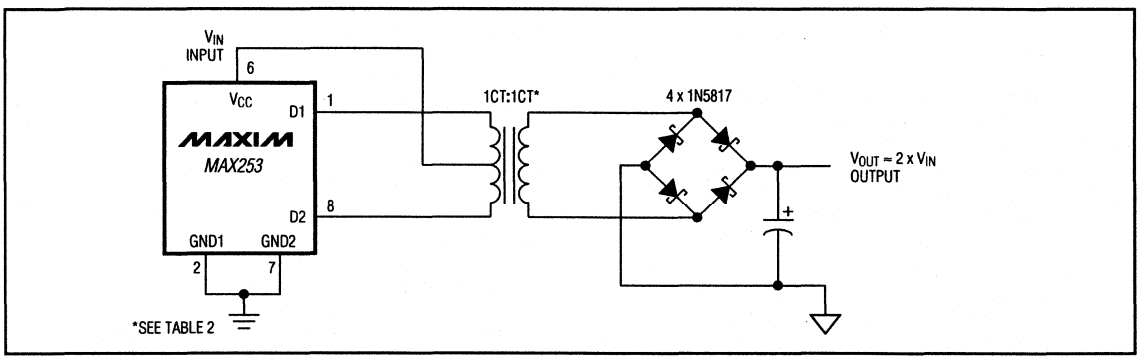


Figure 9c. Full-Wave Rectifier—Unipolar

Transformer Driver for Isolated RS-485 Interface

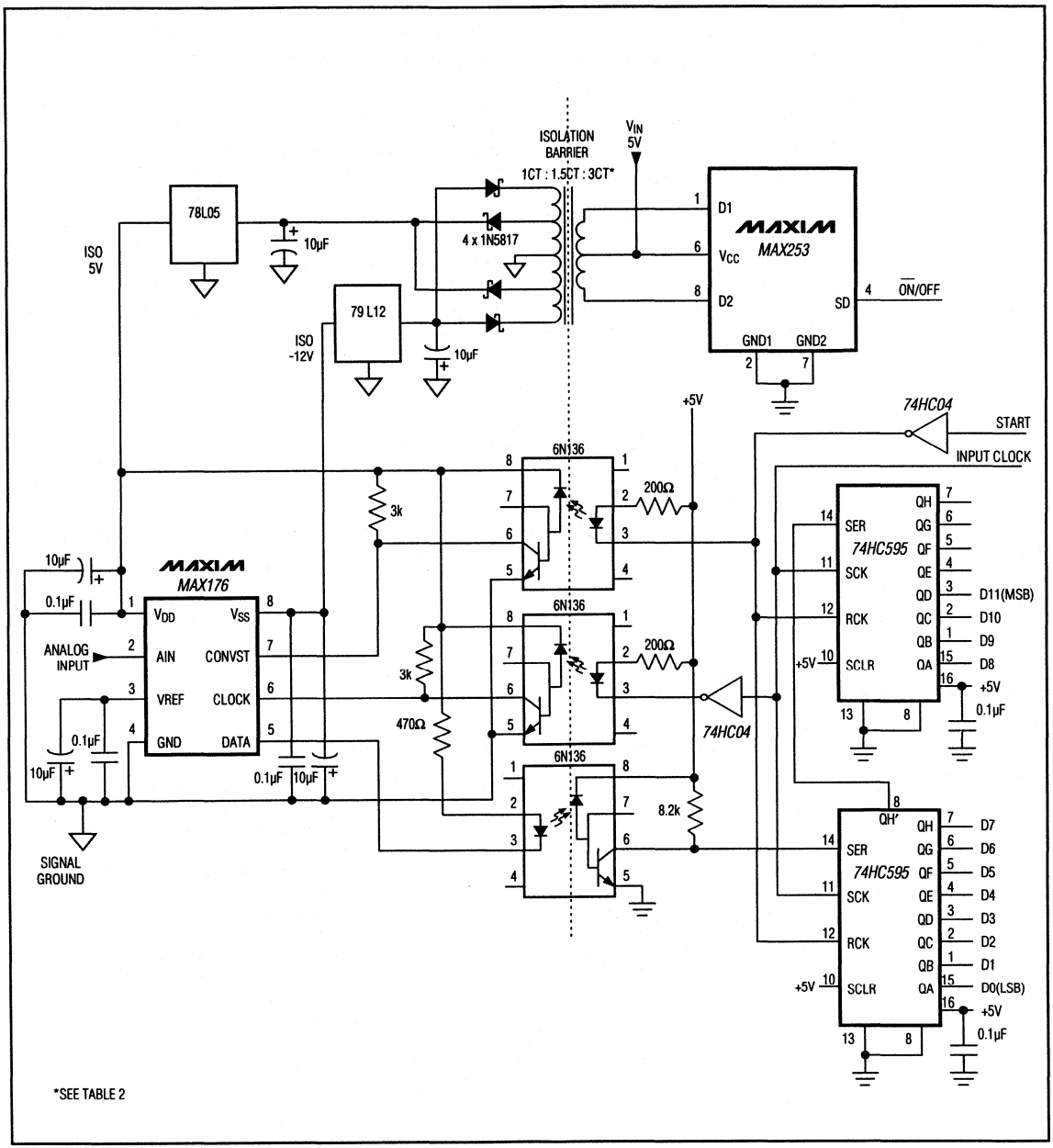


Figure 10. Typical Isolated ADC Application

Transformer Driver for Isolated RS-485 Interface

sensor, an extra several hundred milliwatts could easily be supplied by the circuit, as shown. A +12V supply could be generated by adding two more diodes to the ends of the secondary, and a -5V supply could be generated by connecting additional diodes to the 1/4 and 3/4 tap points on the secondary. For +5V only applications, the MAX187 is recommended.

Component Selection

Transformer Selection

The transformer primary used with the MAX253 must be a center-tapped winding with sufficient ET product to prevent saturation at the worst-case lowest selected frequency. The MAX253's guaranteed minimum frequency with the FS pin held low is 150kHz, equating to a maximum period of 6.67µs. The required ET product for half the primary is simply the product of the maximum supply voltage and half the maximum period. With FS tied high, the guaranteed minimum frequency is 250kHz, giving a maximum period of 4µs.

The secondary winding may or may not be center tapped, depending on the rectifier topology used. The phasing of the secondary winding is not critical. In some applications, multiple secondaries might be required. Half-wave rectification could be used, but is discouraged because it normally adds a DC imbalance to the magnetic flux in the core, reducing the ET product. If the DC load is imbalanced, full-wave rectification is recommended, as shown in Figure 9b.

The transformer turns ratio must be set to provide the minimum required output voltage at the maximum anticipated load with the minimum expected input volt-

Table 2. Typical Transformer Characteristics

CHARACTERISTIC		+5V to ±10V	+5V to +5V	+3.3V to +5V	+5V to +24V	+5V to ±5V; ±12V
Figure		9a	2, 3, 5, 6	4, 7	8	10
Turns Ratio		1CT*:1	1CT:1.3CT	1CT:2.1CT	1CT:5CT	1CT:1.5CT:3CT
Typical Windings	Primary	44CT	44CT	28CT	44CT	44CT
	Secondary	44	56CT	56CT	220CT	66CT, 132CT
Primary ET Product	FS Low	18.3V-µs	18.3V-µs	12V-µs	18.3V-µs	18.3V-µs
	FS High	11V-µs	11V-µs	7.2V-µs	11V-µs	11V-µs

*CT = Center Tapped

Table 3. Transformer, Transformer Core, and Optocoupler Suppliers

TRANSFORMERS	TRANSFORMER CORES	OPTOCOUPLERS
BH Electronics Phone: (507) 532-3211 FAX: (507) 532-3705	Philips Components Phone: (407) 881-3200 FAX: (407) 881-3300	Quality Technology Phone: (408) 720-1440 FAX: (408) 720-0848
Coilcraft Phone: (708) 639-6400 FAX: (708) 639-1469	Magnetics Inc. Phone: (412) 282-8282 FAX: (412) 282-6955	Sharp Electronics Phone: (206) 834-2500 FAX: (206) 834-8903
Coiltronics Phone: (407) 241-7876 FAX: (407) 241-9339	Fair-Rite Products Phone: (914) 895-2055 FAX: (914) 895-2629	Siemens Components Phone: (408) 777-4500 FAX: (408) 777-4983

age. In addition, include in the calculations an allowance for worst-case losses in the rectifiers. Since the turns ratio determined in this manner will ordinarily produce a much higher voltage at the secondary under conditions of high input voltage and/or light loading, be careful to prevent an overvoltage condition from occurring (see Output Voltage vs. Load Current in the *Typical Operating Characteristics*).

Transformers used with the MAX253 will ordinarily be wound on high-permeability magnetic material. To minimize radiated noise, use common closed-magnetic-path physical shapes (e.g., pot cores, toroids, E/I/U cores). A typical core is the Philips 213CT050-3B7, which is a toroid 0.190" in diameter and 0.05" thick. For operation with this core at 5.5V maximum supply voltage, the primary should have about 22 turns on each side of the center tap, or 44 turns total. This will result in a nominal primary inductance of about 832µH. The secondary can be scaled to produce the required DC output.

Diode Selection

The MAX253's high switching frequency demands high-speed rectifiers. Schottky diodes are recommended. Ensure that the Schottky diode average current rating exceeds the load-current level. The 1N5817 is a good choice for through-hole applications, and the NIEC* SB05W05C dual in an SOT-23 package is recommended for surface-mount applications. Use the higher frequency setting to reduce ripple.

Output Filter Capacitor

In applications sensitive to output-ripple noise, the output filter capacitor C2 should have a low effective series resistance (ESR), and its capacitance should remain fairly constant over temperature. Sprague 595D surface-mount solid tantalum capacitors and Sanyo OS-CON through-hole capacitors are recommended due to their extremely low ESR. Capacitor ESR usually rises at low temperatures, but OS-CON capacitors provide very low ESR below 0°C.

In applications where output ripple is not critical, a 0.1µF chip or ceramic capacitor is sufficient. Refer to Table 4 for suggested capacitor suppliers. Use the higher frequency setting to reduce ripple.

Input Bypass Capacitor

The input bypass capacitor C1 is not critical. Unlike switching regulators, the MAX253's supply current is fairly constant, and is therefore less dependent on the input bypass capacitor. A low-cost 0.1µF chip or ceramic capacitor is normally sufficient for input

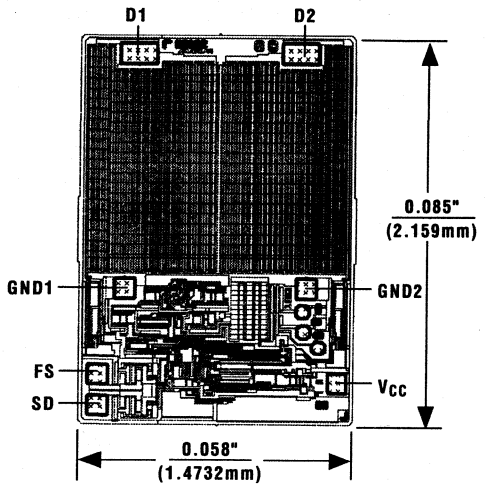
Table 4. Suggested Capacitor Suppliers

PRODUCTION METHOD	CAPACITORS
Surface Mount	Matsuo 267 series (low ESR) USA Phone: (714) 969-2491, FAX: (714) 960-6492 Sprague Electric Co. 595D/293D series (very low ESR) USA Phone: (603) 224-1961, FAX: (603) 224-1430 Murata Erie Ceramic USA Phone: (800) 831-9172, FAX: (404) 436-3030
High-Performance Through Hole	Sanyo OS-CON series (very low ESR) USA Phone: (619) 661-6835, FAX: (619) 661-1055 Japan Phone: 81-7-2070-1005, FAX: 81-7-2070-1174
Through Hole	Nichicon PL series (low ESR) USA Phone: (708) 843-7500, FAX: (708) 843-2798 Japan Phone: 81-7-5231-8461, FAX: 81-7-5256-4158

* Nihon Inter Electronics Corp.
USA Phone: (805) 867-2555
FAX: (805) 867-2556
Japan Phone: 81-3-3494-7411
FAX: 81-3-3494-7414

Transformer Driver for Isolated RS-485 Interface

Chip Topography



TRANSISTOR COUNT: 31;

SUBSTRATE CONNECTED TO V_{CC}.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/94

MAXIM

+2.7V to +3.6V Powered, 1µA Supply Current, 3-Driver, 5-Receiver, True RS-232 Transceiver

General Description

The MAX3212 uses Maxim's new AutoShutdown mode to reduce supply current to 1µA. The MAX3212, with 3 RS-232 drivers and 5 RS-232 receivers, is intended for 2.7V to 3.6V-powered EIA/TIA-232E and V.28/V.24 serial interface. True RS-232 levels are maintained across the operating range. A guaranteed data rate of 230kbps provides compatibility with popular software for communicating with personal computers.

Supply current is reduced to 1µA with Maxim's new AutoShutdown feature. When the MAX3212 does not sense a valid signal level on the receiver inputs, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing software. A second power-management feature is incorporated to permit automatic shutdown when the RS-232 connection is valid but inactive. In this case, a transition detector facilitates shutdown when the receivers are presented with stationary RS-232 levels for long periods. Additionally, the MAX3212 can be forced to shut down or forced out of shutdown, under logic control.

Three-state drivers are provided on receiver outputs so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART. The MAX3212 is available in 28-pin SO and SSOP packages.

Applications

Computers:
- Notebooks
- Palmtops

Printers

Peripherals

Instruments

Battery-Powered Equipment

Typical Operating Circuit on next page.
** Patent pending*

Features

BETTER THAN BIPOLAR!

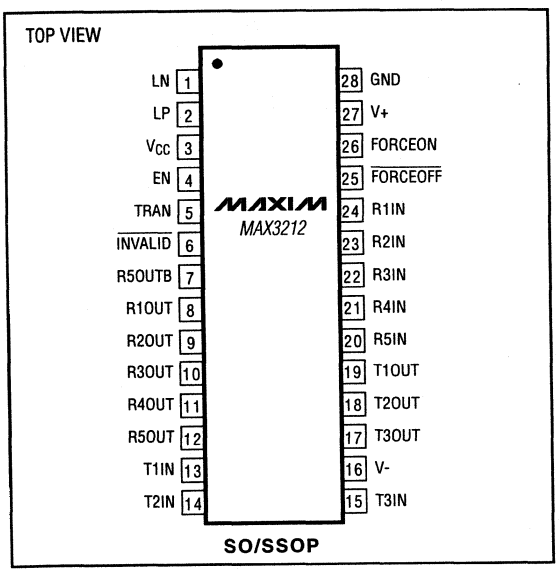
- ♦ **1µA Supply Current**
- ♦ **Operates From Single +2.7V to +3.6V Supply**
- ♦ **28-Pin SSOP or Wide SO Packages**
- ♦ **Meets All EIA/TIA-232E & EIA/TIA-562 Specifications**
- ♦ **Mouse Compatible**
- ♦ **Low-Cost, Surface-Mount External Components**
- ♦ **230kbps Guaranteed Data Rate–LapLink™ Compatible**
- ♦ **Three-State Receiver Outputs**
- ♦ **Spare Receiver Output Always Active**
- ♦ **Flow-Through Pinout**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3212CWI	0°C to +70°C	28 Wide SO
MAX3212CAI	0°C to +70°C	28 SSOP
MAX3212C/D	0°C to +70°C	Dice†
MAX3212EWI	-40°C to +85°C	28 Wide SO
MAX3212EAI	-40°C to +85°C	28 SSOP

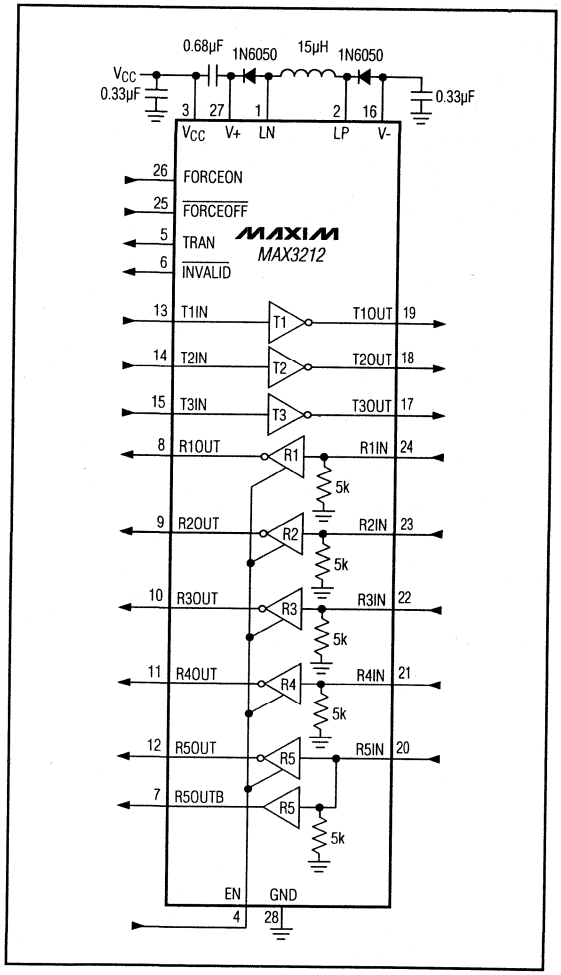
† Contact factory for dice specifications.

Pin Configuration



+2.7V to +3.6V Powered, 1μA Supply Current, 3-Driver, 5-Receiver, True RS-232 Transceiver

Typical Operating Circuit



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/94

MAXIM

1µA Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown

General Description

The MAX3218 RS-232 transceiver is intended for battery-powered EIA/TIA-232E and V.28/V.24 communications interfaces that need two drivers and two receivers with minimum power consumption from a single low-voltage supply. It provides a wide +1.8V to +4.25V operating voltage range while maintaining true RS-232 and EIA/TIA-562 voltage levels. The MAX3218 runs from 2 Alkaline, NiCd, or NiMH cells without any form of voltage regulator. A guaranteed 230kbps data rate provides compatibility with popular software for communicating with personal computers.

Supply current is reduced to 1µA with Maxim's new AutoShutdown feature. When the MAX3218 does not sense a valid signal level on the receiver inputs, the on-board power-supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to either RS-232 receiver input. As a result, the system saves power without changes to the existing software. Additionally, the MAX3218 can be forced to shutdown, or forced out of shutdown, under logic control.

While shut down, all receivers can remain active or can be disabled under logic control, permitting a system incorporating the CMOS MAX3218 to monitor external devices while in low-power shutdown. Three-state drivers are provided on both receiver outputs so that multiple receivers, generally of different interface standards, can be wire-ORed at the UART. The MAX3218 is available in 20-pin DIP, SO, and SSOP packages.

Applications

Battery-Powered Equipment
Subnotebook Computers
PDAs
Hand-Held Equipment
Peripherals

Typical Operating Circuit on next page.
** Patent Pending*

Features

BETTER THAN BIPOLAR!

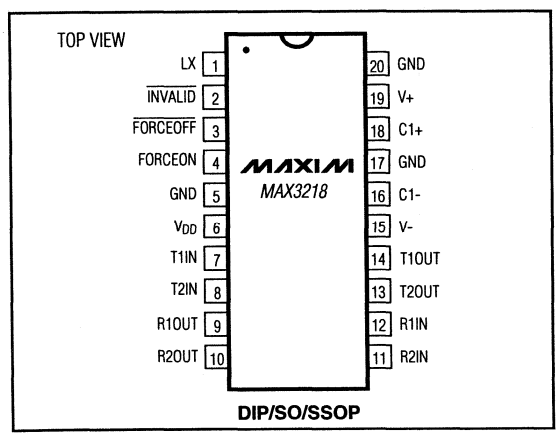
- **1µA Supply Current**
- **Operates Directly From Two Alkaline, NiCd or NiMH Cells**
- **+1.8V to +4.25V Single-Supply Voltage Range**
- **230kbps Data Rate Guaranteed**
- **Low-Cost Surface-Mount Components**
- **Meets EIA/TIA-232E Specifications**
- **Three-State Receiver Outputs**
- **Flow-Through Pinout**
- **On-Board DC-DC Converters**
- **20-Pin SSOP, Wide SO or DIP Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3218CPP	0°C to +70°C	20 Plastic DIP
MAX3218CWP	0°C to +70°C	20 SO
MAX3218CAP	0°C to +70°C	20 SSOP
MAX3218C/D	0°C to +70°C	Dice†
MAX3218EPP	-40°C to +85°C	20 Plastic DIP
MAX3218EWP	-40°C to +85°C	20 SO
MAX3218EAP	-40°C to +85°C	20 SSOP

† Contact factory for dice specifications.

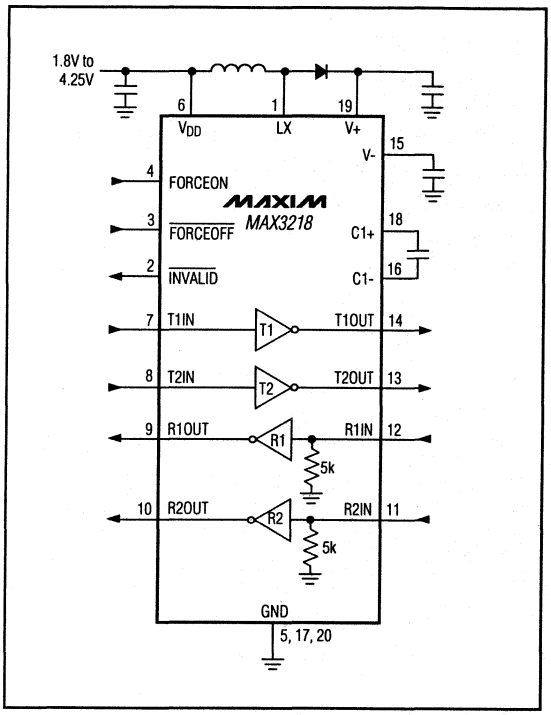
Pin Configuration



DIP/SO/SSOP

1µA Supply Current, 1.8V to 4.25V-Powered RS-232 Transceiver with AutoShutdown

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

3V to 5.5V-Powered, 2-Driver, 2-Receiver RS-232 Transceivers Using Four 0.1µF External Capacitors

General Description

The MAX3222/MAX3232 have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from 3.0V to 5.5V supplies with a dual charge pump. The devices require only four small 0.1µF external capacitors and are guaranteed to run at data rates of 120kbps while maintaining RS-232 output levels.

The MAX3222/MAX3232 are ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5.0V-only systems that require true RS-232 performance.

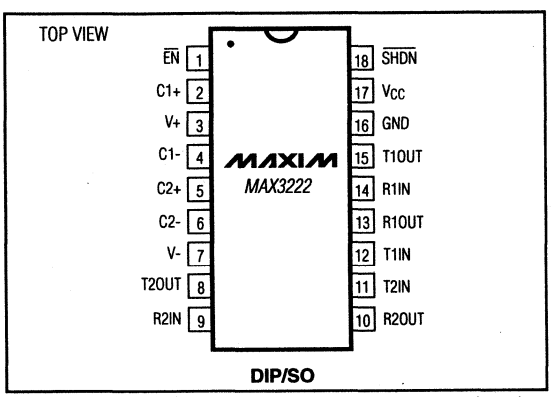
The MAX3222/MAX3232 have two receivers and two drivers. The MAX3222 has the same features as the MAX3232, but in addition has a 1µA shutdown mode that reduces power consumption and extends battery life in portable systems. The MAX3222 receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1µA supply current.

The MAX3222/MAX3232 require only four 0.1µF capacitors and consume only 250µA. Plus, the MAX3232 is pin and functionally compatible with the industry-standard MAX232.

Applications

Computers
Notebooks, Palmtops, etc.
Battery-Powered Equipment
Hand-Held Equipment
Peripherals

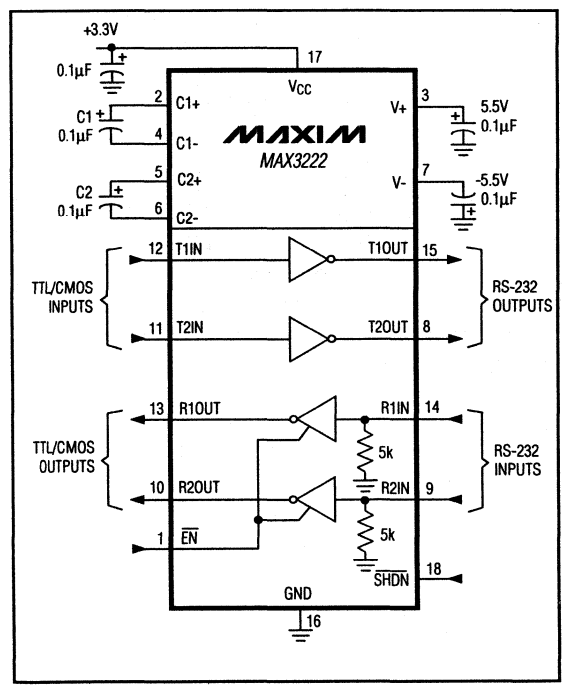
Pin Configurations



Features

- ♦ **True RS-232 Performance from 3.0V to 5.5V**
- ♦ **Low 250µA Supply Current**
- ♦ **Guaranteed 120kbps Data Rate**
- ♦ **1µA Low-Power Shutdown Current (MAX3222)**
- ♦ **4V/µs Minimum Guaranteed Slew Rate**
- ♦ **2 Receivers Active in Shutdown (MAX3222)**
- ♦ **Industry-Standard MAX232 Pinout (MAX3232)**

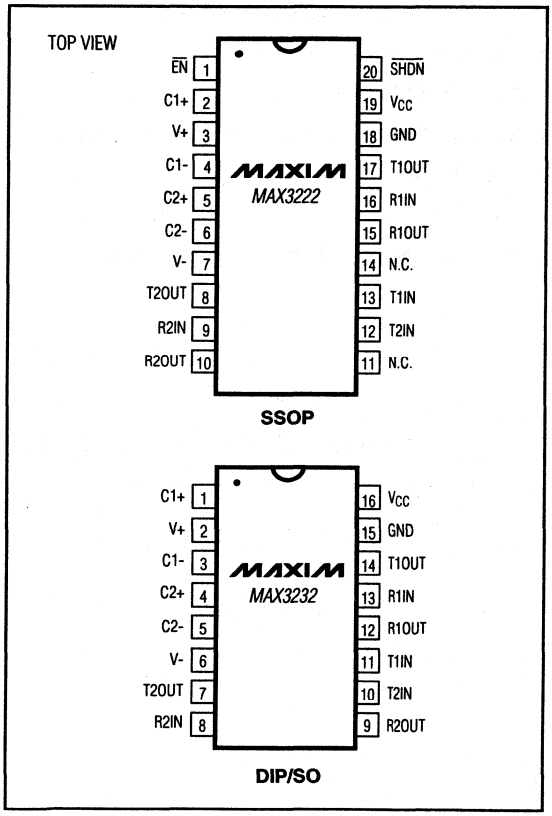
Typical Operating Circuits



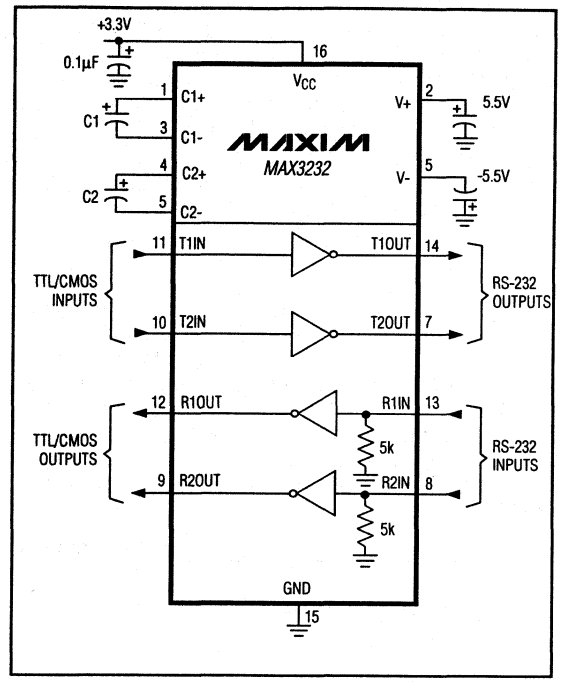
Pin Configurations and Typical Operating Circuits continued on next page.

3V to 5.5V-Powered, 2-Driver, 2-Receiver RS-232 Transceivers Using Four 0.1µF External Capacitors

Pin Configurations (cont.)



Typical Operating Circuits (cont.)



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/94

MAXIM

1µA Supply Current, True +3V to +5.5V RS-232 Transceivers Using Four 0.1µF Capacitors

General Description

The MAX3223/MAX3243 transceivers use Maxim's new AutoShutdown mode to reduce supply current to 1µA. A proprietary low-drop voltage doubler and output stage combine to deliver true RS-232 performance from 3.0V to 5.5V supplies. A guaranteed data rate of 120kbps provides compatibility with popular software for communicating with personal computers.

Supply current of 1µA is achieved with MAXIM's new AutoShutdown feature. When the MAX3223/MAX3243 do not sense a valid signal level on their receiver inputs, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system.

The MAX3223/MAX3243 require only 0.1µF capacitors in 3.3V operation, and can operate from input voltages ranging from 3.0V to 5.5V. They are ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5.0V-only systems that require true RS-232 performance.

The MAX3243 3 driver/5 receiver, complete serial port is ideal for notebook or subnotebook computers. Besides having all receivers active in shutdown, one receiver has a second, complementary output that is always active. This receiver can monitor an external device (such as a modem) in shutdown, without forward biasing the protection diodes in a UART that may have V_{DD} completely removed.

The MAX3223 2 driver/2 receiver serial port is a space-saving serial interface available in a 20 pin SSOP.

Applications

Notebook, Subnotebook, and Palmtop Computers

Battery-Powered Equipment

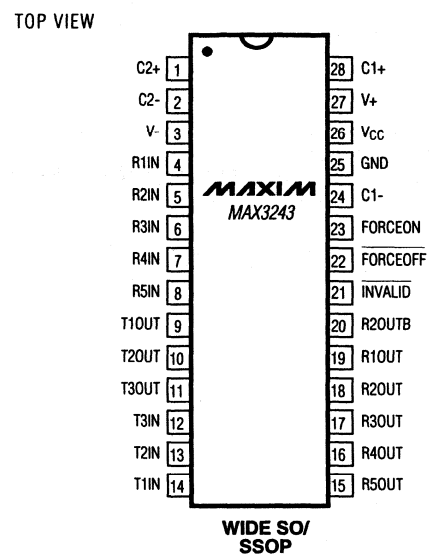
Hand-Held Equipment

Peripherals

Features

- ♦ **1µA Supply Current**
- ♦ **Small 0.1µF Capacitors**
- ♦ **True RS-232 Operation from V_{CC} = 3.0V to 5.5V**
- ♦ **Meets EIA/TIA-562 Specifications Down to 2.8V**
- ♦ **Guaranteed 120kbps Data Rate**
- ♦ **4V/µs Min Guaranteed Slew Rate**
- ♦ **Guaranteed Mouse Driveability (MAX3243)**
- ♦ **Flow-Through Pinout (MAX3243)**

Pin Configurations



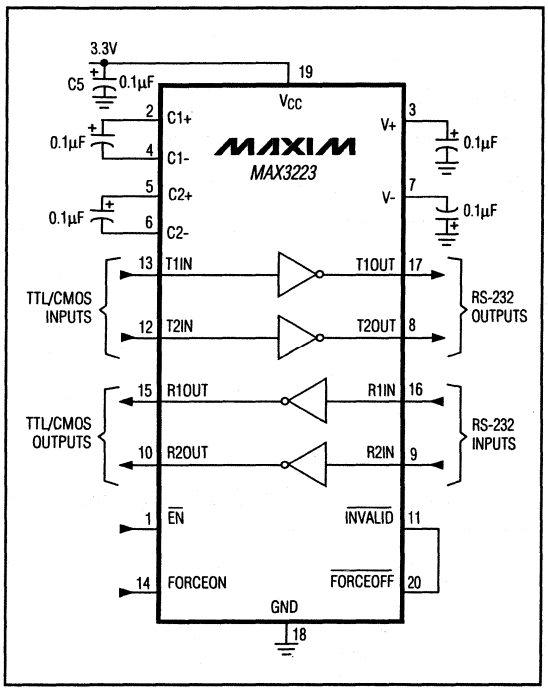
Typical Operating Circuits on next page.

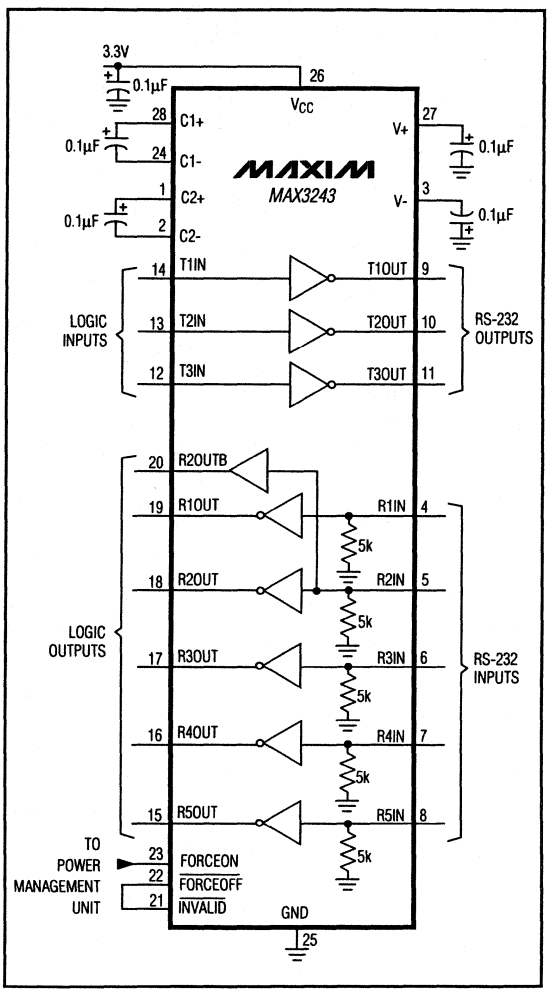
Pin Configurations continued on next page.

* *Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.*

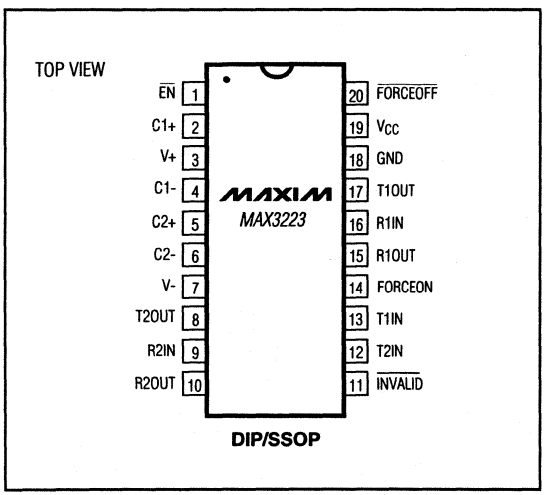
1µA Supply Current, True +3V to +5.5V RS-232 Transceivers Using Four 0.1µF Capacitors

Typical Operating Circuits





Pin Configurations (continued)



19-0273; Rev 0; 7/94

MAXIM

3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

General Description

The MAX3241 has a proprietary low dropout transmitter output stage enabling true RS-232 performance from 3.0V to 5.5V supplies, with a dual charge pump. The device requires only four small 0.1µF external capacitors, and is guaranteed to run at data rates up to 120kbps while maintaining RS-232 output levels.

The MAX3241 is ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5.0V-only systems that require true RS-232 performance.

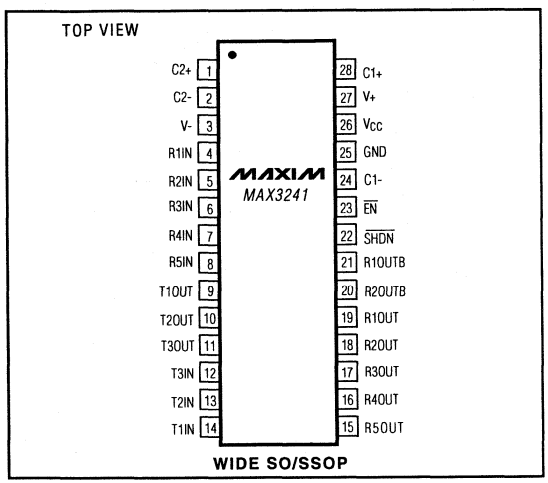
The MAX3241 is a complete serial port (3 drivers/5 receivers) designed for notebook and subnotebook computers. The MAX3241 uses only tiny 0.1µF external capacitors and has a low 1mA max operating supply current.

In shutdown, all 5 receivers can remain active using only 1µA supply current. Receivers R1 and R2 have two extra outputs in addition to their standard outputs. These outputs are always active allowing external devices, such as a modem, to be monitored without forward biasing the protection diodes in circuitry that may have V_{CC} completely removed.

Applications

Notebook, Subnotebook, and Palmtop Computers
Battery-Powered Equipment
Hand-Held Equipment
Peripherals

Pin Configuration



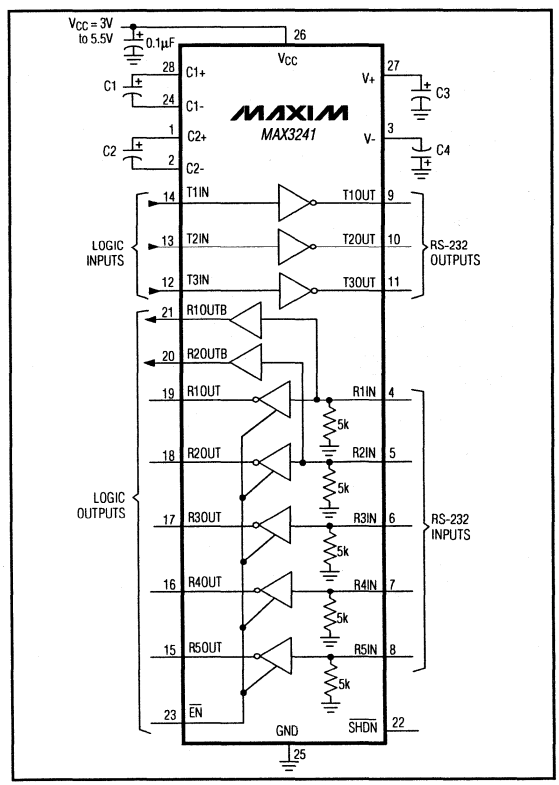
Features

- ♦ **Low 300µA Supply Current**
- ♦ **Guaranteed 120kbps Data Rate**
- ♦ **Guaranteed Mouse Driveability**
- ♦ **1µA Low-Power Shutdown Mode**
- ♦ **5 Receivers Active in Shutdown**
- ♦ **Flow-Through Pinout**
- ♦ **28-Pin SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3241CWI	0°C to +70°C	28 Wide SO
MAX3241CAI	0°C to +70°C	28 SSOP

Typical Operating Circuit



*Covered by U.S. Patent numbers 4,636,930; 4,679,134; 4,777,577; 4,797,899; 4,809,152; 4,897,774; 4,999,761; and other patents pending.

3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ (Note 1) ..... -0.3V to +7V
V- (Note 1) ..... +0.3V to -7V
V+ + IV-I (Note 1) ..... +13V
Input Voltages
T_IN, $\overline{SHDN}$, $\overline{EN}$ ..... -0.3V to +6V
R_IN ..... ±25V
Output Voltages
T_OUT ..... ±13.2V
R_OUT, R_OUTB ..... -0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
T_OUT ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Wide SO 1000mW
SSOP 762mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.5V; C1–C4 = 0.1µF (Note 2); T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{CC} Power-Supply Current	No load, V_{CC} = 3.3V or 5.0V, T_A = +25°C			0.3	1.0	mA
Shutdown Supply Current	Figure 3, T_A = +25°C			1	10	µA
LOGIC						
Input Logic Threshold Low	T_IN, $\overline{EN}$, $\overline{SHDN}$				0.8	V
Input Logic Threshold High	T_IN, $\overline{EN}$, $\overline{SHDN}$	V_{CC} = 3.3V	2.0			V
		V_{CC} = 5.0V	2.4			
Input Leakage Current	T_IN, $\overline{EN}$, $\overline{SHDN}$ = 0V or V_{CC}			±0.01	±1.0	µA
Output Leakage Current	$\overline{EN}$ = V_{CC}			±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6V	V_{CC} - 0.1V		V
RECEIVER INPUTS						
Input Voltage Range			-25		+25	V
Input Threshold Low	T_A = +25°C	V_{CC} = 3.3V	0.6	1.2		V
		V_{CC} = 5.0V	0.8	1.5		
Input Threshold High	T_A = +25°C	V_{CC} = 3.3V		1.7	2.4	V
		V_{CC} = 5.0V		1.5	2.4	
Input Hysteresis				0.1		V
Input Resistance	T_A = +25°C		3	5	7	kΩ

3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 5.5V; C1–C4 = 0.1µF (Note 2); T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

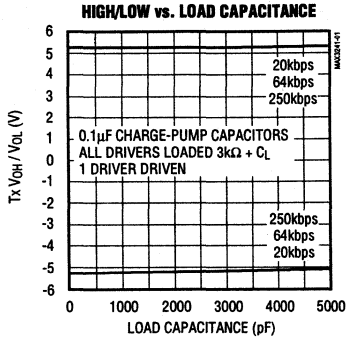
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMITTER OUTPUTS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current				±35	±50	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3.0V to 5.5V, $\overline{SHDN}$ = 0V				±25	µA
MOUSE DRIVEABILITY						
Transmitter Output Voltage	T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to GND, T1OUT and T2OUT loaded with 5mA		±5			V
TIMING CHARACTERISTICS						
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		120	230		kbps
Receiver Propagation Delay	Receiver IN to receiver OUT, C_L = 150pF	t_{PHL}		0.3		µs
		t_{PLH}		0.3		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	| t_{PHL} - t_{PLH} |			300		ns
Receiver Skew	| t_{PHL} - t_{PLH} |			300		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, T_A = +25°C, C_L = 100pF to 2500pF, measured from +3V to -3V or -3V to +3V, Figure 1		4	8.0	30	V/µs

Note 2: C1–C4 = 0.1µF, tested at 3.3V ±10%.
C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%.

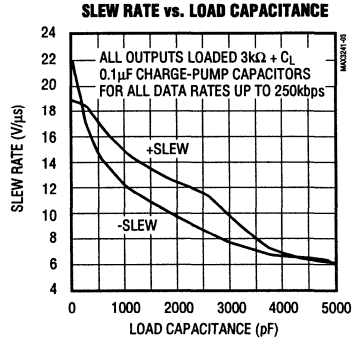
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = 3.3V, unless otherwise noted.)

TRANSMITTER OUTPUT VOLTAGE HIGH/LOW vs. LOAD CAPACITANCE



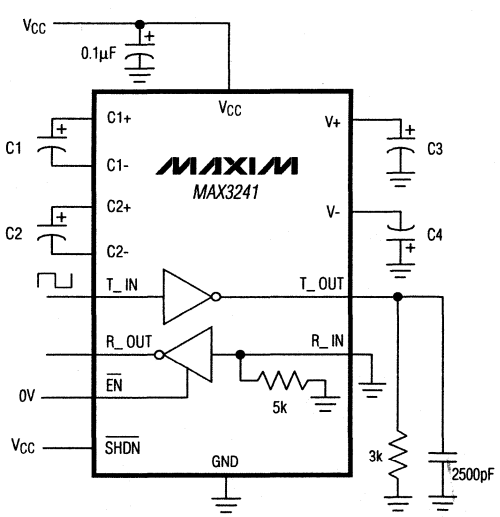
SLEW RATE vs. LOAD CAPACITANCE



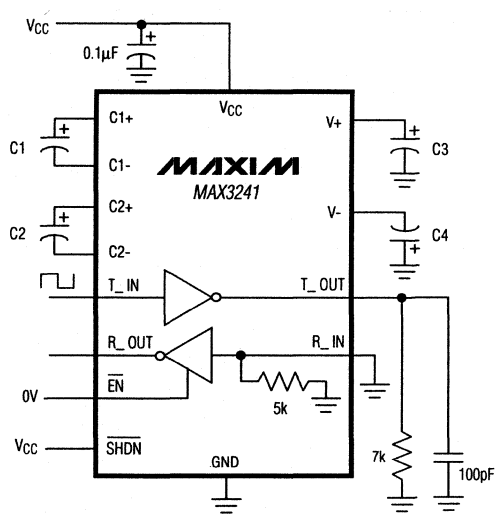
3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

Pin Description

PIN	NAME	FUNCTION
1	C2+	Positive Terminal of Inverting Charge-Pump Capacitor
2	C2-	Negative Terminal of Inverting Charge-Pump Capacitor
3	V-	-5.4V Generated by the Charge Pump
4–8	R1IN - R5IN	RS-232 Receiver Inputs
9, 10, 11	T1OUT, T2OUT, T3OUT	RS-232 Driver Outputs
12, 13, 14	T3IN, T2IN, T1IN	TTL/CMOS Driver Inputs
15–19	R5OUT - R1OUT	TTL/CMOS Receiver Outputs
20, 21	R2OUTB, R1OUTB	Noninverting Complementary Receiver Outputs—always active
22	$\overline{SHDN}$	Active-Low Shutdown Control
23	$\overline{EN}$	Active-Low Receiver Enable
24	C1-	Negative Terminal of Positive Charge-Pump Capacitor
25	GND	Ground
26	V_{CC}	+3.0V to +5.5V Supply Voltage
27	V+	+5.4V Generated by the Charge Pump
28	C1+	Positive Terminal of Positive Charge-Pump Capacitor



MINIMUM SLEW-RATE TEST CIRCUIT



MAXIMUM SLEW-RATE TEST CIRCUIT

Figure 1. Slew-Rate Test Circuit

3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3241 internal power supply consists of a regulated dual charge pump that provides output voltages of +5.4V (doubling charge pump) and -5.4V (inverting charge pump), regardless of the input voltage (V_{CC}) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode; if the output voltages are less than 5.4V, the charge pumps are enabled, and if the output voltages exceed 5.4V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Drivers

The MAX3241's drivers are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels.

The transmitters guarantee a 120kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Typically, the MAX3241 can operate at data rates above 230kbps. Transmitters can be paralleled to drive multiple receivers or mice.

The output stage is turned off (high impedance) when the device is in shutdown mode or when the power is off, permitting the outputs to be driven up to ±12V.

The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

RS-232 Receivers

The MAX3241's receivers convert RS-232 signals to CMOS-logic output levels. All receivers have one inverting three-state output, and two of them also have complementary (noninverting) outputs. In shutdown, all five inverting receivers can be either active or inactive.

The two complementary outputs (R1OUTB, R2OUTB) are always active, regardless of the state of $\overline{EN}$ or $\overline{SHDN}$, allowing ring indicator to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accomodate peripherals, such as UARTs (Figure 2).

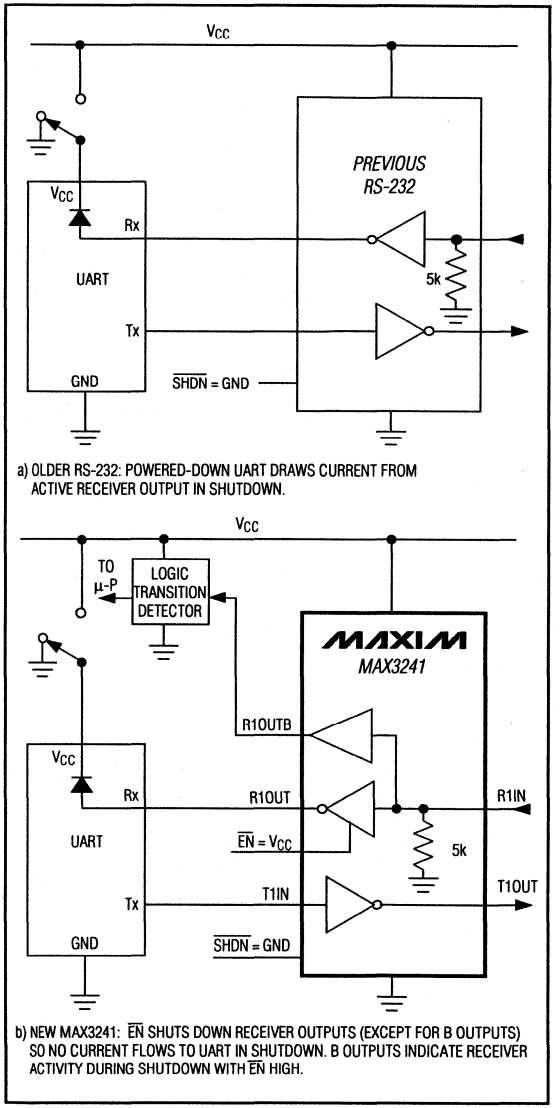


Figure 2. Detection of RS-232 Activity when the UART and Interface are Shut Down; Comparison of MAX3241 (b) with Previous Transceivers (a).

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3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

Shutdown Mode

Supply current reduces to less than 1µA in shutdown mode ($\overline{SHDN}$ = low). When shut down, the device's charge pumps are turned off, V+ is pulled down to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled (high impedance). The time required to exit shutdown is typically 100µs, as shown in Figure 3. Connect $\overline{SHDN}$ to V_{CC} if the shutdown mode is not used. $\overline{SHDN}$ has no effect on R_OUT or R_OUTB.

Enable Control

The five inverting receiver outputs (R_OUT) are put into a high-impedance state when $\overline{EN}$ is high. The complementary outputs R1OUTB and R2OUTB are always active, regardless of the state of $\overline{EN}$ and $\overline{SHDN}$ (Table 1). $\overline{EN}$ has no effect on T_OUT.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX3241 requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 2 for recommended capacitor values. Do not use values smaller than those listed in Table 2. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing the value of C1. However, do not increase C1 without also increasing the values of C2, C3, and C4, to maintain the proper ratios (C1 to the other capacitors).

When using the minimum recommended capacitor values, make sure the capacitor value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Power-Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C1. Connect bypass capacitors as close to the IC as possible.

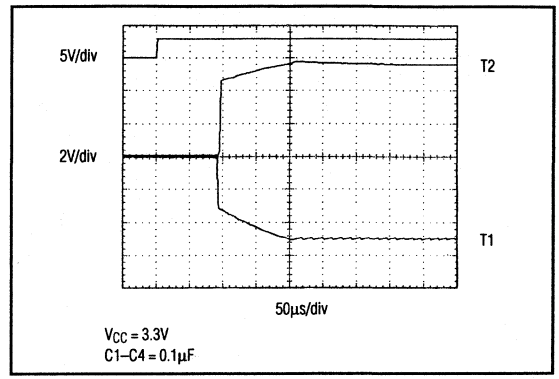


Figure 3. MAX3241 Driver Outputs when Exiting Shutdown

Table 1. Shutdown and Enable Control Truth Table

$\overline{SHDN}$	$\overline{EN}$	T_OUT	R_OUT	R_OUTB
0	0	High-Z	Active	Active
0	1	High-Z	High-Z	Active
1	0	Active	Active	Active
1	1	Active	High-Z	Active

Table 2. Recommended Capacitor Values

V_{CC} (V)	C1 (µF)	C2, C3, C4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

Driver Outputs when Exiting Shutdown

Figure 3 shows two MAX3241 transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V.

3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

High Data Rates

The MAX3241 maintains the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 4 shows a transmitter loopback test circuit. Figure 5 shows a loopback test result at 120kbps, and Figure 6 shows the same test at 240kbps. For Figure 5, all three transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 6, a single transmitter was driven at 240kbps, but all three transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

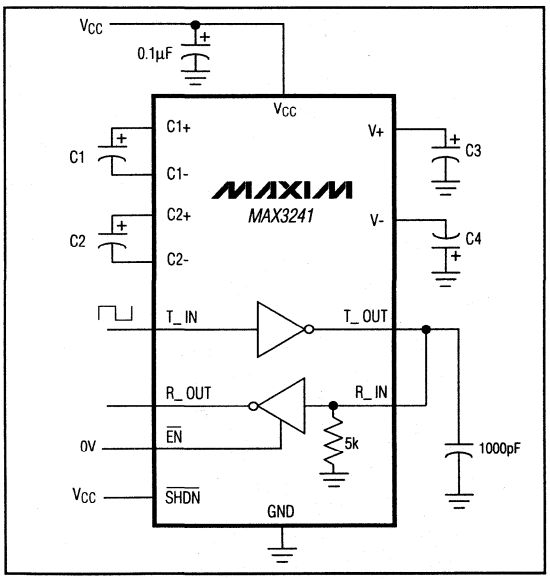


Figure 4. Loopback Test Circuit

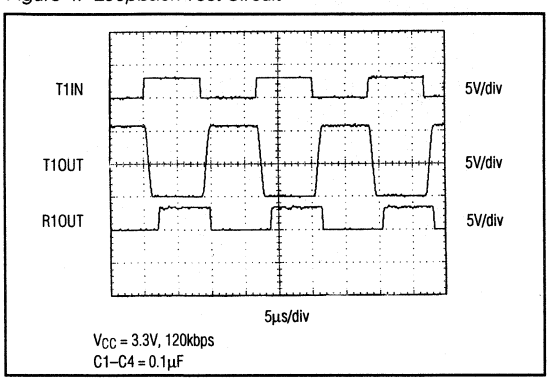


Figure 5. Loopback Test Result at 120kbps

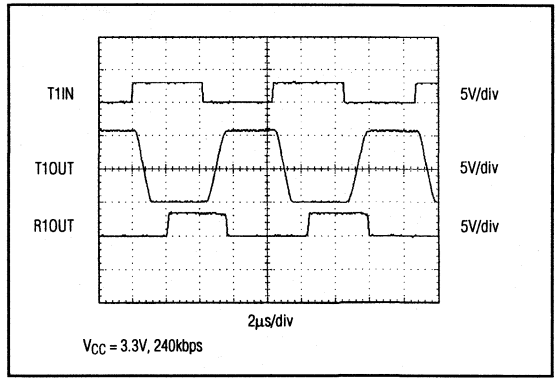


Figure 6. Loopback Test Result at 240kbps

Interconnection with 3V and 5V Logic

The MAX3241 operates at V_{CC} = 3.0V to 5.5V. For interconnection with +3.3V logic, V_{CC} should be 3.3V. For interconnection with +5.0V logic, V_{CC} should be 5.0V. See Table 3 for more information on all possible combinations of interconnections.

Table 3. Logic Family Compatibility with Various Supply Voltages

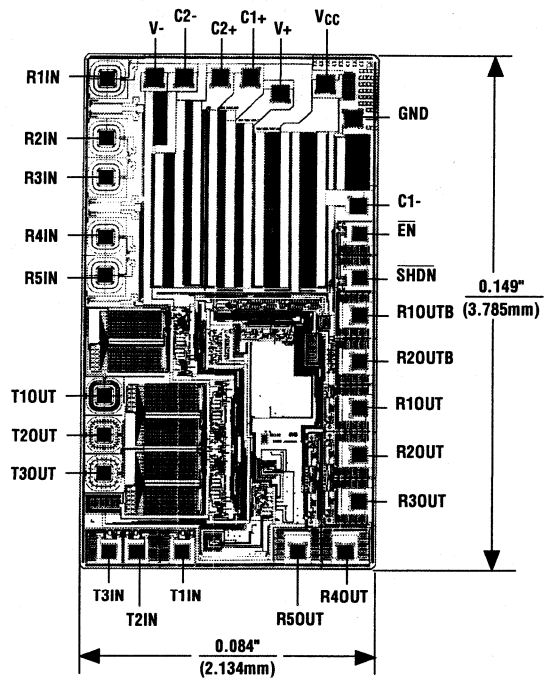
SYSTEM POWER-SUPPLY VOLTAGE	V_{CC} SUPPLY VOLTAGE	COMPATIBILITY
3.3V	3.3V	Compatible with all CMOS families.
5V	5V	Compatible with all TTL and CMOS-logic families.
5V	3.3V	Compatible with ACT and HCT CMOS, and with TTL. Incompatible with AC, HC, or CD4000 CMOS.

3V to 5.5V, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors

3V-Powered EIA/TIA-232 and EIA/TIA-562 Transceivers from Maxim

PART	POWER SUPPLY VOLTAGE (V)	No. OF TRANSMITTERS/ RECEIVERS	No. OF RECEIVERS ACTIVE IN SHUTDOWN	DATA RATE (kbps)	EIA/TIA-232 OR 562	FEATURES
MAX212	3.0 to 3.6	3/5	5	230	232	Drives mice
MAX218	1.8 to 4.25	2/2	2	230	232	Operates directly from batteries without a voltage regulator
MAX560	3.0 to 3.6	4/5	2	120	562	Pin compatible with MAX213
MAX561	3.0 to 3.6	4/5	0	120	562	Pin compatible with MAX241
MAX562	2.7 to 5.25	3/5	5	250	562	Wide supply range
MAX563	3.0 to 3.6	2/2	2	230	562	0.1µF capacitors
MAX3241	**3.0 to 5.5**	**3/5**	**5**	**230**	**232**	**0.1µF capacitors, 2 complementary receivers, drives mice**

Chip Topography



TRANSISTOR COUNT: 466

SUBSTRATE CONNECTED TO GND

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

High-Speed Transimpedance Amplifier

General Description

The MAX3260, a high-speed, transimpedance amplifier, is ideally suited for fiber optic applications. The low noise and wide bandwidth characteristics make it useful for RF and general purpose applications as well.

The amplifier converts a current input to a voltage output. The small signal transimpedance gain of 2kΩ is set by a NiCr resistor with a temperature coefficient of 150ppm/°C.

A DC restore feedback network prevents amplifier saturation at high input currents, allowing input currents as high as 900µA to be amplified linearly. The restore function is disabled at low input levels to reduce noise. The low noise floor of the amplifier allows detection of signals as small as 2.4µA. This extended dynamic range makes the MAX3260 useful in optical receiver systems with as much as 25dB of input signal range.

A 1kΩ NiCr resistor is provided on the IC for use in the bias filter network of a photodiode.

The circuit operates from a single +5V supply, and consumes less than 0.25W of power.

The MAX3260 is fully compatible with the MAX3262 post amplifier.

This product is only available as dice.

Features

- **1GHz Bandwidth**
- **Single 5V Supply**
- **Low Noise**
- **Wide Dynamic Range**

Applications

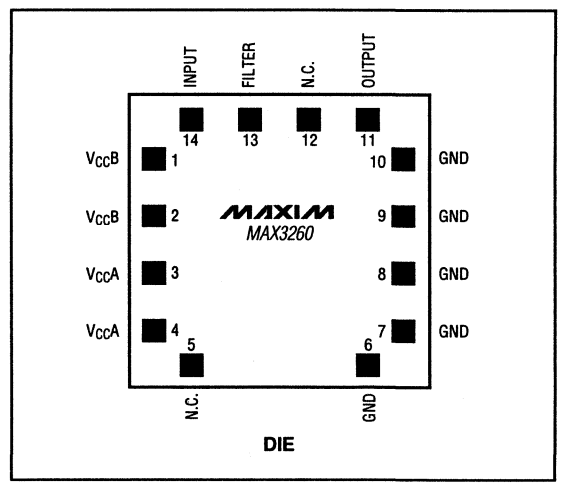
High-Speed Fiber Optics

531Mbps and 1062Mbps Fibre Channel

622Mbps SDH/SONET

Current to Voltage Converters

Die Configuration



MAXIM

High-Speed Laser Diode Driver

General Description

The MAX3261 high-speed laser diode driver can drive NRZ bit rates up to 1200Mbps.

The device accepts differential PECL inputs and provides complementary output currents programmable from 5mA to 25mA modulation and 5mA to 60mA bias. The output modulation current and output bias currents are set by external resistors.

An automatic power control (APC) circuit is provided to maintain constant laser power in transmitters that use a monitor photodiode. Only one external resistor is needed to implement the APC function.

Complementary enable inputs allow the MAX3261 to interface with Open Fiber Control Architectures.

Laser failure is indicated through the TTL-compatible fail output.

System power-up is controlled by a slowstart system to prevent laser damage. The slowstart is preset to 50ns, and can be extended by the addition of external capacitors.

A temperature stabilized reference voltage is provided to make laser current level programming simple.

This product is available as dice and in a 32-pin TQFP package.

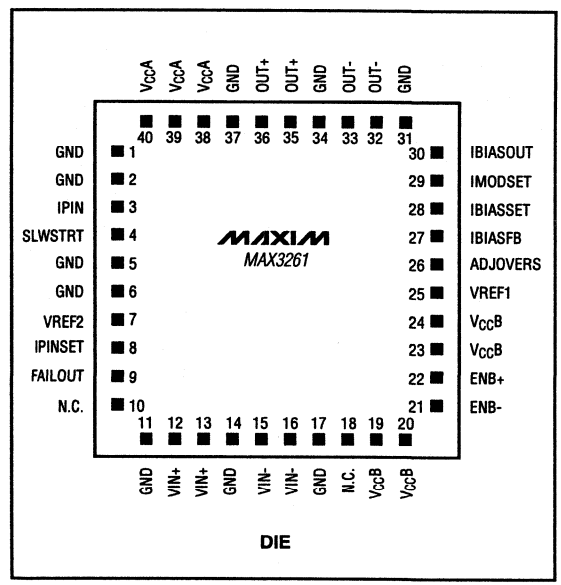
Features

- ♦ **300ps Rise Time**
- ♦ **Differential PECL Inputs**
- ♦ **Single 5V Supply**
- ♦ **Automatic Power Control**
- ♦ **1.2Gbps NRZ**
- ♦ **Low Cost**

Applications

Laser Diode Transmitters
531Mbps and 1062Mbps Fibre Channel
622Mbps SDH/SONET
Current Driver

Die Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

High-Speed Limiting Amplifier

General Description

The MAX3262 limiting amplifier with its high gain and wide bandwidth is ideal for use as a post amplifier in fiber optic receivers with data rates up to 1Gbps.

The DIV2 input to the amplifier allows the gain to be set in either a 30dB or 50dB range. In the 50dB gain mode, signals as small as $6mV_{P-P}$ can be amplified to PECL levels.

The VLOS input is used to control the loss of signal assertion point, which can be set between 3mV and 24mV (input signal level, peak to peak). Level detect hysteresis for any programmed LOS level is nominally 4dB. Complementary LOS outputs are provided.

An offset zeroing circuit uses external capacitance to reduce output offset to negligible levels.

The Enable Input (EN) allows the output to be disabled without removing the incoming signal. EN also renders the LOS inoperative.

The MAX3262 operates from a single 5V power supply, and uses less than 1/3W of power.

This product is available as dice and in a 24-pin SSOP package.

Features

- ♦ **1GHz Bandwidth**
- ♦ **Up to 50dB Gain**
- ♦ **Selectable Gain**
- ♦ **Loss of Signal Indicator**
- ♦ **Single 5V Power Supply**
- ♦ **Differential PECL Inputs and Outputs**

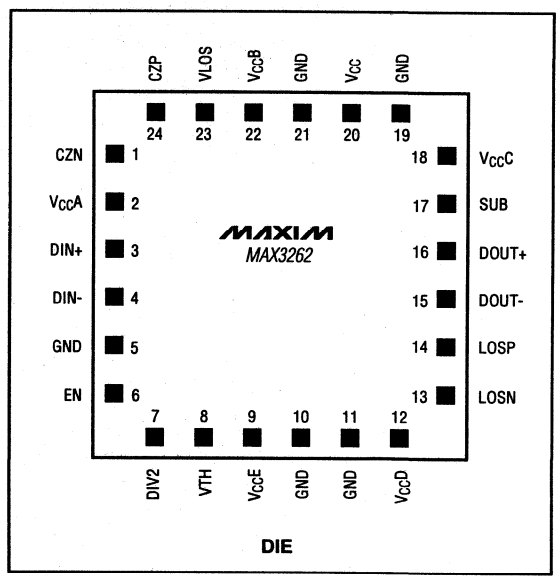
Applications

531Mbps and 1062Mbps Fibre Channel

622Mbps SONET

Digital Receivers

Die Configuration



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19-0122; Rev 3; 4/94

MAXIM

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

General Description

The MAX481, MAX483, MAX485, and MAX487–MAX491 are low-power transceivers for RS-485 and RS-422 communication. Each part contains one driver and one receiver. The MAX483, MAX487, MAX488, and MAX489 feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission at data rates up to 250kbps. The driver slew rates of the MAX481, MAX485, MAX490, and MAX491 are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw between 120µA and 500µA of supply current. Additionally, the MAX481, MAX483, and MAX487 have a low-current shutdown mode in which they consume only 0.1µA. All parts operate from a single 5V supply.

Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487 features a quarter-unit-load receiver input impedance, allowing up to 128 MAX487 transceivers on the bus. Full-duplex communications are obtained using the MAX488–MAX491, while the MAX481, MAX483, MAX485, and MAX487 are designed for half-duplex applications.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Features

- **In µMAX Package: Smallest 8-Pin SO**
- **Slew-Rate Limited for Errorless Data Transmission (MAX483/487/488/489)**
- **0.1µA Low-Current Shutdown Mode (MAX481/483/487)**
- **Low Quiescent Current: 120µA (MAX483/487/488/489) 300µA (MAX481/485/490/491)**
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481/485/490/491)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Operate from a Single 5V Supply**
- **Allows up to 128 Transceivers on the Bus (MAX487)**
- **Current-Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481CPA	0°C to +70°C	8 Plastic DIP
MAX481CSA	0°C to +70°C	8 SO
MAX481CUA	0°C to +70°C	8 µMAX
MAX481C/D	0°C to +70°C	Dice*
MAX481EPA	-40°C to +85°C	8 Plastic DIP
MAX481ESA	-40°C to +85°C	8 SO
MAX481MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481	Half	2.5	No	Yes	Yes	300	32	8
MAX483	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485	Half	2.5	No	No	Yes	300	32	8
MAX487	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488	Full	0.25	Yes	No	No	120	32	8
MAX489	Full	0.25	Yes	No	Yes	120	32	14
MAX490	Full	2.5	No	No	No	300	32	8
MAX491	Full	2.5	No	No	Yes	300	32	14

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} +0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 830mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487C_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487E_ A ..... -40°C to +85°C
MAX4_ _MJ_/MAX1487MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 4		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 4				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 4				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487/MAX1487	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487/MAX1487, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487/MAX1487		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487/MAX1487		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current (See Note 3 for No Load)	I_{CC}	MAX488/MAX489 DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490/MAX491 DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481/MAX485 $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX483/MAX487 $\overline{RE}$ = 0V or V_{CC}	DE = 5V	MAX483		350	650	
				MAX487		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481/483/487, DE = 0V, $\overline{RE}$ = V_{CC}				0.1	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA

SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	30	60	ns
	t_{PHL}			10	30	60	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485	3	15	40	ns
			MAX490C/E, MAX491C/E	5	15	25	
			MAX490M, MAX491M	3	15	40	
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed			40	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed			40	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed			40	70	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed			40	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481, MAX485	20	90	200	ns
			MAX490C/E, MAX491C/E	20	90	150	
			MAX490M, MAX491M	20	90	200	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			13		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481 (Note 5)		50	200	600	ns

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

SWITCHING CHARACTERISTICS—MAX481/MAX485, MAX490/MAX491 (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 7 and 9, C_L = 100pF, S2 closed		40	100	ns
Driver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 7 and 9, C_L = 100pF, S1 closed		40	100	ns
Receiver Enable from Shutdown to Output High (MAX481)	$t_{ZH(SHDN)}$	Figures 5 and 11, C_L = 15pF, S2 closed, A - B = 2V		300	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481)	$t_{ZL(SHDN)}$	Figures 5 and 11, C_L = 15pF, S1 closed, B - A = 2V		300	1000	ns

SWITCHING CHARACTERISTICS—MAX483, MAX487/MAX488/MAX489

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 6 and 8, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 7 and 9, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 7 and 9, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 7 and 9, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 7 and 9, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 6 and 10, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 5 and 11, C_{RL} = 15pF, S1 closed		20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 5 and 11, C_{RL} = 15pF, S2 closed		20	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	(Note 5) MAX483/MAX487	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 7 and 9, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483/MAX487, Figures 5 and 11, C_L = 15pF, S1 closed			2500	ns

NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Supply current specification is valid for loaded transmitters when DE = V_{CC}.

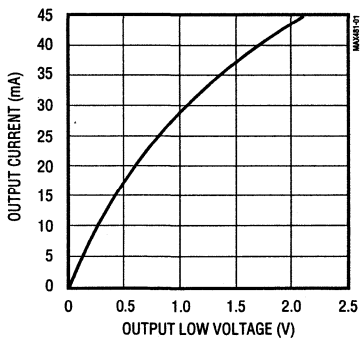
Note 4: Applies to peak current. See *Typical Operating Characteristics.*

Note 5: The MAX481/MAX483/MAX487 are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

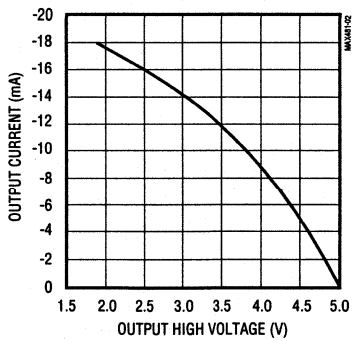
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

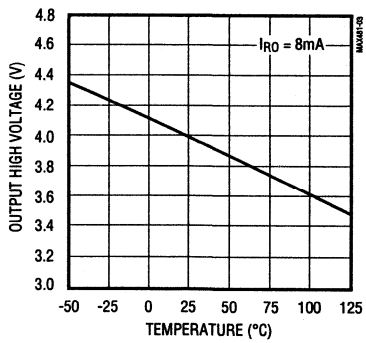
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



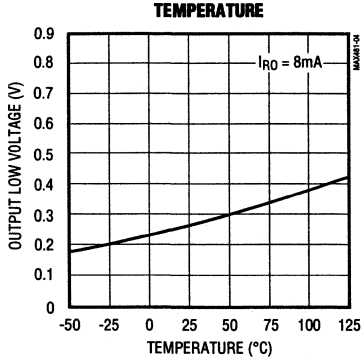
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



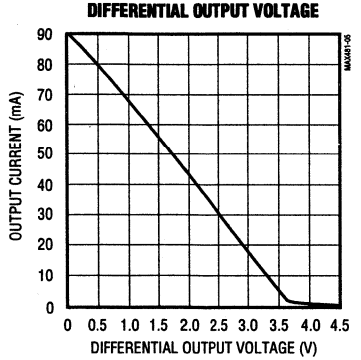
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



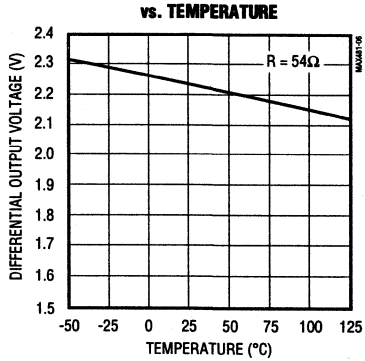
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE

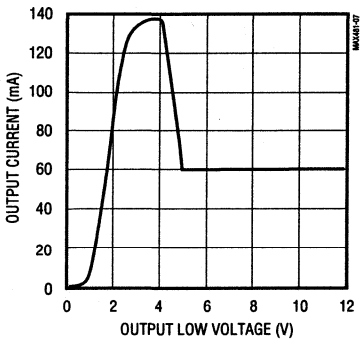


Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

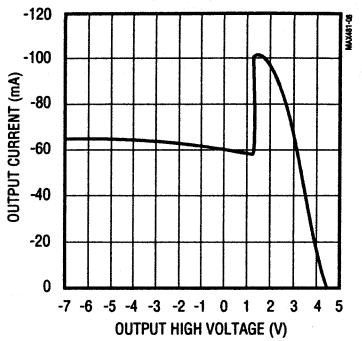
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

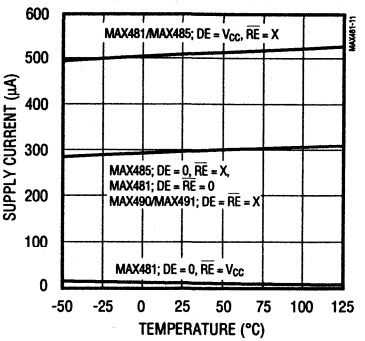
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



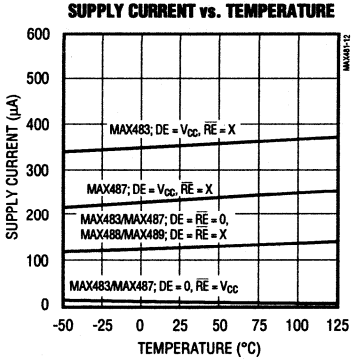
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



MAX481/MAX485/MAX490/MAX491 SUPPLY CURRENT vs. TEMPERATURE



MAX483/MAX487–MAX489 SUPPLY CURRENT vs. TEMPERATURE



PIN					NAME	FUNCTION
MAX481/MAX483/ MAX485/MAX487		MAX488/ MAX490		MAX489/ MAX491		
DIP/SO	µMAX	DIP/SO	µMAX	DIP/SO		
1	3	2	4	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	4	—	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	5	—	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	6	3	5	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	7	4	6	6, 7	GND	Ground
—	—	5	7	9	Y	Noninverting Driver Output
—	—	6	8	10	Z	Inverting Driver Output
6	8	—	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	—	8	2	12	A	Noninverting Receiver Input
7	1	—	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	—	7	1	11	B	Inverting Receiver Input
8	2	1	3	14	V_{CC}	Positive Supply: 4.75V ≤ V_{CC} ≤ 5.25V
—	—	—	—	1, 8, 13	N.C.	No Connect—not internally connected

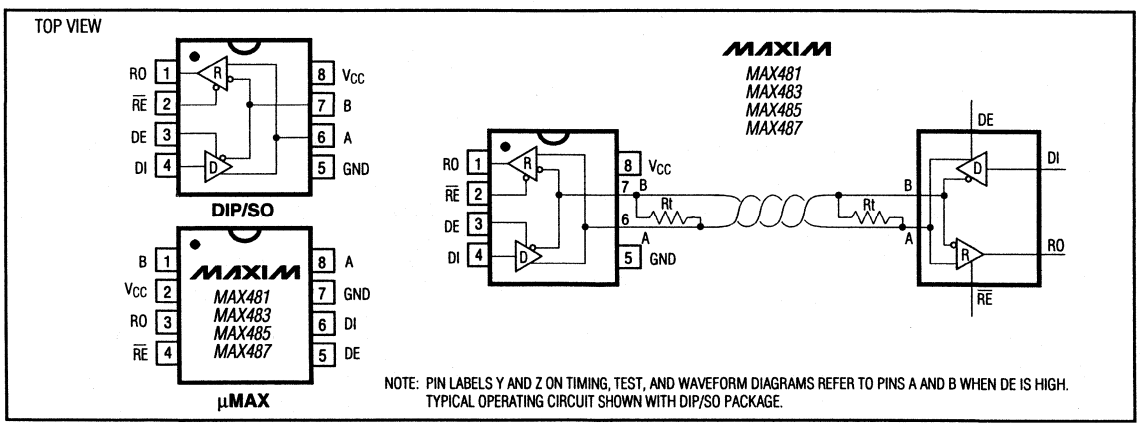


Figure 1. MAX481/MAX483/MAX485/MAX487 Pin Configuration and Typical Operating Circuit

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

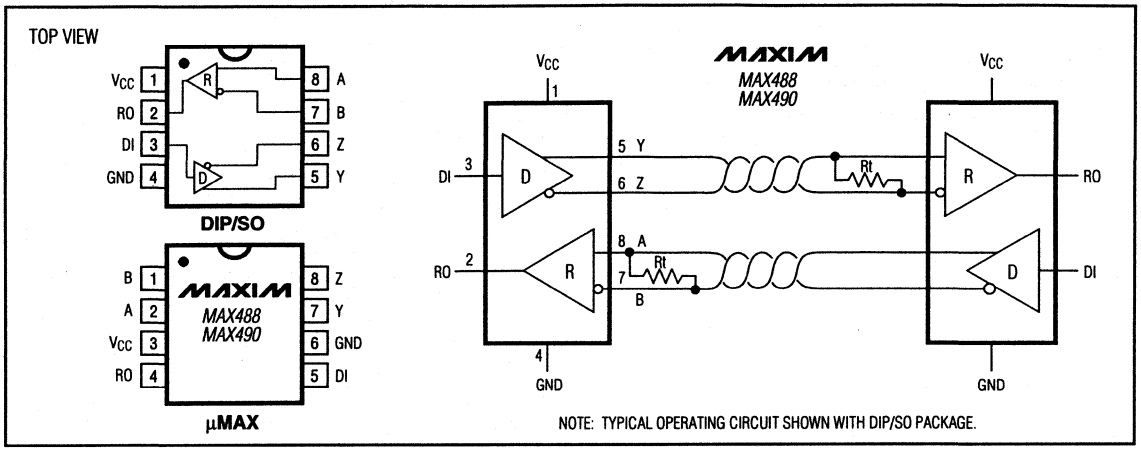


Figure 2. MAX488/MAX490 Pin Configuration and Typical Operating Circuit

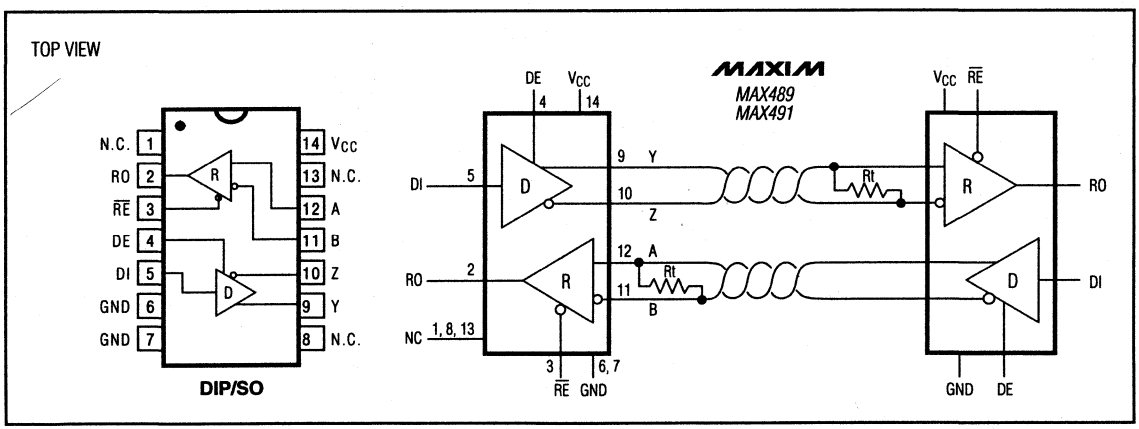


Figure 3. MAX489/MAX491 Pin Configuration and Typical Operating Circuit

Applications Information

The MAX481/MAX483/MAX485 and MAX487-MAX491 are low-power transceivers for RS-485 and RS-422 communications. The MAX481, MAX485, MAX490, and MAX491 can transmit and receive at data rates up to 2.5Mbps, while the MAX483, MAX487, MAX488, and MAX489 are specified for data rates up to 250kbps. The MAX488-MAX491 are full-duplex transceivers while the MAX481, MAX483, MAX485, and MAX487 are half-duplex. In addition, Driver Enable (DE) and Receiver Enable ($\overline{RE}$) pins are included on the MAX481, MAX483, MAX485, MAX487, MAX489, and MAX491. When disabled, the driver and receiver outputs are high impedance.

MAX487: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487 allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487 and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481/MAX483/MAX485 and MAX488-MAX491 have standard 12kΩ impedance.

Test Circuits

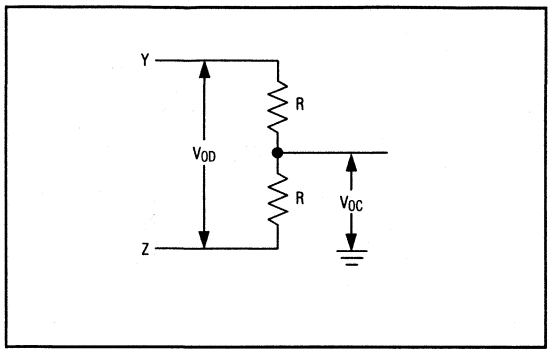


Figure 4. Driver DC Test Load

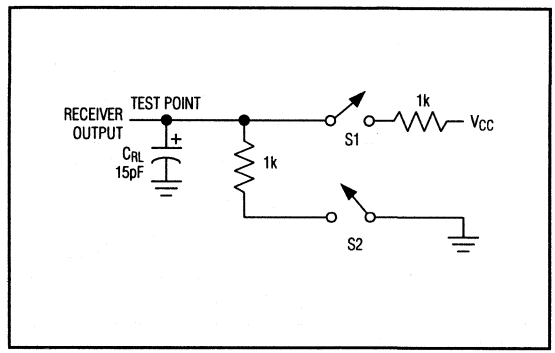


Figure 5. Receiver Timing Test Load

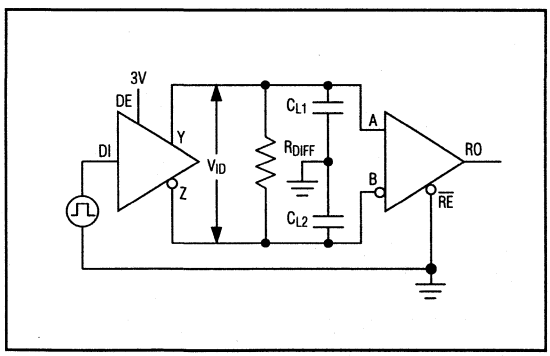


Figure 6. Driver/Receiver Timing Test Circuit

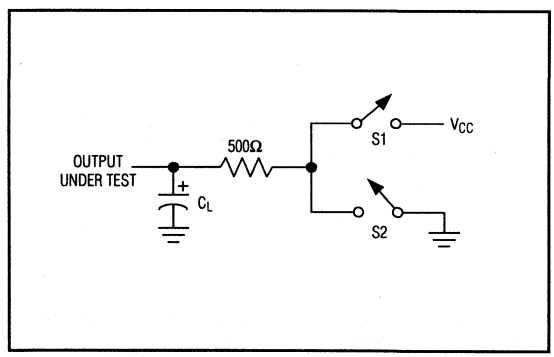


Figure 7. Driver Timing Test Load

MAX483/MAX487/MAX488/MAX489: Reduced EMI and Reflections

The MAX483 and MAX487–MAX489 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 12 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481, MAX485, MAX490, or MAX491. High-frequency harmonics with large amplitudes are evident. Figure 13 shows the same information displayed for a MAX483, MAX487, MAX488, or MAX489 transmitting under the same conditions. Figure 13's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Switching Waveforms

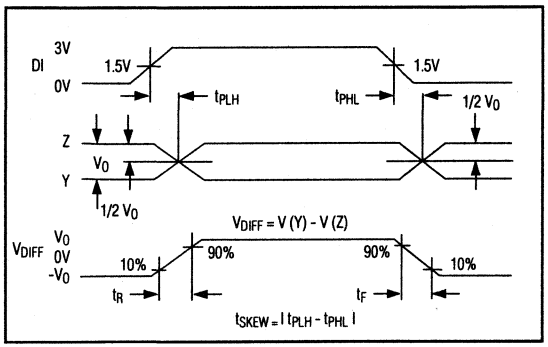


Figure 8. Driver Propagation Delays

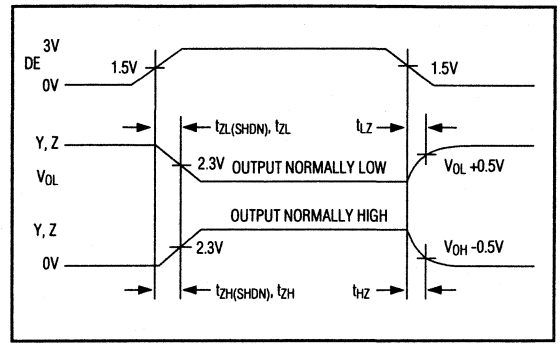


Figure 9. Driver Enable and Disable Times for MAX481/MAX483/MAX485/MAX487/MAX489/MAX491

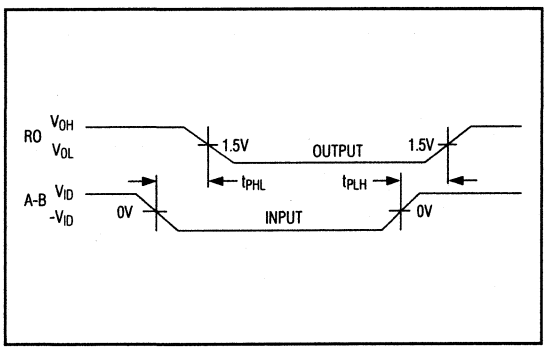


Figure 10. Receiver Propagation Delays

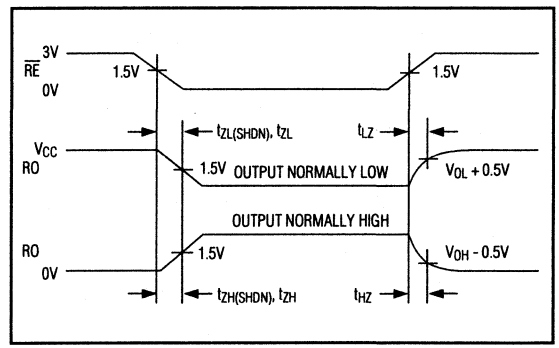


Figure 11. Receiver Enable and Disable Times for MAX481/MAX483/MAX485/MAX487/MAX489/MAX491

Function Tables (MAX481/MAX483/MAX485/MAX487)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	Hi-Z	Hi-Z
1	0	X	Hi-Z*	Hi-Z*

X = Don't care
Hi-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	Hi-Z*

X = Don't care
Hi-Z = High impedance
* Shutdown mode for MAX481/MAX483/MAX487

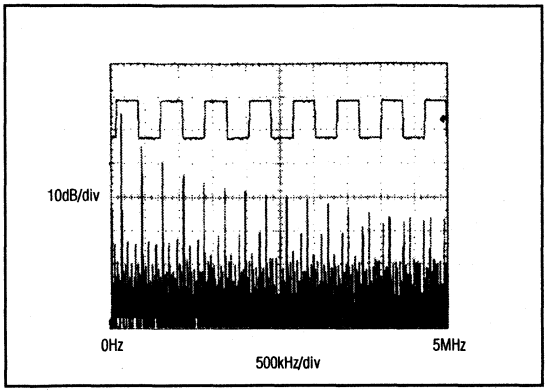


Figure 12. Driver Output Waveform and FFT Plot of MAX481/ MAX485/MAX490/MAX491 Transmitting a 150kHz Signal

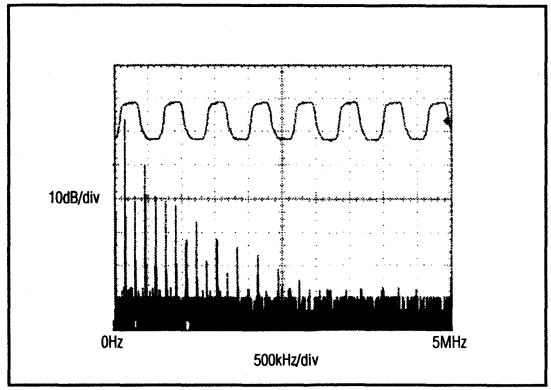


Figure 13. Driver Output Waveform and FFT Plot of MAX483/ MAX487–MAX489 Transmitting a 150kHz Signal

Low-Power Shutdown Mode (MAX481/MAX483/MAX487)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.1µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481, MAX483, and MAX487, the t_{ZH} and t_{ZL} enable times assume that the part was not in the low-power shutdown state (the MAX485 and MAX488-MAX491 can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume that the parts were shut down (see *Electrical Characteristics*).

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0,0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 15-18 using the test circuit of Figure 14.

The difference in receiver delay times, $|t_{PLH} - t_{PHL}|$, is typically under 13ns for the MAX481, MAX485, MAX490 and MAX491, and is typically less than 100ns for the MAX483 and MAX487-MAX489.

The driver skew times are typically 5ns (10ns max) for the MAX481, MAX485, MAX490, and MAX491, and are typically 100ns (800ns max) for the MAX483 and MAX487-MAX489.

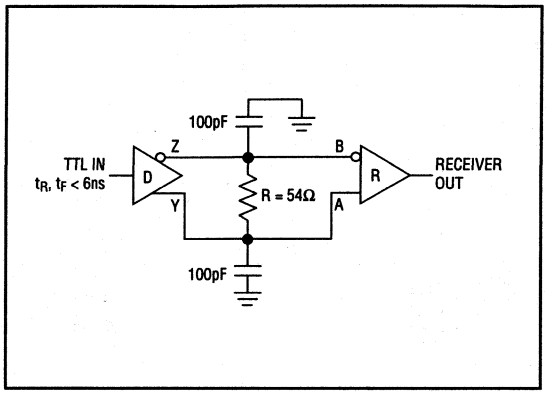


Figure 14. Receiver Propagation Delay Test Circuit

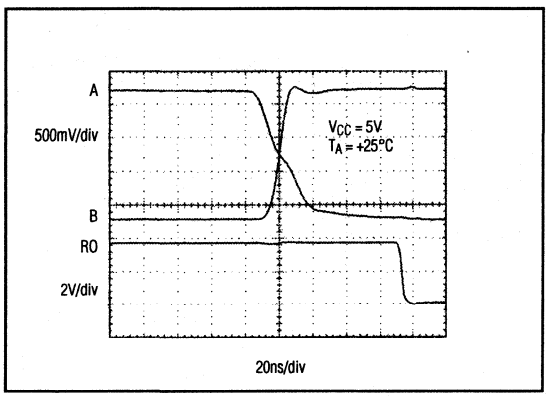


Figure 15. MAX481/MAX485/MAX490/MAX491 Receiver t_{PHL}

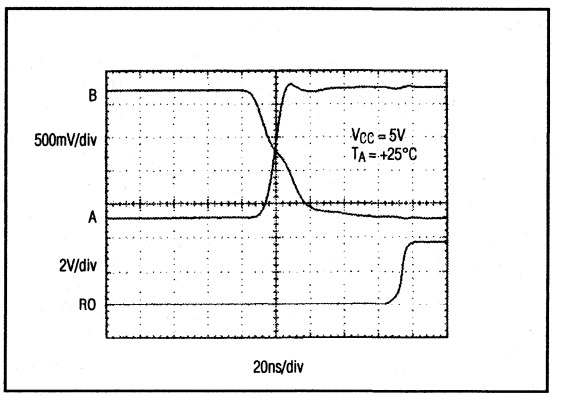


Figure 16. MAX481/MAX485/MAX490/MAX491 Receiver t_{PLH}

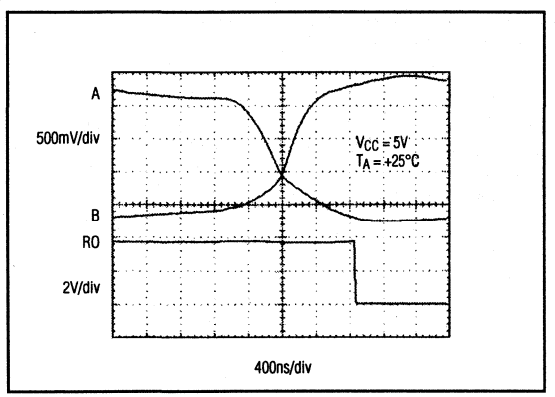


Figure 17. MAX483, MAX487–MAX489 Receiver t_{PHL}

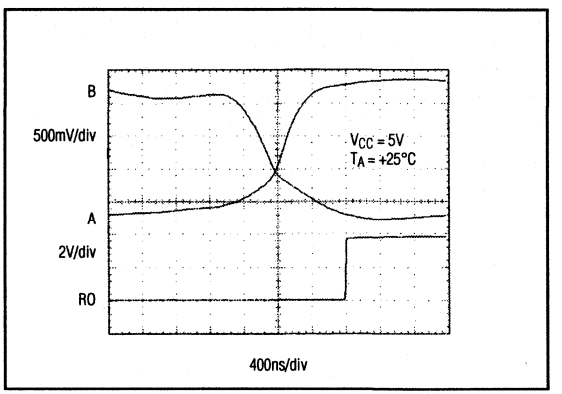


Figure 18. MAX483, MAX487–MAX489 Receiver t_{PLH}

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. For line lengths greater than 4000 feet, see Figure 23.

Figures 19 and 20 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 120Ω loads.

Typical Applications

The MAX481, MAX483, MAX485, and MAX487-MAX491 transceivers are designed for bidirectional data communications on multipoint bus transmission lines.

Figures 21 and 22 show typical network applications circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet, as shown in Figure 23.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483 and MAX487-MAX489 are more tolerant of imperfect termination.

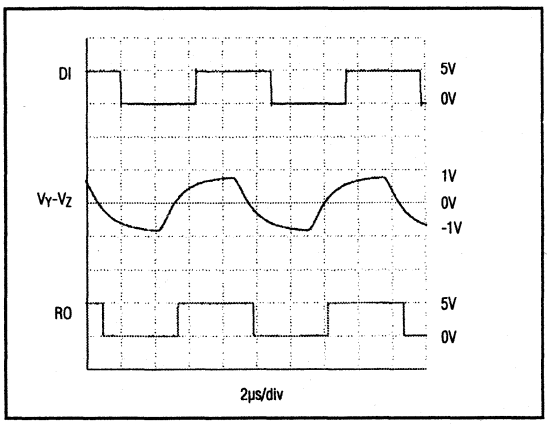


Figure 19. MAX481/MAX485/MAX490/MAX491 System Differential Voltage at 110kHz Driving 4000ft of Cable

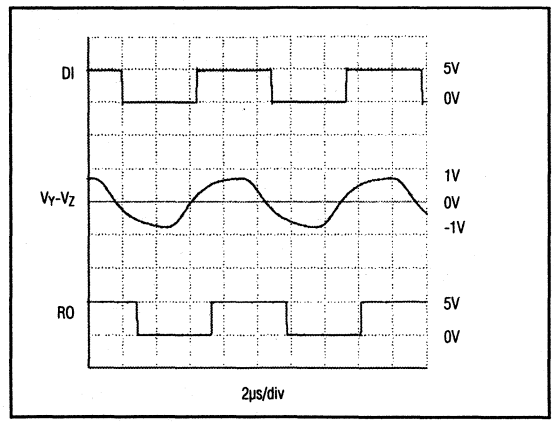


Figure 20. MAX483, MAX487–MAX489 System Differential Voltage at 110kHz Driving 4000ft of Cable

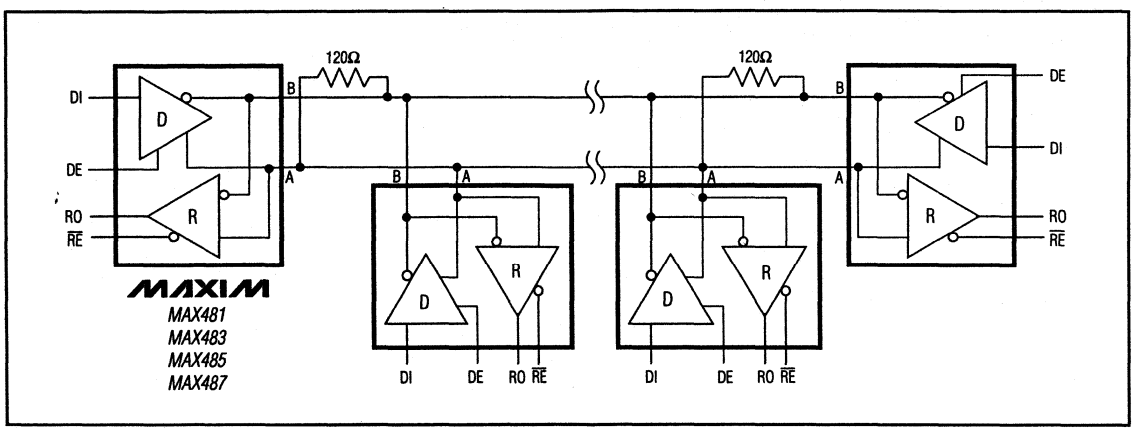


Figure 21. MAX481/MAX483/MAX485/MAX487 Typical RS-485 Network

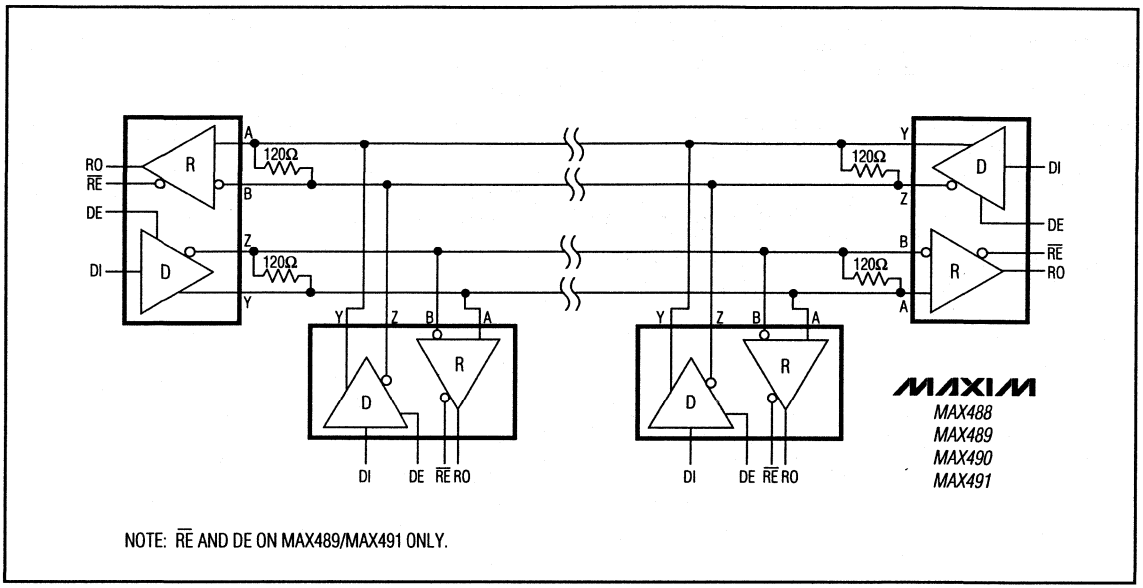


Figure 22. MAX488–MAX491 Full-Duplex RS-485 Network

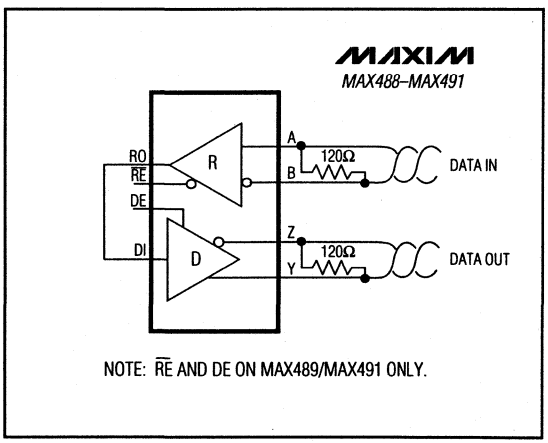


Figure 23. Line Repeater for MAX488–MAX491

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483CPA	0°C to +70°C	8 Plastic DIP
MAX483CSA	0°C to +70°C	8 SO
MAX483CUA	0°C to +70°C	8 µMAX
MAX483C/D	0°C to +70°C	Dice*
MAX483EPA	-40°C to +85°C	8 Plastic DIP
MAX483ESA	-40°C to +85°C	8 SO
MAX483MJA	-55°C to +125°C	8 CERDIP
MAX485CPA	0°C to +70°C	8 Plastic DIP
MAX485CSA	0°C to +70°C	8 SO
MAX485CUA	0°C to +70°C	8 µMAX
MAX485C/D	0°C to +70°C	Dice*
MAX485EPA	-40°C to +85°C	8 Plastic DIP
MAX485ESA	-40°C to +85°C	8 SO
MAX485MJA	-55°C to +125°C	8 CERDIP
MAX487CPA	0°C to +70°C	8 Plastic DIP
MAX487CSA	0°C to +70°C	8 SO
MAX487CUA	0°C to +70°C	8 µMAX
MAX487C/D	0°C to +70°C	Dice*
MAX487EPA	-40°C to +85°C	8 Plastic DIP
MAX487ESA	-40°C to +85°C	8 SO
MAX487MJA	-55°C to +125°C	8 CERDIP
MAX488CPA	0°C to +70°C	8 Plastic DIP
MAX488CSA	0°C to +70°C	8 SO
MAX488CUA	0°C to +70°C	8 µMAX
MAX488C/D	0°C to +70°C	Dice*
MAX488EPA	-40°C to +85°C	8 Plastic DIP
MAX488ESA	-40°C to +85°C	8 SO
MAX488MJA	-55°C to +125°C	8 CERDIP
MAX489CPD	0°C to +70°C	14 Plastic DIP
MAX489CSD	0°C to +70°C	14 SO
MAX489C/D	0°C to +70°C	Dice*
MAX489EPD	-40°C to +85°C	14 Plastic DIP
MAX489ESD	-40°C to +85°C	14 SO
MAX489MJD	-55°C to +125°C	14 CERDIP

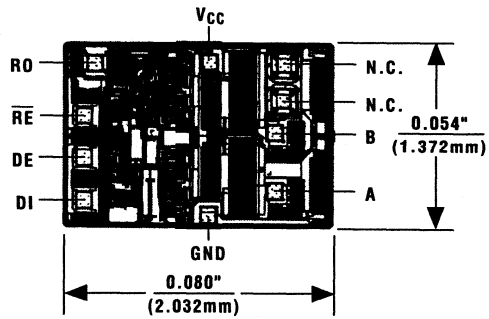
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX490CPA	0°C to +70°C	8 Plastic DIP
MAX490CSA	0°C to +70°C	8 SO
MAX490CUA	0°C to +70°C	8 µMAX
MAX490C/D	0°C to +70°C	Dice*
MAX490EPA	-40°C to +85°C	8 Plastic DIP
MAX490ESA	-40°C to +85°C	8 SO
MAX490MJA	-55°C to +125°C	8 CERDIP
MAX491CPD	0°C to +70°C	14 Plastic DIP
MAX491CSD	0°C to +70°C	14 SO
MAX491C/D	0°C to +70°C	Dice*
MAX491EPD	-40°C to +85°C	14 Plastic DIP
MAX491ESD	-40°C to +85°C	14 SO
MAX491MJD	-55°C to +125°C	14 CERDIP

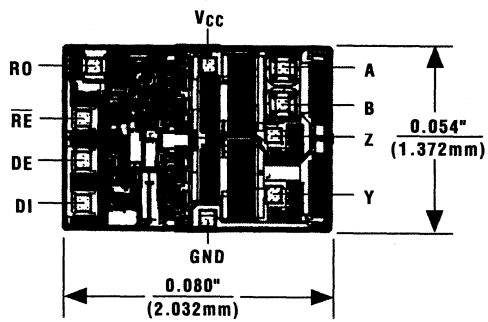
** Contact factory for dice specifications.*

Chip Topographies

MAX481/MAX483/MAX485/MAX487



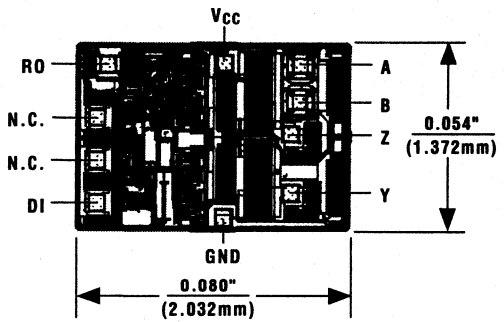
MAX489/MAX491



Low-Power, Slew-Rate-Limited RS-485/RS-422 Transceivers

____Chip Topographies (continued)

MAX488/MAX490



TRANSISTOR COUNT: 248

SUBSTRATE CONNECTED TO GND

19-0144; Rev. 0; 9/93

MAXIM

Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

General Description

The MAX562 is designed specifically for notebook and palmtop computers that need to transfer data quickly. It runs at data rates up to 230kbps, and has a guaranteed 4V/µs slew rate. This device meets the new EIA/TIA-562 standard that guarantees compatibility with RS-232 interfaces.

The MAX562 has low-power shutdown and keep-awake modes. In keep-awake mode, the transmitters are disabled but all receivers are active, allowing unidirectional communication. In shutdown mode, the entire chip is disabled and all outputs are in a high-impedance state.

The MAX562 is available in a standard 28-pin SO package, and in a smaller footprint shrink small-outline package (SSOP).

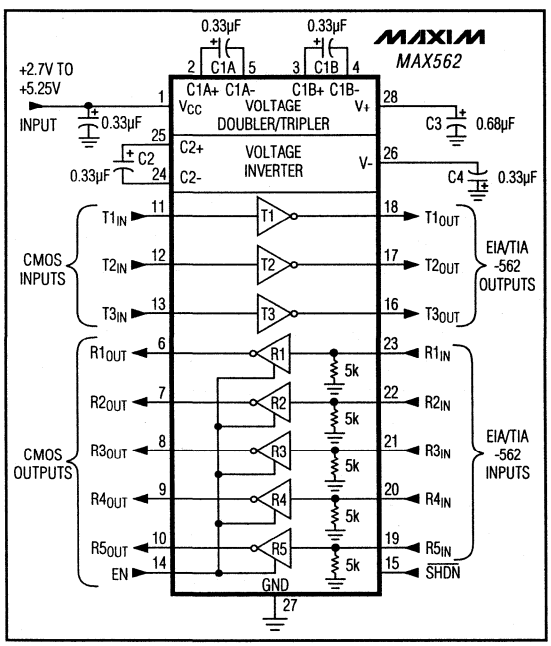
Applications

Palmtop, Notebook, and Subnotebook Computers

Peripherals

Battery-Powered Equipment

Typical Operating Circuit



™ LapLink is a registered trademark of Traveling Software, Inc.

Features

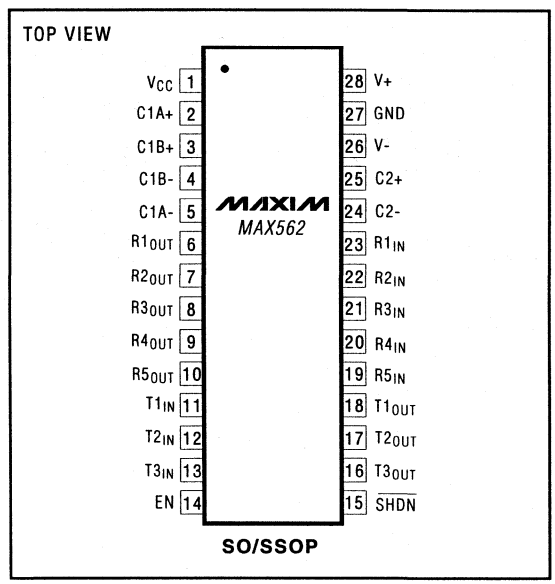
- ♦ **230kbps Data Rate, LapLink™ Compatible**
- ♦ **Operates from a 2.7V to 5.25V Supply**
- ♦ **Designed for EIA/TIA-562 and EIA/TIA-232 Applications**
- ♦ **Guaranteed 4.0V/µs Slew Rate**
- ♦ **3 Drivers, 5 Receivers**
- ♦ **Flow Through Pinout**
- ♦ **Low-Power Shutdown and Keep-Awake Modes**
- ♦ **Low-Cost, Surface-Mount External Capacitors**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX562CWI	0°C to +70°C	28 SO
MAX562CAI	0°C to +70°C	28 SSOP
MAX562C/D	0°C to +70°C	Dice*
MAX562EWI	-40°C to +85°C	28 SO
MAX562EAI	-40°C to +85°C	28 SSOP

** Contact factory for dice specifications.*

Pin Configuration



Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +6V
V- ..... +0.3V to -6V
C1A+, C1B+ ..... -6V to (V+ + 0.3V)
C1A-, C1B-, C2+ ..... -0.3V to (V+ + 0.3V)
C2- ..... (V- - 0.3V) to +6V
Input Voltages
  T_{IN}, EN, $\overline{SHDN}$ ..... -0.3V to (V_{CC} + 0.3V)
  R_{IN} ..... ±25V
Output Voltages
  T_{OUT} ..... ±15V
  R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
  T_{OUT} to GND ..... Continuous
  R_{OUT} to GND, V_{CC} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  SO (derate 12.50mW/°C above +70°C) 1000mW
  SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
  MAX562C_ _ ..... 0°C to +70°C
  MAX562E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.25V, C1A = C1B = C2 = C4 = 0.33µF, C3 = 0.68µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
EIA/TIA-562 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±3.7	±4.5	±6.0	V
Input Logic Threshold Low	T_{IN}, EN, $\overline{SHDN}$	V_{CC} = 2.7V to 3.6V			0.6	V
		V_{CC} = 5.0V +5%, -10%			0.8	
Input Logic Threshold High	T_{IN}, EN, $\overline{SHDN}$	V_{CC} = 2.7V to 3.6V	1.8			V
		V_{CC} = 5.0V +5%, -10%	3.0			
Output Leakage Current					±10	µA
Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Output Short-Circuit Current	V_{OUT} = 0V				±60	mA
EIA/TIA-562 RECEIVERS						
Input Voltage Operating Range					±25	V
Input Threshold Low			0.8			V
Input Threshold High					2.4	V
Input Hysteresis	No hysteresis when $\overline{SHDN}$ = 0V			0.3		V
Input Resistance	-15V < V_{IN} < 15V		3	5	7	kΩ
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} -0.5			V
Output Leakage Current	EN = GND, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
POWER SUPPLY						
Operating Supply Voltage			2.7		5.25	V
V_{CC} Power-Supply Current	V_{CC} = 3.3V	No load		20	33	mA
		All outputs loaded 3kΩ		24		
Shutdown Supply Current with Receivers Active	EN = V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C			45	130	µA
Shutdown Supply Current	$\overline{SHDN}$ = EN = GND, T_A = +25°C			1	50	µA

AC CHARACTERISTICS

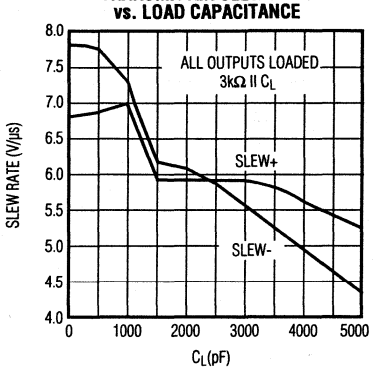
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Data Rate	1000pF ‖ 3kΩ load each transmitter output, 150pF load each receiver output		230.4	280.0		kbits/sec
Transmitter Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ. Measured from +3V to -3V, or -3V to +3V		4	6	30	V/µs
Transmitter Rise/Fall Time	R_L = 3kΩ measured from +3.3V to -3.3V or -3.3V to +3.3V	C_L = 2500pF	0.22		3.1	µs
		C_L = 1000pF	0.22		2.1	
Transmitter Propagation Delay	2500pF ‖ 3kΩ load, Figure 1	t_{PHLT}		900	1700	ns
		t_{PLHT}		1000	1700	
Transmitter-Output Enable Time		t_{ET}		100		µs
Transmitter-Output Disable Time	Figure 3	t_{DT}		600		ns
Receiver Propagation Delay, Normal Operation	C_L = 150pF, $\overline{SHDN}$ = V_{CC} Figure 2	t_{PHLR}		100	250	ns
		t_{PLHR}		250	500	
Receiver Propagation Delay, Keep-Awake Mode	C_L = 150pF, $\overline{SHDN}$ = GND Figure 2	t_{PHLS}		3000	4000	ns
		t_{PLHS}		2000	3000	
Receiver-Output Enable Time	Figure 4	t_{ER}		100	250	ns
Receiver-Output Disable Time	Figure 4	t_{DR}		250	500	ns

Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

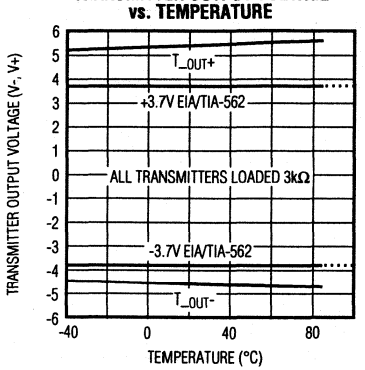
Typical Operating Characteristics

(V_{CC} = 3.3V, C1A = C1B = C2 = C4 = 0.33µF, C3 = 0.68µF, T_A=+25°C, unless otherwise noted.)

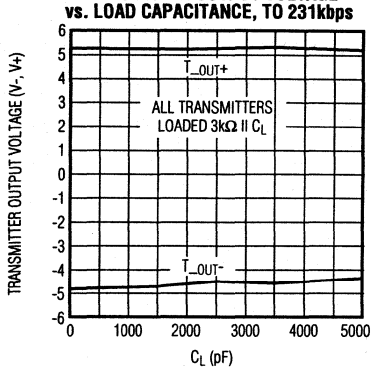
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



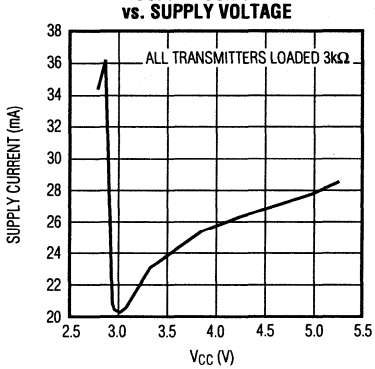
TRANSMITTER OUTPUT VOLTAGE vs. TEMPERATURE



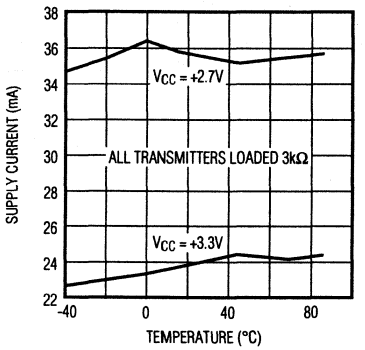
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE, TO 231kbps



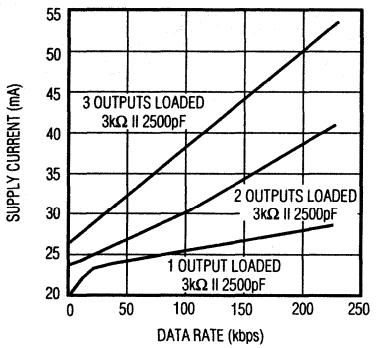
SUPPLY CURRENT vs. SUPPLY VOLTAGE



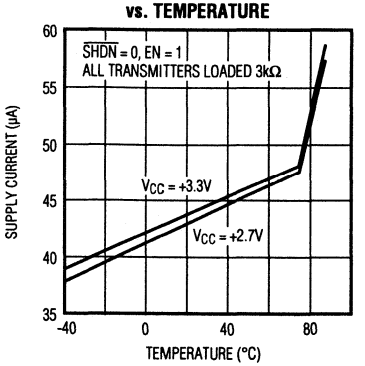
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. TRANSMITTER DATA RATE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
28	V+	Positive charge-pump output, typically 5.8V
2, 5	C1A+, C1A-	Terminals for positive charge-pump capacitor
3, 4	C1B+, C1B-	Terminals for positive charge-pump capacitor
6, 7, 8, 9, 10	$R_{\_OUT}$	TTL/CMOS Receiver Outputs.
11, 12, 13	$T_{\_IN}$	TTL/CMOS Driver Inputs
14	EN	Receiver Enable, see *Shutdown and Enable Control* section.
15	$\overline{SHDN}$	Shutdown Control, see *Shutdown and Enable Control* section.
16, 17, 18	$T_{\_OUT}$	EIA/TIA-562 Driver Outputs
19, 20, 21, 22, 23	$R_{\_IN}$	EIA/TIA-562 Receiver Inputs
24, 25	C2+, C2-	Terminals for negative charge-pump capacitor
26	V-	Negative charge-pump output, typically -5.2V
27	GND	Ground
1	V_{CC}	+2.7V to +5.25V Supply Voltage

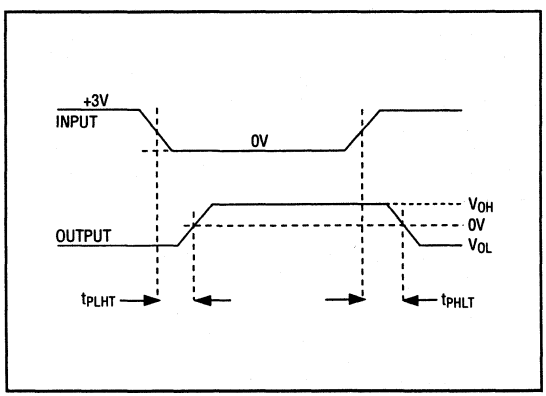


Figure 1. Transmitter Propagation Delay Timing

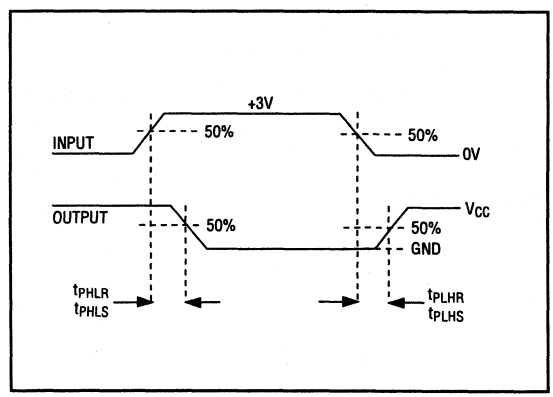


Figure 2. Receiver Propagation Delay Timing

Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

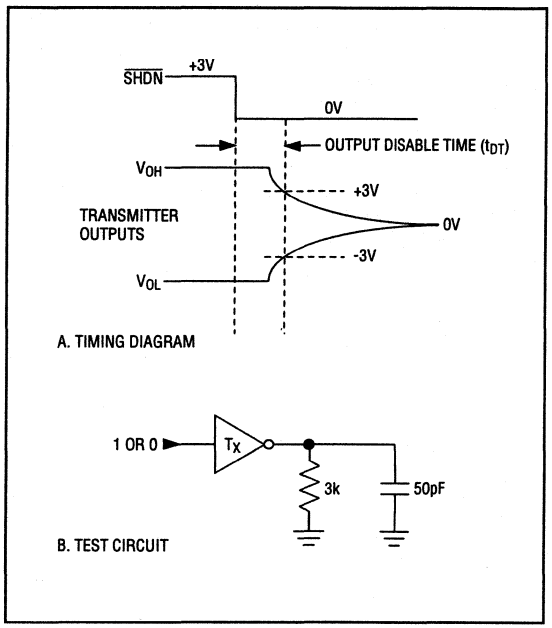


Figure 3. Transmitter-Output Disable Timing

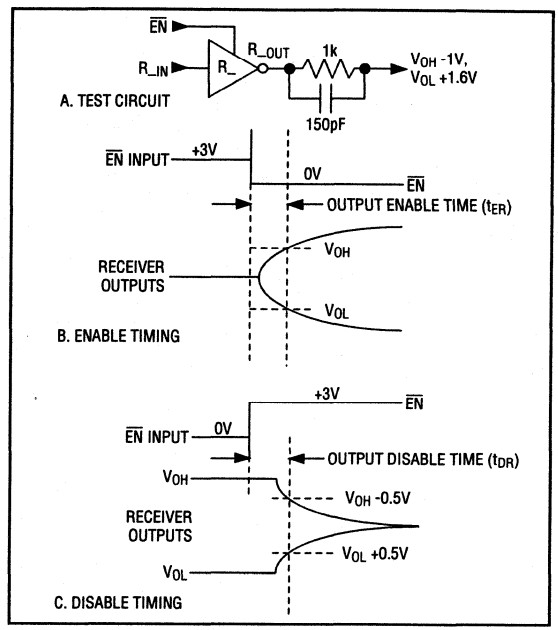


Figure 4. Receiver-Output Enable and Disable Timing

Detailed Description

The MAX562 has three sections: the charge-pump voltage converter, the drivers (transmitters), and the receivers.

Charge-Pump Voltage Converter

The charge-pump voltage converter is used to produce a positive and a negative supply to drive the transmitters. The positive voltage (V+) is generated by a regulated charge pump working as either a doubler or a tripler (depending on the V_{CC} level) and using capacitors C1A, C1B and C3 (see *Typical Operating Circuit*). The negative voltage (V-) derives from V+ using a simple charge-pump inverter that employs capacitors C2 and C4.

These charge-pump converters are regulated to give output voltages of +5.8V and -5.2V. Having regulated supplies generated on-chip makes the MAX562's performance insensitive to variations in V_{CC} from 2.7V to 5.25V, transmitter loading changes, and operating temperature changes.

When $\overline{SHDN}$ is low, the charge pumps are disabled, V+ is internally connected to V_{CC}, and V- is internally connected to GND.

EIA/TIA-562 Drivers

The driver output voltage is guaranteed to meet the ±3.7V EIA/TIA-562 specification over the full range of operating temperatures and voltages, when each transmitter is loaded with up to 3kΩ and operated up to 230kbps (see *Typical Operating Characteristics*). The typical driver output voltage swing exceeds ±4V with a 3kΩ load on all transmitter outputs. The open-circuit output voltage swing is typically from (V+ - 0.7V) to (V- + 0.7V). Output swing is not significantly dependent on V_{CC} since the charge pumps are regulated.

Input thresholds are CMOS and TTL compatible. Connect unused inputs to V_{CC} or to GND.

When $\overline{SHDN}$ is low, the driver outputs are off and their leakage currents are less than 10µA, even if the transmitter outputs are back-driven between -7V and +15V. Taking $\overline{SHDN}$ low does not disable the receivers.

When $\overline{SHDN}$ and EN are both low, the entire chip is disabled and all outputs are high impedance. Power consumption is lowest in this condition. Exiting shutdown takes about 100µs, but depends on V_{CC}. Figure 5 shows

Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

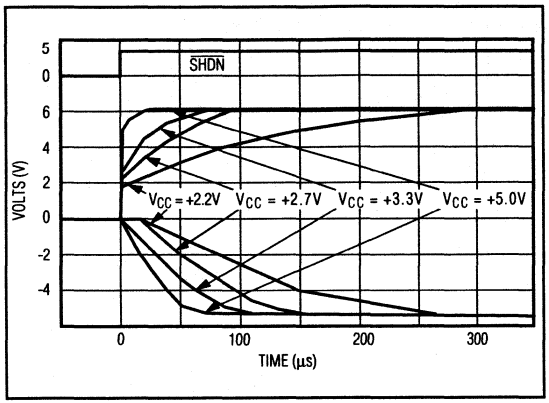


Figure 5. Time for Transmitters to Exit Shutdown

the MAX562 transmitter outputs when $\overline{SHDN}$ rises. Two transmitter outputs are shown going to opposite EIA/TIA-562 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs are well behaved, with no ringing or undesirable transients as they come out of shutdown.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

EIA/TIA-562 Receivers

All 5 receivers are identical and accept EIA/TIA-562 or EIA/TIA-232 signals. The CMOS receiver outputs swing between V_{CC} and GND. They are inverting, maintaining compatibility with the driver outputs.

The guaranteed 0.8V and 2.4V receiver input thresholds are significantly tighter than the ±3.0V thresholds required by the EIA/TIA-562 specification. This allows the receiver inputs to respond to TTL/CMOS logic levels as well as EIA/TIA-562/232 levels. Also, the MAX562's guaranteed 0.8V lower threshold ensures that receivers shorted to ground will have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

The receiver inputs have approximately 0.3V hysteresis when $\overline{SHDN}$ is high. This provides clean output transitions, even with slowly moving input signals with moderate noise and ringing.

The receivers are active when EN is high. When EN is low, the receiver outputs are high impedance. This allows wire-OR connection of two EIA/TIA-562 ports (or ports of different types) at the UART.

The receivers are always active,when EN is high, irrespective of $\overline{SHDN}$'s state. When $\overline{SHDN}$ is high, the receivers have hysteresis and experience the shortest propagation delays (typically 100ns falling, 250ns rising). When $\overline{SHDN}$ is low, the receivers have longer propagation delays (typically 3µs falling, 2µs rising) and have no hysteresis. The receiver outputs are not valid for 50µs after $\overline{SHDN}$ goes low.

Shutdown and Enable Control

$\overline{SHDN}$ and EN determine the operation of the MAX562 as shown in Table 1.

Applications Information

Capacitor Selection

The capacitor type is not critical for proper MAX562 operation. Any low cost ceramic capacitor (e.g., Z5U, Y5V) is acceptable for operating at room temperature,

Table 1. MAX562 Control Pin Configurations

$\overline{SHDN}$	EN	CHARGE-PUMP OPERATION STATUS	TRANSMITTERS T1-T3	RECEIVERS R1-R5	SUPPLY CURRENT TYP (A)
0	0	Shutdown	High-Z	High-Z	1µ
0	1	Shutdown	High-Z	Active*	45µ
1	0	Normal Operation	Active	High-Z	24m
1	1	Normal Operation	Active	Active	24m

* Active, but with reduced performance (see *EIA/TIA-562 Receivers* section). This is "keep-awake" mode.

Complete 230kbps, 2.7V to 5.25V Serial Interface for Notebook Computers

Table 2. Summary of EIA/TIA-232E/V.28 and EIA/TIA-562 Specifications

PARAMETER	CONDITION	EIA/TIA-232E/V.28 SPECIFICATION	EIA/TIA-562 SPECIFICATION
Driver Output Voltage 0 Level	3kΩ to 7kΩ load	5.0V to 15.0V	3.7V to 13.2V
1 Level		-5.0V to -15.0V	-3.7V to -13.2V
Maximum Output Level	No load	±25V	±13.2V
Signal Rate ($3k\Omega \le R_L \le 7k\Omega$)	C_L = 2500pF	Up to 20kbps	Up to 20kbps
	C_L = 1000pF	Not defined	Up to 64kbps

and X7R ceramic capacitors are recommended for operation over the full temperature range.

Larger capacitors may be used for C2 and C4 (see *Typical Operating Circuit*) to reduce ripple on the transmitter output voltages.

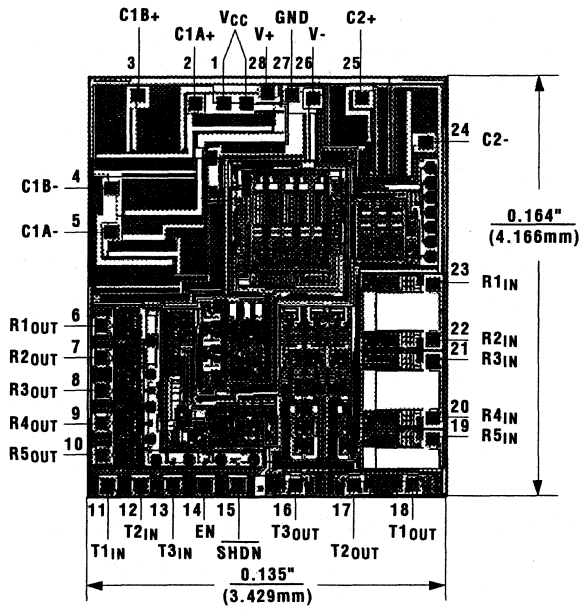
Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor similar in value to that of the C1A and C1B charge-pump capacitors. Connect the bypass capacitor as close as possible to the V_{CC} and GND pins.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-. Excessive loads will cause V+ and V- to fall out of regulation. When V+ or V- are loaded, check for good regulation over the intended operating temperature range.

Chip Topography



Substrate connected to V+

Transistor count: 1892

19-0198; Rev 0; 10/93

MAXIM

+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

General Description

The MAX563 is a +3.3V-powered EIA/TIA-562 transceiver with two transmitters and two receivers. Because it implements the EIA/TIA-562 standard, the MAX563 communicates with RS-232 transceivers, yet consumes far less power; this makes it ideal for battery-powered, hand-held computers. And, the MAX563 guarantees a 116kbps data rate while maintaining ±3.7V EIA/TIA-562 signal levels, which makes it compatible with LapLink™ software.

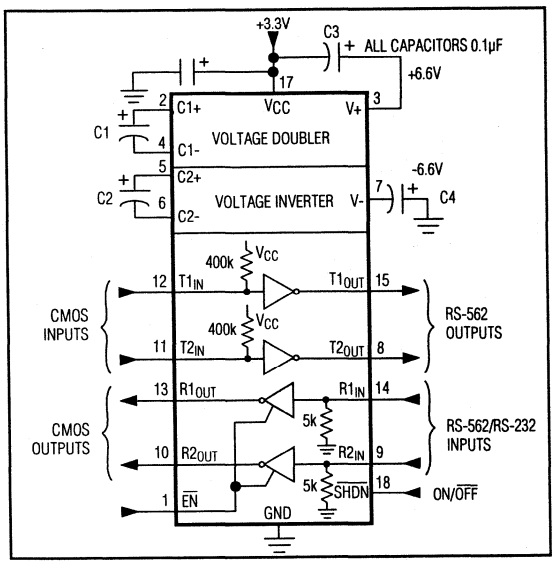
An on-board charge pump converts the +3.3V supply to the ±6.6V needed to produce the EIA/TIA-562 output voltage levels. Four 0.1µF charge-pump capacitors and a bypass capacitor of similar size are the only external components required.

When the MAX563's charge pumps and transmitters are shut down to save power, the receivers remain active to continuously monitor signals from external devices (for example, ring indicator from modems). The two receivers' outputs can be enabled and disabled independently of the shutdown function to allow two ports—generally of different types—to be wire-OR connected at the UART.

Applications

Handiterminals
Battery-Powered Equipment
Bar-Code Readers
Notebook and Palmtop Computers

Typical Operating Circuit



™ LapLink is a registered trademark of Traveling Software, Inc.

Features

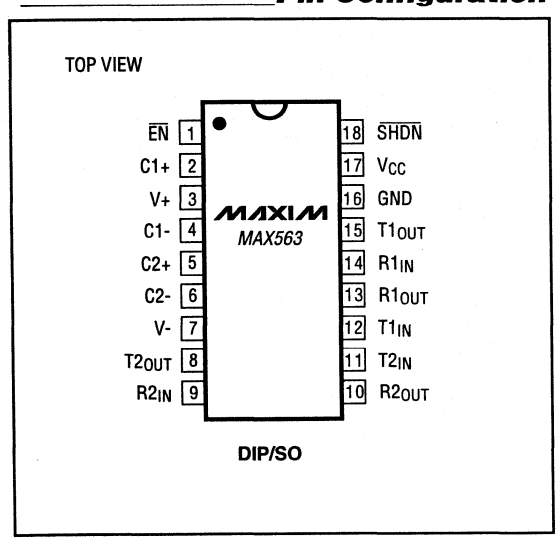
- ♦ **Guaranteed Interoperability with RS-232**
- ♦ **Operates from a Single +3.0V to +3.6V Supply**
- ♦ **2 Drivers, 2 Receivers**
- ♦ **Receivers Active in Shutdown Mode**
- ♦ **Low-Power Shutdown: 10µA Max**
- ♦ **Small Package—18-Pin Wide SO**
- ♦ **Three-State TTL/CMOS Receiver Outputs**
- ♦ **116kbps Guaranteed Data Rate**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX563CPN	0°C to +70°C	18 Plastic DIP
MAX563CWN	0°C to +70°C	18 Wide SO
MAX563C/D	0°C to +70°C	Dice *

* *Dice are specified at T_A = +25°C.*

Pin Configuration



+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

ABSOLUTE MAXIMUM RATINGS

Power Supply Ranges
- Supply Voltage (V_{CC}) ..... -0.3V to +6V
- Input Voltages
  - T_{IN} ..... -0.3V to (V_{CC} -0.3V)
  - R_{IN} ..... ±25V
- T_{OUT} (Note 1) ..... ±15V
- Output Voltages
  - T_{OUT} ..... ±15V
  - R_{OUT} ..... -0.3V to (V_{CC} +0.3V)
- Driver/Receiver Output Short Circuit to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP 889mW
- Wide SO 762mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Input voltage measured with T_{OUT} in high-impedance state. $\overline{SHDN}$ or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 3.6V, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RS-562 TRANSMITTERS						
Output Voltage Swing		All transmitter outputs loaded with 3kΩ to GND	±3.7	±4.5		V
Data Rate		R_L = 3kΩ, C_L = 1000pF, T_A = +25°C		200	116	kbps
Input Logic Threshold Low	V_{IL}				0.6	V
Input Logic Threshold High	V_{IH}		2.4			V
Logic Pull-Up/Input Current		$\overline{SHDN}$ = V_{CC}		2	20	µA
		$\overline{SHDN}$ = 0V		±0.01	±1	
Output Leakage Current		V_{CC} = 3.6V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V		±0.01	±10	µA
		V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V		±0.01	±10	
Transmitter Output Resistance		V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	10M		Ω
Output Short-Circuit Current		V_{OUT} = 0V		±15	±60	mA
RS-232/RS-562 RECEIVERS						
Input Voltage Operating Range					±25	V
Input Threshold Low	V_{IL}	V_{CC} = 3.3V			0.4	V
Input Threshold High	V_{IH}	V_{CC} = 3.3V	2.4			V
Input Hysteresis		$\overline{SHDN}$ = V_{CC} = 3.3V (no hysteresis when $\overline{SHDN}$ = 0V)	0.1	0.5	1.0	V
Input Resistance	R_{IN}		3	5	7	kΩ
Output Voltage Low	V_{OL}	I_{OUT} = 3.2mA		0.2	0.4	V
Output Voltage High	V_{OH}	I_{OUT} = -0.5mA	V_{CC}-0.6	V_{CC}-0.2		V
Output Leakage Current		$\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}		±0.05	±10	µA
$\overline{EN}$ Input Threshold Low	V_{IL}				0.6	V
$\overline{EN}$ Input Threshold High	V_{IH}		2.4			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.0V to 3.6V, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Operating Supply Voltage	V_{CC}			3.0		3.6	V
V_{CC} Supply Current	I_{CC}	No load			3	8	mA
		R_L = 3kΩ on both outputs, inputs static			8		
Shutdown Supply Current	I_{CC}	Figure 1	T_A = +25°C		0.1	10	µA
			T_A = T_{MIN} to T_{MAX}		2	50	
$\overline{SHDN}$ Input Leakage Current					0.1	±1	µA
$\overline{SHDN}$ Threshold Low	V_{IL}					0.6	V
$\overline{SHDN}$ Threshold High	V_{IH}			2.4			V
AC CHARACTERISTICS							
Transition Slew Rate		C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 3.3V, T_A = +25°C, measured from +3V to -3V or -3V to +3V (Note 2)		4	6	30	V/µs
Transmitter Propagation Delay	t_{PHLT}	Figure 2			1.3	3.5	µs
	t_{PLHT}				1.5	3.5	
Receiver Propagation Delay (Normal Operation)	t_{PHLR}	Figure 3			0.5	1.0	µs
	t_{PLHR}				0.6	1.0	
Receiver Propagation Delay (Shutdown)	t_{PHLS}	Figure 3			0.5	10.0	µs
	t_{PLHS}				2.5	10.0	
Receiver-Output Enable Time	t_{ER}	Figure 4			125	500	ns
Receiver-Output Disable Time	t_{DR}	Figure 4			160	500	ns
Transmitter-Output Enable Time	t_{ET}	Includes charge pump start-up			300		µs
Transmitter-Output Disable Time	t_{DT}	Figure 5			600		ns
Transmitter Propagation Delay Skew	t_{PHLT} - t_{PLHT}				300		ns
Receiver Propagation Delay Skew (Normal Operation)	t_{PHLR} - t_{PLHR}				100		ns

Note 2: Minimum slew rate is specified with C_L = 1000pF for data rates above 20kbps, corresponding with EIA/TIA-562.

+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

Pin Description

PIN	NAME	FUNCTION
1	$\overline{EN}$	Receiver enable. Connect $\overline{EN}$ to GND to enable receivers, and take $\overline{EN}$ high to disable receivers.
2	C1+	Positive terminal of positive charge-pump capacitor.
3	V+	$+2V_{CC}$ voltage generated by the positive charge pump. The voltage on V+ collapses to V_{CC} when $\overline{SHDN}$ is low.
4	C1-	Negative terminal of positive charge-pump capacitor.
5	C2+	Positive terminal of inverting charge-pump capacitor.
6	C2-	Negative terminal of inverting charge-pump capacitor.
7	V-	$-2V_{CC}$ voltage generated by the inverting charge pump. The voltage on V- collapses to GND when $\overline{SHDN}$ is low.
8, 15	$T2_{OUT}$, $T1_{OUT}$	EIA/TIA-562 voltage-level transmitter outputs. These outputs are disabled (Hi-Z) when $\overline{SHDN}$ is low.
9, 14	$R2_{IN}$, $R1_{IN}$	EIA/TIA-562 and EIA/TIA-232 voltage-level receiver inputs.
10, 13	$R2_{OUT}$, $R1_{OUT}$	CMOS receiver outputs. These outputs are active regardless of the state of $\overline{SHDN}$. They are enabled when $\overline{EN}$ is low, and disabled (Hi-Z) when $\overline{EN}$ is high.
11, 12	$T2_{IN}$, $T1_{IN}$	CMOS driver inputs.
16	GND	Ground.
17	V_{CC}	+3.0V to +3.6V supply voltage.
18	$\overline{SHDN}$	Shutdown control. Connect to GND to shut down the charge pumps and the transmitters. Take high to turn on the charge pumps and to enable the transmitters.

Detailed Description

The MAX563 consists of three sections: charge-pump voltage converters, transmitters (drivers), and receivers. Both the transmitters and the receivers are inverting.

+3V to ±6V, Dual Charge-Pump Voltage Converter

Two charge pumps either invert or double the incoming V_{CC} to generate the voltages required by the transmitters. The first charge pump uses capacitor C1 to double V_{CC}; the resulting voltage is stored on the V+ reservoir capacitor. The second charge pump uses capacitor C2 to invert V+; this negative voltage is stored on the V- capacitor.

When $\overline{SHDN}$ is low, the charge pumps are turned off, V+ is pulled down to V_{CC} by a 1kΩ resistor, and V- rises to GND.

It is possible to draw some power from the V+ and V- pins for external use. However, doing so diminishes the charge-pump output voltages and reduces noise margins, so it is not recommended.

EIA/TIA-562 Transmitters

The MAX563's drivers are inverting level translators that convert +3V logic inputs to EIA/TIA-562 voltage levels. With a VCC supply of only 3.0V, the driver outputs deliver the EIA/TIA-562 ±3.7V minimum specification under worst-case conditions—when both transmitters are loaded with 3kΩ receivers (either EIA/TIA-232 or EIA/TIA-562).

The transmitters are fast: the guaranteed data rate with standard loads is 116kbps, which is the highest rate commonly used by PC-to-PC communication software, such as LapLink. The highest practical data rate may be reduced if the other communicating device (RS-562 or RS-232) is not as fast, or if the cables present an excessive capacitive load (>1000pF). Each transmitter is designed to drive a single receiver; transmitters can be paralleled to drive multiple receivers.

When $\overline{SHDN}$ is low, the driver outputs are turned off. Their output leakage currents are less than 10µA when pulled to GND or when driven to ±15V. This enables two transmitters to be connected to the same line, provided that one of them is always disabled by taking $\overline{SHDN}$ low.

+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

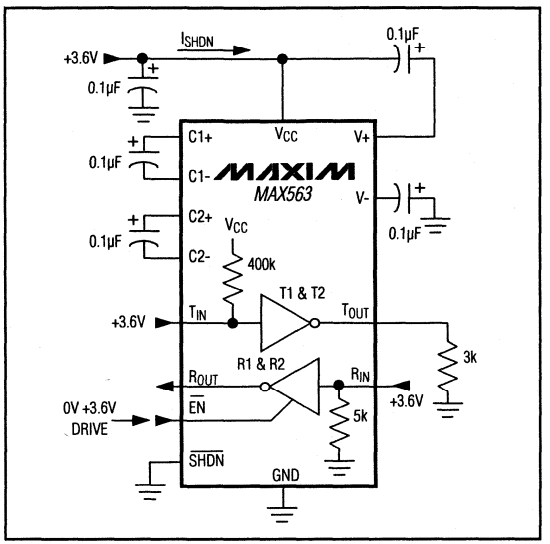


Figure 1. Shutdown Current Test Circuit

The inputs of unused drivers may be left unconnected because they have internal 400kΩ pull-ups to V_{CC}. Unused inputs may also be connected to GND or V_{CC}, but V_{CC} provides lower power consumption because of the internal pull-ups.

EIA/TIA-562 and EIA/TIA-232 Receivers

The MAX563's receivers convert ±3.7V to ±13.2V EIA/TIA-562 signal levels into +3V logic levels; they are rated to receive signals up to ±25V to accommodate EIA/TIA-232 signals as well. Both receivers invert. Their inputs are each equipped with an internal 5kΩ (nominal) terminating resistor connected to ground, and the input logic thresholds are 0.4V and 2.4V. The positive logic-low threshold (V_{IL}) ensures the receiver outputs remain high whenever their inputs are left open.

The receivers are active when $\overline{EN}$ is low, and have high-impedance outputs when $\overline{EN}$ is high.

When $\overline{SHDN}$ is high, the receivers have hysteresis. This produces clean output transitions, even with slow-moving input signals that exhibit moderate amounts of noise and ringing. When shut down, the receivers have no hysteresis, and the propagation delay increases.

Shutdown and Enable Control

The $\overline{SHDN}$ and $\overline{EN}$ controls are independent. Both receivers are always active when $\overline{EN}$ is low. With $\overline{EN}$ low and $\overline{SHDN}$ high, the receivers operate at full speed and have hysteresis. When active in shutdown mode ($\overline{EN}$ = $\overline{SHDN}$ = low), the receivers operate at reduced power and speed, and without hysteresis.

The charge pumps and transmitters operate only when $\overline{SHDN}$ is high; they are unaffected by $\overline{EN}$. When shut down ($\overline{SHDN}$ = low) or unpowered (V_{CC} = 0V), the transmitter outputs are high impedance if they are backdriven with voltages not exceeding ±15V. The pull-up resistors at the driver inputs are disconnected in shutdown mode to save power. During shutdown, V+ is pulled down to V_{CC}, and V- rises to GND.

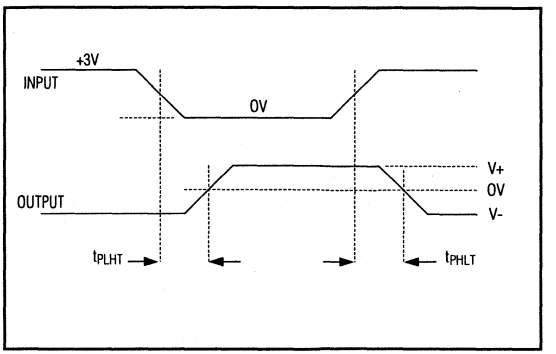


Figure 2. Transmitter Propagation Delay Timing

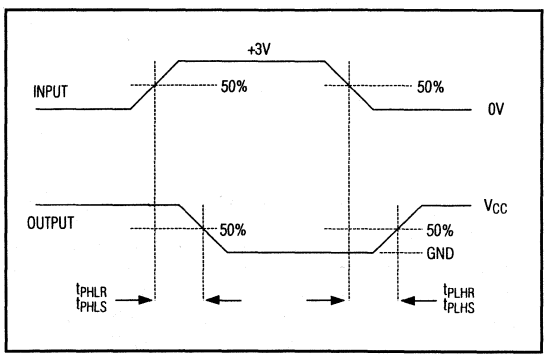


Figure 3. Receiver Propagation Delay Timing

+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

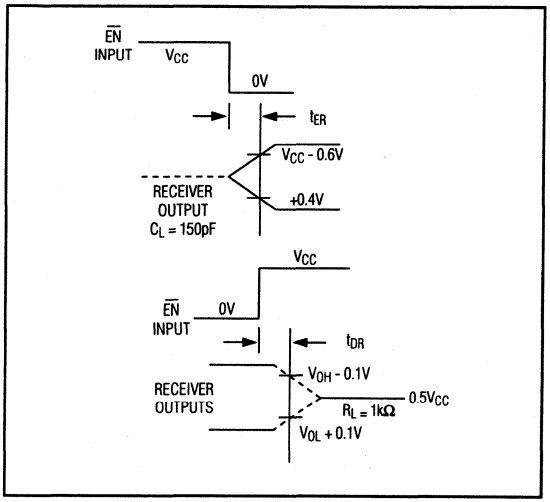


Figure 4. Receiver Output Enable and Disable Timing

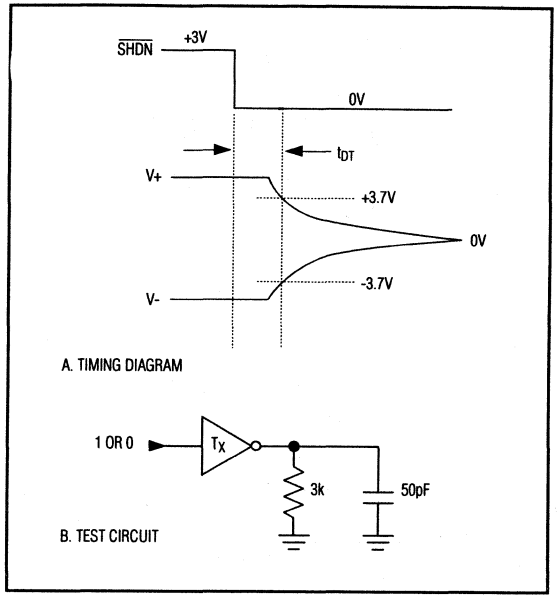


Figure 5. Transmitter Output Disable Timing

Applications Information

Charge-Pump Capacitor Selection

Normally, 0.1µF capacitors can be used for all locations. To reduce output ripple, increase the values of the V+ and V- capacitors. If your capacitors have a very wide tolerance, consider using a nominal value a little larger than 0.1µF to ensure that the actual capacitance does not fall below about 80nF. For circuits designed to operate over a wide range of temperatures, consider using slightly larger capacitors to compensate for any loss of capacitance at temperature extremes. No advantage is gained by using values larger than 10µF.

Power-Supply Decoupling

Use a capacitor with the same value as the charge-pump capacitors.

+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

Table 1. Summary of EIA/TIA-232E/V.28 and EIA/TIA-562 Specifications

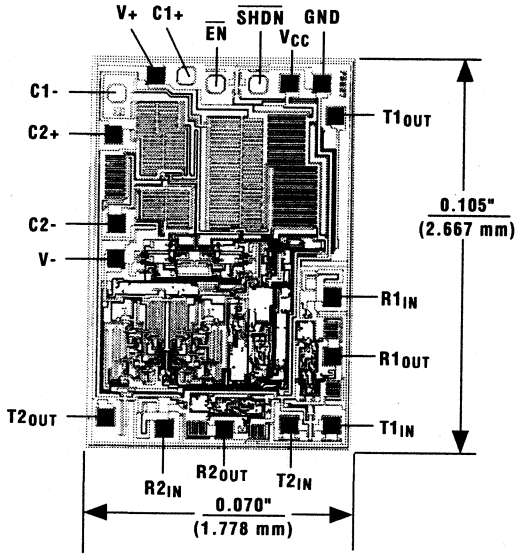
PARAMETER	CONDITION	EIA/TIA-232E/V.28 SPECIFICATION	EIA/TIA-562 SPECIFICATION
Driver Output Voltage 0 Level	3kΩ to 7kΩ load	5.0V to 15.0V	3.7V to 13.2V
1 Level		-5.0V to -15.0V	-3.7V to -13.2V
Maximum Output Level	No load	±25V	±13.2V
Signal Rate (3kΩ ≤ R_L ≤ 7kΩ)	C_L = 2500pF	Up to 20kbps	Up to 20kbps
	C_L = 1000pF	Not defined	Up to 64kbps
Receiver Input Thresholds 0 Level		3.0V to 15.0V	3.0V to 15.0V
1 Level		-3.0V to -15.0V	-3.0V to -15.0V
Maximum Input Level		±25V	±25V
Maximum Instantaneous Slew Rate		30V/µs	30V/µs
Maximum Driver Output Short-Circuit Current		100mA	60mA
Transition Rate on Driver Output		V.28 1ms or 3% of the period	4V/µs
		RS-232 4% of the period	
Driver Output Resistance with Power Off	-2V < V_{OUT} < 2V	300Ω	300Ω

Table 2. DB9/DB25 Cable Connections Commonly Used for EIA/TIA-232E, EIA/TIA-562 and V.24 Asynchronous Interfaces

DB9 PIN	DB25 PIN	NAME	SYMBOL	FUNCTION
1	8	Received Line Signal Detector (sometimes called Data Carrier Detect)	DCD	Handshake from DCE
2	3	Receiver Data	RxD	Data from DCE
3	2	Transmit Data	TxD	Data from DTE
4	20	Data Terminal Ready	DTR	Handshake from DTE
5	7	Signal Ground	GND	Reference point for signals
6	6	Data Set Ready	DSR	Handshake from DCE
7	4	Request to Send	RTS	Handshake from DTE
8	5	Clear to Send	CTS	Handshake from DCE
9	22	Ring Indicator	RI	Handshake from DCE

+3.3V-Powered, EIA/TIA-562 Dual Transceiver with Receivers Active in Shutdown

Chip Topography



TRANSISTOR COUNT: 189;
SUBSTRATE CONNECTED TO V+.

Op Amps/Comparators

3

*Advance Information–first page of data sheet in preparation.

OP AMPS

PRECISION

LOW V_{OS}

BIPOLAR

- **MAX400**
- **MAX427**
- **MAX437**
- † **MAX471** (current-sense amp)
- † **MAX472** (current-sense amp)
- **MAX478** (dual, 17µA)
- **MAX479** (dual, 17µA)
- **MAX480**
- **MXL1001**
- **MXL1007**
- **MXL1013**
- **MXL1014**
- **MXL1178**
- **MXL1179**
- **OP07**
- **OP27**
- **OP37**
- **OP90**

CHOPPERS

- **MAX420**
- **MAX421**
- **MAX422**
- **MAX423**
- **MAX430** (internal caps)
- **MAX432** (internal caps)
- **ICL7650**
- **ICL7652**

PROG GAIN

- **PGA100A**

LOW I_B

- **MAX406** (<1pA)
- **MAX407** (<1pA, dual)
- **MAX409** (<1pA, 150kHz GBW)
- **MAX417** (<1pA, dual, 150kHz GBW)
- **MAX418** (<1pA, quad)
- **MAX419** (<1pA, quad, 150kHz GBW)
- **MAX420**
- **MAX421**
- **MAX422**
- **MAX423**
- **MAX430**
- **MAX432**
- **ICL761x**
- **ICL762x**
- **ICL763x**
- **ICL764x**
- **ICL765x**

LOW NOISE

- **MAX400**
- **MAX410** (<2.4nV/√Hz)
- **MAX412** (dual MAX410)
- **MAX414** (quad MAX410)
- **MAX427**
- **MAX437**
- **OP07**
- **OP27**
- **OP37**
- **MXL1001**
- **MXL1007**

LOW POWER

SINGLE SUPPLY

- **MAX406** (1.2µA, rail-to-rail output)
- **MAX407** (dual MAX406)
- **MAX409** (1.2µA, 150kHz GBW, rail-to-rail output)
- **MAX417** (dual MAX409)
- **MAX418** (quad MAX406)
- **MAX419** (quad MAX409)
- **MAX478** (dual, 17µA)
- **MAX479** (quad, 17µA)
- **MAX480**
- **ICL761x**
- **ICL762x**
- **ICL763x**
- **ICL764x**
- **MXL1013**
- **MXL1014**
- **MXL1178**
- **MXL1179**

SINGLE SUPPLY & HIGH SPEED

- ★ **MAX473** (10MHz)
- ★ **MAX474** (dual MAX473)
- ★ **MAX475** (quad MAX473)
- ★ **MAX492** (dual MAX495)
- ★ **MAX494** (quad MAX495)
- ★ **MAX495** (500kHz, rail-to-rail input/output)

HIGH SPEED

- **MAX402** (2MHz, 75µA)
- **MAX403** (10MHz, 375µA)
- **MAX410** (28MHz, 2.5mA)
- **MAX412** (dual, 28MHz, 2.5mA)
- **MAX414** (quad, 28MHz, 2.5mA)
- **MAX438** (6MHz, 75µA)
- **MAX439** (25MHz, 375µA)
- † **MAX476** (300MHz, 8mA)
- † **MAX477** (500MHz, 8mA)

★ **New product**
† **Future product**

Part Number	V_{OS} (mV max)	TCV_{OS} (µV/°C max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current per Op Amp (mA max)	Features	Price† 1000-up ($)
MAX400	10 to 15µV	0.3	2	0.4	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX402	2	25 typ	5	2	±3 to ±5	75µA	High speed, micropower	1.98
MAX403	2	25 typ	25	10	±3 to ±5	375µA	High speed, micropower	2.75
MAX406/407/418	0.5 to 4.0	10	10pA	8 to 40kHz	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, single supply, rail-to-rail outputs, unity-gain stable	1.95/2.98/3.98
MAX408/428/448	6 to 12	15 to 20	1.1µA	100 (A_V≥3)	±5	10	Single/dual/quad, high speed, high output current	3.02/4.06/6.74
MAX409/417/419	0.5 to 4.0	10	10pA	150kHz (A_V≥10V/V)	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, decompensated (A_V≥10V/V)	1.95/2.98/3.98
MAX410/412/414	250µV (320µV MAX414)	1.0 typ	150	28	±2.4 to ±5.25	2.7	Single/dual/quad, high speed, low noise, < 2.4nV/√Hz at 1kHz guaranteed, unity-gain stable	1.50/2.45/4.50
MAX420/422	5 to 10µV	0.05	0.03 to 0.10	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 to 10µV	0.05	0.03 to 0.10	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/5.57
MAX427/437	15µV	0.8	35	8/60	±15	4	High speed, low noise 3.8nV/√Hz precision	1.83
MAX430/432	5µV	0.05	0.1	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX438	2	25 typ	5	6 (A_V≥5V/V)	±3 to ±5	75µA	High speed, micropower; 10V/µs slew rate	1.98
MAX439	2	25 typ	25	25 (A_V≥5V/V)	±3 to ±5	375µA	High speed, micropower; 48V/µs slew rate	2.75
MAX471	60µV	–	–	–	+3 to +36	100µA (5µA SHDN)	Precision, high-side current-sense amplifier with internal sense resistor, measures charge and discharge	††
MAX472	60µV	–	–	–	+3 to +36 (5µA SHDN)	100µA	Precision, high-side current-sense amplifier	††
MAX473/474/475	1 to 1.5	2 typ	150	10	+2.7 to +6	3	Single/dual/quad, single or dual supply, wide output swing, 15V/µs min slew rate	1.45/2.25/3.60
MAX478/479	70 to 250µV	4.5	6	60kHz	+2.2 to +36 ±1.1 to ±18	17µA	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO, 3V, 5V, and ±15V specs	2.58/3.35
MAX480	70µV	1.5	3	20kHz	±0.8 to ±18 +1.6 to +36	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	3.68
MAX492/494/495	200µV	1 typ	60	500kHz	+2.7 to +6	190µA	Single/dual/quad, precision, rail-to-rail input and output	2.25/3.60/1.45
ICL7611	2 to 15	10 to 25 typ	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current	1.35
ICL7612	5 to 15	15 to 25 typ	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current, rail-to-rail input and output	1.29
ICL7614	2 to 15	15 to 25 typ	0.05	0.48*	±1.0 to ±8	0.25	External compensation	0.95
ICL7616	2 to 15	15 to 25 typ	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current, extended CMVR	1.62
ICL7621/7622	5 to 15	15 to 25 typ	0.05	0.48	±1.0 to ±8	0.25	Dual, low I_{BIAS} & I_{OS}	1.06/1.48
ICL7631/7632	5 to 20	15 to 30 typ	0.05	0.044 to 1.4	±1.0 to ±8	0.022 to 2.5	Triple op amp, programmable quiescent current ICL7632 is externally compensated	2.27/2.12

* External 39pF compensation capacitor added.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Op Amps (continued)

Part Number	V_{OS} (mV max)	TCV_{OS} (µV/°C max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current per Op Amp (mA max)	Features	Price† 1000-up ($)
ICL7641/7642	5 to 25	15 to 30 typ	0.05	0.044 to 1.4	±1.0 to ±8	0.015 to 2.5	Quad, low power, CMOS	1.41/1.56
ICL7650	5 to 10µV	0.05 to 0.10	0.01 to 0.02	2	±5	2	Industry standard, chopper stabilized	2.16
ICL7652	5 to 10µV	0.05	0.03	0.45	±5	2	Low noise, industry standard, chopper stabilized	3.24
LH0101	3 to 10	10 typ	300 to 1k	5	±5 to ±15	35	5A peak power	18.98
MXL1001	15 to 60µV	0.6 to 1.0	2 to 4	0.8	±3 to ±18	2	Precision LT1001 second source	1.73
MXL1007	25 to 60µV	0.6 to 1.0	35 to 55	8	±15	4 to 4.7	Low noise, precision LT1007 second source	1.85
MXL1013/1014	150 to 800µV	2.0 to 5	20 to 30	0.6	+4 to +36 ±2 to ±18	0.50 to 0.55	Dual/quad, precision LT1013/1014 second source	1.57/3.06
MXL1178/1179	70 to 600µV	3 to 4.5	5 to 6	60kHz	+2.2 to +36 ±1.1 to ±18	17 to 21µA	Dual/quad, precision, micropower LT1178/1179 second source	2.50/3.35
OP07	25 to 150µV	0.6 to 2.5	2 to 12	0.6	±3 to ±18	4	Industry standard, precision	1.58
OP27	25 to 100µV	0.6 to 1.8	40 to 80	8	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP37	25 to 100µV	0.6 to 1.8	40 to 80	63 ($A_V \geq 5$)	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP90	150 to 450µV	2 to 5	15 to 25	0.020	±0.8 to ±18 ±1.6 to ±36	15 to 20µA	Industry standard, micropower	1.60
PGA100A	1	6 typ	0.1 typ	5	±15	27 (I_{CC})	Digitally programmable gain amplifier with 8-channel mux, 5MHz GBW, ±0.05% gain accuracy	56.14

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

COMPARATORS

SPECIAL

MAX516
(quad, programmable input threshold voltage)

MAX910
(8ns, programmable input threshold voltage)

MAX911
(4ns, programmable input threshold voltage)

† **MAX951**
(op amp + comparator + reference)

† **MAX952**
(op amp + comparator + reference)

† **MAX953**
(op amp + comparator)

† **MAX954**
(op amp + comparator)

HIGH-SPEED COMPARATORS

TTL OUTPUT

≤10ns

MAX900
(quad, 8ns, single/dual supply)

MAX901
(quad, 8ns, single/dual supply)

MAX902
(dual, 8ns, single/dual supply)

MAX903
(8ns, single/dual supply)

MAX910
(8ns, programmable input threshold)

MAX912
(dual, 10ns, single/dual supply)

MAX913
(10ns, single/dual supply)

MAX915
(6ns, master/slave, clocked)

MAX916
(dual MAX915)

MAX9686
(6ns, industry standard)

MAX9698
(6ns, industry standard)

MXL1016

MXL1116

<50ns

MAX907
(dual, 40ns, single supply)

MAX908
(quad, 40ns, single supply)

MAX909
(40ns, single/dual supply)

<100ns

★ **MAX941**
(350µA, 80ns, rail-to-rail inputs)

★ **MAX942**
(dual MAX941)

★ **MAX944**
(quad MAX941)

MICROPOWER

MAX921
(3.2µA comparator + 1% reference)

MAX922
(dual, 3.2µA max supply current)

MAX923
(dual, 4.5µA comparator + 1% reference)

MAX924
(quad, 6.5µA comparator + 1% reference)

MAX931
(3.2µA comparator + 2% reference)

MAX932
(dual, 4.5µA comparator + 2% reference)

MAX933
(dual, 4.5µA comparator + 2% reference, window comparator)

MAX934
(quad, 6.5µA comparator + 2% reference)

ECL OUTPUT

MAX905
(master/slave, clocked)

MAX906
(dual, master/slave, clocked)

MAX911
(4ns, programmable input threshold voltage)

MAX9685
(industry standard)

MAX9687
(industry standard, dual)

MAX9690 (8-pin SO)

★ **New product**
† **Future product**

Comparators (High-Speed & Micropower)

Part Number	Comps. per Pkg.	Logic	Latched Outputs	Complementary Outputs	Supply Current per Comparator (mA max)	Tpd (ns)	Features	Price† 1000-up ($)
HIGH SPEED								
MAX516	4	TTL/CMOS	No	No	10.01(Total)	800	Quad comparator + quad 8-bit DAC for independent threshold setting, single-supply capability, rail-to-rail input voltage ranges	3.00
MAX900	4	TTL	Yes	No	4 (I_{CC})	8.0	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	TTL	No	No	4 (I_{CC})	8.0	MAX900 without output latch	5.98
MAX902	2	TTL	Yes	No	4 (I_{CC})	8.0	Dual MAX900	4.01
MAX903	1	TTL	Yes	No	4 (I_{CC})	8.0	Single MAX900	3.15
MAX905	1	ECL	Yes	Yes	24 (I_{EE})	1.8	Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages	3.54
MAX906	2	ECL	Yes	Yes	24 (I_{EE})	1.8	Dual MAX905	5.23
MAX907	2	TTL	No	No	1	30	High speed, ultra-low power, single +5V, 8-pin DIP/SO, built-in hysteresis	1.70
MAX908	4	TTL	No	No	1	30	High speed, ultra-low power, single +5V, 14-pin DIP/SO, built-in hysteresis	2.95
MAX909	1	TTL	Yes	Yes	1.8	30	High speed, low power, single or dual supply, input range includes ground, complementary	1.50
MAX910	1	TTL	Yes	No	30 (I_{CC})	8.0	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX911	1	ECL	Yes	Yes	30 (I_{EE})	4.0	MAX910 with differential ECL outputs	5.20
MAX912	2	TTL	Yes	Yes	10	10	Dual MAX913	3.90
MAX913	1	TTL	Yes	Yes	10	10	Lowest power 10ns comparator with complementary outputs single/dual supply, CMVR extends below ground to V+ -1.5V	2.55
MAX915	1	TTL	Yes	Yes	18 (ICC)	6	No oscillations, master/slave, clocked	2.55
MAX916	2	TTL	Yes	Yes	18 (ICC)	6	Dual MAX915	3.90
MAX941	1	TTL/CMOS	Yes	No	600µA	75	Low power, 3V or 5V single supply, rail-to-rail inputs (5µA SHDN)	1.40
MAX942	2	TTL/CMOS	No	No	600µA	75	Dual MAX941, 8-pin DIP/SO	1.50
MAX944	4	TTL/CMOS	No	No	600µA	75	Quad MAX941	2.50
MAX9685	1	ECL	Yes	Yes	32 (I_{EE})	1.3	Higher-speed industry standard	3.38
MAX9686	1	TTL	Yes	Yes	25 (I_{CC})	6.0	Higher-speed industry standard	2.31
MAX9687	2	ECL	Yes	Yes	68 (I_{EE})	1.4	Higher-speed industry standard	5.12
MAX9690	1	ECL	No	Yes	32 (I_{EE})	1.3	8-pin DIP/SO package	3.29
MAX9698	2	TTL	Yes	Yes	50 (I_{CC})	6.0	Higher-speed industry standard	3.92
MXL1016	1	TTL	Yes	Yes	35 (I_{CC})	10	High speed, complementary outputs, LT1016 second source	2.57
MXL1116	1	TTL	Yes	Yes	38 (I_{CC})	12	High speed, single supply, complementary outputs, LT1116 second source	2.57

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Comparators (High-Speed & Micropower) (continued)

Part Number	Comps. per Pkg.	Logic	Latched Outputs	Complementary Outputs	Supply Current per Comparator (µA max)	Tpd (µs)	Features	Price† 1000-up ($)
MICROPOWER								
MAX921	1 + ref	TTL/CMOS	No	No	3.2 (total pkg.)	12	Micropower comparator + 1% reference & hysteresis, single-supply capability, CMVR extends to GND	1.50
MAX922	2	TTL/CMOS	No	No	3.2 (total pkg.)	12	Dual, single-supply micropower comparator in 8-pin DIP/SO package	1.50
MAX923	2 + ref	TTL/CMOS	No	No	4.5 (total pkg.)	12	Dual, single-supply comparator with 1% voltage reference in 8-pin DIP/SO package	1.95
MAX924	4 + ref	TTL/CMOS	No	No	6.5 (total pkg.)	12	Quad, micropower comparator with 1% voltage reference	2.25
MAX931	1 + ref	TTL/CMOS	No	No	3.2 (total pkg.)	12	Comparator + 2% reference & hysteresis, single-supply, CMVR extends to GND	0.98
MAX932	2 + ref	TTL/CMOS	No	No	4.5 (total pkg.)	12	Dual, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO	1.26
MAX933	2 + ref	TTL/CMOS	No	No	4.5 (total pkg.)	12	Dual, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO (window comparator input configuration)	1.26
MAX934	4 + ref	TTL/CMOS	No	No	6.5 (total pkg.)	12	Quad comparator + 2%-accurate reference, single/dual supply	1.31
MAX951	1 + ref + amp	TTL/CMOS	No	No	7 (total pkg.)	12	Micropower, single-supply, rail-to-rail output, unity-gain-stable op amp + 1% reference and comparator with hysteresis	††
MAX952	1 + ref + amp	TTL/CMOS	No	No	7 (total pkg.)	12	Micropower, single-supply, rail-to-rail output, decompensated op amp + 1% refererence and comparator with hysteresis	††
MAX953	1 + amp	TTL/CMOS	No	No	5 (total pkg.)	12	Micropower, single-supply rail-to-rail output, unity-gain-stable op amp and comparator	††
MAX954	1 + amp	TTL/CMOS	No	No	5 (total pkg.)	12	Micropower, single-supply rail-to-rail output, decompensated op amp and comparator	††

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Precision, High-Side Current-Sense Amplifiers

General Description

The MAX471/MAX472 are complete, bidirectional, high-side current-sense amplifiers for portable PCs, telephones, and other systems where battery/DC power-line monitoring is critical. High-side power-line monitoring is especially useful in battery-powered systems, since it does not interfere with the ground paths of the battery chargers or monitors often found in "smart" batteries.

The MAX471 has an internal 35mΩ current-sense resistor and measures battery currents up to ±3A. For applications requiring higher current or increased flexibility, the MAX472 functions with external sense and gain-setting resistors. Both devices have a current output that can be converted to a ground-referred voltage with a single resistor, allowing a wide range of battery voltages and currents.

An open-collector SIGN output indicates current-flow direction, so the user can monitor whether a battery is being charged or discharged. Both devices operate from 3V to 36V, draw less than 100µA over temperature, and include a 5µA max shutdown mode.

Applications

Portable PCs:
Notebooks/Subnotebooks/Palmtops

Smart Battery Packs

Cellular Phones

Portable Phones

Portable Test/Measurement Systems

Battery-Operated Systems

Energy Management Systems

Features

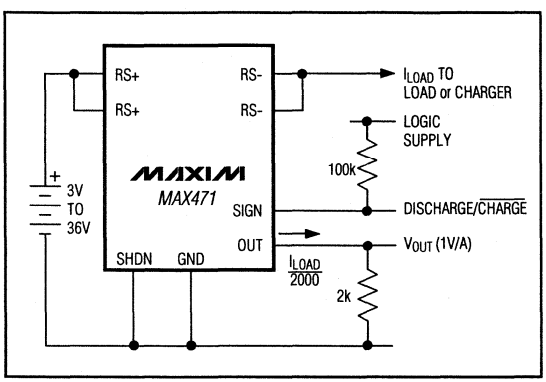
- ♦ **Complete High-Side Current Sensing**
- ♦ **Precision Internal Sense Resistor (MAX471)**
- ♦ **Accurate to within 2% Over Temperature**
- ♦ **Monitors Both Charge and Discharge**
- ♦ **3A Sense Capability with Internal Sense Resistor (MAX471)**
- ♦ **Higher Current-Sense Capability with External Sense Resistor (MAX472)**
- ♦ **100µA Max Supply Current**
- ♦ **5µA Max Shutdown Mode**
- ♦ **3V to 36V Supply Operation**
- ♦ **8-Pin DIP/SO Packages**

Ordering Information

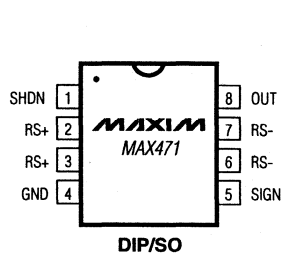
PART	TEMP. RANGE	PIN-PACKAGE
MAX471CPA	0°C to +70°C	8 Plastic DIP
MAX471CSA	0°C to +70°C	8 SO
MAX471EPA	-40°C to +85°C	8 Plastic DIP
MAX471ESA	-40°C to +85°C	8 SO
MAX472CPA	0°C to +70°C	8 Plastic DIP
MAX472CSA	0°C to +70°C	8 SO
MAX472C/D	0°C to +70°C	Dice*
MAX472EPA	-40°C to +85°C	8 Plastic DIP
MAX472ESA	-40°C to +85°C	8 SO

** Dice are specified at T_A = +25°C.*

Typical Operating Circuit



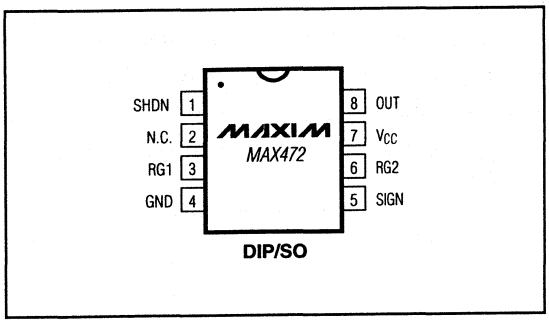
Pin Configurations



Pin Configurations continued on next page.

Precision, High-Side Current-Sense Amplifiers

Pin Configurations (continued)



19-0260; Rev 0; 6/94

MAXIM

Single/Dual/Quad, 10MHz Single-Supply Op Amps

General Description

The single MAX473, dual MAX474, and quad MAX475 are single-supply (2.7V to 5.25V), unity-gain-stable op amps with rail-to-rail output swing. Each op amp guarantees a 10MHz unity-gain bandwidth, 15V/µs slew rate, and 600Ω drive capability while typically consuming only 2mA supply current. In addition, the input range includes the negative supply rail and the output swings to within 50mV of each supply rail.

Single-supply operation makes these devices ideal for low-power and low-voltage portable applications. With their fast slew rate and settling time, they can replace higher-current op amps in large-signal applications. The MAX473/MAX474/MAX475 are available in DIP and SO packages in the industry-standard op-amp pin configurations.

Applications

Portable Equipment
Battery-Powered Instruments
Signal Processing
Discrete Filters
Signal Conditioning
Servo-Loops

Features

- ♦ **15V/µs Min Slew Rate**
- ♦ **+3V Single-Supply Operation**
- ♦ **Guaranteed 10MHz Unity-Gain Bandwidth**
- ♦ **2mA Supply Current per Amplifier**
- ♦ **Input Range Includes Negative Rail**
- ♦ **Outputs Short-Circuit Protected**
- ♦ **Rail-to-Rail Output Swing (to within ±50mV)**

Ordering Information

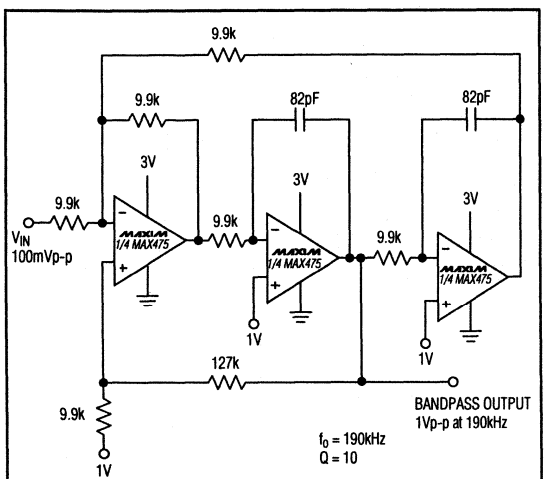
PART	TEMP. RANGE	PIN-PACKAGE
MAX473CPA	0°C to +70°C	8 Plastic DIP
MAX473CSA	0°C to +70°C	8 SO
MAX473CUA	0°C to +70°C	8 µMax**
MAX473C/D	0°C to +70°C	Dice*
MAX473EPA	-40°C to +85°C	8 Plastic DIP
MAX473ESA	-40°C to +85°C	8 SO
MAX473MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* *Dice are specified at T_A = +25°C, DC parameters only.*

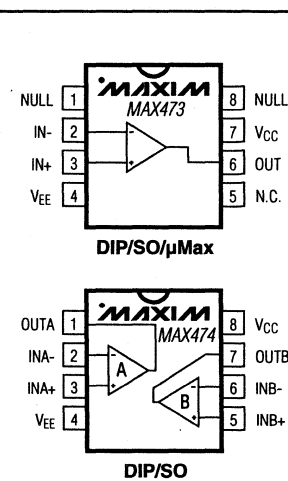
** *Contact factory for 8-pin µMax surface-mount package availability and specifications.*

Typical Operating Circuit



BANDPASS FILTER

Pin Configurations



Pin Configurations continued on last page.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE}) 7V
Input Voltage (IN+, IN-, IN_+, IN_-) ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ... 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges
MAX47_C_ _ ..... 0°C to +70°C
MAX47_E_ _ ..... -40°C to +85°C
MAX47_MJ_ ..... -55°C to +125°C
Junction Temperatures
MAX47_C_ /E_ _ ..... +150°C
MAX47_MJ_ ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($+3V \le V_{CC} \le +5V$, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473			±0.70	±2.0	mV
		MAX474			±0.70	±2.0	
		MAX475			±0.80	±2.5	
Input Bias Current	I_B	Current flows out of terminals		0	80	150	nA
Input Offset Current	I_{OS}				±10	±30	nA
Common-Mode Voltage	V_{CM}	High		V_{CC} - 1.9	V_{CC} - 1.7		V
		Low			V_{EE} - 0.1	V_{EE}	
Common-Mode Rejection Ratio	CMRR	$V_{EE} \le V_{CM} \le (V_{CC} - 1.9V)$		80	90		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 5.25V		80	90		dB
Input Noise-Voltage Density	e_n	f = 10kHz			40		nV/√Hz
Large-Signal Gain (Note 1)	A_{VOL}	0.3V ≤ V_{OUT} ≤ (V_{CC} - 0.5V)	R_L = no load		110		dB
			R_L = 10kΩ	94	105		
			R_L = 600Ω	82	90		
		Sinking 5mA	V_{CC} = 5V		76		
			V_{CC} = 3V		100		
		Sourcing 5mA	V_{CC} = 5V		76		
			V_{CC} = 3V		90		
Output Voltage	V_{OH}	V_{IN+} - V_{IN-} = +1V, R_L = no load		V_{CC} - 0.05			V
	V_{OL}	V_{IN+} - V_{IN-} = -1V, R_L = no load				V_{EE} + 0.05	
Slew Rate	SR	V_{CC} = 5V, R_L = 10kΩ, C_L = 20pF, V_{IN+} - V_{IN-} = +1V step		15	17		V/µs
Unity-Gain Bandwidth (Note 2)	GBW	3V ≤ V_{CC} ≤ 5V		10	12		MHz
		V_{CC} = 2.7V			10		

ELECTRICAL CHARACTERISTICS (continued)

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Settling Time	t_S	To 0.1%, C_L = 20pF			400		ns
Power-Up Time	t_{PU}	A_V = +1, V_{IN} = 1/2 V_{CC} step, see *Typical Operating Characteristics*			700		ns
Overshoot		C_L = 150pF			10		%
		C_L = 20pF			5		
Phase Margin		R_L = 10kΩ, C_L = 20pF	V_{CC} = 5V		63		degrees
			V_{CC} = 3V		58		
Gain Margin		R_L = 10kΩ, C_L = 20pF	V_{CC} = 5V		10		dB
			V_{CC} = 3V		12		
Supply Current	I_S	Per amplifier			2.0	3.0	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473				±2.0	mV
		MAX474				±2.0	
		MAX475				±3.0	
Input Bias Current	I_B	Current flows out of terminals		0		175	nA
Input Offset Current	I_{OS}					±35	nA
Common-Mode Rejection Ratio	CMRR	V_{EE} ≤ V_{CM} ≤ (V_{CC} - 1.9V)		78			dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 5.25V		78			dB
Large-Signal Gain (Note 1)	A_{VOL}	0.4V ≤ V_{OUT} ≤ (V_{CC} - 0.6V)	R_L = 10kΩ	94			dB
			R_L = 600Ω	80			
Output Voltage	V_{OH}	V_{IN+} - V_{IN-} = +1V, R_L = no load		V_{CC} - 0.07			V
	V_{OL}	V_{IN+} - V_{IN-} = -1V, R_L = no load				V_{EE} + 0.07	
Slew Rate	SR	V_{CC} = 5V, R_L = 10kΩ, C_L = 20pF, V_{IN+} - V_{IN-} = +1V step		12			V/µs
Supply Current	I_S	Per amplifier				3.3	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

Single/Dual/Quad, 10MHz Single-Supply Op Amps

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473				±2.3	mV
		MAX474				±2.3	
		MAX475				±3.3	
Input Bias Current	I_B	Current flows out of terminals		0		200	nA
Input Offset Current	I_{OS}					±50	nA
Common-Mode Rejection Ratio	CMRR	$V_{EE} \le V_{CM} \le (V_{CC} - 2.0V)$		72			dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 5.25V		72			dB
Large-Signal Gain (Note 1)	A_{VOL}	0.4V ≤ V_{OUT} ≤ (V_{CC} - 0.6V)	R_L = 10kΩ	94			dB
			R_L = 600Ω	72			
Output Voltage	V_{OH}	$V_{IN+} - V_{IN-}$ = +1V, R_L = no load		V_{CC} - 0.08			V
	V_{OL}	$V_{IN+} - V_{IN-}$ = - 1V, R_L = no load				V_{EE} + 0.08	
Slew Rate	SR	V_{CC} = 5V, R_L = 10kΩ, C_L = 20pF, $V_{IN+} - V_{IN-}$ = +1V step		10			V/µs
Supply Current	I_S	Per amplifier				3.4	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

ELECTRICAL CHARACTERISTICS

(+3V ≤ V_{CC} ≤ +5V, V_{EE} = 0V, V_{CM} = 0.5V, V_{OUT} = 0.5V, T_A = -55°C to +125°C, unless otherwise noted.)

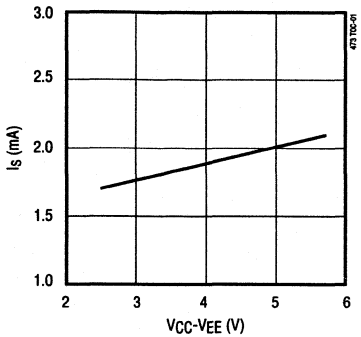
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX473				±2.8	mV
		MAX474				±2.8	
		MAX475				±4.0	
Input Bias Current	I_B	Current flows out of terminals		0		225	nA
Input Offset Current	I_{OS}					±60	nA
Common-Mode Rejection Ratio	CMRR	$V_{EE} \le V_{CM} \le (V_{CC} - 2.15V)$		70			dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 5.25V		70			dB
Large-Signal Gain (Note 1)	A_{VOL}	0.5V ≤ V_{OUT} ≤ (V_{CC} - 0.6V)	R_L = 10kΩ	90			dB
			R_L = 600Ω	70			
Output Voltage	V_{OH}	$V_{IN+} - V_{IN-}$ = +1V, R_L = no load		V_{CC} - 0.1			V
	V_{OL}	$V_{IN+} - V_{IN-}$ = -1V, R_L = no load				V_{EE} + 0.1	
Slew Rate	SR	V_{CC} = 5V, R_L = 10kΩ, C_L = 20pF, $V_{IN+} - V_{IN-}$ = +1V step		9			V/µs
Supply Current	I_S	Per amplifier				3.6	mA
Operating Supply-Voltage Range		Single supply		2.7		5.25	V
		Dual supplies		±1.35		±2.625	

Note 1: Gain decreases to zero as the output swings beyond the specified limits.
Note 2: Guaranteed by correlation to slew rate.

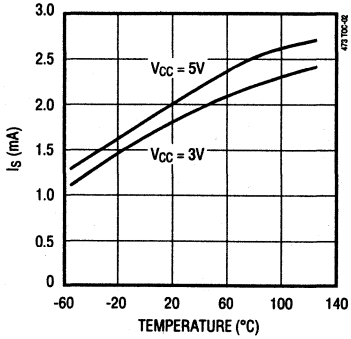
Typical Operating Characteristics

(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

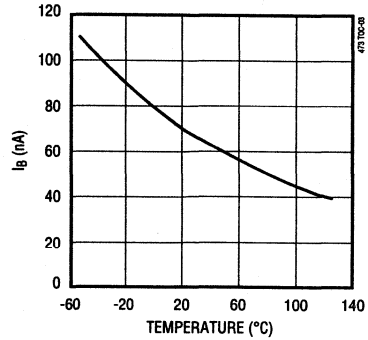
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



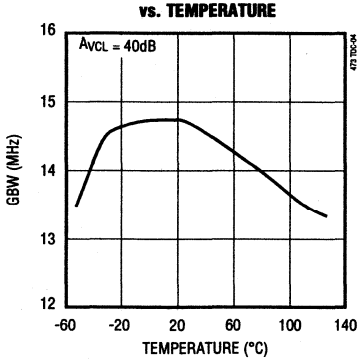
SUPPLY CURRENT vs. TEMPERATURE



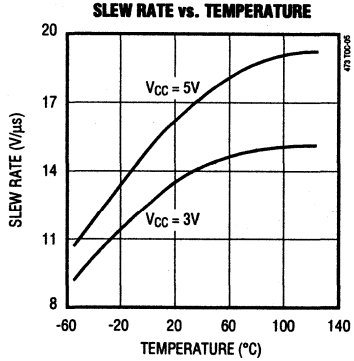
INPUT BIAS CURRENT vs. TEMPERATURE



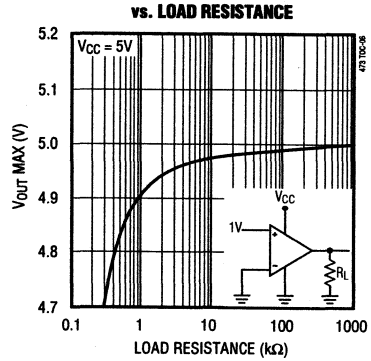
GAIN-BANDWIDTH PRODUCT vs. TEMPERATURE



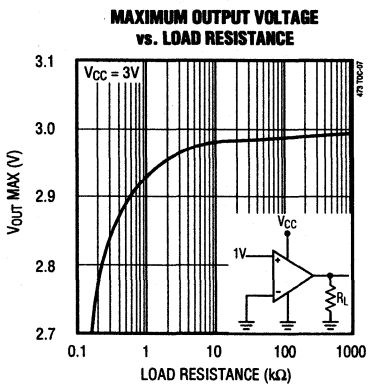
SLEW RATE vs. TEMPERATURE



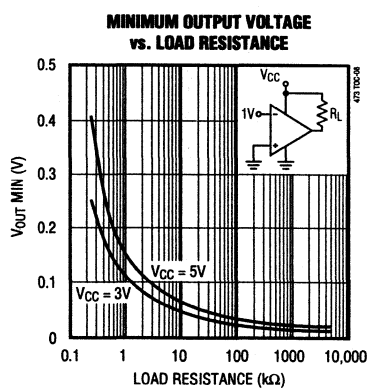
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE



MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE



MINIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE

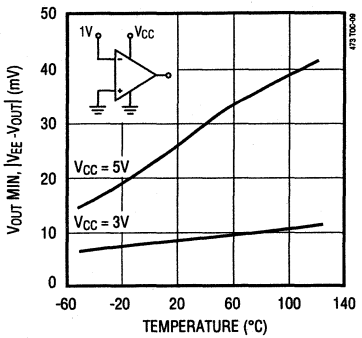


Single/Dual/Quad, 10MHz Single-Supply Op Amps

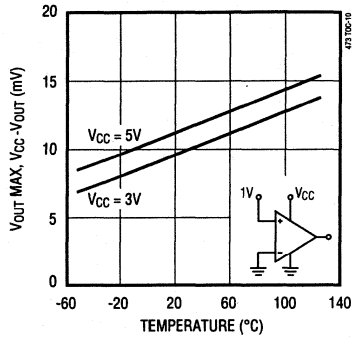
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

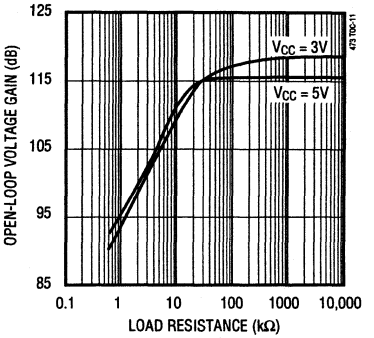
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



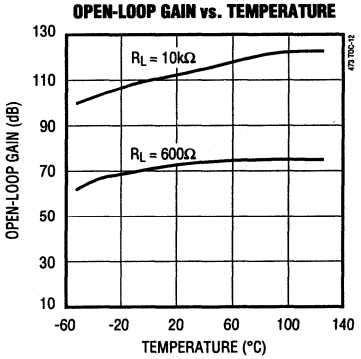
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



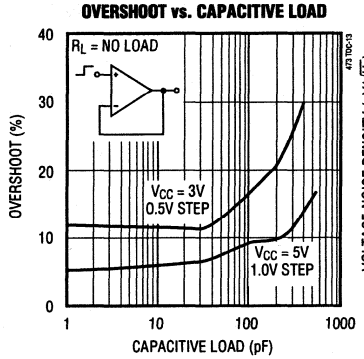
OPEN-LOOP VOLTAGE GAIN vs. LOAD RESISTANCE



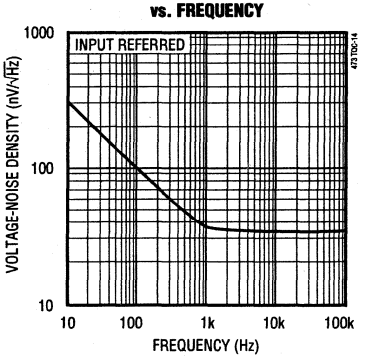
OPEN-LOOP GAIN vs. TEMPERATURE



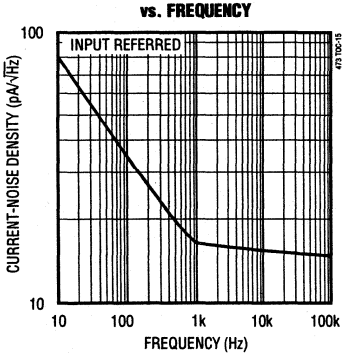
OVERSHOOT vs. CAPACITIVE LOAD



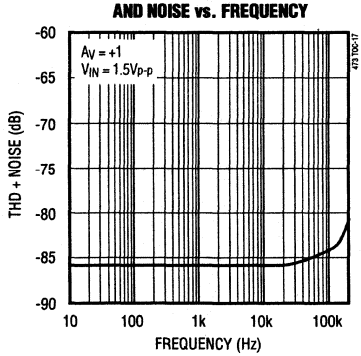
VOLTAGE-NOISE DENSITY vs. FREQUENCY



CURRENT-NOISE DENSITY vs. FREQUENCY



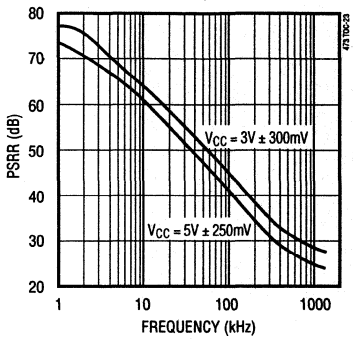
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY



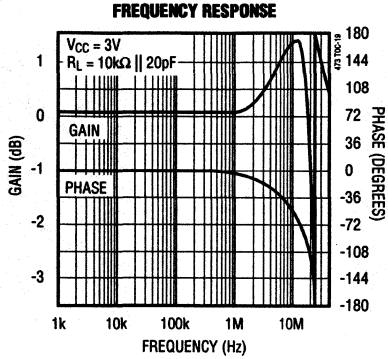
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

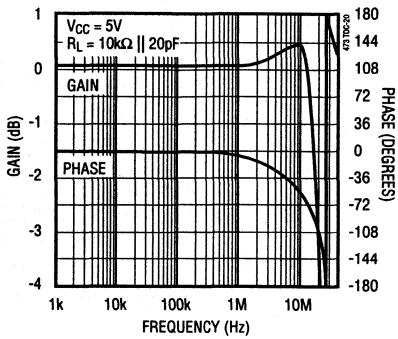
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



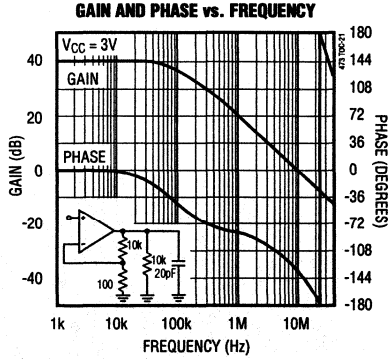
UNITY-GAIN FOLLOWER FREQUENCY RESPONSE



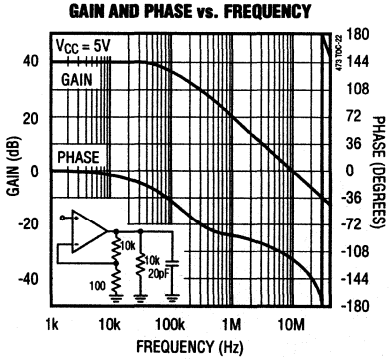
UNITY-GAIN FOLLOWER FREQUENCY RESPONSE



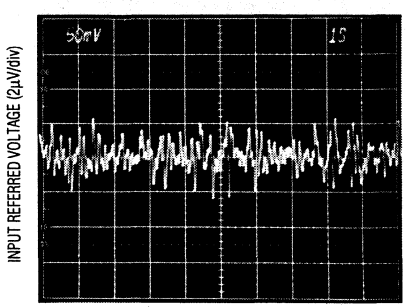
GAIN AND PHASE vs. FREQUENCY



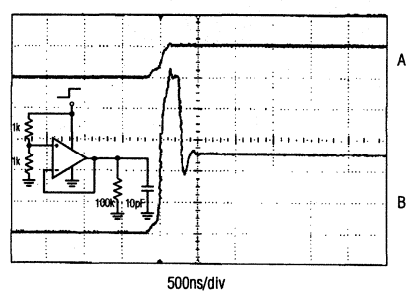
GAIN AND PHASE vs. FREQUENCY



0.1Hz to 10Hz VOLTAGE NOISE



POWER-UP TIME



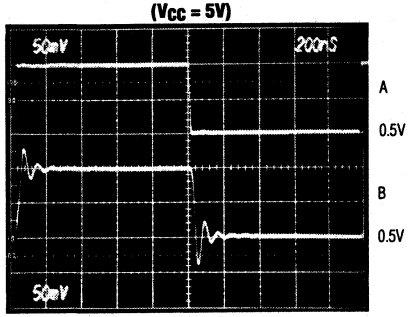
A : V_{CC}, 5V/div
B : V_{OUT}, 1V/div

Single/Dual/Quad, 10MHz Single-Supply Op Amps

Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

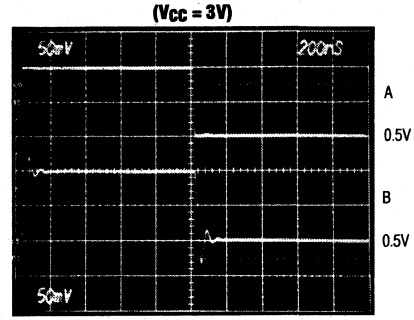
SMALL-SIGNAL TRANSIENT RESPONSE (V_{CC} = 5V)



200ns/div

V_{CC} = 5V, A_V = +1, R_L = 10kΩ, C_L = 220pF
A : V_{IN}, 50mV/div
B : V_{OUT}, 50mV/div

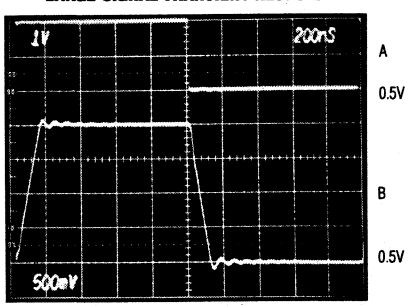
SMALL-SIGNAL TRANSIENT RESPONSE (V_{CC} = 3V)



200ns/div

V_{CC} = 3V, A_V = +1, R_L = 10kΩ, C_L = 100pF
A : V_{IN}, 50mV/div
B : V_{OUT}, 50mV/div

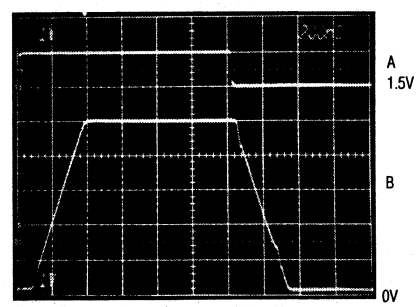
LARGE-SIGNAL TRANSIENT RESPONSE



200ns/div

V_{CC} = 5V, A_V = +1, R_L = 10kΩ, C_L = 220pF
A : V_{IN}, 1V/div
B : V_{OUT}, 500mV/div

OVERDRIVING THE OUTPUT



200ns/div

V_{CC} = 5V, V_{IN-} = 2.0V, R_L = 10kΩ, C_L = 33pF
A : V_{IN+}, 1V/div
B : V_{OUT}, 1V/div

Pin Description

PIN			NAME	FUNCTION
MAX473	MAX474	MAX475		
1, 8	—	—	NULL	Offset Null Input. Connect to one end of 2kΩ potentiometer for offset voltage trimming. Connect wiper to V_{EE}. See Figure 1.
—	1	1	OUTA	Amplifier A Output
2	—	—	IN-	Inverting Input
—	2	2	INA-	Amplifier A Inverting Input
3	—	—	IN+	Noninverting Input
—	3	3	INA+	Amplifier A Noninverting Input
4	4	11	V_{EE}	Negative Power-Supply Pin. Connect to ground or a negative voltage.
5	—	—	N.C.	No Connect—not internally connected
—	5	5	INB+	Amplifier B Noninverting Input
6	—	—	OUT	Amplifier Output
—	6	6	INB-	Amplifier B Inverting Input
—	7	7	OUTB	Amplifier B Output
7	8	4	V_{CC}	Positive Power-Supply Pin. Connect to (+) terminal of power supply.
—	—	8	OUTC	Amplifier C Output
—	—	9	INC-	Amplifier C Inverting Input
—	—	10	INC+	Amplifier C Noninverting Input
—	—	12	IND+	Amplifier D Noninverting Input
—	—	13	IND-	Amplifier D Inverting Input
—	—	14	OUTD	Amplifier D Output

Applications Information

Power Supplies

The MAX473/MAX474/MAX475 operate from a single 2.7V to 5.25V power supply, or from dual supplies of ±1.35V to ±2.625V. For single-supply operation, bypass the power supply with 0.1µF. If operating from dual supplies, bypass each supply to ground. With 0.1µF bypass capacitance, channel separation (MAX474/MAX475) is typically better than 120dB with signal frequencies up to 300kHz. Increasing the bypass capacitance (e.g. 10µF || 0.1µF) maintains channel separation at higher frequencies.

Minimizing Offsets

The MAX473's maximum offset voltage is ±2mV (T_A = +25°C). If additional offset adjustment is required, connect a 2kΩ trim potentiometer between pins 1, 8, and 4 (Figure 1). Input offset voltage for the dual MAX474 and quad MAX475 cannot be externally trimmed.

The MAX473/MAX474/MAX475 are bipolar op amps with low input bias currents. The bias currents at both inputs flow out of the device. Matching the resistance at the op amp's inputs significantly reduces the offset error caused by the bias currents. Place a resistor (R3) from the noninverting input to ground when using the inverting configuration (Figure 2a); place R3 in series with the noninverting input when using the noninverting configuration (Figure 2b). Select R3 such that the parallel combination of R2 and R1 equals R3. Adding R3 will slightly increase the op amp's voltage noise.

Output Loading and Stability

The MAX473/MAX474/MAX475 op amps are unity-gain stable. Any op amp's stability depends on the configuration, closed-loop gain, and load capacitance. The unity-gain, noninverting buffer is the most sensitive gain configuration, and driving capacitive loads decreases stability.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

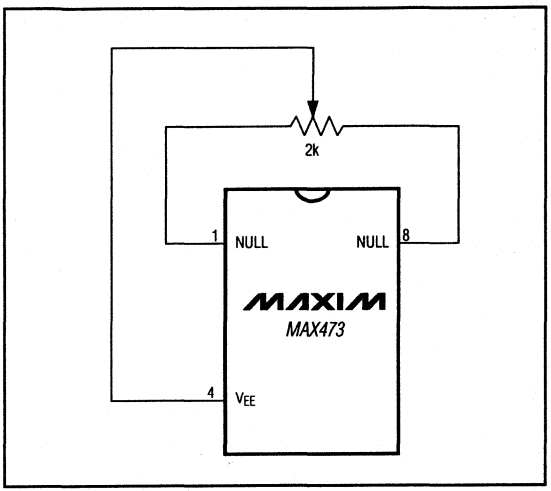


Figure 1. Offset Null Circuit

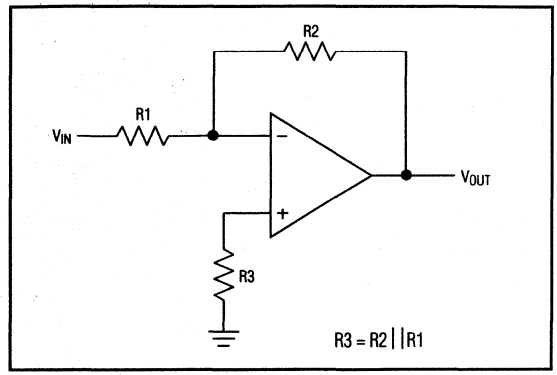


Figure 2a. Reducing Offset Error Due to Bias Current: Inverting Configuration

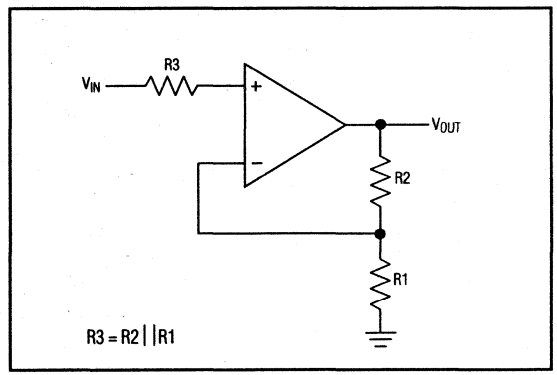


Figure 2b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

The MAX473/MAX474/MAX475 have excellent phase margin (the difference between 180° and the unity-gain phase angle). It is typically 63° with a load of 10kΩ in parallel with 20pF. Generally, higher phase margins indicate greater stability.

Capacitive loads form an RC network with the op amp's output resistance, causing additional phase shift that reduces the phase margin. Figure 3 shows the MAX473/MAX474/MAX475 output response when driving a 390pF load in parallel with 10kΩ.

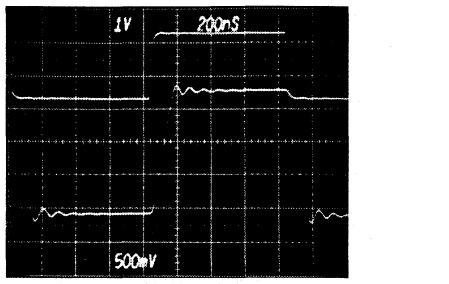
When driving large capacitive loads, add an output isolation resistor, as shown in Figure 4. This resistor improves the phase margin by isolating the load capacitance from the amplifier output. Figure 5 shows the MAX473/MAX474/MAX475 driving a capacitive load of 1000pF using the circuit of Figure 4.

Feedback Resistors

The feedback resistors appear as a resistance network to the op amp's feedback input (Figure 2). This resistance, combined with the op amp's input and stray capacitance (total input capacitance), forms a pole that adds unwanted phase shift when either the total input capacitance or feedback resistance is too large. For example, using the noninverting configuration with a gain of 10, if the total capacitance at the negative input is 10pF and the effective resistance (R1 || R2) is 9kΩ, this RC network introduces a pole at f_o = 1.8MHz. At input frequencies above f_o, the pole introduces additional phase shift, which reduces the overall bandwidth and adversely affects stability. Choose feedback resistors small enough so they do not adversely affect the op amp's operation at the frequencies of interest.

Overdriving the Outputs

The output voltage swing for specified operation is from (V_{EE} + 0.3V) to (V_{CC} - 0.5V) (*see Electrical Characteristics*). Exercising the outputs beyond these limits drives the output transistors toward saturation, resulting in bandwidth degradation, response-time increase, and gain decrease (which affects linearity). Operation in this region causes a slight distortion in the output waveform, but does not adversely affect the op amp.



Driving 390pF in parallel with 10kΩ,
V_{CC} = 5V, buffer configuration

Figure 3. MAX474 Driving 390pF

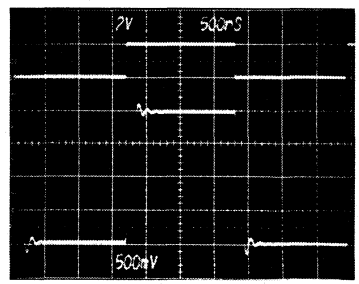


Figure 5. The MAX473 easily drives 1000pF using the Capacitive-Load Driving Circuit (Figure 4).

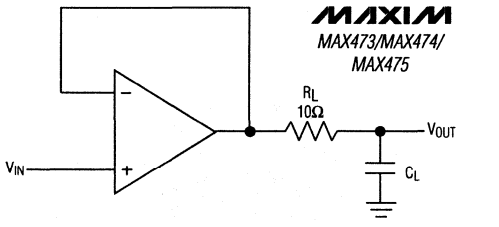


Figure 4. Capacitive-Load Driving Circuit

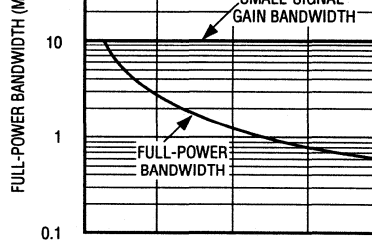


Figure 6. Full-Power Bandwidth vs. Peak-to-Peak AC Voltage

Full-Power Bandwidth

The MAX473/MAX474/MAX475's fast 15V/µs slew rate maximizes full-power bandwidth (FPBW). The FPBW is given by:

$$FPBW\ (Hz) = \frac{SR}{\pi\ [V_{OUT}\ peak\text{-}to\text{-}peak(max)]}$$

where the slew rate (SR) is 15V/µs min. Figure 6 shows the full-power bandwidth as a function of the peak-to-peak AC output voltage.

Layout

A good layout improves performance by decreasing the amount of stray capacitance at the amplifier's inputs and output. Since stray capacitance might be unavoidable, minimize trace lengths and resistor leads, and place external components as close to the pins as possible.

Single/Dual/Quad, 10MHz Single-Supply Op Amps

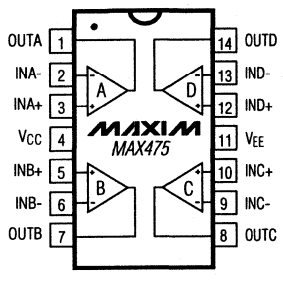
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX474CPA	0°C to +70°C	8 Plastic DIP
MAX474CSA	0°C to +70°C	8 SO
MAX474C/D	0°C to +70°C	Dice*
MAX474EPA	-40°C to +85°C	8 Plastic DIP
MAX474ESA	-40°C to +85°C	8 SO
MAX474MJA	-55°C to +125°C	8 CERDIP
MAX475CPD	0°C to +70°C	14 Plastic DIP
MAX475CSD	0°C to +70°C	14 SO
MAX475EPD	-40°C to +85°C	14 Plastic DIP
MAX475ESD	-40°C to +85°C	14 SO
MAX475MJD	-55°C to +125°C	8 CERDIP

* *Dice are specified at T_A = +25°C, DC parameters only.*

____Pin Configurations (continued)

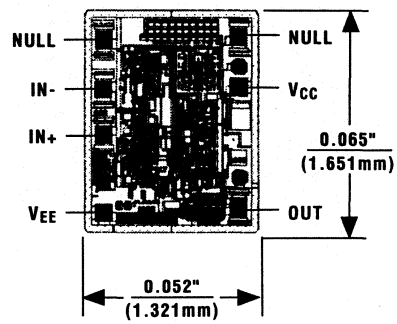
TOP VIEW



DIP/SO

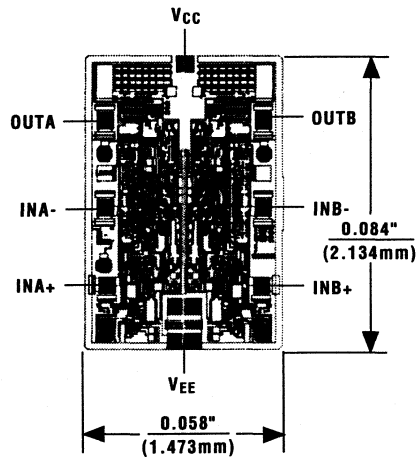
_____Chip Topographies

MAX473



TRANSISTOR COUNT: 185
SUBSTRATE CONNECTED TO V_{EE}

MAX474



TRANSISTOR COUNT: 355
SUBSTRATE CONNECTED TO V_{EE}

19-0265; Rev 0; 6/94

MAXIM

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

General Description

The dual MAX492, quad MAX494, and single MAX495 operational amplifiers combine excellent DC accuracy with rail-to-rail operation at the input and output. Since the common-mode voltage extends from V_{CC} to V_{EE}, the devices can operate from either a single supply (+2.7V to +6V) or split supplies (±1.35V to ±3V). Each op amp requires less than 150µA supply current. Even with this low current, the op amps are capable of driving a 1kΩ load, and the input referred voltage noise is only 25nV/√Hz. In addition, these op amps can drive loads in excess of 1nF.

The precision performance of the MAX492/MAX494/MAX495, combined with their wide input and output dynamic range, low-voltage single-supply operation, and very low supply current, makes them an ideal choice for battery-operated equipment and other low-voltage applications.

Applications

Portable Equipment

Battery-Powered Instruments

Data Acquisition

Signal Conditioning

Low-Voltage Applications

Features

- ♦ **Low-Voltage Single-Supply Operation (+2.7V to +6V)**
- ♦ **Rail-to-Rail Input Common-Mode Voltage Range**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **500kHz Gain-Bandwidth Product**
- ♦ **Unity-Gain Stable**
- ♦ **150µA Max Quiescent Current per Op Amp**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **200µV Offset Voltage**
- ♦ **High Voltage Gain (108dB)**
- ♦ **High CMRR (90dB) and PSRR (110dB)**
- ♦ **Drives 1kΩ Load**
- ♦ **Drives Large Capacitive Loads**

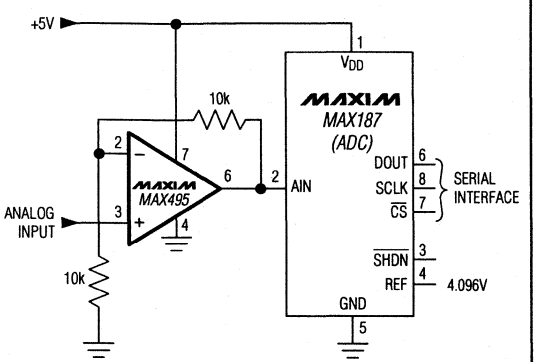
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX492CPA	0°C to +70°C	8 Plastic DIP
MAX492CSA	0°C to +70°C	8 SO
MAX492C/D	0°C to +70°C	Dice*
MAX492EPA	-40°C to +85°C	8 Plastic DIP
MAX492ESA	-40°C to +85°C	8 SO
MAX492MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

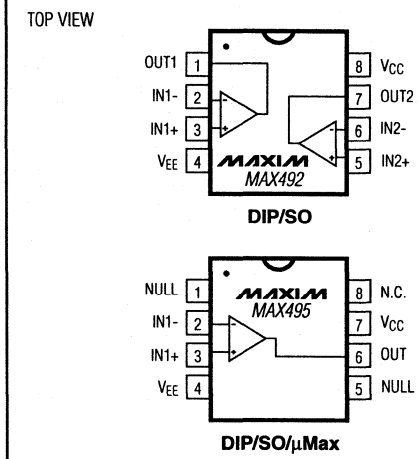
** Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



INPUT SIGNAL CONDITIONING FOR LOW-VOLTAGE ADC

Pin Configurations



DIP/SO

DIP/SO/µMax

Pin Configurations continued at end of data sheet.

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 7V
Common-Mode Input Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Differential Input Voltage ..... ±(V_{CC} - V_{EE})
Input Current (IN+, IN-, NULL1, NULL2) ..... ±10mA
Output Short-Circuit Duration ..... Indefinite short circuit to either supply
Voltage Applied to NULL Pins ..... V_{CC} to V_{EE}
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin Plastic SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
8-Pin µMax (derate 4.1mW/°C above +70°C) 330mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C)...800mW
14-Pin Plastic SO (derate 8.33mW/°C above +70°C) ...667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX49_C_ _ ..... 0°C to +70°C
MAX49_E_ _ ..... -40°C to +85°C
MAX49_M_ _ ..... -55°C to +125°C
Junction Temperatures
MAX49_C_ _/E_ _ ..... +150°C
MAX49_M_ _ ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}			±200	±500	µV
Input Bias Current	V_{CM} = V_{EE} to V_{CC}			±25	±60	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}			±0.5	±6	nA
Differential Input Resistance				2		MΩ
Common-Mode Input Voltage Range			V_{EE} - 0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	(V_{EE} - 0.25V) ≤ V_{CM} ≤ (V_{CC} + 0.25V)		74	90		dB
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6V		88	110		dB
Large-Signal Voltage Gain (Note 1)	V_{CC} = 2.7V, R_L = 100kΩ, V_{OUT} = 0.25V to 2.45V	Sourcing	90	104		dB
		Sinking	90	102		
	V_{CC} = 2.7V, R_L = 1kΩ, V_{OUT} = 0.5V to 2.2V	Sourcing	94	105		
		Sinking	78	90		
	V_{CC} = 5.0V, R_L = 100kΩ, V_{OUT} = 0.25V to 4.75V	Sourcing	98	108		
		Sinking	92	100		
	V_{CC} = 5.0V, R_L = 1kΩ, V_{OUT} = 0.5V to 4.5V	Sourcing	98	110		
		Sinking	86	98		
Output Voltage Swing (Note 1)	R_L = 100kΩ	V_{OH}	V_{CC} - 0.075	V_{CC} - 0.04		V
		V_{OL}		V_{EE} + 0.04	V_{EE} + 0.075	
	R_L = 1kΩ	V_{OH}	V_{CC} - 0.20	V_{CC} - 0.15		
		V_{OL}		V_{EE} + 0.15	V_{EE} + 0.20	
Output Short-Circuit Current				30		mA
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	V_{CM} = V_{OUT} = V_{CC} / 2	V_{CC} = 2.7V		135	150	µA
		V_{CC} = 5V		150	170	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	R_L = 100kΩ, C_L = 100pF		500		kHz
Phase Margin	R_L = 100kΩ, C_L = 100pF		60		degrees
Gain Margin	R_L = 100kΩ, C_L = 100pF		10		dB
Total Harmonic Distortion	R_L = 10kΩ, C_L = 15pF, V_{OUT} = $2V_{p-p}$, A_V = +1, f = 1kHz		0.003		%
Slew Rate	R_L = 100kΩ, C_L = 15pF		0.20		V/µs
Settling Time	To 0.1%, 2V step		12		µs
Turn-On Time	V_{CC} = 0V to 3V step, V_{IN} = V_{CC} / 2, A_V = +1		5		µs
Input Noise-Voltage Density	f = 1kHz		25		$nV/\sqrt{Hz}$
Input Noise-Current Density	f = 1kHz		0.1		$pA/\sqrt{Hz}$
Amp-Amp Isolation	f = 1kHz		125		dB

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}				±650	µV
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V_{CM} = V_{EE} to V_{CC}				±75	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}				±6	nA
Common-Mode Input Voltage Range			V_{EE} - 0.20		V_{CC} + 0.20	V
Common-Mode Rejection Ratio	(V_{EE} - 0.20) ≤ V_{CM} ≤ (V_{CC} + 0.20)		72			dB
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6V		86			dB
Large-Signal Voltage Gain (Note 1)	V_{CC} = 2.7V, R_L = 100kΩ, V_{OUT} = 0.25V to 2.45V	Sourcing	88			dB
		Sinking	84			
	V_{CC} = 2.7V, R_L = 1kΩ, V_{OUT} = 0.5V to 2.2V	Sourcing	92			
		Sinking	76			
	V_{CC} = 5.0V, R_L = 100kΩ, V_{OUT} = 0.25V to 4.75V	Sourcing	92			
		Sinking	88			
	V_{CC} = 5.0V, R_L = 1kΩ, V_{OUT} = 0.5V to 4.5V	Sourcing	96			
		Sinking	82			
Output Voltage Swing (Note 1)	R_L = 100kΩ	V_{OH}	V_{CC} - 0.075			V
		V_{OL}			V_{EE} + 0.075	
	R_L = 1kΩ	V_{OH}	V_{CC} - 0.20			
		V_{OL}			V_{EE} + 0.20	
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	V_{CM} = V_{OUT} = V_{CC} / 2	V_{CC} = 2.7V			175	µA
		V_{CC} = 5V			190	

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}				±950	µV
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V_{CM} = V_{EE} to V_{CC}				±100	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}				±8	nA
Common-Mode Input Voltage Range			V_{EE} - 0.15		V_{CC} + 0.15	V
Common-Mode Rejection Ratio	(V_{EE} - 0.15) ≤ V_{CM} ≤ (V_{CC} + 0.15)		68			dB
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6V, V_{CM} = 0V		84			dB
Large-Signal Voltage Gain (Note 1)	V_{CC} = 2.7V, R_L = 100kΩ, V_{OUT} = 0.25V to 2.45V	Sourcing	86			dB
		Sinking	84			
	V_{CC} = 2.7V, R_L = 1kΩ, V_{OUT} = 0.5V to 2.2V	Sourcing	92			
		Sinking	76			
	V_{CC} = 5.0V, R_L = 100kΩ, V_{OUT} = 0.25V to 4.75V	Sourcing	92			
		Sinking	86			
	V_{CC} = 5.0V, R_L = 1kΩ, V_{OUT} = 0.5V to 4.5V	Sourcing	96			
		Sinking	80			
Output Voltage Swing (Note 1)	R_L = 100kΩ	V_{OH}	V_{CC} - 0.075			V
		V_{OL}			V_{EE} + 0.075	
	R_L = 1kΩ	V_{OH}	V_{CC} - 0.20			
		V_{OL}			V_{EE} + 0.20	
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	V_{CM} = V_{OUT} = V_{CC} / 2	V_{CC} = 2.7V			185	µA
		V_{CC} = 5V			200	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 6V, V_{EE} = GND, V_{CM} = 0V, V_{OUT} = V_{CC} / 2, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{CM} = V_{EE} to V_{CC}				±1.2	mV
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V_{CM} = V_{EE} to V_{CC}				±200	nA
Input Offset Current	V_{CM} = V_{EE} to V_{CC}				±10	nA
Common-Mode Input Voltage Range			V_{EE} - 0.05		V_{CC} + 0.05	V
Common-Mode Rejection Ratio	(V_{EE} - 0.05V) ≤ V_{CM} ≤ (V_{CC} + 0.05V)		66			dB
Power-Supply Rejection Ratio	V_{CC} = 2.7V to 6V		80			dB
Large-Signal Voltage Gain (Note 1)	V_{CC} = 2.7V, R_L = 100kΩ, V_{OUT} = 0.25V to 2.45V	Sourcing	82			dB
		Sinking	80			
	V_{CC} = 2.7V, R_L = 1kΩ, V_{OUT} = 0.5V to 2.2V	Sourcing	90			
		Sinking	72			
	V_{CC} = 5.0V, R_L = 100kΩ, V_{OUT} = 0.25V to 4.75V	Sourcing	86			
		Sinking	82			
	V_{CC} = 5.0V, R_L = 1kΩ, V_{OUT} = 0.5V to 4.5V	Sourcing	94			
		Sinking	76			
Output Voltage Swing (Note 1)	R_L = 100kΩ	V_{OH}	V_{CC} - 0.075			V
		V_{OL}			V_{EE} + 0.075	
	R_L = 1kΩ	V_{OH}	V_{CC} - 0.250			
		V_{OL}			V_{EE} + 0.250	
Operating Supply Voltage Range			2.7		6.0	V
Supply Current (per amplifier)	V_{CM} = V_{OUT} = V_{CC} / 2	V_{CC} = 2.7V			200	µA
		V_{CC} = 5V			225	

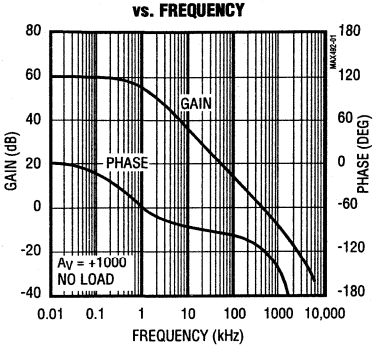
Note 1: R_L to V_{EE} for sourcing and V_{OH} tests; R_L to V_{CC} for sinking and V_{OL} tests.

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

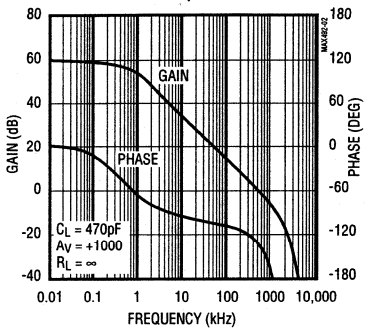
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = 5V, V_{EE} = 0V, unless otherwise noted.)

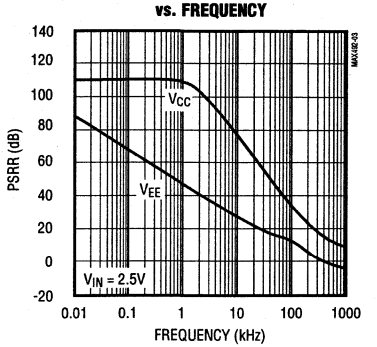
GAIN AND PHASE vs. FREQUENCY



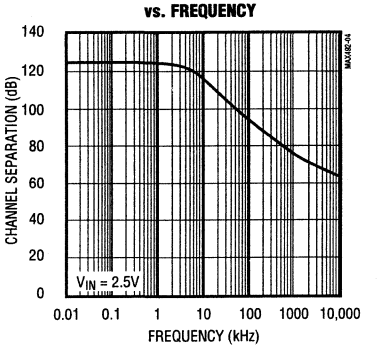
GAIN AND PHASE vs. FREQUENCY



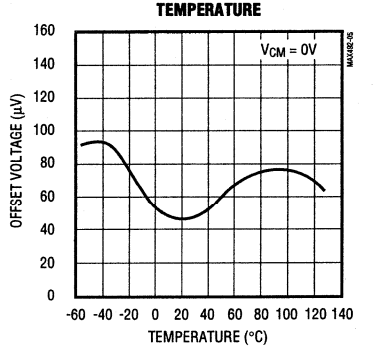
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



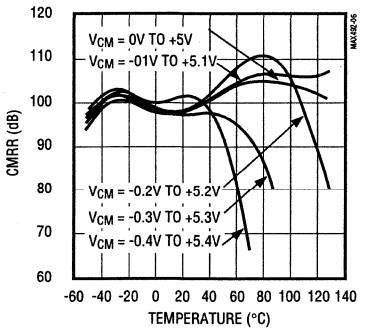
CHANNEL SEPARATION vs. FREQUENCY



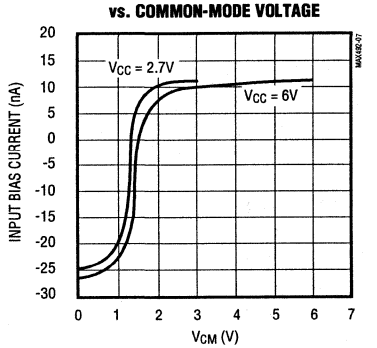
OFFSET VOLTAGE vs. TEMPERATURE



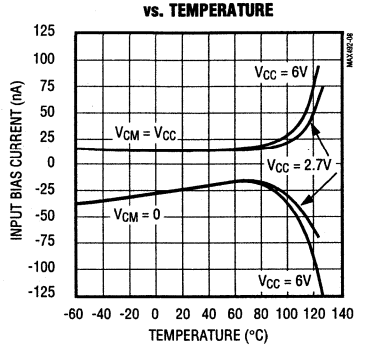
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



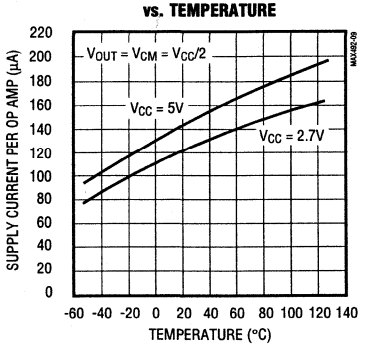
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs. TEMPERATURE



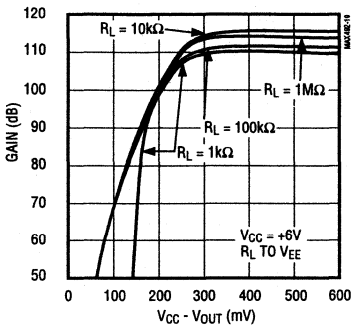
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



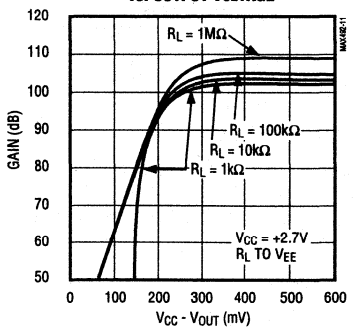
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = 5V, V_{EE} = 0V, unless otherwise noted.)

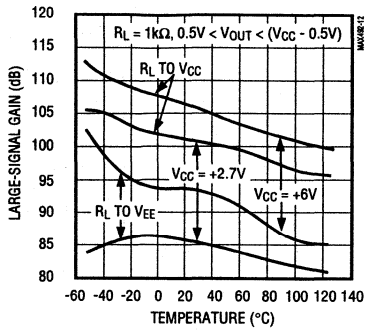
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



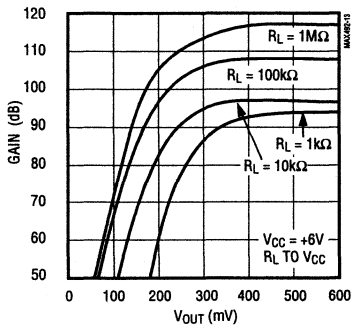
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



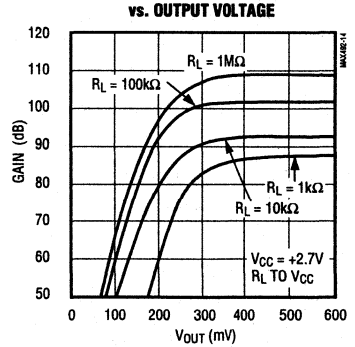
LARGE-SIGNAL GAIN vs. TEMPERATURE



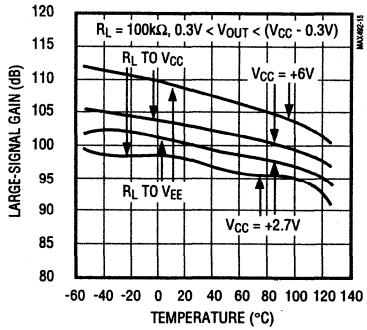
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



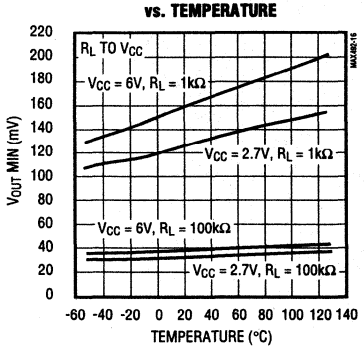
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE



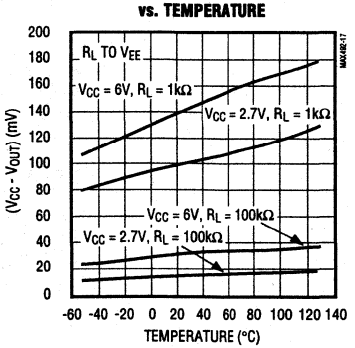
LARGE-SIGNAL GAIN vs. TEMPERATURE



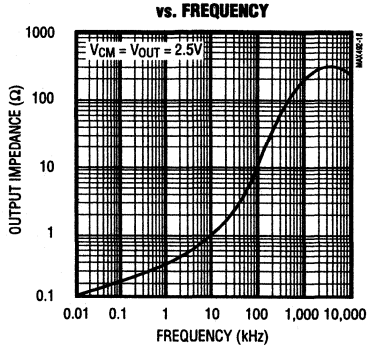
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE



MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



OUTPUT IMPEDANCE vs. FREQUENCY

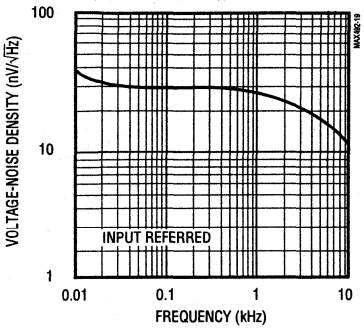


Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

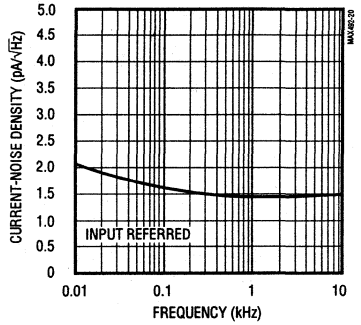
Typical Operating Characteristics (continued)

(T_A = +25°C, V_{CC} = 5V, V_{EE} = 0V, unless otherwise noted.)

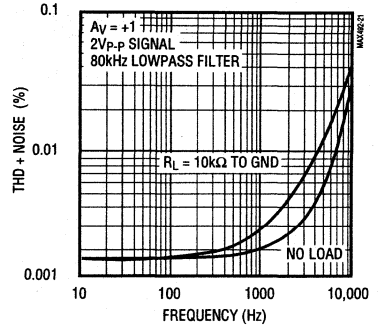
VOLTAGE-NOISE DENSITY vs. FREQUENCY



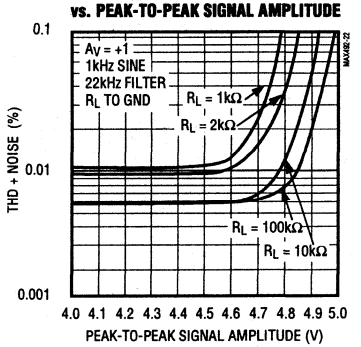
CURRENT-NOISE DENSITY vs. FREQUENCY



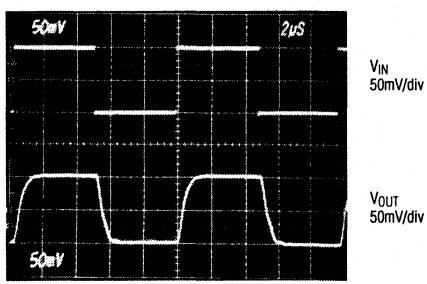
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



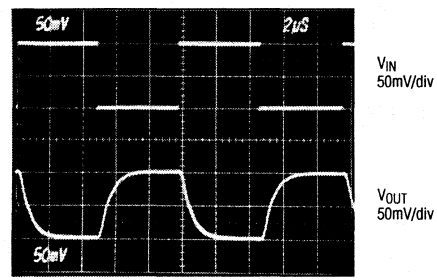
SMALL-SIGNAL TRANSIENT RESPONSE



2µs/div

V_{CC} = +5V, A_V = +1, R_L = 10kΩ

SMALL-SIGNAL TRANSIENT RESPONSE

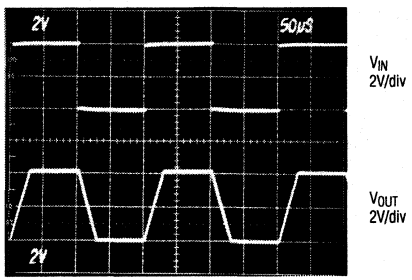


2µs/div

V_{CC} = +5V, A_V = -1, R_L = 10kΩ

Typical Operating Characteristics (continued)

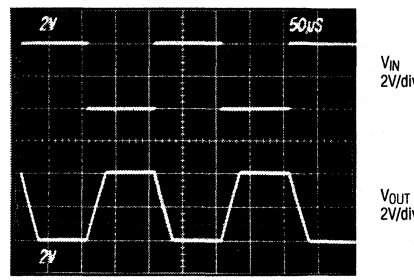
LARGE-SIGNAL TRANSIENT RESPONSE



50µs/div

V_{CC} = +5V, A_V = +1, R_L = 10kΩ

LARGE-SIGNAL TRANSIENT RESPONSE



50µs/div

V_{CC} = +5V, A_V = -1, R_L = 10kΩ

Pin Description

PIN			NAME	FUNCTION
MAX492	MAX494	MAX495		
1	1	—	OUT1	Amplifier 1 Output
—	—	1, 5	NULL	Offset Null Input. Connect to a 10kΩ potentiometer for offset-voltage trimming. Connect wiper to V_{EE}. See Figure 3.
—	—	2	IN-	Inverting Input
2	2	—	IN1-	Amplifier 1 Inverting Input
—	—	3	IN+	Noninverting Input
3	3	—	IN1+	Amplifier 1 Noninverting Input
4	11	4	V_{EE}	Negative Power-Supply Pin. Connect to ground or a negative voltage.
5	5	—	IN2+	Amplifier 2 Noninverting Input
—	—	6	OUT	Amplifier Output
6	6	—	IN2-	Amplifier 2 Inverting Input
7	7	—	OUT2	Amplifier 2 Output
8	4	7	V_{CC}	Positive Power-Supply Pin. Connect to (+) terminal of power supply.
—	8	—	OUT3	Amplifier 3 Output
—	9	—	IN3-	Amplifier 3 Inverting Input
—	10	—	IN3+	Amplifier 3 Noninverting Input
—	12	—	IN4+	Amplifier 4 Noninverting Input
—	13	—	IN4-	Amplifier 4 Inverting Input
—	14	—	OUT4	Amplifier 4 Output
—	—	8	N.C.	No Connect. Not internally connected.

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

Applications Information

The dual MAX492, quad MAX494, and single MAX495 op amps combine excellent DC accuracy with rail-to-rail operation at both input and output. With their precision performance, wide dynamic range at low supply voltages, and very low supply current, these op amps are ideal for battery-operated equipment and other low-voltage applications.

Rail-to-Rail Inputs and Outputs

The MAX492/MAX494/MAX495's input common-mode range extends 0.25V **beyond** the positive and negative supply rails, with excellent common-mode rejection. Beyond the specified common-mode range, the outputs are guaranteed not to undergo phase reversal or latchup. Therefore, the MAX492/MAX494/MAX495 can be used in applications with common-mode signals at or even beyond the supplies, without the problems associated with typical op amps.

The MAX492/MAX494/MAX495's output voltage swings to within 50mV of the supplies with a 100kΩ load. This rail-to-rail swing at the input and output substantially increases the dynamic range, especially in low supply-voltage applications. Figure 1 shows the input and output waveforms for the MAX492, configured as a unity-gain noninverting buffer operating from a single +3V supply. The input signal is $3.0V_{p-p}$, 1kHz sinusoid centered at +1.5V. The output amplitude is approximately $2.95V_{p-p}$.

Input Offset Voltage

Rail-to-rail common-mode swing at the input is obtained by two complementary input stages in parallel, which feed a folded cascoded stage. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages close to the positive rail.

The offsets of the two pairs are trimmed, however there is some small residual mismatch between them. This mismatch results in a two-level input offset characteristic, with a transition region between the levels occurring at a common-mode voltage of approximately 1.3V. Unlike other rail-to-rail op amps, the transition region has been widened to approximately 600mV in order to minimize the slight degradation in CMRR caused by this mismatch.

To adjust the MAX495's input offset voltage (500µV max at +25°C), connect a 10kΩ trim potentiometer between the two NULL pins (pins 1 and 5), with the wiper connected to V_{EE} (pin 4) (Figure 2). The trim range of this circuit is ±6mV. External offset adjustment is not available for the dual MAX492 or quad MAX494.

The input bias currents of the MAX492/MAX494/MAX495 are typically less than 50nA. The bias current flows into the device when the NPN input stage is active, and it flows out when the PNP input stage is active. To reduce the offset error caused by input bias current flowing through external source resistances, match the effective resistance seen at each input. Connect resistor R3 between the noninverting input and ground when using

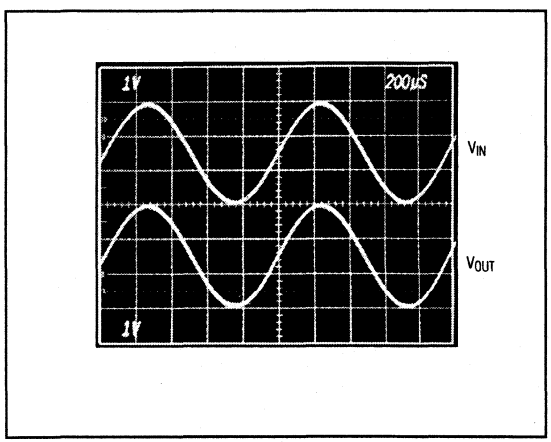


Figure 1. Rail-to-Rail Input and Output (Voltage Follower Circuit, VCC = +3V, VEE = 0V)

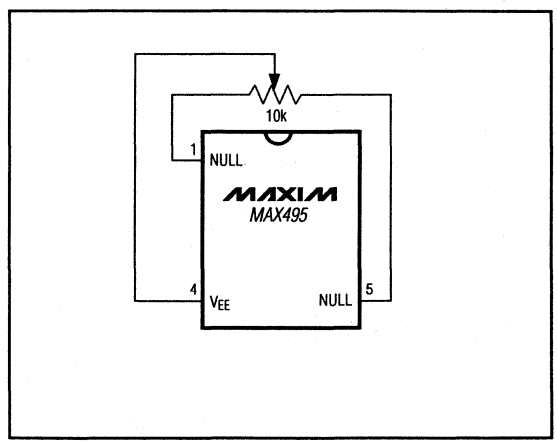


Figure 2. Offset Null Circuit

the op amp in an inverting configuration (Figure 3a); connect resistor R3 between the noninverting input and the input signal when using the op amp in a noninverting configuration (Figure 3b). Select R3 to equal the parallel combination of R1 and R2. High source resistances will degrade noise performance, due to the thermal noise of the resistor and the input current noise (which is multiplied by the source resistance).

Output Loading and Stability

Even with their low quiescent current of less than 150µA per op amp, the MAX492/MAX494/MAX495 are well suited for driving loads up to 1kΩ while maintaining DC accuracy. Stability while driving heavy capacitive loads is another key advantage over comparable CMOS rail-to-rail op amps.

In op amp circuits, driving large capacitive loads increases the likelihood of oscillation. This is especially true for circuits with high loop gains, such as a unity-gain voltage follower. The output impedance and a capacitive load form an RC network that adds a pole to the loop response and induces phase lag. If the pole frequency is low enough—as when driving a large capacitive load—the circuit phase margin is degraded, leading to either an under-damped pulse response or oscillation.

The MAX492/MAX494/MAX495 can drive capacitive loads in excess of 1000pF under certain conditions (Figure 4). When driving capacitive loads, the greatest potential for instability occurs when the op amp is sourcing approximately 100µA. Even in this case, sta-

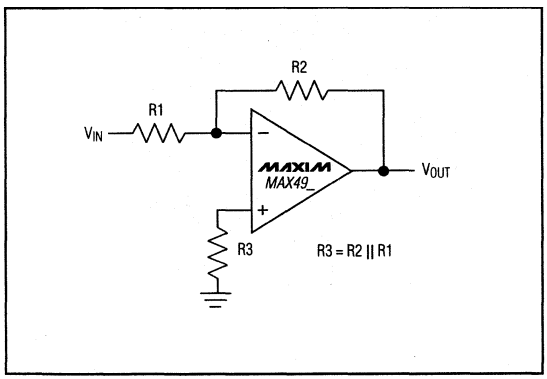


Figure 3a. Reducing Offset Error Due to Bias Current: Inverting Configuration

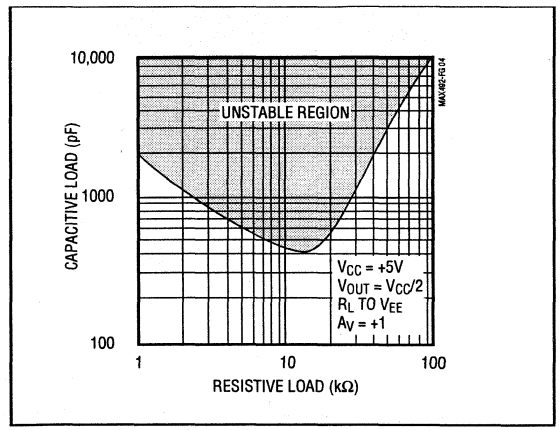


Figure 4. Capacitive-Load Stable Region Sourcing Current

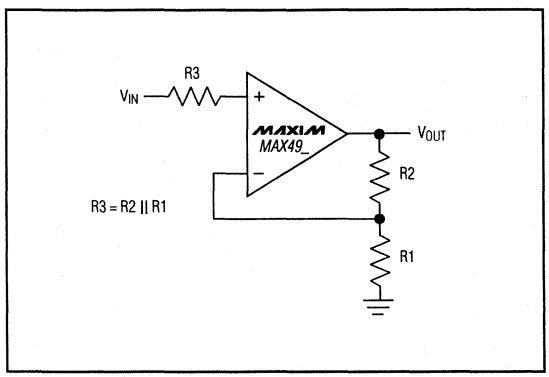


Figure 3b. Reducing Offset Error Due to Bias Current: Noninverting Configuration

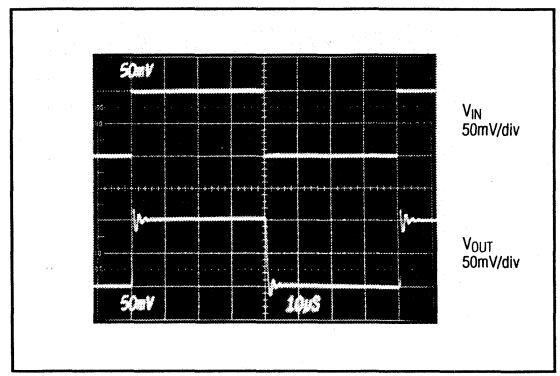


Figure 5. MAX492 Voltage Follower with 1000pF Load ($R_L = \infty$)

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

bility is maintained with up to 400pF of output capacitance. If the output sources either more or less current, stability is increased. These devices perform well with a 1000pF pure capacitive load (Figure 5). Figure 6 shows the performance with a 500pF load in parallel with various load resistors.

To increase stability while driving large capacitive loads, connect a pull-up resistor at the output to decrease the current that the amplifier must source. If the amplifier is made to sink current rather than source, stability is further increased.

Frequency stability can be improved by adding an output isolation resistor (R_S) to the voltage follower circuit (Figure 7). This resistor improves the phase margin of the circuit by isolating the load capacitor from the op amp's output. Figure 8a shows the MAX492 driving 10,000pF ($R_L \geq 100k\Omega$), while Figure 8b adds a 47Ω isolation resistor.

Because the MAX492/MAX494/MAX495 have excellent stability, no isolation resistor is required, except in the most demanding applications. This is beneficial because an isolation resistor would degrade the low-frequency performance of the circuit.

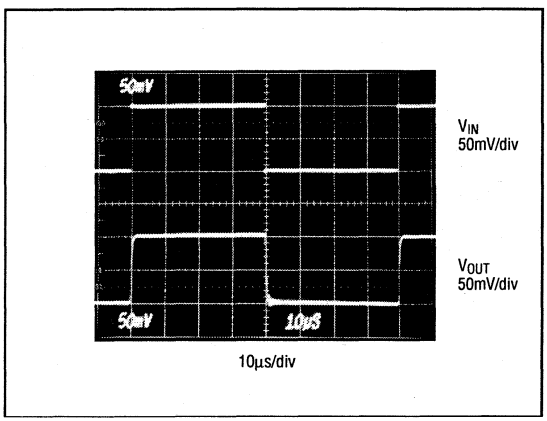


Figure 6a. MAX492 Voltage Follower with 500pF Load— $R_L = 5k\Omega$

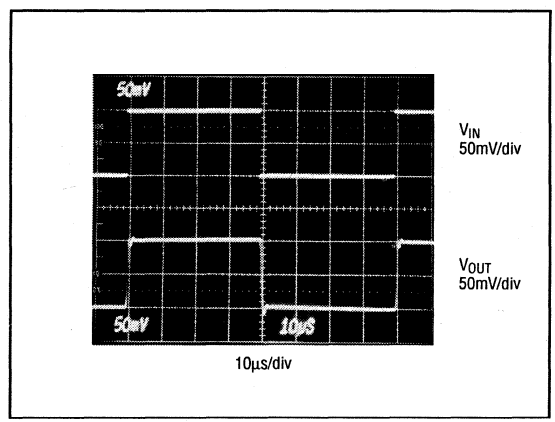


Figure 6c. MAX492 Voltage Follower with 500pF Load— $R_L = \infty$

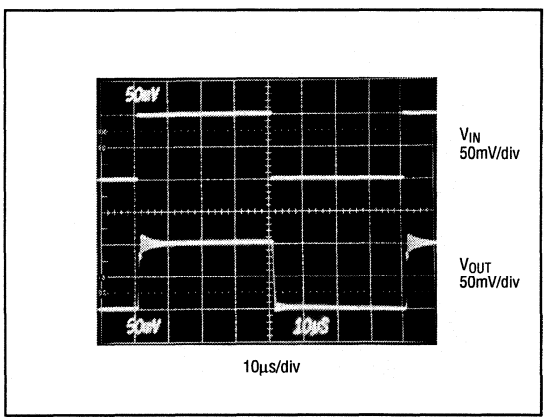


Figure 6b. MAX492 Voltage Follower with 500pF Load— $R_L = 20k\Omega$

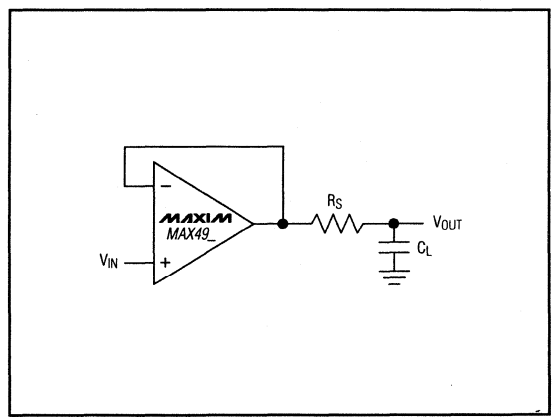


Figure 7. Capacitive-Load Driving Circuit

Power-Up Settling Time

The MAX492/MAX494/MAX495 have a typical supply current of 150µA per op amp. Although supply current is already low, it is sometimes desirable to reduce it further by powering down the op amp and associated ICs for periods of time. For example, when using a MAX494 to buffer the inputs to a multi-channel analog-to-digital converter (ADC), much of the circuitry could be powered down between data samples to increase battery life. If samples are taken infrequently, the op amps, along with the ADC, may be powered down most of the time.

When power is reapplied to the MAX492/MAX494/MAX495, it takes some time for the voltages on the supply pin and the output pin of the op amp to settle. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op amp settling time depends primarily on the output voltage and is slew-rate limited. With the noninverting input to a voltage follower held at mid-supply (Figure 9), when the supply steps from 0V to VCC, the output settles in approximately 4µs for VCC = +3V (Figure 10a) or 10µs for VCC = +5V (Figure 10b).

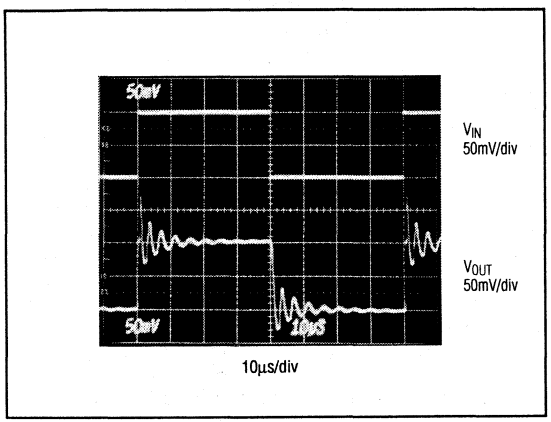


Figure 8a. Driving a 10,000pF Capacitive Load

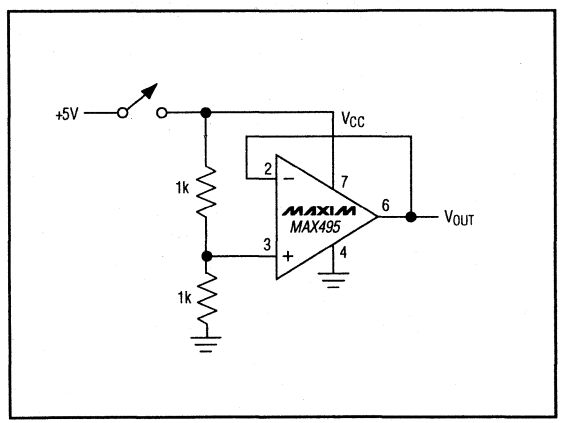


Figure 9. Power-Up Test Configuration

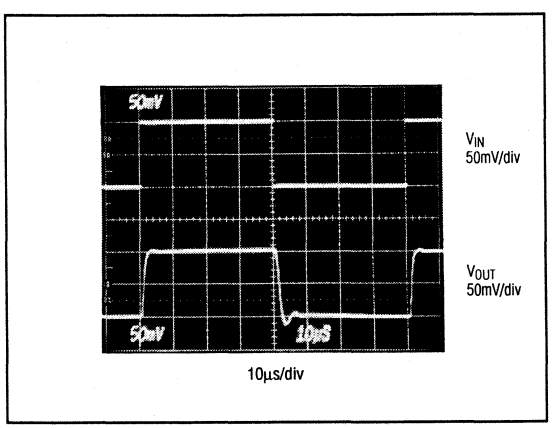


Figure 8b. Driving a 10,000pF Capacitive Load with a 47Ω Isolation Resistor

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

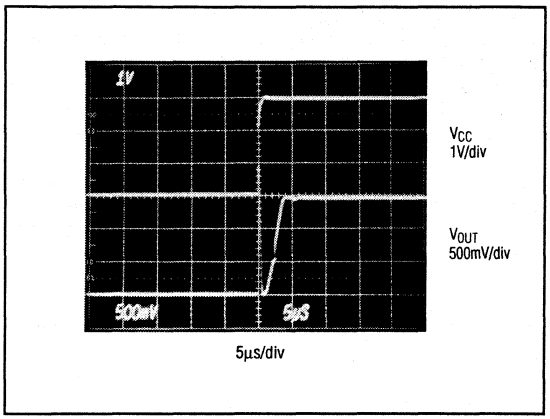


Figure 10a. Power-Up Settling Time (V_{CC} = +3V)

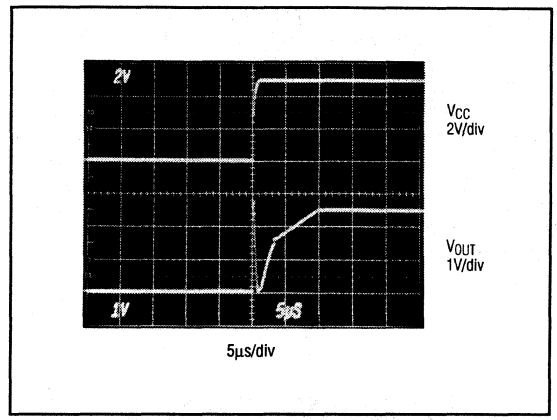


Figure 10b. Power-Up Settling Time (V_{CC} = +5V)

Power Supplies and Layout

The MAX492/MAX494/MAX495 operate from a single 2.7V to 6V power supply, or from dual supplies of ±1.35V to ±3V. For single-supply operation, bypass the power supply with a 1µF capacitor in parallel with a 0.1µF ceramic capacitor. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize both trace lengths and resistor leads and place external components close to the op amp's pins.

Rail-to-Rail Buffers

The *Typical Operating Circuit* shows a MAX495 gain-of-two buffer driving the analog input to a MAX187 12-bit ADC. Both devices run from a single 5V supply, and the converter's internal reference is 4.096V. The MAX495's typical input offset voltage is 200µV. This results in an error at the ADC input of 400µV, or less than half of one least significant bit (LSB). Without offset trimming, the op amp contributes negligible error to the conversion result.

Single/Dual/Quad, Micropower, Single-Supply Rail-to-Rail Op Amps

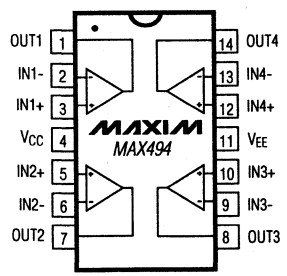
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX494CPD	0°C to +70°C	14 Plastic DIP
MAX494CSD	0°C to +70°C	14 SO
MAX494EPD	-40°C to +85°C	14 Plastic DIP
MAX494ESD	-40°C to +85°C	14 SO
MAX494MJD	-55°C to +125°C	14 CERDIP
MAX495CPA	0°C to +70°C	8 Plastic DIP
MAX495CSA	0°C to +70°C	8 SO
MAX495CUA	0°C to +70°C	8 µMax**
MAX495C/D	0°C to +70°C	Dice*
MAX495EPA	-40°C to +85°C	8 Plastic DIP
MAX495ESA	-40°C to +85°C	8 SO
MAX495MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and specifications.*

____Pin Configurations (continued)

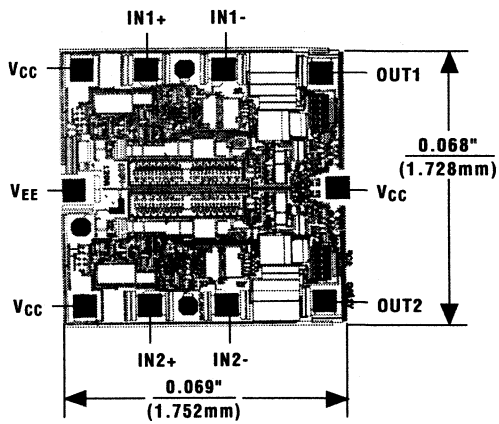
TOP VIEW



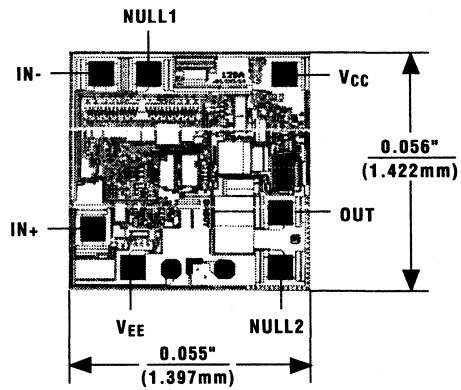
DIP/SO

_____Chip Topographies

MAX492



MAX495



TRANSISTOR COUNT: 134 (single MAX495)
268 (dual MAX492)
536 (quad MAX494)
SUBSTRATE CONNECTED TO V_{EE}

19-0157; Rev 1; 1/94

MAXIM

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

General Description

The MAX913 single and MAX912 dual high-speed, low-power comparators have differential inputs and complementary TTL outputs. Fast propagation delay (10ns typ), extremely low supply current, and a wide common-mode input range that includes the negative rail make the MAX912/MAX913 ideal for low-power, high-speed, single +5V (or ±5V) applications such as V/F converters or switching regulators.

The MAX912/MAX913 outputs remain stable through the linear region. This feature eliminates output instability common to high-speed comparators when driven with a slow-moving input signal.

The MAX912/MAX913 can be powered from a single +5V supply or a ±5V split supply. The MAX913 is an improved plug-in replacement for the LT1016. It provides significantly wider input voltage range **and** equivalent speed at a fraction of the power. The MAX912 dual comparator has equal performance to the MAX913 and includes independent latch controls.

Applications

Zero-Crossing Detectors
Ethernet Line Receivers
Switching Regulators
High-Speed Sampling Circuits
High-Speed Triggers
Extended Range V/F Converters
Fast Pulse Width/Height Discriminators

Features

- **Ultra Fast (10ns)**
- **Single +5V or Dual ±5V Supply Operation**
- **Input Range Extends Below Negative Supply**
- **Low Power: 6mA (+5V) Per Comparator**
- **No Minimum Input Signal Slew-Rate Requirement**
- **No Power-Supply Current Spiking**
- **Stable in the Linear Region**
- **Inputs Can Exceed Either Supply**
- **Low Offset Voltage: 0.8mV**

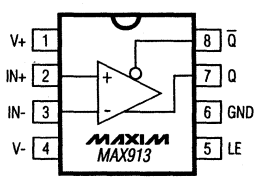
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX912CPE	0°C to +70°C	16 Plastic DIP
MAX912CSE	0°C to +70°C	16 Narrow SO
MAX912C/D	0°C to +70°C	Dice*
MAX912EPE	-40°C to +85°C	16 Plastic DIP
MAX912ESE	-40°C to +85°C	16 Narrow SO
MAX912MJE	-55°C to +125°C	16 CERDIP
MAX913CPA	0°C to +70°C	8 Plastic DIP
MAX913CSA	0°C to +70°C	8 SO
MAX913C/D	0°C to +70°C	Dice*
MAX913EPA	-40°C to +85°C	8 Plastic DIP
MAX913ESA	-40°C to +85°C	8 SO
MAX913MJA	-55°C to +125°C	8 CERDIP

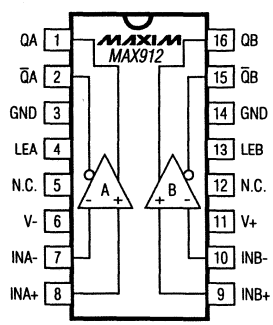
** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations

TOP VIEW



DIP/SO



DIP/Narrow SO

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage 7V
Negative Supply Voltage ..... -7V
Differential Input Voltage ..... ±15V
Input Voltage (Referred to V-) ..... - 0.3V to 15V
Latch Pin Voltage ..... Equal to Supplies
Continuous Output Current ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ... 696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges:
MAX91_ C_ _ ..... 0°C to +70°C
MAX91_ E_ _ ..... -40°C to +85°C
MAX91_ MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V+$ = +5V, $V-$ = -5V, V_Q = 1.4V, V_{LE} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1)	V_{OS}	$R_S \le 100\Omega$	T_A = +25°C		0.8	2	mV
			T_A = T_{MIN} to T_{MAX}			3	
Offset Drift	TCV_{OS}				2		µV/°C
Input Offset Current (Note 1)	I_{OS}		T_A = +25°C		0.3	0.5	µA
			T_A = T_{MIN} to T_{MAX}			0.8	
Input Bias Current	I_B		T_A = +25°C		3	5	µA
		C, E temp. ranges				8	
		M temp. range				10	
Input Voltage Range	V_{CM}	C, E temp. ranges		-5.2		+3.5	V
		M temp. range		-5.0		+3.5	
		Single +5V	C, E temp. ranges	-0.2		+3.5	
			M temp. range	0		+3.5	
Common-Mode Rejection Ratio	CMRR	$-5.0V \le V_{CM} \le +3.5V$		80	110		dB
Power-Supply Rejection Ratio	PSRR	Positive supply: $4.5V \le V+ \le 5.5V$		60	85		dB
		Negative supply: $-2V \ge V- \ge -7V$		80	100		
Small-Signal Voltage Gain	A_V	$1V \le V_Q \le 2V$, T_A = +25°C		1500	3500		V/V
Output Voltage	V_{OH}	$V+ \ge 4.5V$	I_{OUT} = 1mA	2.7	3.4		V
			I_{OUT} = 10mA	2.4	3.0		
	V_{OL}	I_{SINK} = 4mA			0.3	0.5	
		T_A = +25°C, I_{SINK} = 10mA			0.4		
Positive Supply Current Per Comparator	I+	C, E temp. ranges			6	10	mA
		M temp. range				12	
Negative Supply Current Per Comparator	I-				0.4	2	mA
Latch-Pin High Input Voltage	V_{IH}			2.0			V
Latch-Pin Low Input Voltage	V_{IL}					0.8	V
Latch-Pin Current	I_{IL}	V_{LE} = 0V				-20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V, V_Q = 1.4V, V_{LE} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Propagation Delay (Note 2)	t_{PD+}, t_{PD-}	ΔV_{IN} = 100mV, V_{OD} = 5mV	T_A = +25°C			10	14	ns
			T_A = T_{MIN} to T_{MAX}				16	
		ΔV_{IN} = 100mV, V_{OD} = 20mV	T_A = +25°C			9	12	
			T_A = T_{MIN} to T_{MAX}				15	
Differential Propagation Delay (Note 2)	Δt_{PD}	ΔV_{IN} = 100mV, V_{OD} = 5mV	T_A = +25°C	MAX913		2	3	ns
				MAX912		3	5	
Channel-to-Channel Propagation Delay (Note 2)		ΔV_{IN} = 100mV, V_{OD} = 5mV (MAX912 only)	T_A = +25°C			500		ps
Latch Setup Time (Note 3)	t_{SU}				2	0		ns
Latch Hold Time (Note 3)	t_H				3	2		ns
Latch Propagation Delay (Note 4)	t_{LPD}					7		ns

Note 1: Input Offset Voltage (V_{OS}) is defined as the average of the two input offset voltages, measured by forcing first one output, then the other to 1.4V. Input Offset Current (I_{OS}) is defined the same way.

Note 2: Propagation Delay (t_{PD}) and Differential Propagation Delay (Δt_{PD}) cannot be measured in automatic handling equipment with low input overdrive values. The MAX912/MAX913 are sample tested to 0.1% AQL with a 1V step and 500mV overdrive at +25°C only. Correlation tests show that t_{PD} and Δt_{PD} can be guaranteed with this test, if additional DC tests are performed to guarantee that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive. Differential Propagation Delay is defined as: $\Delta t_{PD} = t_{PD+} - t_{PD-}$.

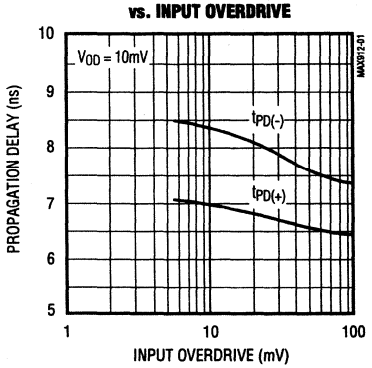
Note 3: Input latch setup time (t_{SU}) is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time (t_H) is the interval after the latch is asserted in which the input signal must be stable. These parameters are guaranteed by design.

Note 4: Latch Propagation Delay (t_{LPD}) is the delay time for the output to respond when the latch-enable pin is deasserted. See Timing Diagram.

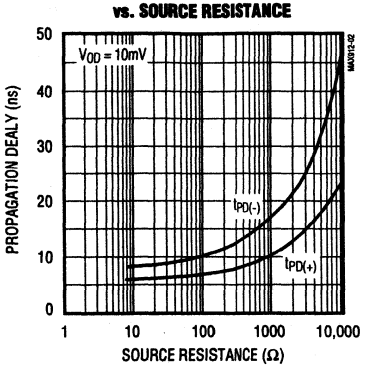
Typical Operating Characteristics

(V+ = 5V, V- = -5V, V_{LE} = 0V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

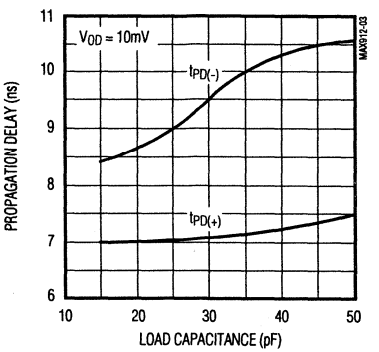
PROPAGATION DELAY vs. INPUT OVERDRIVE



PROPAGATION DELAY vs. SOURCE RESISTANCE



PROPAGATION DELAY vs. LOAD CAPACITANCE

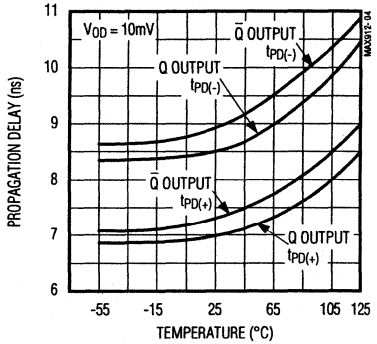


Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

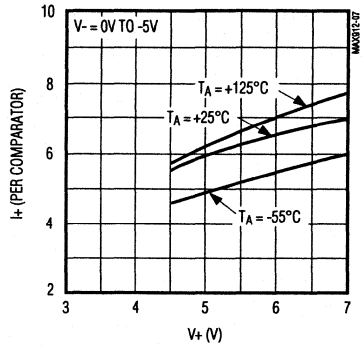
Typical Operating Characteristics (continued)

(V+ = 5V, V- = -5V, V_{LE} = 0V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

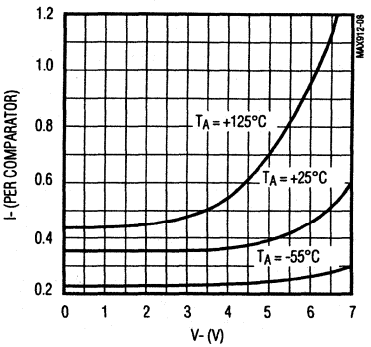
PROPAGATION DELAY vs. TEMPERATURE



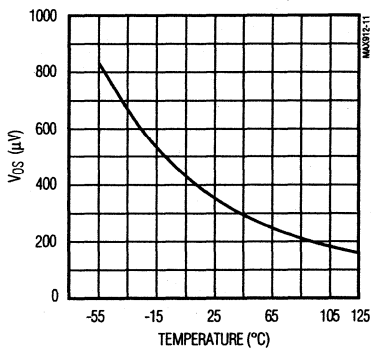
POSITIVE SUPPLY CURRENT (PER COMPARATOR) vs. POSTIVE SUPPLY VOLTAGE



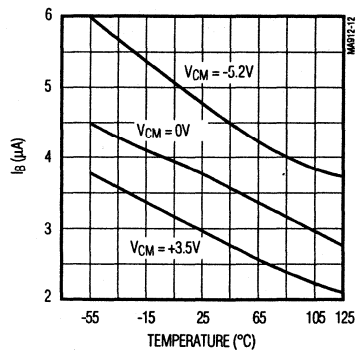
NEGATIVE SUPPLY CURRENT (PER COMPARATOR) vs. NEGATIVE SUPPLY VOLTAGE



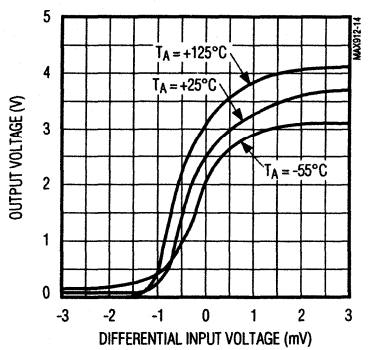
OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. TEMPERATURE



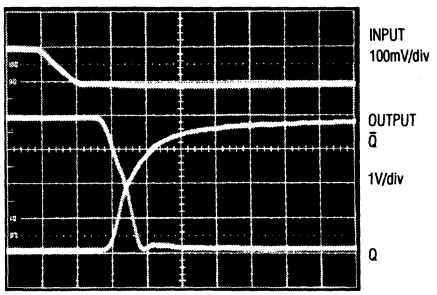
OUTPUT VOLTAGE vs. DIFFERENTIAL INPUT VOLTAGE



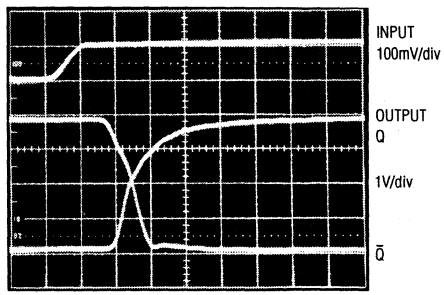
Typical Operating Characteristics (continued)

(V+ = 5V, V- = -5V, V_{LE} = 0V, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

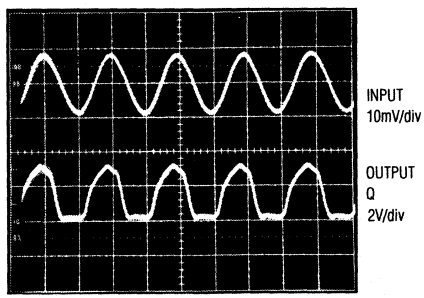
POSITIVE-TO-NEGATIVE PROPAGATION DELAY



NEGATIVE-TO-POSITIVE PROPAGATION DELAY

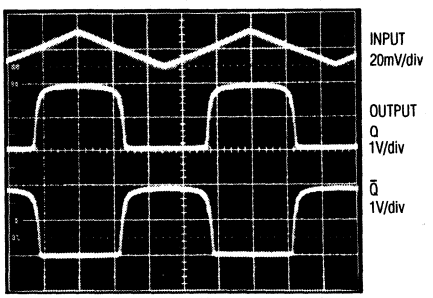


MAX912/MAX913 RESPONSE TO 50MHz (±10mV$_{P-P}$) SINE WAVE

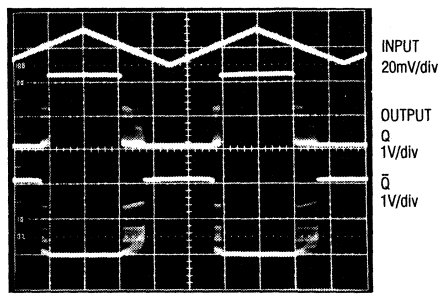


MAX912/MAX913 RESPONSE TO SLOW-MOVING TRIANGLE WAVE

MAX912/MAX913 RESPONSE



INDUSTRY STANDARD 686 RESPONSE



Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

Pin Descriptions

PIN MAX912	NAME	FUNCTION
1	QA	Comparator A TTL output
2	$\overline{Q}$A	Comparator A complementary TTL output
3, 14	GND	Logic ground. Connect **both** GND pins to ground.
4	LEA	Comparator A latch enable. QA and $\overline{Q}$A are latched when LEA is high or floating. Comparator A latch is transparent when LEA is low.
5, 12	N.C.	Not internally connected
6	V-	Negative power supply: -5V for dual supplies (bypass to GND with a 0.1µF capacitor), or GND for a single supply
7	INA-	Comparator A inverting input
8	INA+	Comparator A noninverting input
9	INB+	Comparator B noninverting input
10	INB-	Comparator B inverting input
11	V+	Positive power supply, +5V. Bypass to GND with a 0.1µF capacitor.
13	LEB	Comparator B latch enable. QB and $\overline{Q}$B are latched when LEB is high or floating. Comparator B latch is transparent when LEB is low.
15	$\overline{Q}$B	Comparator B complementary TTL output
16	QB	Comparator B TTL output

PIN MAX913	NAME	FUNCTION
1	V+	Positive power supply. Bypass to GND with a 0.1µF capacitor.
2	IN+	Noninverting input
3	IN-	Inverting input
4	V-	Negative power supply: -5V for dual supplies (bypass to GND with a 0.1µF capacitor), or GND for a single supply
5	LE	Latch enable. Q and $\overline{Q}$ are latched when LE is TTL high or floating. The comparator latch is transparent when LE is low.
6	GND	Logic ground
7	Q	TTL output
8	$\overline{Q}$	Complementary TTL output

Detailed Description

The MAX913 (single) and MAX912 (dual) high-speed comparators have a unique design that prevents oscillation when the comparator is in its linear region. No minimum input slew rate is required.

Many high-speed comparators oscillate in the linear region, as shown in the *Typical Operating Characteristics'* industry-standard 686 response graph. One way to overcome this oscillation is to sample the output after it has passed through the unstable region. Another practical solution is to add hysteresis. Either solution results in a loss of resolution and bandwidth.

Because the MAX912/MAX913 do not need hysteresis, they offer high resolution to all signals—including low-frequency signals.

The MAX912/MAX913 provide a TTL-compatible latch function that holds the comparator output state (Figure 1). As long as Latch Enable (LE) is high or floating, the input signal has no effect on the output state. With LE low, the outputs are controlled by the input differential voltage and the latch is transparent.

Input Amplifier

A comparator can be thought of as having two sections: an input amplifier and a logic interface. The MAX912/MAX913's input amplifier is fully differential, with input offset voltage trimmed to below 2.0mV at +25°C. Input common-mode range extends from 200mV **below** the negative supply rail to 1.5V below the positive power supply. The total common-mode range is 8.7V when operating from ±5VDC supplies.

The MAX912/MAX913's amplifier has no built-in hysteresis. For highest accuracy, do not add hysteresis. Figure 2 shows how hysteresis degrades resolution.

Resolution

A comparator's ability to resolve small signal differences—its resolution—is affected by various factors. As with most amplifiers, the most significant factors are the input offset voltage (V_{OS}) and the common-mode and power-supply rejection ratios (CMRR, PSRR). If source impedance is high, input offset current can be significant. If source impedance is unbalanced, the input bias current can introduce another error.

For high-speed comparators, an additional factor in resolution is the comparator's stability in its linear region. Many high-speed comparators are useless in their linear region because they oscillate. This makes the differential input voltage region around 0V unusable, as does a high V_{OS}. Hysteresis does not cure the problem, but acts to keep the input away from its linear range (Figure 2).

The MAX912/MAX913 do not oscillate in the linear region, which greatly enhances the comparator's resolution.

Applications Information

Power Supplies and Bypassing

The MAX912/MAX913 are tested with ±5V power supplies that provide an input common-mode range (V_{CM}) of 8.7V (-5.2V to +3.5V). Operation from a single +5V supply provides a common-mode input range of 3.7V (-0.2V to +3.5V). Connect V- to GND for single-supply operation. The MAX912/MAX913 will operate from a minimum single-supply voltage of +4.5V.

The V+ supply provides power to both the analog input stage and digital output circuits, whereas the V- supply only powers the analog section. Bypass V+ and V- to ground with 0.1µF to 1.0µF ceramic capacitors in parallel with 10µF or greater tantalum capacitors. Connect the ceramic capacitors very close to the MAX912/MAX913's

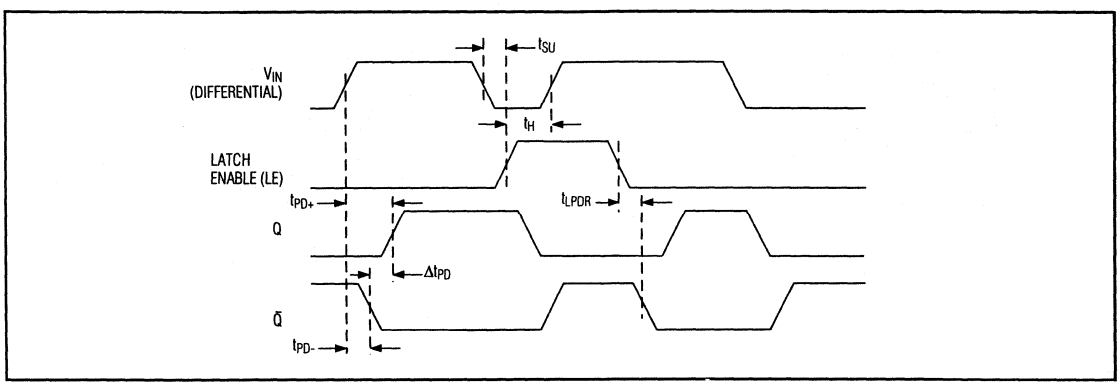


Figure 1. Timing Diagram

Single/Dual, Ultra-Fast, Low-Power, Precision TTL Comparators

supply pins, keeping leads short to minimize lead inductance. For particularly noisy applications, use ferrite beads on the power-supply lines.

Board Layout

As with all high-speed components, careful attention to layout is essential for best performance.

1) Use a printed circuit board with an unbroken ground plane.
2) Pay close attention to the bandwidth of bypass components and keep leads short.
3) Avoid sockets; solder the comparator and other components directly to the board to minimize unwanted parasitic inductance and capacitance.

Input Slew Rate

The MAX912/MAX913 design eliminates the input slew-rate requirement imposed on many standard comparators. As long as LE is high after the maximum propagation delay and the input is greater than the comparator's total DC error, the output will be valid without oscillations.

Maximum Clock (LE) and Signal Rate

The maximum clock and signal rate is 70MHz, based on the comparator's rise and fall time with a 5mV overdrive at +25°C (Figure 1). With a 20mV overdrive, the maximum propagation delay is 12ns and the clock and signal rate is 85MHz.

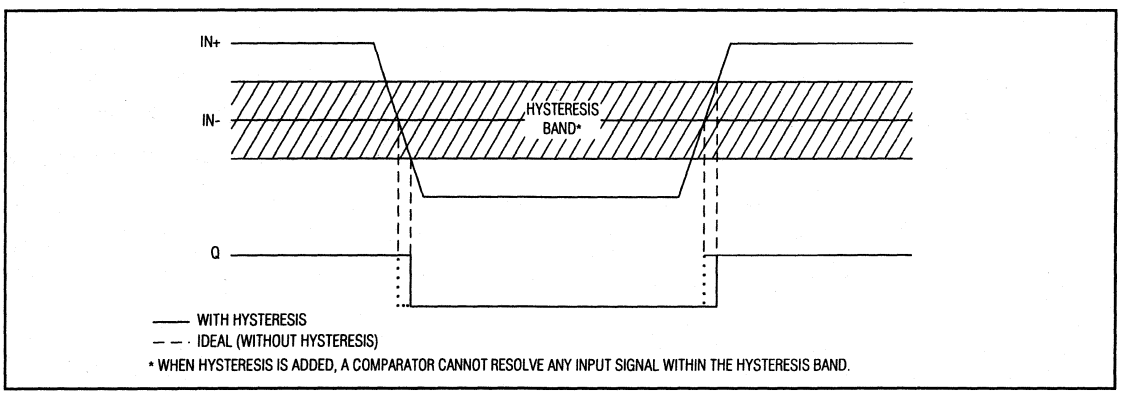
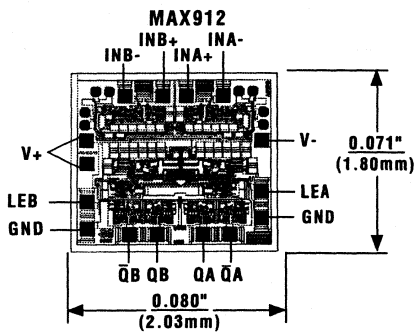
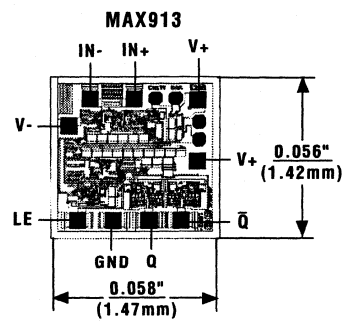


Figure 2. Effect of Hysteresis on Input Resolution

Chip Topographies



TRANSISTOR COUNT: 197;
SUBSTRATE CONNECTED TO V-.



TRANSISTOR COUNT: 100;
SUBSTRATE CONNECTED TO V-.

19-0194; Rev 0; 10/93

MAXIM

Ultra Low-Power, Low-Cost Comparators with 2% Reference

General Description

The MAX931-MAX934 single, dual, and quad micropower, low-voltage comparators plus an on-board 2% accurate reference feature the lowest power consumption available. These comparators draw less than 4µA supply current over temperature (MAX931), and include an internal 1.182V ±2% voltage reference, programmable hysteresis, and TTL/CMOS outputs that sink and source current.

Ideal for 3V or 5V single-supply applications, the MAX931-MAX934 operate from a single +2.5V to +11V supply (or a ±1.25V to ±5V dual supply), and each comparator's input voltage range extends from the negative supply rail to within 1.3V of the positive supply.

The MAX931-MAX934's unique output stage continuously sources as much as 40mA. And by eliminating power-supply glitches that commonly occur when comparators change logic states, the MAX931-MAX934 minimize parasitic feedback, which makes them easier to use.

The single MAX931 and dual MAX932/MAX933 provide a unique and simple method for adding hysteresis without feedback and complicated equations, using the HYST pin and two resistors.

For applications that require increased precision with similar power requirements, see the MAX921-MAX924 data sheet. These devices include a 1% precision reference.

PART	INTERNAL 2% REFERENCE	COMPARATORS PER PACKAGE	INTERNAL HYSTERESIS	PACK-AGE
MAX931	Yes	1	Yes	8-Pin DIP/SO
MAX932	Yes	2	Yes	8-Pin DIP/SO
MAX933	Yes	2	Yes	8-Pin DIP/SO
MAX934	Yes	4	No	16-Pin DIP/SO

Applications

Battery-Powered Systems
Threshold Detectors
Window Comparators
Oscillator Circuits
Alarm Circuits

Features

- ♦ **Ultra-Low 4µA Max Quiescent Current Over Extended Temp. Range (MAX931)**
- ♦ **Power Supplies:**
  Single +2.5V to +11V
  Dual ±1.25V to ±5.5V
- ♦ **Input Voltage Range Includes Negative Supply**
- ♦ **Internal 1.182V ±2% Bandgap Reference**
- ♦ **Adjustable Hysteresis**
- ♦ **TTL-/CMOS-Compatible Outputs**
- ♦ **12µs Propagation Delay (10mV Overdrive)**
- ♦ **No Switching Crowbar Current**
- ♦ **40mA Continuous Source Current**

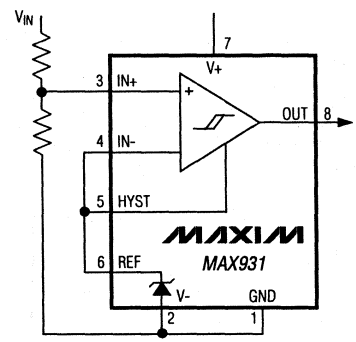
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX931CPA	0°C to +70°C	8 Plastic DIP
MAX931CSA	0°C to +70°C	8 SO
MAX931EPA	-40°C to +85°C	8 Plastic DIP
MAX931ESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

For similar devices guaranteed over the military temp. range, see the MAX921-MAX924 data sheet. The MAX931, MAX933, and MAX934 are pin-compatible with the 1% accurate MAX921, MAX923, and MAX924, respectively. The MAX932 and MAX922 are not pin-compatible.

Typical Operating Circuit



THRESHOLD DETECTOR

Ultra Low-Power, Low-Cost Comparators with 2% Reference

ABSOLUTE MAXIMUM RATINGS

V+ to V-, V+ to GND, GND to V-.....-0.3V, +12V
Inputs
  Current, IN_+, IN_-, HYST.....20mA
  Voltage, IN_+, IN_-, HYST.....(V+ + 0.3V) to (V- – 0.3V)
Outputs
  Current, REF.....20mA
  Current, OUT_.....50mA
  Voltage, REF .....(V+ + 0.3V) to (V- – 0.3V)
  Voltage, OUT_ (MAX931/934) .....(V+ + 0.3V) to (GND – 0.3V)
  Voltage, OUT_ (MAX932/933).....(V+ + 0.3V) to (V- – 0.3V)
  OUT_ Short-Circuit Duration (V+ ≤ 5.5V) .....Continuous

Continuous Power Dissipation (T_A = +70°C)
  8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ...727mW
  8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
  16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)..842mW
  16-Pin SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Ranges:
  MAX93_C_ _ .....0°C to +70°C
  MAX93_E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—5V Operation

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage Range	(Note 1)			2.5		11	V
Supply Current	IN+ = IN- + 100mV	MAX931, HYST = REF	T_A = +25°C		2.5	3.2	µA
			C/E temp. ranges			4	
		MAX932, HYST = REF	T_A = +25°C		3.1	4.5	
			C/E temp. ranges			6	
		MAX933, HYST = REF	T_A = +25°C		3.1	4.5	
			C/E temp. ranges			6	
		MAX934	T_A = +25°C		5.5	6.5	
			C/E temp. ranges			8.5	
COMPARATOR							
Input Offset Voltage	V_{CM} = 2.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 2.5V, C/E temp. ranges						nA
Input Leakage Current (HYST)	MAX931, MAX932, MAX933				±0.02		nA
Input Common-Mode Voltage Range				V-		V+ – 1.3	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)				0.1	1.0	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V				0.1	1.0	mV/V
Voltage Noise	100Hz to 100kHz				20		$µV_{RMS}$
Hysteresis Input Voltage Range	MAX931, MAX932, MAX933			REF – 0.05		REF	V
Response Time	T_A = +25°C, 100pF load		Overdrive = 10mV		12		µs
			Overdrive = 100mV		4		

ELECTRICAL CHARACTERISTICS—5V Operation (continued)

(V+ = 5V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output High Voltage	C/E temp. ranges, I_{OUT} = 17mA		V+ – 0.4			V
Output Low Voltage	C/E temp. ranges, I_{OUT} = 1.8mA	MAX932, MAX933			V- + 0.4	V
		MAX931, MAX934			GND + 0.4	
REFERENCE						
Reference Voltage	C temp. range		1.158	1.182	1.206	V
	E temp. range		1.147		1.217	
Source Current	T_A = +25°C		15	25		µA
	C/E temp. ranges		6			
Sink Current	T_A = +25°C		8	15		µA
	C/E temp. ranges		4			
Voltage Noise	100Hz to 100kHz			100		μV_{RMS}

Note 1: MAX934 comparators work below 2.5V, see *Low-Voltage Operation* section for more details.

ELECTRICAL CHARACTERISTICS—3V Operation

(V+ = 3V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Current	IN+ = (IN- + 100mV)	MAX931, HYST=REF	T_A = +25°C		2.4	3.0	µA
			C/E temp. ranges			3.8	
		MAX932, HYST=REF	T_A = +25°C		3.4	4.3	
			C/E temp. ranges			5.8	
		MAX933, HYST=REF	T_A = +25°C		3.4	4.3	
			C/E temp. ranges			5.8	
		MAX934	T_A = +25°C		5.2	6.2	
			C/E temp. ranges			8.0	
COMPARATOR							
Input Offset Voltage	V_{CM} = 1.5V					±10	mV
Input Leakage Current (IN-, IN+)	IN+ = IN- = 1.5V, C/E temp. ranges				±0.01	±1	nA
Input Leakage Current (HYST)	MAX931, MAX932, MAX933				±0.02		nA

Ultra Low-Power, Low-Cost Comparators with 2% Reference

ELECTRICAL CHARACTERISTICS—3V Operation (continued)

(V+ = 3V, V- = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

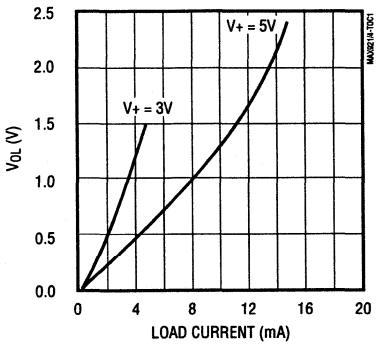
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range			V-		V+ – 1.3	V
Common-Mode Rejection Ratio	V- to (V+ – 1.3V)			0.2	1	mV/V
Power-Supply Rejection Ratio	V+ = 2.5V to 11V			0.1	1	mV/V
Voltage Noise	100Hz to 100kHz			20		μV_{RMS}
Hysteresis Input Voltage Range	MAX931, MAX932, MAX933		REF – 0.05		REF	V
Response Time	T_A = +25°C, 100pF load	Overdrive = 10mV		14		µs
		Overdrive = 100mV		5		
Output High Voltage	C/E temp. ranges, I_{OUT} = 10mA		V+ – 0.4			V
Output Low Voltage	C/E temp. ranges, I_{OUT} = 0.8mA	MAX932, MAX933			V- + 0.4	V
		MAX931			GND + 0.4	
REFERENCE						
Reference Voltage	C temp. range		1.158	1.182	1.206	V
	E temp. range		1.147		1.217	
Source Current	T_A = +25°C		15	25		µA
	C/E temp. ranges		6			
Sink Current	T_A = +25°C		8	15		µA
	C/E temp. ranges		4			
Voltage Noise	100Hz to 100kHz			100		μV_{RMS}

Ultra Low-Power, Low-Cost Comparators with 2% Reference

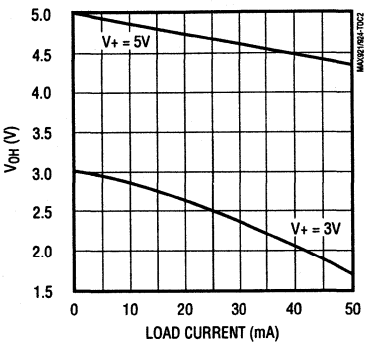
Typical Operating Characteristics

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted.)

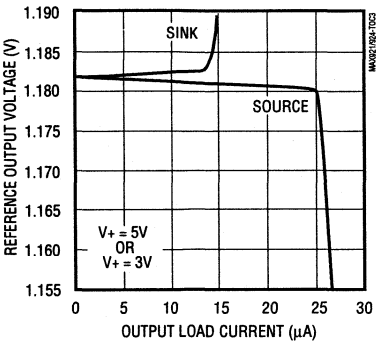
OUTPUT VOLTAGE LOW vs. LOAD CURRENT



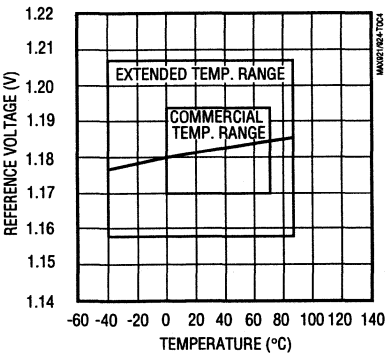
OUTPUT VOLTAGE HIGH vs. LOAD CURRENT



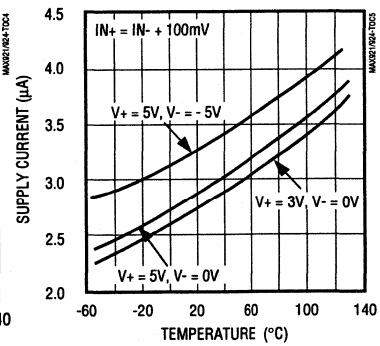
REFERENCE OUTPUT VOLTAGE vs. OUTPUT LOAD CURRENT



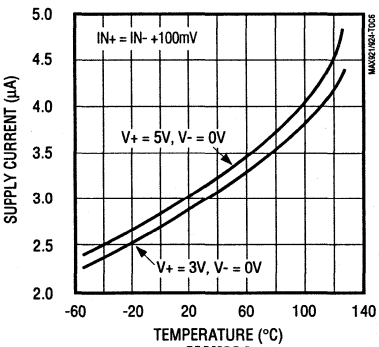
REFERENCE VOLTAGE vs. TEMPERATURE



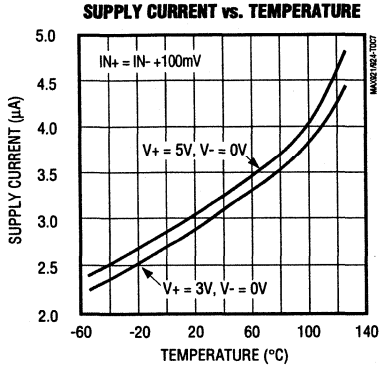
MAX931 SUPPLY CURRENT vs. TEMPERATURE



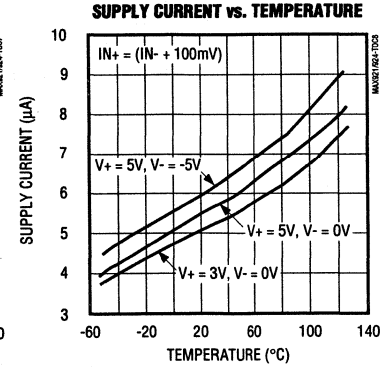
MAX932 SUPPLY CURRENT vs. TEMPERATURE



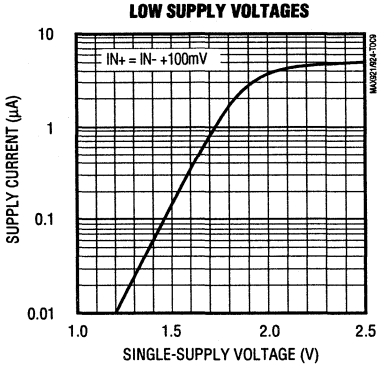
MAX933 SUPPLY CURRENT vs. TEMPERATURE



MAX934 SUPPLY CURRENT vs. TEMPERATURE



MAX934 SUPPLY CURRENT vs. LOW SUPPLY VOLTAGES

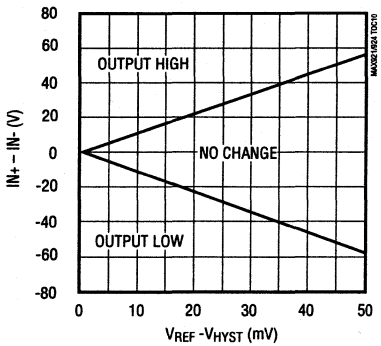


Ultra Low-Power, Low-Cost Comparators with 2% Reference

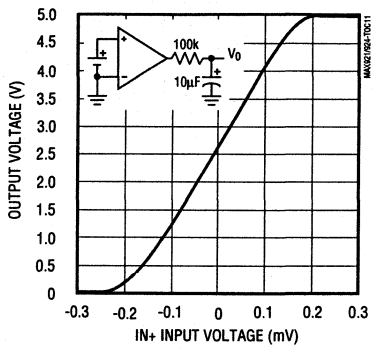
Typical Operating Characteristics (continued)

(V+ = 5V, V- = GND, T_A = +25°C, unless otherwise noted.)

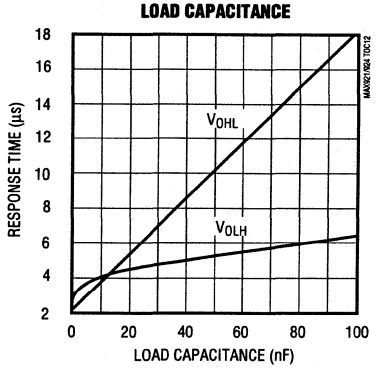
HYSTERESIS CONTROL



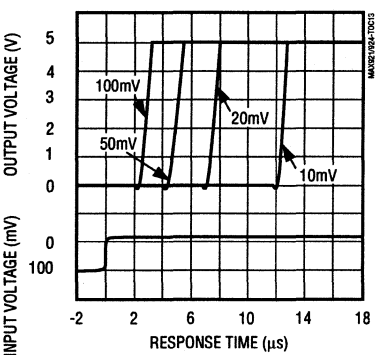
TRANSFER FUNCTION



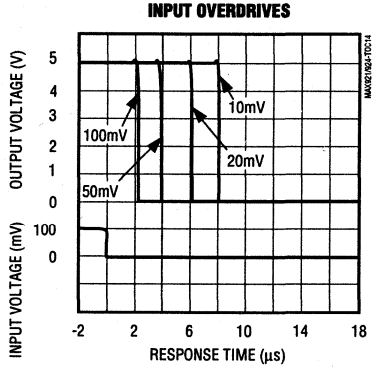
RESPONSE TIME vs. LOAD CAPACITANCE



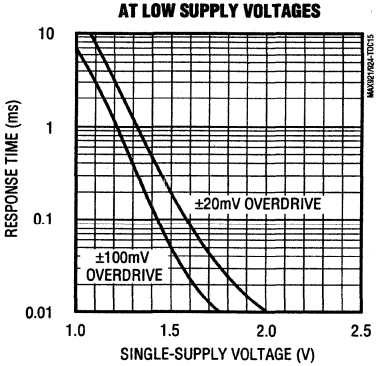
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



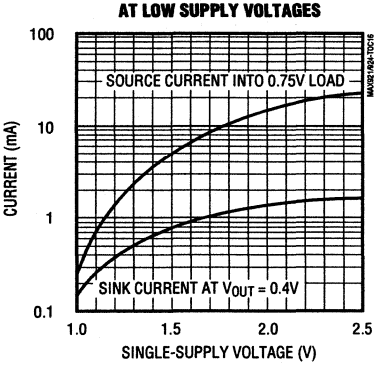
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



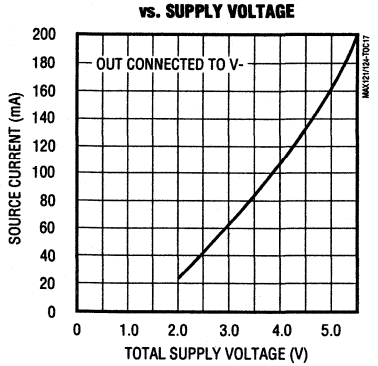
MAX934 RESPONSE TIME AT LOW SUPPLY VOLTAGES



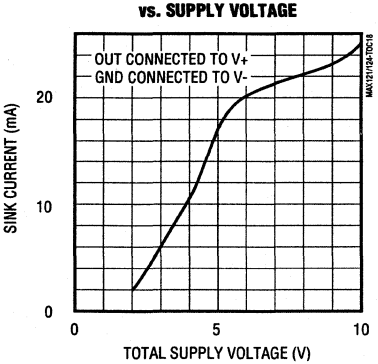
MAX934 OUTPUT DRIVE AT LOW SUPPLY VOLTAGES



SHORT-CIRCUIT SOURCE CURRENT vs. SUPPLY VOLTAGE



SHORT-CIRCUIT SINK CURRENT vs. SUPPLY VOLTAGE



Pin Descriptions

PIN			NAME	FUNCTION
MAX931	MAX932	MAX933		
1	–	–	GND	Ground. Connect to V- for single-supply operation. Output swings from V+ to GND.
–	1	1	OUTA	Comparator A output. Sinks and sources current. Swings from V+ to V-.
2	2	2	V-	Negative supply. Connect to ground for single-supply operation (MAX931).
3	–	–	IN+	Noninverting comparator input
–	3	3	INA+	Noninverting input of comparator A
4	–	–	IN-	Inverting comparator input
–	4	–	INB+	Noninverting input of comparator B
–	–	4	INB-	Inverting input of comparator B
5	5	5	HYST	Hysteresis input. Connect to REF if not used. Input voltage range is from V_{REF} to V_{REF} - 50mV.
6	6	6	REF	Reference output. 1.182V with respect to V-.
7	7	7	V+	Positive supply
8	–	–	OUT	Comparator output. Sinks and sources current. Swings from V+ to GND.
–	8	8	OUTB	Comparator B output. Sinks and sources current. Swings from V+ to V-.

PIN	NAME	FUNCTION
MAX934		
1	OUTB	Comparator B output. Sinks and sources current. Swings from V+ to GND.
2	OUTA	Comparator A output. Sinks and sources current. Swings from V+ to GND.
3	V+	Positive supply
4	INA-	Inverting input of comparator A
5	INA+	Noninverting input of comparator A
6	INB-	Inverting input of comparator B
7	INB+	Noninverting input of comparator B
8	REF	Reference output. 1.182V with respect to V-.
9	V-	Negative supply. Connect to ground for single-supply operation.
10	INC-	Inverting input of comparator C
11	INC+	Noninverting input of comparator C
12	IND-	Inverting input of comparator D
13	IND+	Noninverting input of comparator D
14	GND	Ground. Connect to V- for single-supply operation.
15	OUTD	Comparator D output. Sinks and sources current. Swings from V+ to GND.
16	OUTC	Comparator C output. Sinks and sources current. Swings from V+ to GND.

Ultra Low-Power, Low-Cost Comparators with 2% Reference

Detailed Description

The MAX931-MAX934 comprise various combinations of a micropower 1.182V reference and a micropower comparator. The *Typical Operating Circuit* shows the MAX931 configuration, and Figures 1a-1c show the MAX932/MAX933/MAX934 configurations.

Each comparator continuously sources up to 40mA, and the unique output stage eliminates crowbar glitches during output transitions. This makes them immune to parasitic feedback (which can cause instability) and provides excellent performance, even when circuit-board layout is not optimal.

Internal hysteresis in the MAX931/MAX932/MAX933 provides the easiest method for implementing hysteresis. It also produces faster hysteresis action and consumes much less current than circuits using external positive feedback.

Power-Supply and Input Signal Ranges

This family of devices operates from a single +2.5V to +11V power supply. The MAX931 and MAX934 have a separate ground for the output driver, allowing operation with dual supplies ranging from ±1.25V to ±5.5V. Connect V- to GND when operating the MAX931 and the MAX934 from a single supply. The maximum supply voltage in this case is still 11V.

For proper comparator operation, the input signal can be driven from the negative supply (V-) to within one volt of the positive supply (V+ - 1V). The guaranteed common-mode input voltage range extends from V- to (V+ - 1.3V). The inputs can be taken above and below the supply rails by up to 300mV without damage.

Operating the MAX931 and MAX934 at ±5V provides TTL/CMOS compatibility when monitoring bipolar input signals. TTL compatibility for the MAX932 and MAX933 is achieved by operation from a single +5V supply.

Low-Voltage Operation: V+ = 1V (MAX934 Only)

The guaranteed minimum operating voltage is 2.5V (or ±1.25V). As the total supply voltage is reduced below 2.5V, the performance degrades and the supply

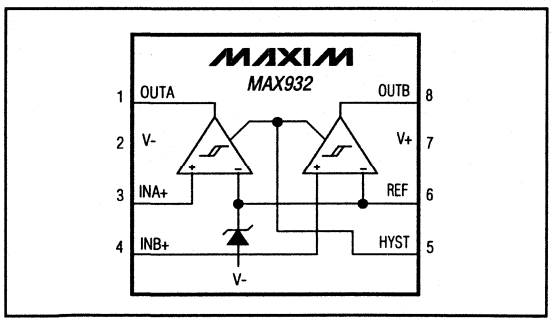


Figure 1a. MAX932 Functional Diagram

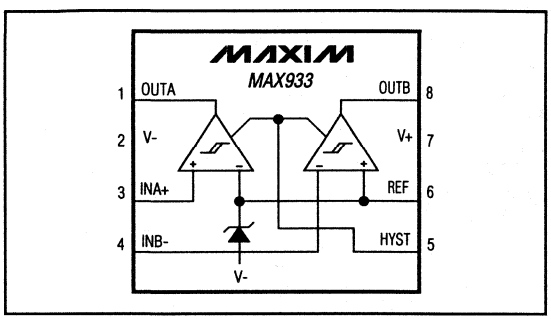


Figure 1b. MAX933 Functional Diagram

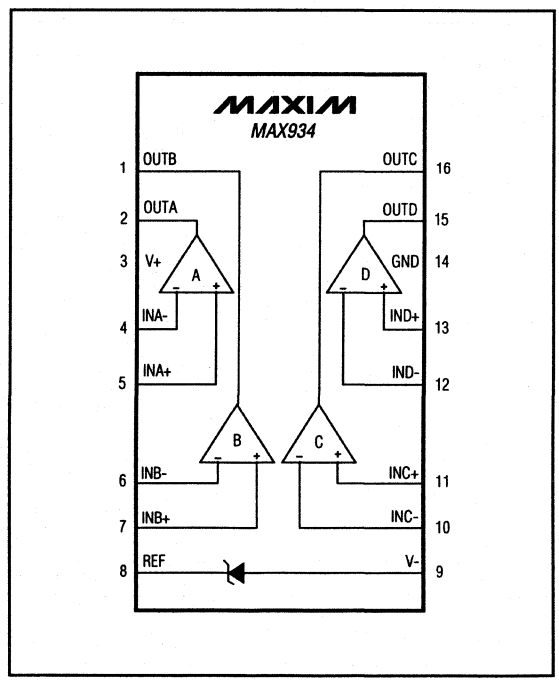


Figure 1c. MAX934 Functional Diagram

current falls. The reference will not function below about 2.2V, although the comparators will continue to operate with a total supply voltage as low as 1V. While the MAX934 has comparators that may be used at supply voltages below 2V, the MAX931, MAX932, and MAX933 may not be used with supply voltages significantly below 2.5V.

At low supply voltages, the comparators' output drive is reduced and the propagation delay increases (see *Typical Operating Characteristics*). The useful input voltage range extends from the negative supply to a little under 1V below the positive supply, which is slightly closer to the positive rail than the device operating from higher supply voltages. Test your prototype over the full temperature and supply-voltage range if operation below 2.5V is anticipated.

Comparator Output

With 100mV of overdrive, propagation delay is typically 3µs. The *Typical Operating Characteristics* show the propagation delay for various overdrive levels.

The MAX931 and MAX934 output swings from V+ to GND, so TTL compatibility is assured by using a +5V ±10% supply. The negative supply does not affect the output swing, and can range from 0V to -5V ±10%.

The MAX932 and MAX933 do not have a GND pin, and their outputs swing from V+ to V-. Connect V- to ground and V+ to a +5V supply to achieve TTL compatibility.

The MAX931-MAX934's unique design achieves an output source current of more than 40mA and a sink current of over 5mA, while keeping quiescent currents in the microampere range. The output can source 100mA (at V+ = 5V) for short pulses, as long as the package's maximum power dissipation is not exceeded. The output stage does not generate crowbar switching currents during transitions, which minimizes feedback through the supplies and helps ensure stability without bypassing.

Voltage Reference

The internal bandgap voltage reference has an output of 1.182V above V-. Note that the REF voltage is referenced to V-, not to GND. Its accuracy is ±2% in the range 0°C to +70°C. The REF output is typically capable of sourcing 15µA and sinking 8µA. Do not bypass the REF output. For applications that require a 1% precision reference, see the MAX921-MAX924 data sheet.

Noise Considerations

Although the comparators have a very high gain, useful gain is limited by noise. This is shown in the Transfer Function graph (see *Typical Operating Characteristics*). As the input voltage approaches the comparator's offset, the output begins to bounce back and forth; this peaks when $V_{IN} = V_{OS}$. (The lowpass filter shown on the graph averages out the bouncing, making the transfer function easy to observe.) Consequently, the comparator has an effective wideband peak-to-peak noise of around 0.3mV. The voltage reference has peak-to peak noise approaching 1mV. Thus, when a comparator is used with the reference, the combined peak-to-peak noise is about 1mV. This, of course, is much higher than the RMS noise of the individual components. Care should be taken in the layout to avoid capacitive coupling from any output to the reference pin. Crosstalk can significantly increase the actual noise of the reference.

Applications Information

Hysteresis

Hysteresis increases the comparators' noise margin by increasing the upper threshold and decreasing the lower threshold (see Figure 2).

Hysteresis (MAX931/MAX932/MAX933)

To add hysteresis to the MAX931/MAX932/MAX933, connect resistor R1 between REF and HYST, and connect resistor R2 between HYST and V- (Figure 3). If no hysteresis is required, connect HYST to REF. When hysteresis is added, the upper threshold increases by the same amount that the lower threshold decreases. The hysteresis band (the difference between the upper and lower thresholds, V_{HB}) is approximately equal to twice the voltage between REF and HYST. The HYST input can be adjusted to a maximum voltage of REF and to a minimum voltage of (REF - 50mV). The

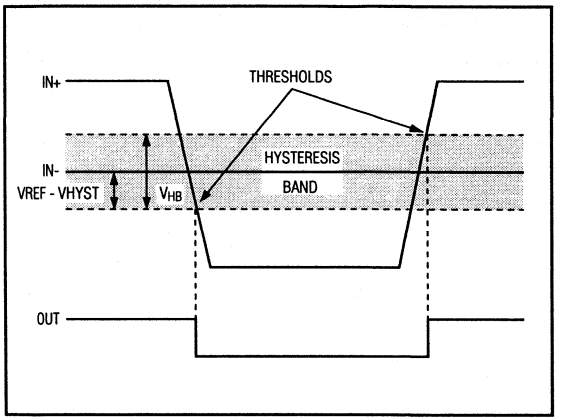


Figure 2. Threshold Hysteresis Band

Ultra Low-Power, Low-Cost Comparators with 2% Reference

maximum difference between REF and HYST (50mV) will therefore produce a 100mV max hysteresis band. Use the following equations to determine R1 and R2:

$$R1 = \frac{V_{HB}}{(2 \times I_{REF})}$$

$$R2 = \frac{\left(1.182 - \frac{V_{HB}}{2}\right)}{I_{REF}}$$

Where I_{REF} (the current sourced by the reference) should not exceed the REF source capability, and should be significantly larger than the HYST input current. I_{REF} values between 0.1µA and 4µA are usually appropriate. If 2.4MΩ is chosen for R2 (I_{REF} = 0.5µA), the equation for R1 and V_{HB} can be approximated as:

$$R1\ (k\Omega) = V_{HB}(mV)$$

When hysteresis is obtained in this manner for the MAX932/MAX933, the same hysteresis applies to both comparators.

Hysteresis (MAX934)

Hysteresis can be set with two resistors using positive feedback, as shown in Figure 4. This circuit generally draws more current than the circuits using the HYST pin on the MAX931/MAX932/MAX933, and the high feedback impedance slows hysteresis. The design procedure is as follows:

1. Choose R3. The leakage current of IN+ is under 1nA (up to +85°C), so the current through R3 can be around 100nA and still maintain good accuracy. The current through R3 at the trip point is V_{REF}/R3, or 100nA for R3 = 11.8MΩ. 10MΩ is a good practical value.
2. Choose the hysteresis voltage (V_{HB}), the voltage between the upper and lower thresholds. In this example, choose V_{HB} = 50mV.
3. Calculate R1.

$$R1 = R3 \times \frac{V_{HB}}{V+}$$

$$= 10M \times \frac{0.05}{5}$$

$$= 100k\Omega$$

4. Choose the threshold voltage for V_{IN} rising (V_{THR}). In this example, choose V_{THR} = 3V.
5. Calculate R2.

$$R2 = \frac{1}{\left[\left(\frac{V_{THR}}{(V_{REF} \times R1)}\right) - \frac{1}{R1} - \frac{1}{R3}\right]}$$

$$= \frac{1}{\left[\left(\frac{3}{(1.182 \times 100k)}\right) - \frac{1}{100k} - \frac{1}{10M}\right]}$$

$$= 65.44k\Omega$$

A 1% preferred value is 64.9kΩ.

6. Verify the threshold voltages with these formulas:

V_{IN} rising:

$$V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - \frac{(R1 \times V+)}{R3}$$

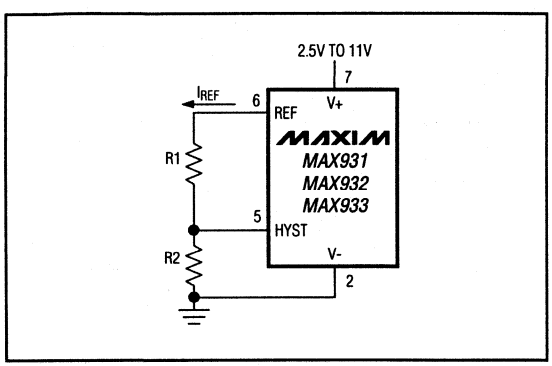


Figure 3. Programming the HYST Pin

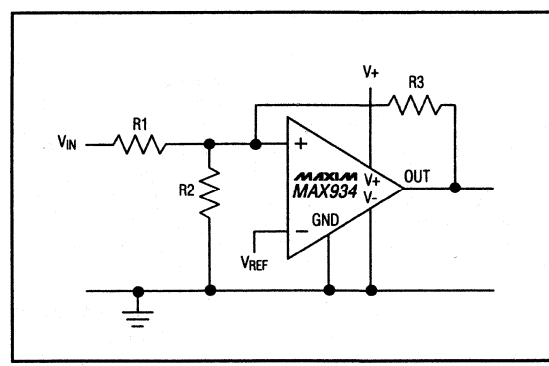


Figure 4. External Hysteresis

Board Layout and Bypassing

Power-supply bypass capacitors are not needed if the supply impedance is low, but 100nF bypass capacitors should be used when the supply impedance is high or when the supply leads are long. Minimize signal lead lengths to reduce stray capacitance between the input and output that might cause instability. Do not bypass the reference output.

Typical Applications

Auto-Off Power Source

Figure 5 shows the schematic for a 40mA power supply that has a timed auto power-off function. The comparator output is the switched power-supply output. With a 10mA load, it typically provides a voltage of (V_{BATT} - 0.12V), but draws only 3.5µA quiescent current. This circuit takes advantage of the four key features of the MAX931: 2.5µA supply current, an internal reference, hysteresis, and high current output. Using the component values shown, the three-resistor voltage divider programs the maximum ±50mV of hysteresis and sets the IN- voltage at 100mV. This gives an IN+ trip threshold of approximately 50mV for IN+ falling.

The RC time constant determines the maximum power-on time of the OUT pin before power-down occurs. This period can be approximated by:

R x C x 4.6sec

For example: 2MΩ x 10µF x 4.6 = 92sec. The actual time will vary with both the leakage current of the capacitor and the voltage applied to the circuit.

Window Detector

The MAX933 is ideal for making window detectors (undervoltage/overvoltage detectors). The schematic is shown in Figure 6, with component values selected for an 4.5V undervoltage threshold, and a 5.5V overvoltage threshold. Choose different thresholds by changing the values of R1, R2, and R3. To prevent chatter at the output when the supply voltage is close to a threshold, hysteresis has been added using R4 and R5. OUTA provides an active-low undervoltage indication, and OUTB gives an active-low overvoltage indication. ANDing the two outputs provides an active-high, power-good signal.

The design procedure is as follows:

1. Choose the required hysteresis level and calculate values for R4 and R5 according to the formulas in the *Hysteresis (MAX931/MAX932/MAX933)* section. In this example, ±5mV of hysteresis has been added *at the comparator input* ($V_H = V_{HB}/2$). This means that the hysteresis apparent at V_{IN} will be larger because of the input resistor divider.
2. Select R1. The leakage current into INB- is normally under 1nA, so the current through R1 should exceed

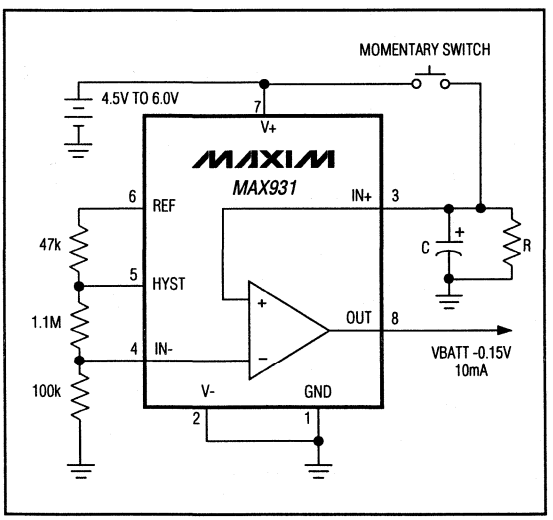


Figure 5. Auto-off power switch operates on 2.5µA quiescent current.

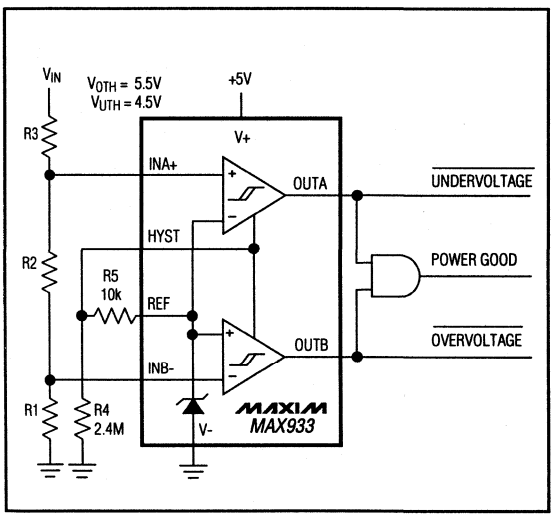


Figure 6. Window Detector

Ultra Low-Power, Low-Cost Comparators with 2% Reference

100nA for the thresholds to be accurate. R1 values up to about 10MΩ can be used, but values in the 100kΩ to 1MΩ range are usually easier to deal with. In this example, choose R1 = 294kΩ.

3. Calculate R2 + R3. The overvoltage threshold should be 5.5V when V_{IN} is rising. The design equation is as follows:

$$R2 + R3 = R1 \times \left(\frac{V_{OTH}}{V_{REF} + V_H} - 1 \right)$$

$$= 294k \times \left(\frac{5.5}{(1.182 + 0.005)} - 1 \right)$$

$$= 1.068M\Omega$$

4. Calculate R2. The undervoltage threshold should be 4.5V when V_{IN} is falling. The design equation is as follows:

$$R2 = (R1 + R2 + R3) \times \frac{(V_{REF} - V_H)}{V_{UTH}} - R1$$

$$= (294k + 1.068M) \times \frac{(1.182 - 0.005)}{4.5} - 294k$$

$$= 62.2k\Omega$$

Choose R2 = 61.9kΩ (1% standard value).

5. Calculate R3.

$$R3 = (R2 + R3) - R2$$

$$= 1.068M - 61.9k$$

$$= 1.006M\Omega$$

Choose R3 = 1MΩ (1% standard value).

6. Verify the resistor values. The equations are as follows, evaluated for the above example.

Overvoltage threshold:

$$V_{OTH} = (V_{REF} + V_H) \times \frac{(R1 + R2 + R3)}{R1}$$

$$= 5.474V.$$

Undervoltage threshold:

$$V_{UTH} = (V_{REF} - V_H) \times \frac{(R1 + R2 + R3)}{(R1 + R2)}$$

$$= 4.484V,$$

where the hysteresis voltage $V_H = V_{REF} \times \frac{R5}{R4}$.

Bar-Graph Level Gauge

The high output source capability of the MAX931 series is useful for driving LEDs. An example of this is the simple four-stage level detector shown in Figure 7. The full-scale threshold (all LEDs on) is given by V_{IN} = (R1 + R2)/R1 volts. The other thresholds are at 3/4 full scale, 1/2 full scale, and 1/4 full scale. The output resistors limit the current into the LEDs.

Level Shifter

Figure 8 shows a circuit to shift from bipolar ±5V inputs to TTL signals. The 10kΩ resistors protect the comparator inputs, and do not materially affect the operation of the circuit.

Two-Stage Low-Voltage Detector

Figure 9 shows the MAX932 monitoring an input voltage in two steps. When V_{IN} is higher than the LOW and FAIL thresholds, outputs are high. Threshold calculations are simliar to those for the window-detector application.

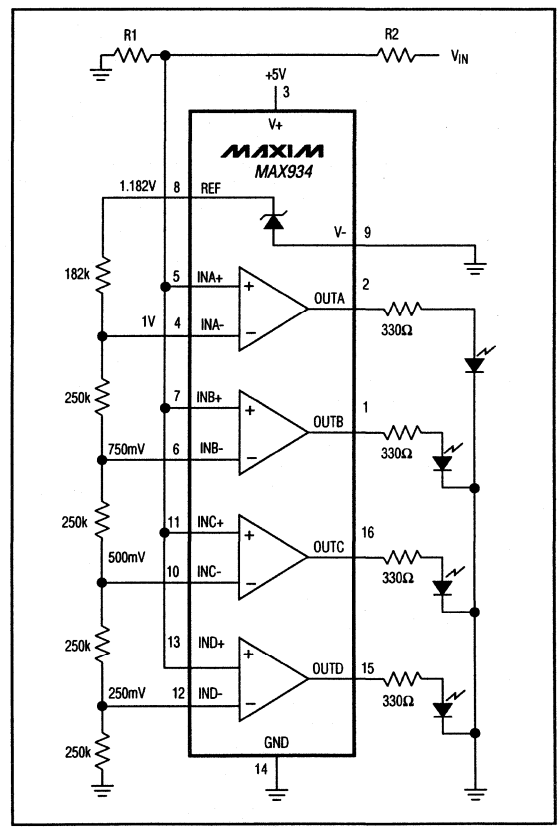


Figure 7. Bar-Graph Level Gauge

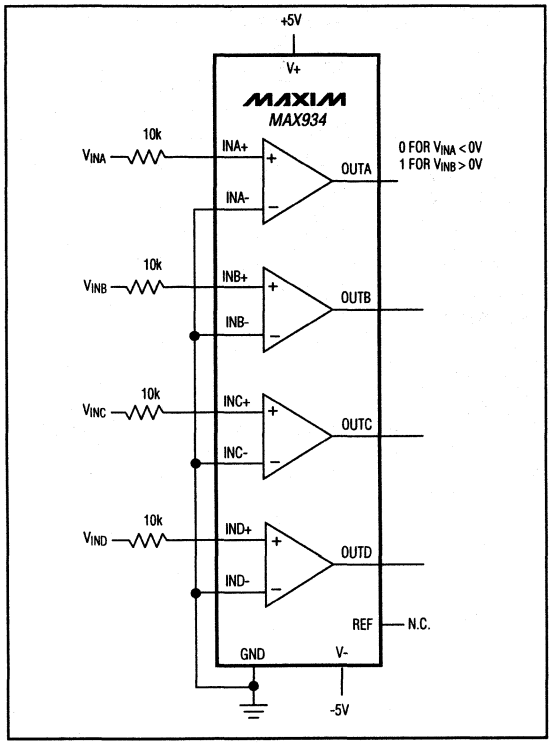


Figure 8. Level Shifter: ±5V Input to CMOS Output

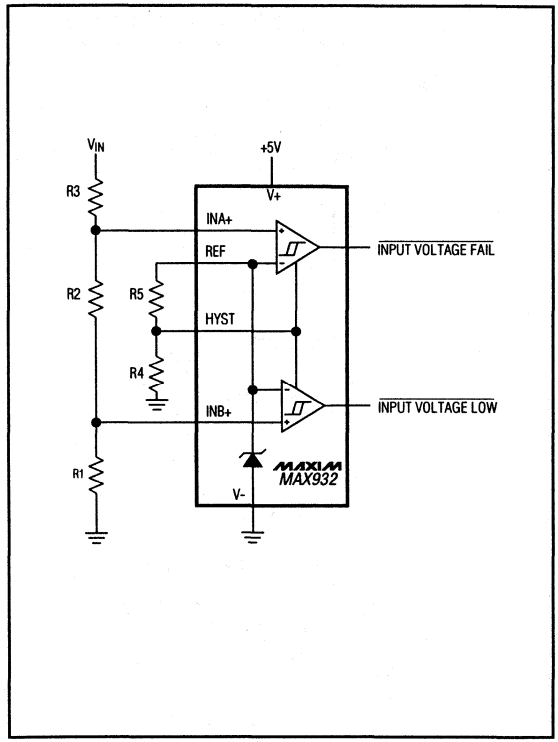
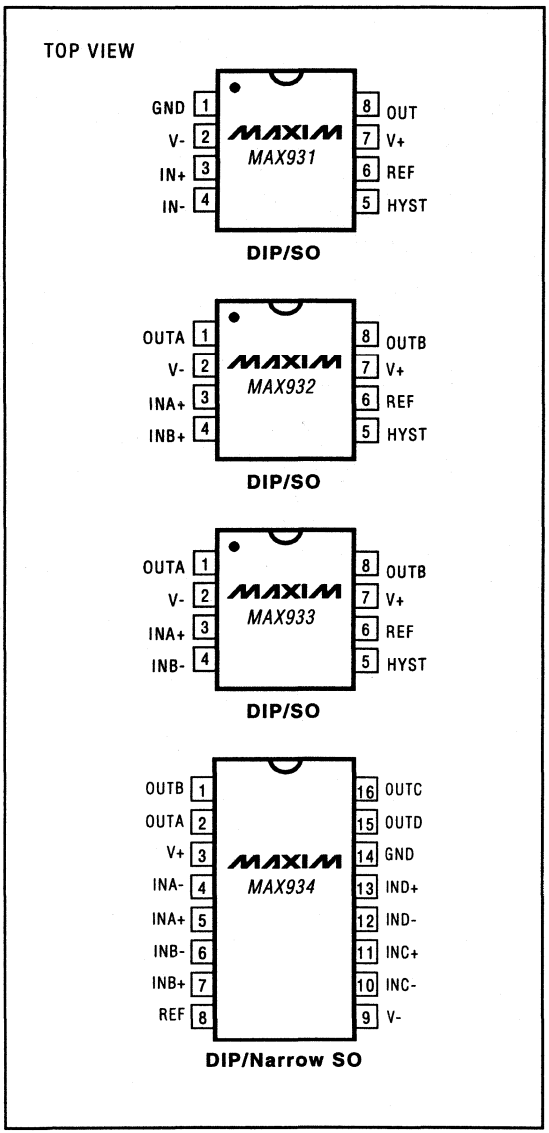


Figure 9. Two-Stage Low-Voltage Detector

Ultra Low-Power, Low-Cost Comparators with 2% Reference

Pin Configurations



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX932CPA	0°C to +70°C	8 Plastic DIP
MAX932CSA	0°C to +70°C	8 SO
MAX932EPA	-40°C to +85°C	8 Plastic DIP
MAX932ESA	-40°C to +85°C	8 SO
MAX933CPA	0°C to +70°C	8 Plastic DIP
MAX933CSA	0°C to +70°C	8 SO
MAX933EPA	-40°C to +85°C	8 Plastic DIP
MAX933ESA	-40°C to +85°C	8 SO
MAX934CPE	0°C to +70°C	16 Plastic DIP
MAX934CSE	0°C to +70°C	16 Narrow SO
MAX934EPE	-40°C to +85°C	16 Plastic DIP
MAX934ESE	-40°C to +85°C	16 Narrow SO

For similar devices guaranteed over the military temp. range, see the MAX921-MAX924 data sheet. The MAX931, MAX933, and MAX934 are pin-compatible with the 1% accurate MAX921, MAX923, and MAX924, respectively. The MAX932 and MAX922 are not pin-compatible.

19-0229; Rev 1; 5/94

MAXIM

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

General Description

The MAX941/MAX942/MAX944 are single/dual/quad high-speed comparators optimized for systems powered from a 3V or 5V supply. These devices combine high speed, low power, and rail-to-rail inputs. Propagation delay is 80ns, while supply current is only 350µA per comparator.

The input common-mode range of the MAX941/MAX942/MAX944 extends beyond both power-supply rails. The outputs pull to within 0.4V of either supply rail without external pull-up circuitry, making these devices ideal for interface with both CMOS and TTL logic. All input and output pins can tolerate a continuous short-circuit fault condition to either rail.

Internal hysteresis ensures clean output switching, even with slow-moving input signals. The MAX941 features latch enable and device shutdown.

The single MAX941 is offered in the smallest 8-pin SO: the µMAX package. Both the single and dual MAX942 are available in 8-pin DIP and SO packages. And, the quad MAX944 comes in 14-pin DIP and narrow SO packages.

Applications

3V/5V Systems
Battery-Powered Systems
Threshold Detectors/Discriminators
Line Receivers
Zero-Crossing Detectors
Sampling Circuits

Features

- **In µMAX Package: Smallest 8-Pin SO**
- **Optimized for 3V and 5V Applications (operation down to 2.7V)**
- **Fast, 80ns Propagation Delay (5mV overdrive)**
- **Rail-to-Rail Input Voltage Range**
- **Low Power:**
  1mW Power Dissipation per Comparator (3V)
  350µA Supply Current
- **Low, 1mV Offset Voltage**
- **Internal Hysteresis for Clean Switching**
- **Outputs Swing 200mV of Power Rails**
- **CMOS/TTL-Compatible Outputs**
- **Output Latch (MAX941 only)**
- **Shutdown Function (MAX941 only)**

Ordering Information

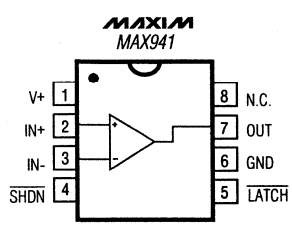
PART	TEMP. RANGE	PIN-PACKAGE
MAX941CPA	0°C to +70°C	8 Plastic DIP
MAX941CSA	0°C to +70°C	8 SO
MAX941CUA	0°C to +70°C	8 µMAX
MAX941C/D	0°C to +70°C	Dice*
MAX941EPA	-40°C to +85°C	8 Plastic DIP
MAX941ESA	-40°C to +85°C	8 SO
MAX941MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued at end of data sheet.

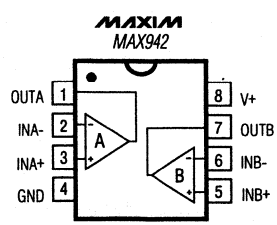
** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations

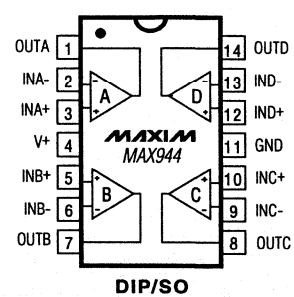
TOP VIEW



DIP/SO/µMAX



DIP/SO



DIP/SO

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
- Supply Voltage V+ to GND ..... +7V
- Differential Input Voltage ..... -0.3V to (V+ + 0.3V)
- Common-Mode Input Voltage ..... -0.3V to (V+ + 0.3V)
- $\overline{LATCH}$ Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)
- $\overline{SHDN}$ Control Input (MAX941 only) ..... -0.3V to (V+ + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
- 8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
- 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
- 14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
- 14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges
- MAX94_C_ _ ..... 0°C to +70°C
- MAX94_E_ _ ..... -40°C to +85°C
- MAX94_MJ _ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.7V to 6.0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Supply Voltage	V+			2.7		6.0	V
Input Voltage Range	V_{CMR}	(Note 1)		-0.2		V+ + 0.2	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = 0V or V_{CM} = V+ (Note 2)	T_A = +25°C		1	3	mV
			$T_A = T_{MIN}$ to T_{MAX}			4	
Input Offset Voltage	V_{OS}	V_{CM} = 0V or V_{CM} = V+ (Note 3)	T_A = +25°C		1	2	mV
			$T_A = T_{MIN}$ to T_{MAX}			3	
Input Bias Current	I_B	$V_{IN} = V_{OS}$, V_{CM} = 0V or V_{CM} = V+ (Note 4)	MAX94_C		150	300	nA
			MAX94_E/M		150	400	
Input Offset Current	I_{OS}	$V_{IN} = V_{OS}$, V_{CM} = 0V or V+			10	100	nA
Common-Mode Rejection Ratio	CMRR	(Note 5)			80	300	µV/V
Power-Supply Rejection Ratio	PSRR	2.7V ≤ V+ ≤ 6.0V, V_{CM} = 0V			80	300	µV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 400µA		V+ - 0.4	V+ - 0.2		V
		I_{SOURCE} = 4mA		V+ - 0.4	V+ - 0.3		
Output Low Voltage	V_{OL}	I_{SINK} = 400µA			0.2	0.4	V
		I_{SINK} = 4mA			0.3	0.4	
Output Leakage Current	I_{LEAK}	(Note 6)				1	µA
Supply Current per Comparator	I_{CC}	V+ = 3V	MAX941		380	600	µA
			MAX942/MAX944		350	500	
		V+ = 5V	MAX941		430	700	
			MAX942/MAX944		400	600	
		MAX941 only, shutdown mode (V+ = 3V)			12	30	
Power Dissipation per Comparator	PD	(Note 7)	MAX941		1.0	4.2	mW
			MAX942/MAX944		1.0	3.6	
Propagation Delay	t_{PD+}, t_{PD-}	(Note 8)	MAX94_C		80	150	ns
			MAX94_E/M		80	200	
Differential Propagation Delay	dt_{PD}	(Note 9)			10		ns

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.7V to 6.0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Skew		(Note 10)		10		ns
Logic Input Voltage High	V_{IH}	(Note 11)	$\frac{V+}{2}$ + 0.4	$\frac{V+}{2}$		V
Logic Input Voltage Low	V_{IL}	(Note 11)		$\frac{V+}{2}$	$\frac{V+}{2}$ - 0.4	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0V or V+ (Note 11)		2	10	µA
Data-to-Latch Setup Time	t_S	(Note 12)		20		ns
Latch-to-Data Hold Time	t_H	(Note 12)		30		ns
Latch Pulse Width	t_{LPW}	MAX941 only		50		ns
Latch Propagation Delay	t_{LPD}	MAX941 only		70		ns
Shutdown Time		(Note 13)		3		µs
Shutdown Disable Time		(Note 13)		10		µs

Note 1: Inferred from the CMRR test. Note also that either or both inputs can be driven to the absolute maximum limit (0.3V beyond either supply rail) without damage or false output inversion.

Note 2: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. See Figure 1.

Note 3: V_{OS} is defined as the center of the input-referred hysteresis zone. See Figure 1.

Note 4: The polarity of I_B reverses direction as V_{CM} approaches either supply rail. See *Typical Operating Characteristics* for more detail.

Note 5: Specified over the full common-mode range (V_{CMR}).

Note 6: Applies to the MAX941 only when in shutdown mode. Specification is for current flowing into or out of the output pin for V_{OUT} driven to any voltage from V+ to GND.

Note 7: Typical power dissipation specified with V+ = 3V; maximum with V+ = 6V.

Note 8: Parameter is guaranteed by design and specified with V_{OD} = 5mV and C_{LOAD} = 15pF in parallel with 400µA of sink or source current. V_{OS} is added to the overdrive voltage for low values of overdrive. See Figure 2.

Note 9: Specified between any two channels in the MAX942/MAX944.

Note 10: Specified as the difference between t_{PD+} and t_{PD-} for any one comparator.

Note 11: Applies to the MAX941 only for both $\overline{SHDN}$ and $\overline{LATCH}$ pins.

Note 12: Applies to the MAX941 only. Comparator is active with $\overline{LATCH}$ pin driven high and is latched with $\overline{LATCH}$ pin driven low. See Figure 2.

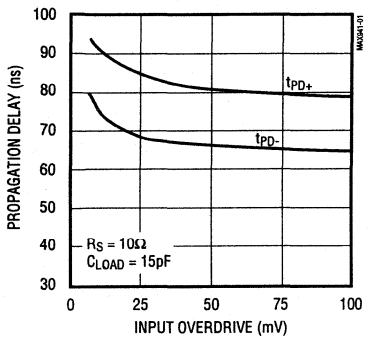
Note 13: Applicable to the MAX941 only. Comparator is active with $\overline{SHDN}$ pin driven high and is in shutdown with $\overline{SHDN}$ pin driven low. Shutdown disable time is the delay when $\overline{SHDN}$ is driven high to the time the output is valid.

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

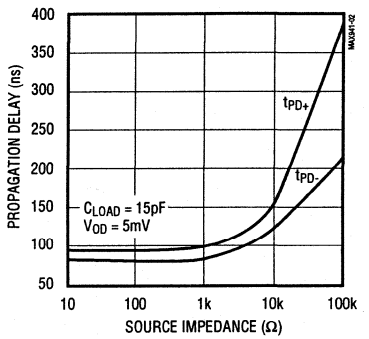
Typical Operating Characteristics

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

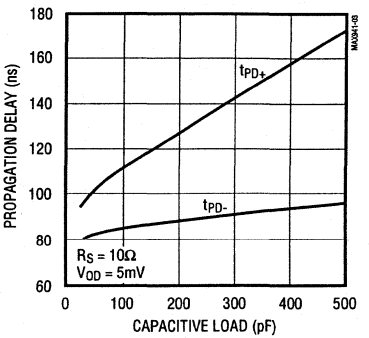
PROPAGATION DELAY vs. INPUT OVERDRIVE



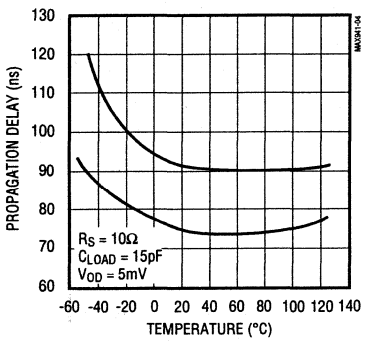
PROPAGATION DELAY vs. SOURCE IMPEDANCE



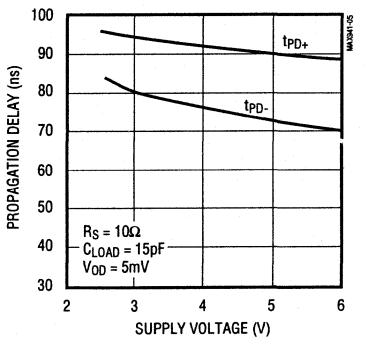
PROPAGATION DELAY vs. CAPACITIVE LOAD



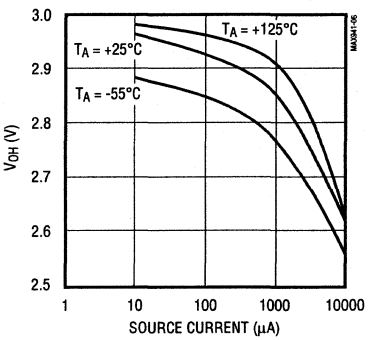
PROPAGATION DELAY vs. TEMPERATURE



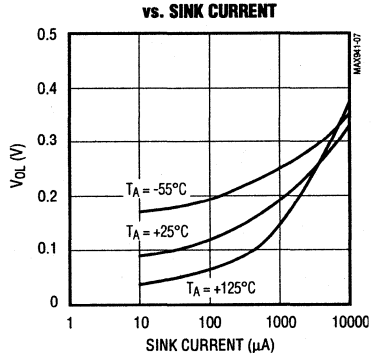
PROPAGATION DELAY vs. SUPPLY VOLTAGE



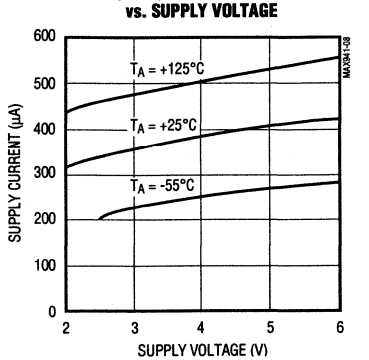
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



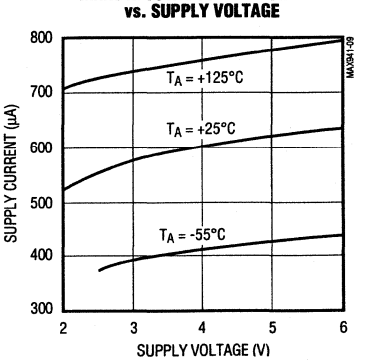
OUTPUT LOW VOLTAGE vs. SINK CURRENT



MAX941 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX942 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE

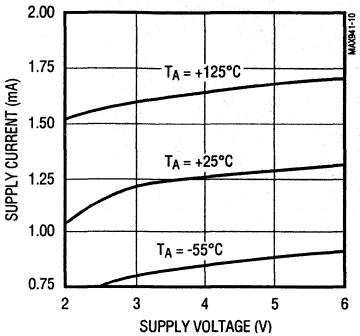


High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

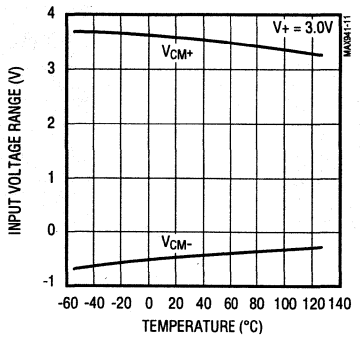
Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

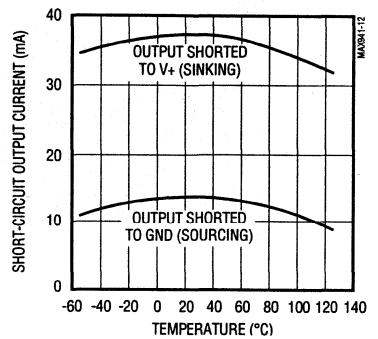
MAX944 TOTAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



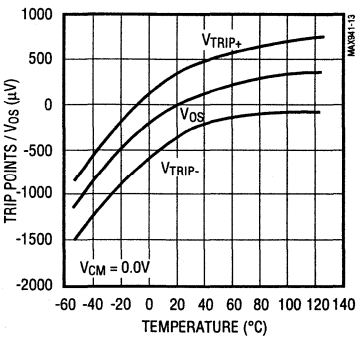
INPUT VOLTAGE RANGE vs. TEMPERATURE



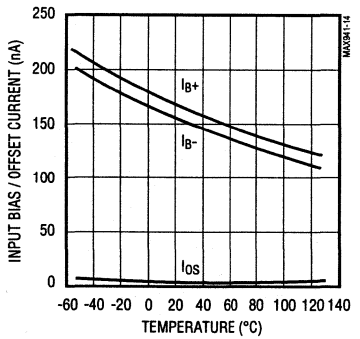
SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



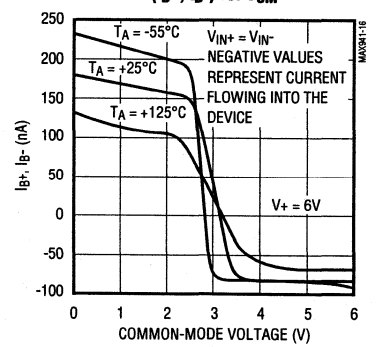
VOLTAGE TRIP POINTS / INPUT OFFSET VOLTAGE vs. TEMPERATURE



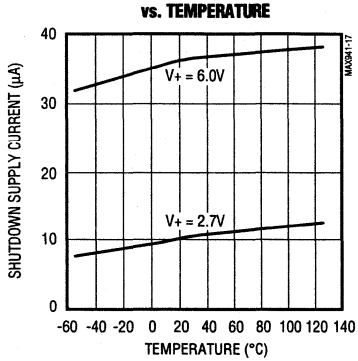
INPUT BIAS CURRENT / INPUT OFFSET CURRENT vs. TEMPERATURE



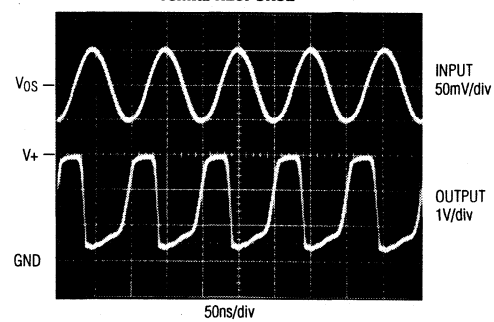
INPUT BIAS CURRENT (I_{B+}, I_{B-}) vs. V_{CM}



MAX941 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



10MHz RESPONSE

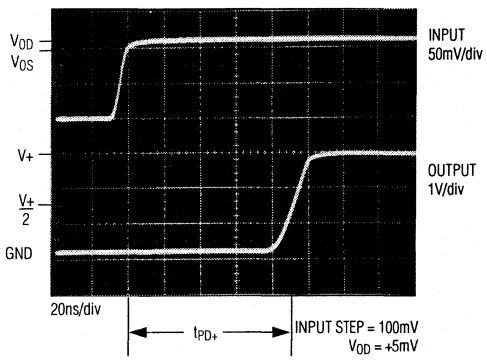


High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

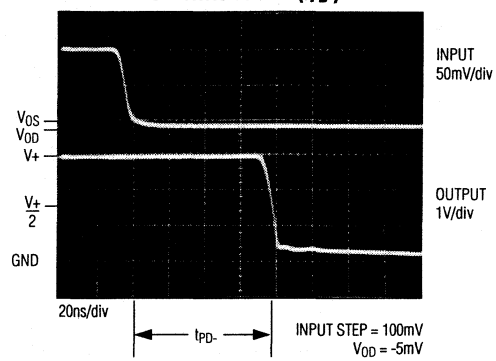
Typical Operating Characteristics (continued)

(V+ = 3.0V, T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



Pin Description

PIN			NAME	FUNCTION
MAX941	MAX942	MAX944		
—	1	1	OUTA	Comparator A output
—	2	2	INA-	Comparator A inverting input
—	3	3	INA+	Comparator A noninverting input
1	8	4	V+	Positive supply (V+ to GND must be ≤ 7V)
—	5	5	INB+	Comparator B noninverting input
—	6	6	INB-	Comparator B inverting input
—	7	7	OUTB	Comparator B output
—	—	8	OUTC	Comparator C output
—	—	9	INC-	Comparator C inverting input
—	—	10	INC+	Comparator C noninverting input
6	4	11	GND	Ground
—	—	12	IND+	Comparator D noninverting input
—	—	13	IND-	Comparator D inverting input
—	—	14	OUTD	Comparator D output
2	—	—	IN+	Noninverting input
3	—	—	IN-	Inverting input
4	—	—	$\overline{SHDN}$	Shutdown: MAX941 is active when $\overline{SHDN}$ is driven high; MAX941 is in shutdown when $\overline{SHDN}$ is driven low.
5	—	—	$\overline{LATCH}$	The output is latched when $\overline{LATCH}$ is low. The latch is transparent when $\overline{LATCH}$ is high.
7	—	—	OUT	Comparator output
8	—	—	N.C.	No connect—not internally connected

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

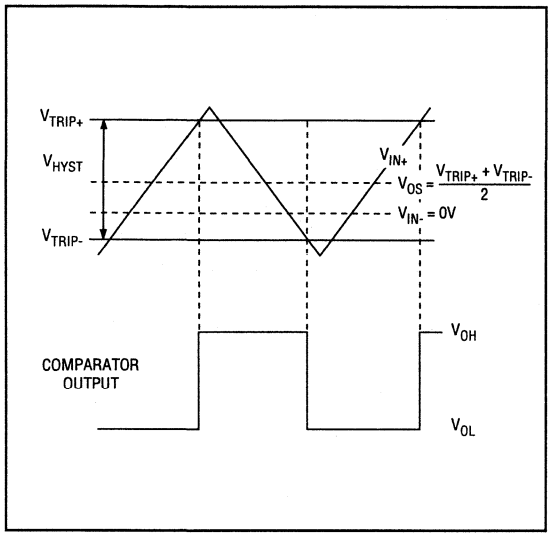


Figure 1. Input and Output Waveform, Noninverting Input Varied

Detailed Description

The MAX941/MAX942/MAX944 single-supply comparators feature internal hysteresis, high speed, and low power. Their outputs are guaranteed to pull within 0.4V of either supply rail without external pull-up or pull-down circuitry. Rail-to-rail input voltage range and low-voltage single-supply operation make these devices ideal for portable equipment. The MAX941/MAX942/MAX944 interface directly to CMOS and TTL logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the MAX941/MAX942/MAX944 have internal hysteresis.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX941/MAX942/MAX944's fixed internal hysteresis eliminates these resistors and the equations needed to determine appropriate values.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

The MAX941 includes an internal latch that allows storage of comparison results. The $\overline{LATCH}$ pin has a high input impedance. If $\overline{LATCH}$ is high, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when $\overline{LATCH}$ is pulled low. All timing constraints must be met when using the latch function (Figure 2).

Shutdown Mode (MAX941 Only)

The MAX941 shuts down when $\overline{SHDN}$ is low. When shut down, the supply current drops to less than 30µA, and the three-state output becomes high impedance. The $\overline{SHDN}$ pin has a high input impedance. Connect $\overline{SHDN}$ to V+ for normal operation. Exit shutdown with $\overline{LATCH}$ high; otherwise, the output will be indeterminate.

Input Stage Circuitry

The MAX941/MAX942/MAX944 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of four back-to-back diodes between IN+ and IN- as well as two 2.5kΩ resistors (Figure 3). The diodes limit the differential voltage applied to the internal circuitry of the comparators to be no more than $4V_F$, where V_F is the forward voltage drop of the diode (about 0.7V at +25°C).

For a large differential input voltage (exceeding $4V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input Current} = \frac{(IN+ - IN-) - 4V_F}{2 \times 2.5k\Omega}$$

Input current with large differential input voltages should not be confused with input bias current (I_B). As long as the differential input voltage is less than $4V_F$, this input current is equal to I_B. The protection circuitry also allows for the input common-mode range of the MAX941/MAX942/MAX944 to extend beyond both power-supply rails. The output is in the correct logic state if one or both inputs are within the common-mode range.

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

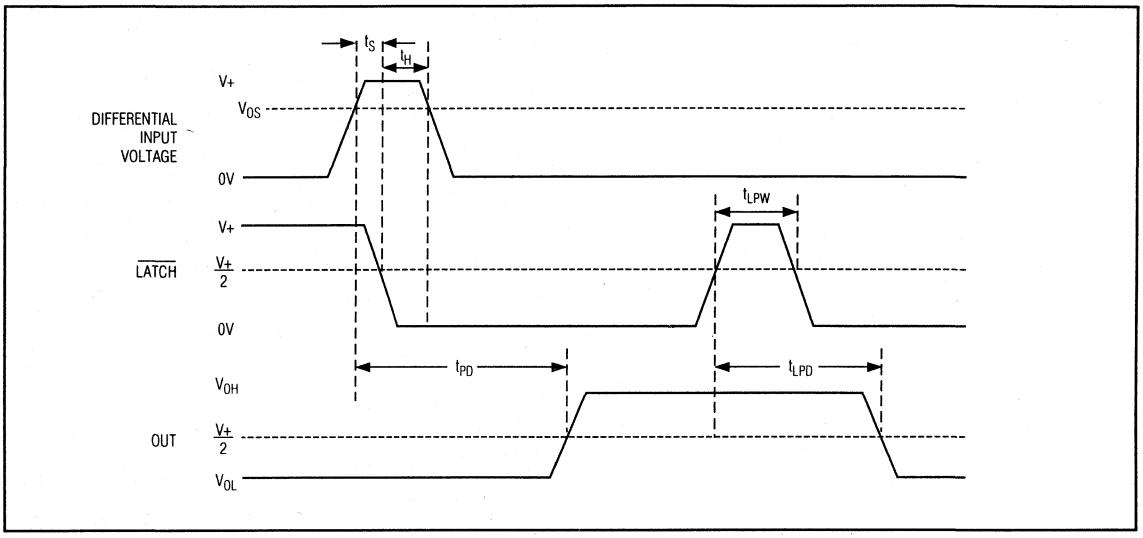


Figure 2. MAX941 Timing Diagram with Latch Operator

Output Stage Circuitry

The MAX941/MAX942/MAX944 contain a current-driven output stage as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} static condition. This significant decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load will slow down a voltage output transition. This can be useful in noise-sensitive applications where fast edges may cause interference.

Applications Information

Circuit Layout and Bypassing

The high gain bandwidth of the MAX941/MAX942/MAX944 requires design precautions to realize the comparators' full high-speed capability. The recommended precautions are:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V+ as possible.
3) Pay close attention to the decoupling capacitor's bandwidth, keeping leads short.
4) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
5) Solder the device directly to the printed circuit board instead of using a socket.

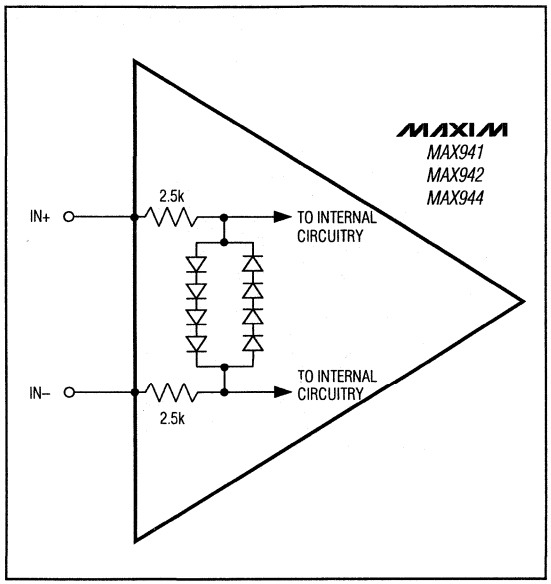


Figure 3. Input Stage Circuitry

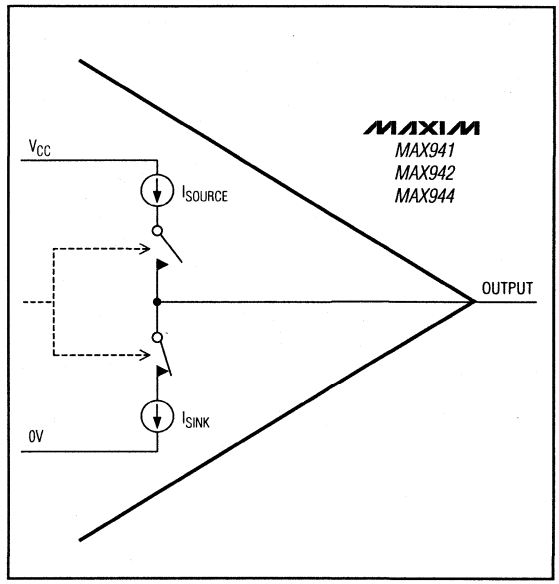


Figure 4. Output Stage Circuitry

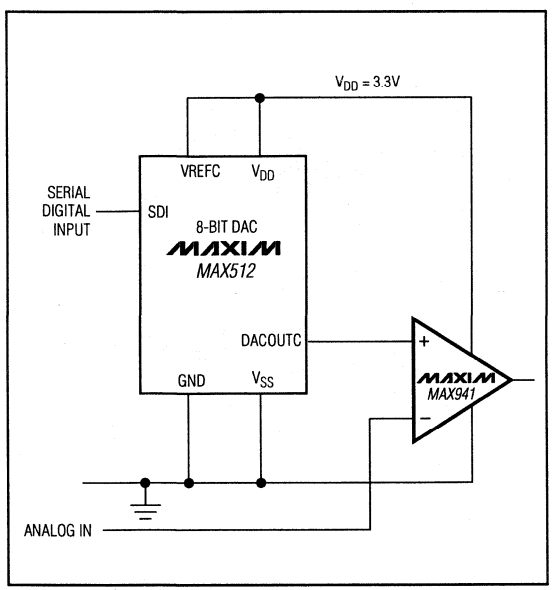


Figure 5. 3.3V Digitally Controlled Threshold Detector

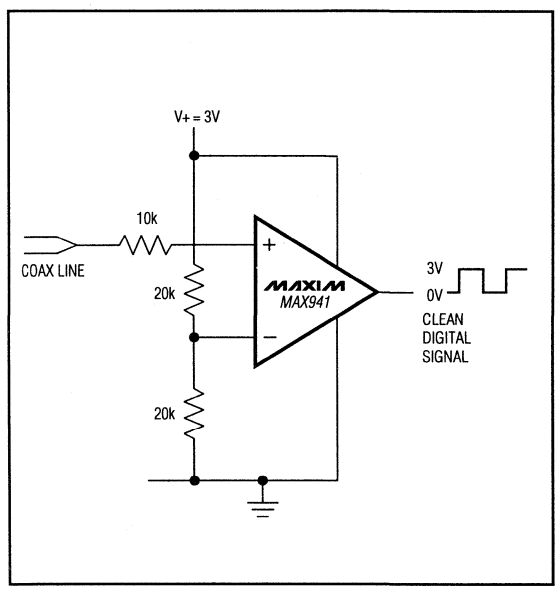


Figure 6. Line Transceiver Application

High-Speed, Low-Power, 3V/5V, Rail-to-Rail Single-Supply Comparators

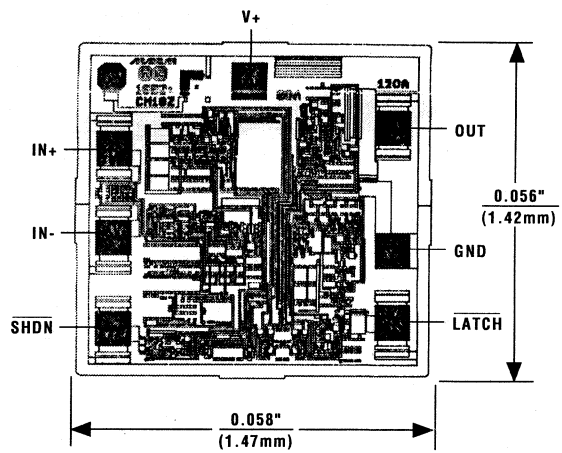
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX942CPA	0°C to +70°C	8 Plastic DIP
MAX942CSA	0°C to +70°C	8 SO
MAX942C/D	0°C to +70°C	Dice*
MAX942EPA	-40°C to +85°C	8 Plastic DIP
MAX942ESA	-40°C to +85°C	8 SO
MAX942MJA	-55°C to +125°C	8 CERDIP
MAX944CPD	0°C to +70°C	14 Plastic DIP
MAX944CSD	0°C to +70°C	14 SO
MAX944EPD	-40°C to +85°C	14 Plastic DIP
MAX944ESD	-40°C to +85°C	14 SO
MAX944MJD	-55°C to +125°C	14 CERDIP

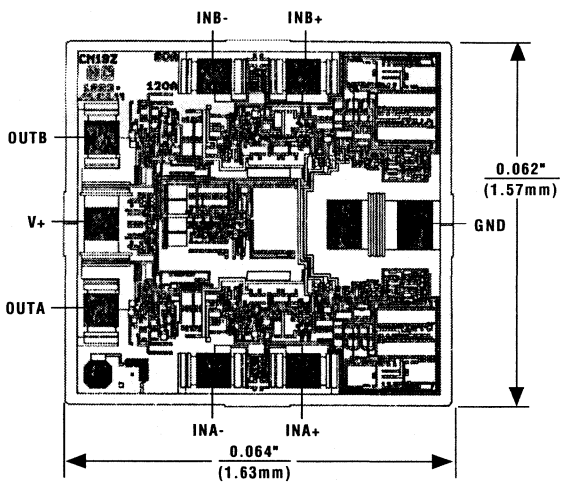
** Dice are specified at T_A = +25°C, DC parameters only.*

Chip Topographies

MAX941



MAX942



TRANSISTOR COUNT: 134(MAX941), 190(MAX942)
SUBSTRATE CONNECTED TO GND

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Ultra-Low-Power Op Amps with Comparator and Reference

General Description

The MAX951–MAX954 are micropower op amps with comparator and reference (MAX951/MAX952). The MAX951 (unity-gain stable) and MAX952 ($A_V \geq 10V/V$) have a 1.2V ±1% bandgap reference and a comparator with its negative input connected to the reference. The MAX953 and MAX954 are equivalent to the MAX951 and MAX952 respectively, but without the internal reference. Maximum supply current over temperature is 10µA for the MAX951/MAX952 and 8µA for the MAX953/MAX954. These devices operate from a single +2.2V to +7V supply. Both the op amp and the comparator feature a common-mode input voltage range that extends from the negative supply rail to within 1.3V of the positive rail, as well as output stages that swing rail-to-rail.

The op amps in the MAX951/MAX953 are internally compensated to be unity-gain stable while the op amps in the MAX952/MAX954 feature 200kHz typical bandwidth, 100V/ms slew rate, and stability for gains of 10V/V or greater. These op amps have a unique output stage that enables them to operate with ultra-low supply current while maintaining linearity under loaded conditions. In addition, they have been designed to exhibit good DC characteristics over their entire operating temperature range, minimizing input-referred errors.

The output stage of the comparators in these devices continuously sources as much as 40mA. These comparators eliminate power-supply glitches that commonly occur when changing logic states, minimizing parasitic feedback and making them easier to use. In addition, they contain ±3mV internal hysteresis to ensure clean output switching, even with slow-moving input signals.

Applications

Instruments, Terminals and Bar-Code Readers
Battery-Powered Systems
Automotive Keyless Entry
Low-Frequency, Local-Area Alarms/Detectors
Photodiode Pre-Amps

Selection Table

PART	INTERNAL ±1% PRECISION REFERENCE	OP-AMP GAIN STABILITY (V/V)	COMPARATOR	SUPPLY CURRENT (µA max)
MAX951	Yes	1	Yes	10
MAX952	Yes	10	Yes	10
MAX953	No	1	Yes	8
MAX954	No	10	Yes	8

Features

- ♦ **Op Amp, Comparator, and Reference in an 8-Pin µMAX Surface-Mount Package**
- ♦ **10µA Max Supply Current (Op Amp + Comparator + Reference)**
- ♦ **Comparator and Op-Amp Input Range Includes Ground**
- ♦ **2.2V to 7V Supply Voltage Range**
- ♦ **Unity-Gain and 20dB Stable Op-Amp Options**
- ♦ **Internal 1.2V ±1% Bandgap Reference**
- ♦ **Outputs Swing Rail-to-Rail**
- ♦ **Internal, Fixed ±3mV Comparator Hysteresis**
- ♦ **Op Amp Capable of Driving up to 1000pF Load**

Ordering Information

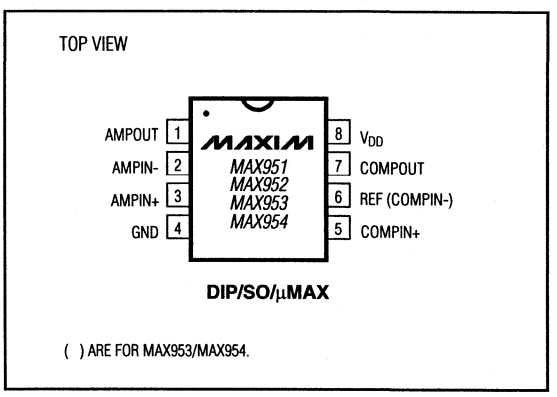
PART	TEMP. RANGE	PIN-PACKAGE
MAX951CPA	0°C to +70°C	8 Plastic DIP
MAX951CSA	0°C to +70°C	8 SO
MAX951CUA	0°C to +70°C	8 µMAX
MAX951C/D	0°C to +70°C	Dice*
MAX951EPA	-40°C to +85°C	8 Plastic DIP
MAX951ESA	-40°C to +85°C	8 SO
MAX951MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

** Dice are tested at T_A = +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



DIP/SO/µMAX

( ) ARE FOR MAX953/MAX954.

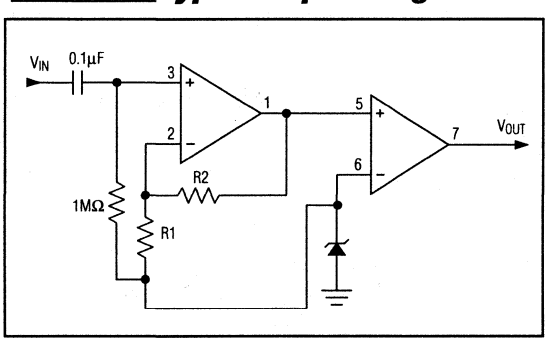
Ultra-Low-Power Op Amps with Comparator and Reference

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX952CPA	0°C to +70°C	8 Plastic DIP
MAX952CSA	0°C to +70°C	8 SO
MAX952CUA	0°C to +70°C	8 µMAX
MAX952C/D	0°C to +70°C	Dice*
MAX952EPA	-40°C to +85°C	8 Plastic DIP
MAX952ESA	-40°C to +85°C	8 SO
MAX952MJA	-55°C to +125°C	8 CERDIP**
MAX953CPA	0°C to +70°C	8 Plastic DIP
MAX953CSA	0°C to +70°C	8 SO
MAX953CUA	0°C to +70°C	8 µMAX
MAX953C/D	0°C to +70°C	Dice*
MAX953EPA	-40°C to +85°C	8 Plastic DIP
MAX953ESA	-40°C to +85°C	8 SO
MAX953MJA	-55°C to +125°C	8 CERDIP**
MAX954CPA	0°C to +70°C	8 Plastic DIP
MAX954CSA	0°C to +70°C	8 SO
MAX954CUA	0°C to +70°C	8 µMAX
MAX954C/D	0°C to +70°C	Dice*
MAX954EPA	-40°C to +85°C	8 Plastic DIP
MAX954ESA	-40°C to +85°C	8 SO
MAX954MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



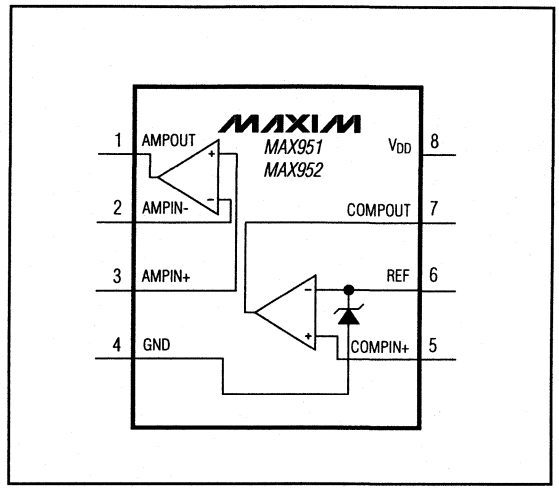


Figure 1. MAX951/MAX952 Functional Diagram

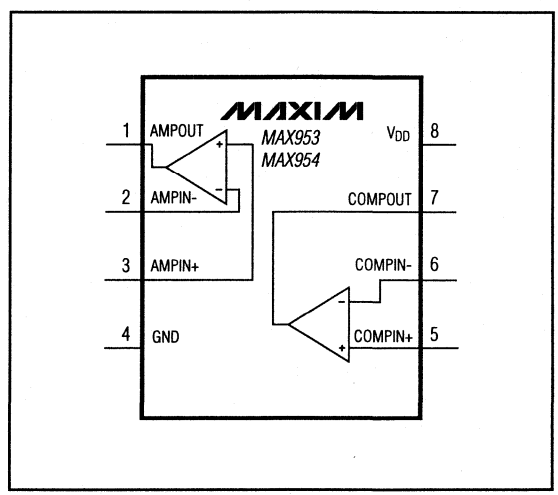


Figure 2. MAX953/MAX954 Functional Diagram

MAXIM

Power-Supply Circuits

*Advance Information–first page of data sheet in preparation.

*Advance Information–first page of data sheet in preparation.

DC-DC CONVERTERS

LOW-DROPOUT LINEAR REGULATORS

POSITIVE

† **MAX603** (5V or adj., I_Q = 15µA, 320mV dropout at 500mA, 1.6W 8-pin SO)

† **MAX604** (3.3V or adj., I_Q = 15µA, 480mV dropout at 400mA, 1.6W 8-pin SO)

MAX663 (5V or adj., I_Q = 6µA)

MAX666 (5V or adj., I_Q = 6µA, low-battery detect)

MAX667 (5V or adj., I_Q = 20µA, 120mV dropout, 200mA, low-battery detect)

† **MAX687** (+3V or +3.3V ±3%, 0.2V dropout at 500mA)

† **MAX688** (+3V or +3.3V ±3%, 0.2V dropout at 500mA)

† **MAX689** (+3V or +3.3V ±3%, 0.2V dropout at 500mA)

† **MAX882** (3.3V or adj., P-Ch, 200mA, low-battery detector, 1.0W 8-pin SO)

† **MAX883** (5V or adj., P-Ch, 300mA, low-battery detector, 1.0W 8-pin SO, 1µA OFF mode)

† **MAX884** (3.3V or adj., P-Ch, 200mA, low-battery detector, 1.0W 8-pin SO, 1µA OFF mode)

ICL7663 (adj., 40mA)

NEGATIVE

MAX664 (-5V or adj., I_Q = 6µA)

ICL7664 (adj., 40mA)

SWITCHING REGULATORS

STEP-UP

PWM

☆ **MAX731** ($2V_{IN}$ to $5V_{OUT}$)

☆ **MAX732** (12V, flash prog.)

☆ **MAX733** (15V)

☆ **MAX734** (12V, flash prog.)

☆ **MAX741U** (step-up controller)

☆ **MAX751** ($2V_{IN}$ to $5V_{OUT}$)

☆ **MAX752** (adj.)

PFM

☆★ **MAX1771** (12V or adj. controller)

MAX4193 (adj.)

MAX630 (adj.)

MAX631 (5V or adj.)

MAX632 (12V or adj.)

MAX633 (15V or adj.)

MAX641 (5V or adj. controller)

MAX642 (12V or adj. controller)

MAX643 (15V or adj. controller)

☆ **MAX756** (3.3V or $5V_{OUT}$ from $1.8V_{IN}$ (min), 250mA)

☆ **MAX757** (adj. V_{OUT} from $1.8V_{IN}$ (min), 250mA)

☆★ **MAX761** (12V, 120mA, flash prog.)

☆★ **MAX762** (15V or adj.)

☆★ **MAX770** (5V or adj. controller)

☆★ **MAX771** (12V or adj. controller)

☆★ **MAX772** (15V or adj. controller)

★ **MAX773** (5V, 12V, 15V, or adj., controller)

☆ **MAX777** ($5V_{OUT}$ from $1V_{IN}$ (min))

☆ **MAX778** (3V or $3.3V_{OUT}$ from $1V_{IN}$ (min))

☆ **MAX779** (adj. V_{OUT} from $1V_{IN}$)

☆★ **MAX856** (3.3V or $5V_{OUT}$ from $1.8V_{IN}$ (min), 100mA)

☆★ **MAX857** (adj. V_{OUT} from $1.8V_{IN}$ (min), 100mA)

☆★ **MAX858** (3.3V or $5V_{OUT}$ from $1.8V_{IN}$ (min), 25mA)

☆★ **MAX859** (adj. V_{OUT} from $1.8V_{IN}$ (min), 25mA)

INVERTING

PWM

MAX735 (-5V)

☆ **MAX736** (-12V)

☆ **MAX737** (-15V)

☆ **MAX739** (-5V)

MAX741N (inverter controller)

MAX755 (adj.)

☆ **MAX759** (adj.)

PFM

MAX4391 (adj.)

MAX634 (adj.)

MAX635 (-5V)

MAX636 (-12V)

MAX637 (-15V)

MAX650 ($5V_{OUT}$ from -48V_{IN})

☆ **MAX749** (digital adj.)

☆† **MAX764** (-5V or adj.)

☆† **MAX765** (-12V or adj.)

☆† **MAX766** (-15V or adj.)

☆★ **MAX774** (-5V or adj. controller)

☆★ **MAX775** (-12V or adj. controller)

☆★ **MAX776** (-15V or adj. controller)

STEP-UP/DOWN

☆ **MAX877** ($5V_{OUT}$ from 1V to $6.2V_{IN}$)

☆ **MAX878** (3V or $3.3V_{OUT}$ from 1V to $6.2V_{IN}$)

☆ **MAX879** (adj. V_{OUT} from 1V to $6.2V_{IN}$)

STEP-DOWN

PWM

MAX724 (adj., 5A)

MAX726 (adj., 2A)

MAX727 (5V, 2A)

MAX728 (3.3V, 2A)

MAX729 (3V, 2A)

☆ **MAX730A** (5V, improved)

☆ **MAX738A** (5V, improved)

☆ **MAX741D** (step-down controller)

☆ **MAX744A** (5V, optimized for cellular comm.)

MAX746 (5V or adj. controller, N-channel FET)

☆ **MAX747** (5V or adj. controller, P-channel FET)

☆ **MAX748A** (3.3V)

☆ **MAX750A** (adj., improved)

☆ **MAX758A** (adj., improved)

☆ **MAX763A** (3.3V)

☆ **MAX767** (3.3V)

☆† **MAX781** (3.3V, battery charger, PCMCIA)

☆ **MAX782** (3.3V or 5V, PCMCIA)

☆ **MAX783** (3.3V or 5V, PCMCIA for 6-cell inputs)

MAX786 (3.3V or 5V)

† **MAX787** (5A, 5V)

† **MAX788** (5A, 3.3V)

† **MAX789** (5A, 3V)

† **MAX796/7/8/9** (5V, 3.3V, 2.9V, or adj. controllers)

† **MAX830** (adj., 1A, SOIC)

☆† **MAX831** (5V or adj., 1A)

† **MAX832** (3.3V or adj., 1A)

† **MAX833** (3V or adj., 1A)

PFM

☆† **MAX1649** (5V or adj. controller)

☆† **MAX1651** (3.3V or adj. controller)

MAX638 (5V or adj.)

☆ **MAX639** (5V or adj., >90% efficiency)

☆ **MAX640** (3.3V or adj.)

☆★ **MAX649** (5V or adj. controller)

☆★ **MAX651** (3.3V or adj. controller)

☆★ **MAX652** (3V or adj. controller)

☆ **MAX653** (3V or adj.)

DUAL OUTPUT

PWM

MAX742 (±12V or ±15V controller)

☆ **MAX743** (±12V or ±15V)

DISPLAY

† **MAX753** (CCFT & –LCD, digital adj.)

† **MAX754** (CCFT & +LCD, digital adj.)

CHARGE PUMPS

$-V_{IN}$ or (2 x V_{IN})

MAX1044 (60kHz osc. freq. boost)

MAX660 (100mA, V_{IN} up to 5V)

MAX665 (100mA, V_{IN} up to 8V)

☆★ **MAX860/1** (50mA, V_{IN} up to 5.5V, 250kHz osc. freq.)

ICL7660 (V_{IN} up to 10V)

ICL7662 (V_{IN} up to 20V)

Si7661 (V_{IN} up to 20V)

$-V_{IN}$ and (2 x V_{IN})

MAX680

MAX681 (internal caps)

12V, 30mA

☆ **MAX662** (programs flash memories)

☆★ **MAX662A** (improved MAX662, "E" temp. range)

5V, 50mA

☆★ **MAX619**

-4.1V/Adj., 5mA

☆★ **MAX850/1/2/3** (low-noise neg. GaAsFET bias)

★ **New product**

† **Future product**

☆ **Evaluation kit available**

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
STEP-UP/STEP-DOWN SWITCHING REGULATORS										
MAX877/878/879	1 to 6.2	5/(3.3 or 3)/adj.	0.310(0.220)	240	PFM	DIP,SO	Yes	C,E,M	Gives regulated output when input above and below the output; no transformer	2.95
STEP-UP SWITCHING REGULATORS										
MAX4193	2.4 to 16.5	Adj.	0.200(0.090)	300mW	PFM	DIP,SO		C,E,M	Improved RC4193 2nd source	1.74
MAX630	2 to 16.5	Adj.	0.125(0.070)	300mW	PFM	DIP,SO		C,E,M	Improved RC4193 2nd source	2.88
MAX631	1.5 to 5.6	5, adj.	0.4(0.135)	40	PFM	DIP,SO		C,E,M	Only 2 external components	2.56
MAX632	1.5 to 12.6	12, adj.	2.0(0.5)	25	PFM	DIP,SO		C,E,M	Only 2 external components	2.56
MAX633	1.5 to 15.6	15, adj.	2.5(0.75)	20	PFM	DIP,SO		C,E,M	Only 2 external components	2.56
MAX641	1.5 to 5.6	5, adj.	0.4(0.135)	300	PFM	DIP,SO		C,E,M	PFM controller	2.87
MAX642	1.5 to 12.6	12, adj.	2.0(0.5)	550	PFM	DIP,SO		C,E,M	PFM controller	2.87
MAX643	1.5 to 15.6	15, adj.	2.5(0.75)	325	PFM	DIP,SO		C,E,M	PFM controller	2.87
MAX731	1.8 to 5.25	5	4(2)	200	PWM	DIP,SO	Yes	C,E,M		2.60
MAX732	4 to 9.3	12	3(1.7)	200	PWM	DIP,SO	Yes	C,E,M	Flash memory programmer, ±4% output voltage tolerance	2.76
MAX733	4 to 11	15	3(1.7)	125	PWM	DIP,SO	Yes	C,E,M		2.60
MAX734	1.9 to 12	12	2.5(1.2)	120	PWM	DIP,SO	Yes	C,E,M	Flash memory programmer	2.23
MAX741U	1.8 to 15.5	5,12,15, adj.	3.5(1.6)	5W	PWM	DIP,SSOP	Yes	C,E,M	PWM step-up controller, $3V_{IN}$ to $5V_{OUT}$ at 1A, 85% efficient	3.64
MAX751	1.2 to 5.25	5	3.5(2)	175	PWM	DIP,SO	Yes	C,E,M		2.35
MAX752	1.8 to 16	Adj.	3(1.7)	2.4W	PWM	DIP,SO	Yes	C,E,M		2.94
MAX756/757	1.1 to 5.5	(3.3 or 5)/adj.	0.060(0.045)	250	PFM	DIP,SO	Yes	C,E	Best combination of low I_Q & high 86% efficiency	1.95
MAX761/762	2 to 16.5	12/15 or adj. to 16.5	0.1(0.080)	120	PFM	DIP,SO	Yes	C,E,M	12V flash programmer, high efficiency over wide I_{OUT} range	2.23
MAX770/771/772	2 to 16.5	5/12/15 or adj.	0.1(0.085)	1A	PFM	DIP,SO	Yes	C,E,M	Controllers, high efficiency over wide I_{OUT} range	1.80
MAX1771	2 to 16.5	12 or adj.	0.1(0.085)	1A	PFM	DIP,SO	Yes	C,E,M	Same as MAX771, but only 100mV current-sense limit	1.80
MAX773	3 to 16.5	Adj. to 48	0.1(0.085)	1A	PFM	DIP,SO		C,E,M	Controller, high-voltage output, high efficiency over wide I_{OUT} range	1.80
MAX777/778/779	1 to 6	5/(3 or 3.3)/adj.	0.310(0.220)	300	PFM	DIP,SO	Yes	C,E,M	On-chip active diode, true turn off in shutdown	2.65
MAX856/857	0.8 to 6	(3.3 or 5)/adj.	0.060(0.025)	100	PFM	DIP,SO, µMAX	Yes	C,E	Best combination of low I_Q & high 85% efficiency	1.72
MAX858/859	0.8 to 6	(3.3 or 5)/adj	0.060(0.025)	25	PFM	DIP,SO, µMAX	Yes	C,E	Small, best combination of low I_Q & high efficiency	1.72
STEP-DOWN SWITCHING REGULATORS										
MAX638	2.6 to 16.5	5, adj.	0.6(0.135)	75	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX639/640/653	4 to 11.5	5/3.3/3 or adj.	0.02(0.01)	225	PFM	DIP,SO	Yes	C,E,M	>90% efficiencies over wide I_{OUT} range (1mA to 225mA)	2.96
MAX649/651/652	4 to 16.5	5/3.3/3 or adj.	0.1(0.080)	2A	PFM	DIP,SO	Yes	C,E,M	>90% efficiency over wide I_{OUT} range, drives external P-channel FET	1.60
MAX1649/1651	4 to 16.5	5/3.3 or adj.	0.1(0.080)	2A	PFM	DIP,SO	Yes	C,E,M	Same as MAX649/651 but 96.5% duty cycle and only 100mV current-sense limit	1.60
MAX724/724H	3.5 to 40/60	Adj.(2.5 to 40)	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	4.52/6.83
MAX726	3.5 to 40/60	Adj.(2.5 to 40)	12(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX727	3.5 to 40/60	5	12(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX728	3.5 to 40/60	3.3	12(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00
MAX729	3.5 to 40/60	3	12(8.5)	2A	PWM	TO-220,TO-3		C,E,M	High power, few external components	3.00

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

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Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
MAX730A	5.2 to 11	5	3(1.7)	300	PWM	DIP,SO	Yes	C,E,M	90% efficiencies, no subharmonic switching noise	2.15
MAX738A	6 to 16	5	3(1.7)	750	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies, no subharmonic switching noise	2.60
MAX741D	2.7 to 15.5	5, adj.	4.25(2.8)	3A	PWM	DIP,SSOP	Yes	C,E,M	PWM step-down controller, 6.5V_{IN} to 5V_{OUT} at 3A, 90% efficient	3.64
MAX744A	4.75 to 16	5	2.5(1.2)	750	PWM	DIP,SO	Yes	C,E,M	Optimized for cellular communications, no subharmonic switching noise	2.90
MAX746	4 to 15	5/adj.	1	2.5A	PWM	DIP,SO		C,E,M	5V to 3.3V Green PC apps., drives external N-channel FET	2.25
MAX747	4 to 15	5/adj.	1.3(0.8)	2.5A	PWM	DIP,SO	Yes	C,E,M	5V to 3.3V Green PC apps., drives external P-channel FET	2.25
MAX748A	3.3 to 16	3.3	3(1.7)	750	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies, no subharmonic switching noise	2.60
MAX750A	4 to 11	Adj.	3(1.7)	1.5W	PWM	DIP,SO	Yes	C,E,M	90% efficiencies, no subharmonic switchin noise	2.15
MAX758A	4 to 16	Adj.	3(1.7)	3.75W	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies, no subharmonic switching noise	2.60
MAX763A	3.3 to 11	3.3	2.5(1.4)	500	PWM	DIP,SO	Yes	C,E,M	>85% efficiencies, no subharmonic switching noise	2.15
MAX767	4.5 to 5.5	3.3, 3.45 (R), or 3.6 (S)	0.75	7A	PWM	SSOP	Yes	C,E	Green PC apps., high-efficiency, small-size controller	3.40
MAX787/787H	3.5 to 40/60	5	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	††
MAX788/788H	3.5 to 40/60	3.3	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	††
MAX789/789H	3.5 to 40/60	3	12(8.5)	5A	PWM	TO-220,TO-3		C,E,M	High power, few external components	††
MAX796-799	4.5 to 30	5.05/3.3/2.9/adj.	1(0.7)	50W	PWM	DIP,SO	Yes	C,E,M	Synchronous rectifier, secondary output regulation, Idle-Mode PWM, high efficiency	††
MAX830-833	3.5 to 40	Adj./5/3/3.3	11(8)	1A	PWM	SO	Yes (MAX831)	C	High power, SOIC	††
INVERTING SWITCHING REGULATORS										
MAX4391	4 to 16.5	up to -20	0.25(0.09)	400mW	PFM	DIP,SO		C,E,M	Improved RC4391 2nd source	2.09
MAX634	2.3 to 16.5	up to -20	0.15(0.07)	400mW	PFM	DIP,SO		C,E,M	Improved RC4391 2nd source	2.61
MAX635	2.3 to 16.5	-5, adj.	0.15(0.08)	50	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX636	2.3 to 16.5	-12, adj.	0.15(0.08)	40	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX637	2.3 to 16.5	-15, adj.	0.15(0.07)	25	PFM	DIP,SO		C,E,M	Only 3 external components	2.56
MAX650	-54 to -42	5	10(0.5)	250	PFM	DIP,SO		C,E,M	Telecom applications	3.50
MAX735	4 to 6.2	-5	3(1.6)	275	PWM	DIP,SO		C,E,M	>80% efficiencies	2.15
MAX736	4 to 8.6	-12	3(1.6)	125	PWM	DIP,SO	Yes	C,E,M	>80% efficiencies	2.75
MAX737	4 to 5.5	-15	4.5(2.5)	100	PWM	DIP,SO	Yes	C,E,M	>80% efficiencies	2.75
MAX739	4 to 15	-5	3(1.6)	500	PWM	DIP,SO	Yes	C,E,M	>80% efficiencies	2.75
MAX741N	2.7 to 15.5	-5,-12,-15, adj.	4.0(2.2)	5W	PWM	DIP,SSOP		C,E,M	PWM inverting controller, high efficiency	3.64
MAX749	2 to 6	Adj.	0.06	5W	PFM	DIP,SO	Yes	C,E,M	Digital adjust for negative LCD	2.49
MAX755	2.7 to 9	Adj.	3.5(1.8)	1.4W	PWM	DIP,SO		C,E,M	>80% efficiencies	2.15
MAX759	4 to 15	Adj.	4(2.1)	1.5W	PWM	DIP,SO	Yes	C,E,M	LCD driver, >80% efficiencies	2.75
MAX764/765/766	3 to 16.5	-5/-12/-15 or adj. to 21ΔV	0.1	200	PFM	DIP,SO	Yes	C,E,M	High efficiency over wide I_{OUT} range	2.38
MAX774/775/776	3 to 16.5	-5/-12/-15 or adj.	0.1	1A	PFM	DIP,SO	Yes	C,E,M	Controllers, high efficiency over wide I_{OUT} range	2.20

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Control Scheme	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
DUAL-OUTPUT SWITCHING REGULATORS										
MAX742	4.2 to 10	±12, ±15	15(8)	±15W	PWM	DIP,SO		C,E,M	Drives external MOSFETs	3.91
MAX743	4.2 to 6	±12, ±15	30(20)	±1.5W	PWM	DIP,SO	Yes	C,E,M	Internal power MOSFETs	4.49

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA typ)	Package Options*	EV Kit	Temp. Ranges**	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS—UNREGULATED									
MAX1044	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.200(0.03)	20	DIP,SO		C,E,M	60kHz osc. boost mode	1.19
MAX660	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	DIP,SO		C,E,M	8-pin SOIC	2.95
MAX665	1.5 to 8	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	DIP,SO		C,E,M		3.96
MAX680	2 to 6	$\pm 2 \times V_{IN}$	2(1)	±10	DIP,SO		C,E,M	Dual output	1.62
MAX681	2 to 6	$\pm 2 \times V_{IN}$	2(1)	±10	DIP		C,E	No external components (internal caps)	4.64
MAX860/861	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.33(0.18)	50	SO, µMAX		C,E,M	Up to 250kHz oscillation frequency	1.45
ICL7660	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.175(0.110)	20	DIP,SO,TO-99, µMAX		C,E,M		1.09
ICL7662	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	0.6(0.25)	10	DIP,SO,TO-99		C,I		1.86
Si7661	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	2(0.3)	10	DIP,SO,TO-99		C,I		1.86
CHARGE-PUMP CONVERTERS—REGULATED									
MAX619	2 to 3.6	5	0.15	60	DIP,SO	Yes	C,E,M	No inductors	1.60
MAX622	3.5 to 16.5	V_{IN} + 11V	0.5(0.07)	500µA	DIP,SO		C,E	3 external capacitors, high-side switching MAX662	1.86
MAX623	3.5 to 16.5	V_{IN} + 11V	0.5(0.07)	500µA	DIP		C,E	No external capacitors, high-side switching	2.85
MAX662	Use MAX662A (pin-for-pin compatible upgrade)								–
MAX662A	4.5 to 5.5	12	0.5(0.19)	30mA, guaranteed over temp.	DIP,SO	Yes	C,E,M	Improved MAX662, flash memory programmer	2.09
MAX850-853	4.5 to 10	-4.1 or adj.	3(2)	5	SO	Yes	C,E	Negative GaAsFET bias, low noise, 1µA shutdown	1.65

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** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

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POWER MANAGEMENT

BATTERY CHARGERS

☆ **MAX712**
(NiCd/NiMH, zero voltage-slope detection)

☆ **MAX713**
(NiCd/NiMH, negative voltage-slope detection)

MULTI-FUNCTION SUPPLIES

2- OR 3-CELL PORTABLES

☆ **MAX717**
(3.3V & 12V flash prog.)

☆ **MAX718**
(3.3V/5V & 12V flash prog.)

☆ **MAX719**
(3V/5V & 12V flash prog.)

MAX720
(3.3V/5V & 12V flash prog.)

MAX721
(3V/5V & 12V flash prog.)

☆ **MAX722**
(3.3V/5V_{OUT}, neg. LCD)

☆ **MAX723**
(3V/5V_{OUT}, neg. LCD)

5- OR 6-CELL PORTABLES

MAX714
(2 at +5V, -26V LCD, µP super.)

MAX715
(3 at +5V, -26V LCD, -5V, +12V, µP super.)

☆ **MAX716**
(4 at +5V, -26V LCD, -5V, +12V, µP super.)

5 to 12 CELL PORTABLES/ NOTEBOOKS

☆★† **MAX781**
(3.3V, battery charger, PCMCIA)

☆ **MAX782**
(3.3V, 5V, PCMCIA)

☆ **MAX783**
(3.3V, 5V, PCMCIA, optimized for 6-cell inputs)

MAX786
(3.3V, 5V)

LOW-SIDE MOSFET DRIVERS

MAX626
(2A, 4Ω, dual inverting)

MAX627
(2A, 4Ω, dual noninverting)

MAX628
(2A, 4Ω, dual mixed)

MAX4420
(6A, 1.5Ω, single noninverting)

MAX4426
(1.5A, 4Ω, dual inverting)

MAX4427
(1.5A, 4Ω, dual noninverting)

MAX4428
(1.5A, 4Ω, dual mixed)

MAX4429
(6A, 1.5Ω, single inverting)

TSC426
(1.5A, 6Ω, dual inverting)

TSC427
(1.5A, 6Ω, dual noninverting)

TSC428
(1.5A, 6Ω, dual mixed)

MXT429
(6A, 1.5Ω, single inverting)

ICL7667
(1.5A, 4Ω, dual inverting)

HIGH-SIDE MOSFET DRIVERS

MAX613
(PCMCIA controller, dual V_{PP})

MAX614
(PCMCIA controller, single V_{PP})

MAX620 (quad driver)

MAX621
(quad driver, internal caps)

MAX622
($V_{OUT} = V_{IN} + 11V$)

MAX623
($V_{OUT} = V_{IN} + 11V$, internal caps)

MAX625
(quad driver, internal MOSFETs & caps)

MAX780
(PCMCIA controller, 4 level translators, dual V_{PP}, power ready)

★ **New product**
† **Future product**
☆ **Evaluation kit available**

Power Management Supplies

Part Number	Input Voltage Range (V)	Linear Output Voltage (V)	DC-DC Output Voltages (V)	Auxiliary Outputs (V)	Quiescent Supply Current, Over Temp. (µA max)	EV Kit	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX714	5.05 to 11	2 at +5V	-5 to -26 adj. LCD driver	–	200 per enabled output line		DIP,SO	C,E,M	Independent shutdowns, backup-battery switchover, $\overline{\text{RESET}}$ and power-fail warning outputs	3.40
MAX715	5.05 to 11	3 at +5V	-5 to -26 adj.	-5 adj., +12 or +15 adj.	200 per enabled output line		DIP,SO	C,E,M	PC layout and parts list available	5.75
MAX716	5.05 to 11	4 at +5V	-5 to -26 adj.	-5 adj., +12 or +15 adj.	200 per enabled output line	Yes	DIP,SO SSOP	C,E,M,	Independent shutdowns, backup-battery switchover, $\overline{\text{RESET}}$ and power-fail warning outputs	5.95
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	–	+3.3 (MAX717), +3.3 or +5 (MAX718/720), +3.0 or +5 (MAX719/721)	+5 or +12 (all)	60, 40 shutdown	Yes (MAX717-MAX719)	SO	C,E	Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX722/723	0.85 to 5.5 (battery), 7 to 18 (plug-in adapter)	–	+3.3 or +5 (MAX722), +3 or +5 (MAX723)	Neg. LCD (0 to -40)	60, 40 shutdown	Yes	SO	C,E	Built-in switchover from main batttery to plug-in adapter power, low-voltage warning	4.63
MAX781	5 to 18	3.3 at 10mA 5.0 at 25mA	3.3, 14, battery charger	Battery charger, current source, dual V_{PP} outputs	100 shutdown, 750 standby, 2mA operating	Yes	SSOP	C,E	High-power controller to 50W or more, dual PCMCIA V_{PP} outputs, analog mux, SPI interface	††
MAX782	5.5 to 30 5.0 at 25mA	3.3 at 5mA	3.3‡, 5.0, 14	Dual V_{PP} outputs 750 per output	70 standby, enabled	Yes	SSOP	C,E	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors,	5.95
MAX783	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3‡, 5.0, 14	Dual V_{PP} outputs	70 standby 750 per output enabled	Yes	SSOP	C,E	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors, optimized for 6-cell operation	5.95
MAX786	5.5 to 30	3.3 at 5mA 5.0 at 25mA	3.3‡, 5.0	–	40 shutdown 70 standby 750 per output enabled		SSOP	C,E	High-power dual controller to 50W or more, two precision voltage monitors	4.15

Battery Chargers

Part Number	No. of Cells Charged	Fast-Charge Rate	Trickle-Charge Rates	Charge Termination Method	EV Kit	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX712	1 to 16 NiMH	C/3 to 4C	C/16, adj.	$\Delta V/\Delta t = 0$, Temp., Timer	Yes	DIP,SO	C,E,M	Inexpensive, few external components, uses switch-mode regulator or linear regulator to control current, supply load while charging	3.09
MAX713	1 to 16 NiMH or NiCd	C/3 to 4C	C/16, adj.	$\Delta V/\Delta t < 0$, Temp., Timer	Yes	DIP,SO	C,E,M	Inexpensive, few external components, uses switch-mode regulator or linear regulator to control current, supply load while charging	3.09

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

‡ Or 3.45V ("R" version), 3.6V ("S" version)

MOSFET Drivers

Part Number	Output Resistance (Ω), max(typ)	Rise/Fall, T_A=+25°C (ns max)	Rise/Fall, Over Temp. (ns max)	Peak Output Current (A)	Supply Voltage (V)	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX4420/4429	2.5(1.5)	30/30(2500pF)	60/60(2500pF)	6	4.5 to 18	DIP,SO	C,E,M	Single noninverting/single inverting	1.71
MAX4426/4427/4428	10(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 18	DIP,SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.61
MAX626/627/628	15(4)	30/30(1000pF)	40/40(1000pF)	2	4.5 to 18	DIP,SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.49
TSC426/427/428	15(6)	30/30(1000pF)	60/40(1000pF)	1.5	4.5 to 18	DIP,SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.06
MXT429	2.5(1.5)	35/35(2500pF)	70/70(2500pF)	6	7.0 to 18	DIP,SO	C,E,M	Single inverting	1.67
ICL7667	12(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 15	DIP,SO	C,E,M	Dual inverting	1.12

High-Side MOSFET Drivers

Part Number	Supply Voltage Range (V)	Quiescent Supply Current (mA), max(typ)	Switching Frequency (kHz)	Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX620	4.5 to 16.5	0.5(0.070)	70	DIP,SO	C,E	Quad high-side driver, V_{CC} + 11V output	3.85
MAX621	4.5 to 16.5	0.5(0.070)	70	DIP	C,E	Quad high-side driver, V_{CC} + 11V output, internal capacitors	5.82
MAX625	4.5 to 16.5	0.5(0.070)	70	DIP	C,E	Quad high-side switch, 4 internal 0.2Ω N-channel MOSFETs, internal capacitors	9.98

PCMCIA / Flash Memory Supplies

Part Number	Input Voltage Range (V)	12V Output Current (mA)	EV Kit	Package Options*	Features	Price† 1000-up ($)
MAX613	3.3/5/12	Two V_{PP} outputs, 60mA each		DIP,SO	Industry-standard interface	1.68
MAX614	3.3/5/12	One V_{PP} output, 60mA		DIP,SO	Industry-standard interface	1.48
MAX662A	4.5 to 5.5	30	Yes	DIP,SO	No inductors, low cost, C/E/M temp. ranges	2.09
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	120	Yes (MAX717/18/19)	SO	Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX732	4.0 to 9.3	200	Yes	DIP,SO	4% output tolerance	2.76
MAX734	1.9 to 12	120	Yes	DIP,SO	Small 8-pin package, adjustable soft-start	2.23
MAX761	2 to 16.5	120	Yes	DIP,SO	12V flash programmer, high efficiency over wide I_{OUT} range	2.23
MAX780	3.3/5/12	Two V_{PP} outputs, 60mA each		DIP,SO	Industry-standard interface, V_{PP} outputs, V_{CC} control	2.25

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C

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Linear Voltage Regulators

Part Number	Input Voltage Range (V)	Output Voltage (V)	Dropout Voltage (V)	Quiescent Current (µA), max(typ)	Output Voltage Accuracy (%)	Shutdown	Package Options*	Temp. Ranges**	Price† 1000-up ($)
DC LINEAR REGULATORS—POSITIVE OUTPUT									
MAX603	2.8 to 11.5	5 or adj. (1.3 to 11.5)	0.25 at 500mA	35(15)	±5	2µA off	DIP,SO (P_{DISS} = 1.6W)	C,E,M	††
MAX604	2.8 to 11.5	3.3 or adj. (1.3 to 11.5)	0.5 at 500mA	35(15)	±5	2µA off	DIP,SO (P_{DISS} = 1.6W)	C,E,M	††
MAX663	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	DIP,SO	C,E,M	1.91
MAX666	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	DIP,SO	C,E,M	2.22
MAX667	3.5 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.15 at 200mA	25(20)	±4	Yes	DIP,SO	C,E,M	2.35
MAX687	2.7 to 11	3.0	0.2 at 500mA	150(250)	±3	Yes 25µA, off 1µA	DIP,SO	C,E	††
MAX688	2.7 to 11	3.3	0.2 at 500mA	150(250)	±3	Yes 25µA, off 1µA	DIP,SO	C,E	††
MAX689	2.7 to 11	3.0	0.2 at 500mA	150(250)	±3	Yes 25µA, off 1µA	DIP,SO	C,E	††
MAX882	2.8 to 11.5	3.3 or adj. (1.5 to 11.25)	0.25 at 200mA	18(7)	±5	18µA standby	DIP,SO (P_{DISS} = 1W)	C,E,M	††
MAX883	2.8 to 11.5	5 or adj. (1.5 to 11.25)	0.25 at 300mA	18(7)	±5	1µA off	DIP,SO (P_{DISS} = 1W)	C,E,M	††
MAX884	2.8 to 11.5	3.3 or adj. (1.5 to 11.25)	0.25 at 200mA	18(7)	±5	1µA off	DIP,SO (P_{DISS} = 1W)	C,E,M	††
ICL7663	1.5 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±8	Yes	DIP,SO,TO-99	C,E,I,M	1.81
ICL7663A	2.0 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±1.9	Yes	DIP,SO,TO-99	C,E,I,M	1.99
DC LINEAR REGULATORS—NEGATIVE OUTPUT									
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	0.35 at 40mA	12(6)	±5	Yes	DIP,SO	C,E,M	2.33
ICL7664A	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±1	Yes	DIP,SO,TO-99	C,I,M	1.56

Display Power Supplies

Part Number	Input Voltage Range (V)	DC-DC Output Voltages (V)	Quiescent Supply Current (µA typ)	EV Kit	Package Options*	Features	Price† 1000-up ($)
MAX749	2 to 6	Negative LCD	60	Yes	DIP,SO	Digital LCD adjustment	2.49
MAX753	6 to 24	CCFT drive, configurable; negative LCD, configurable	100		DIP,SO	Digital CCFT and LCD adjustment	††
MAX754	6 to 24	CCFT drive, configurable; positive LCD, configurable	100		DIP,SO	Digital CCFT and LCD adjustment	††
MAX759	4 to 15	Negative LCD, adjustable	1.2mA	Yes	DIP,SO	Internal MOSFET	2.75

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

MAXIM

5V/3.3V or Adjustable, High-Efficiency, Low Dropout, Step-Down DC-DC Controllers

General Description

The MAX1649/MAX1651 BiCMOS, step-down, DC-DC switching controllers provide high efficiency over loads ranging from 10mA to more than 2.5A. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 100µA of supply current (vs. 2mA to 10mA for PWM converters). Dropout performance down to 300mV is provided by a high switch duty cycle (96.5%) and a single current-sense threshold (110mV).

These devices use miniature external components. Their high switching frequency (up to 300kHz) allows for less than 9mm diameter surface-mount inductors.

The MAX1649/MAX1651 have dropout voltages less than 0.3V at 500mA and accept input voltages up to 16V. Output voltages are preset at 5V (MAX1649), or 3.3V (MAX1651). They can also be adjusted to any voltage from 1.5V to the input voltage by using two resistors.

These step-down controllers drive external P-channel MOSFETs at loads greater than 12.5W. If less power is required, use the MAX639/MAX640/MAX653 step-down converters with on-chip FETs, which allow up to a 225mA load current.

Applications

PDAs

High-Efficiency Step-Down Regulation

5V-to-3.3V Green PC Applications

Battery-Powered Applications

Features

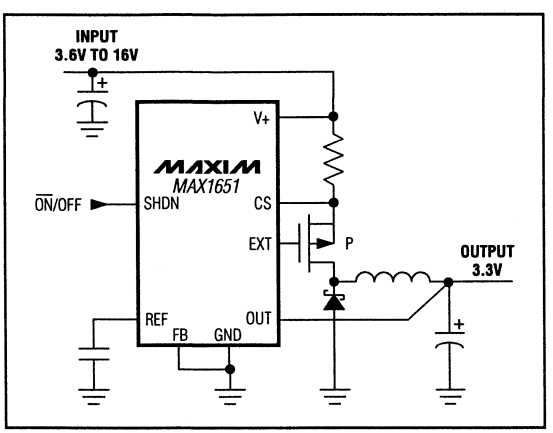
- **More than 90% Efficiency (10mA to 1.5A Loads)**
- **Up to 96.5% Duty Cycle**
- **More than 12.5W Output Power**
- **Less than 0.3V Dropout Voltage at 500mA**
- **100µA Max Quiescent Supply Current**
- **5µA Max Shutdown Supply Current**
- **16V Max Input Voltage**
- **5V (MAX1649), 3.3V (MAX1651), or Adjustable Output Voltage**
- **Current-Limited Control Scheme**
- **Up to 300kHz Switching Frequency**

Ordering Information

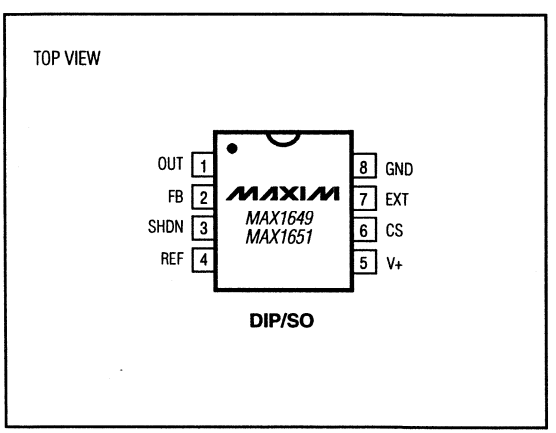
PART	TEMP. RANGE	PIN-PACKAGE
MAX1649CPA	0°C to +70°C	8 Plastic DIP
MAX1649CSA	0°C to +70°C	8 SO
MAX1649C/D	0°C to +70°C	Dice*
MAX1649EPA	-40°C to +85°C	8 Plastic DIP
MAX1649ESA	-40°C to +85°C	8 SO
MAX1651CPA	0°C to +70°C	8 Plastic DIP
MAX1651CSA	0°C to +70°C	8 SO
MAX1651C/D	0°C to +70°C	Dice*
MAX1651EPA	-40°C to +85°C	8 Plastic DIP
MAX1651ESA	-40°C to +85°C	8 SO

* *Dice are tested at T_A = +25°C.*

Typical Operating Circuit



Pin Configuration



19-0263; Rev 0; 6/94

EVALUATION KIT AVAILABLE

MAXIM

12V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller

General Description

The MAX1771 step-up switching controller provides 90% efficiency over a 30mA to 2A load. A unique current-limited pulse-frequency-modulation (PFM) control scheme gives this device the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using less than 110µA of supply current (vs. 2mA to 10mA for PWM converters).

This controller uses miniature external components. Its high switching frequency (up to 300kHz) allows surface-mount magnetics of 5mm height and 9mm diameter. It accepts input voltages from 2V to 16.5V. The output voltage is preset at 12V, or can be adjusted using two resistors.

The MAX1771 optimizes efficiency at low input voltages and reduces noise by using a single 100mV current-limit threshold under all load conditions. A family of similar devices, the MAX770–MAX773, trades some full-load efficiency for greater current-limit accuracy; they provide a 200mV current limit at full load, and switch to 100mV for light loads.

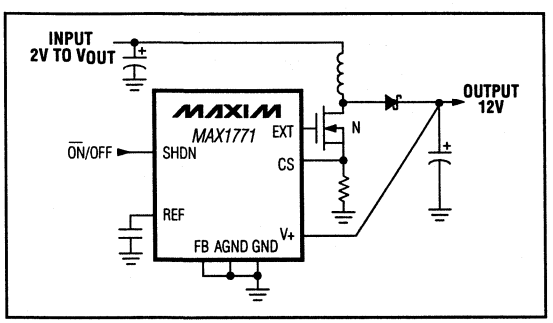
The MAX1771 drives an external N-channel MOSFET switch, allowing it to power loads up to 24W. If less power is required, use the MAX756/MAX757 or MAX761/MAX762 step-up switching regulators with on-board MOSFETs.

An evaluation kit is available. Order the MAX770EVKIT-SO plus a MAX1771CSA sample.

Applications

Flash Memory Programmers
Palmtops/Hand-Held Terminals
High-Efficiency DC-DC Converters
Battery-Powered Applications
Positive LCD-Bias Generators
Portable Communicators

Typical Operating Circuit



Features

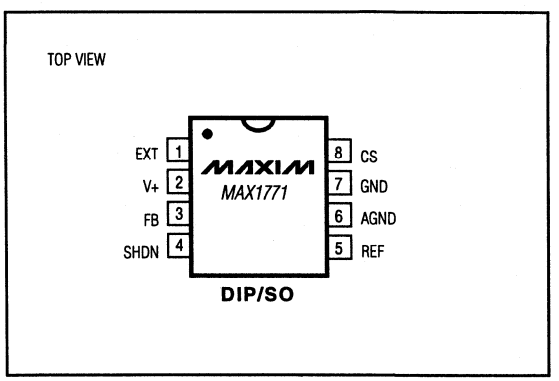
- ♦ **90% Efficiency for 30mA to 2A Load Currents**
- ♦ **Up to 24W Output Power**
- ♦ **110µA Max Supply Current**
- ♦ **5µA Max Shutdown Current**
- ♦ **2V to 16.5V Input Range**
- ♦ **Preset 12V or Adjustable Output Voltage**
- ♦ **Current-Limited PFM Control Scheme**
- ♦ **Up to 300kHz Switching Frequency**
- ♦ **Evaluation Kit Available**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1771CPA	0°C to +70°C	8 Plastic DIP
MAX1771CSA	0°C to +70°C	8 SO
MAX1771C/D	0°C to +70°C	Dice*
MAX1771EPA	-40°C to +85°C	8 Plastic DIP
MAX1771ESA	-40°C to +85°C	8 SO
MAX1771MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883B.*

Pin Configuration



12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V+ to GND .....-0.3V, 17V
EXT, CS, REF, SHDN, FB to GND .....-0.3V, (V+ + 0.3V)
GND to AGND.....0.1V, -0.1V
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX1771C_A .....0°C to +70°C
MAX1771E_A .....-40°C to +85°C
MAX1771MJA .....-55°C to +125°C
Junction Temperatures
MAX1771C_A/E_A.....+150°C
MAX1771MJA .....+175°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		MAX1771 (internal feedback resistors)		2.0		12.5	V
		MAX1771C/E (external resistors)		3.0		16.5	
		MAX1771MJA (external resistors)		3.1		16.5	
Minimum Start-Up Voltage					1.8	2.0	V
Supply Current		V+ = 16.5V, SHDN = 0V (normal operation)			85	110	µA
Standby Current		V+ = 10.0V, SHDN ≥ 1.6V (shutdown)			2	5	µA
		V+ = 16.5V, SHDN ≥ 1.6V (shutdown)			4		
Output Voltage (Note 1)		V+ = 2.0V to 12.0V, over full load range, Circuit of Figure 2a		11.52	12.0	12.48	V
Output Voltage Line Regulation (Note 2)		V+ = 5V to 7V, V_{OUT} = 12V I_{LOAD} = 700mA, Circuit of Figure 2a			5		mV/V
Output Voltage Load Regulation (Note 2)		V+ = 6V, V_{OUT} = 12V, I_{LOAD} = 0mA to 500mA, Circuit of Figure 2a			20		mV/A
Maximum Switch On-Time	t_{ON}(max)			12	16	20	µs
Minimum Switch Off-Time	t_{OFF}(min)			1.8	2.3	2.8	µs
Efficiency		V+ = 5V, V_{OUT} = 12V, I_{LOAD} = 500mA, Circuit of Figure 2a			92		%
Reference Voltage	V_{REF}	I_{REF} = 0µA	MAX1771C	1.4700	1.5	1.5300	V
			MAX1771E	1.4625	1.5	1.5375	
			MAX1771M	1.4550	1.5	1.5450	
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA	MAX1771C/E		4	10	mV
			MAX1771M		4	15	
REF Line Regulation		3V ≤ V+ ≤ 16.5V			40	100	µV/V
FB Trip Point Voltage	V_{FB}	MAX1771C		1.4700	1.5	1.5300	V
		MAX1771E		1.4625	1.5	1.5375	
		MAX1771M		1.4550	1.5	1.5450	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FB Input Current	I_{FB}	MAX1771C				±20	nA
		MAX1771E				±40	
		MAX1771M				±60	
SHDN Input High Voltage	V_{IH}	V+ = 2.0V to 16.5V		1.6			V
SHDN Input Low Voltage	V_{IL}	V+ = 2.0V to 16.5V				0.4	V
SHDN Input Current		V+ = 16.5V, SHDN = 0V or V+				±1	µA
Current-Limit Trip Level	V_{CS}	V+ = 5V to 16V	MAX1771C/E	85	100	115	mV
			MAX1771M	75	100	125	
CS Input Current					0.01	±1	µA
EXT Rise Time		V+ = 5V, 1nF from EXT to ground			55		ns
EXT Fall Time		V+ = 5V, 1nF from EXT to ground			55		ns

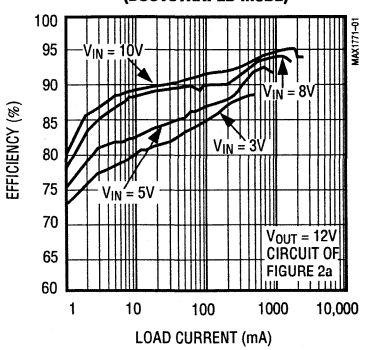
Note 1: Output voltage guaranteed using preset voltages. See Figures 4a–4d for output current capability versus input voltage.
Note 2: Output voltage line and load regulation depend on external circuit components.

4

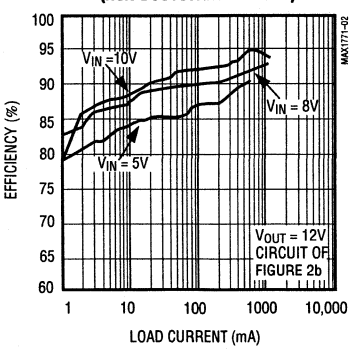
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

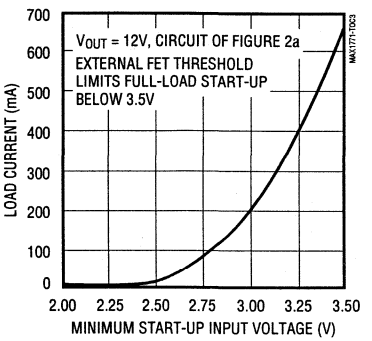
EFFICIENCY vs. LOAD CURRENT (BOOTSTRAPED MODE)



EFFICIENCY vs. LOAD CURRENT (NON-BOOTSTRAPED MODE)



LOAD CURRENT vs. MINIMUM START-UP INPUT VOLTAGE

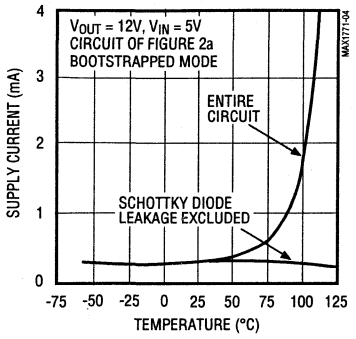


12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller

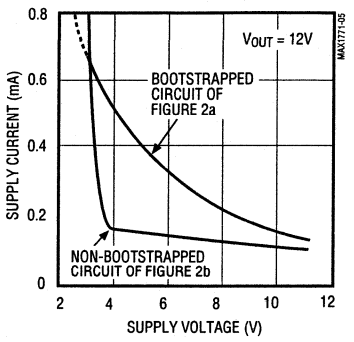
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

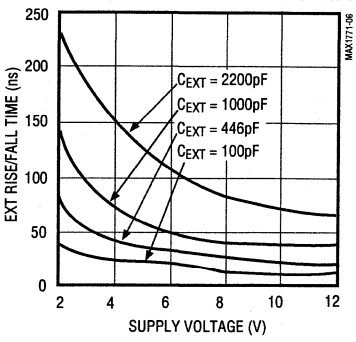
SUPPLY CURRENT vs. TEMPERATURE



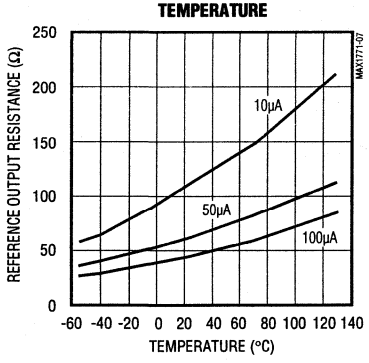
SUPPLY CURRENT vs. SUPPLY VOLTAGE



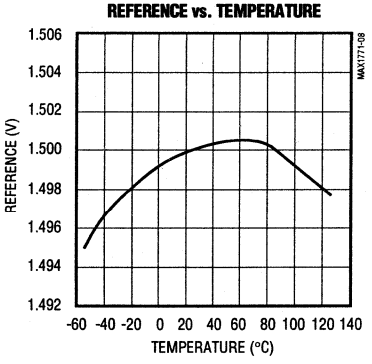
EXT RISE/FALL TIME vs. SUPPLY VOLTAGE



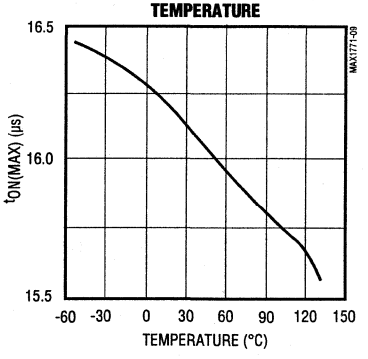
REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE



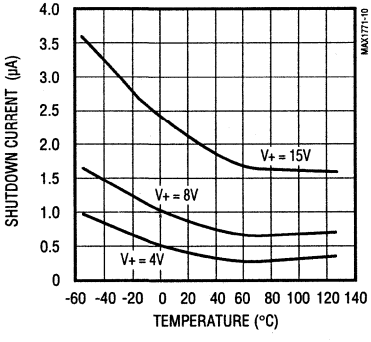
REFERENCE vs. TEMPERATURE



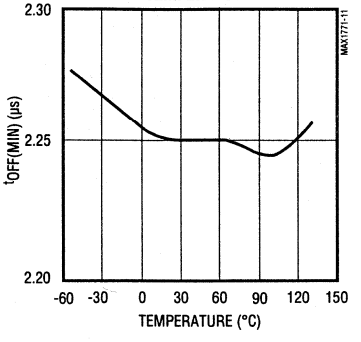
MAXIMUM SWITCH ON-TIME vs. TEMPERATURE



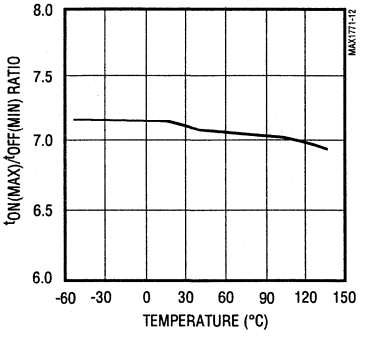
SHUTDOWN CURRENT vs. TEMPERATURE



MINIMUM SWITCH OFF-TIME vs. TEMPERATURE



MAXIMUM SWITCH ON-TIME/ MINIMUM SWITCH OFF-TIME RATIO vs. TEMPERATURE

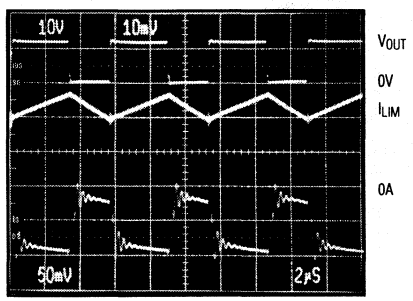


12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, T_A = +25°C, unless otherwise noted.)

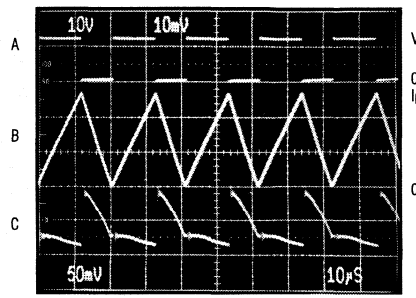
HEAVY-LOAD SWITCHING WAVEFORMS



2µs/div

V_{IN} = 5V, I_{OUT} = 900mA, V_{OUT} = 12V
A: EXT VOLTAGE, 10V/div
B: INDUCTOR CURRENT, 1A/div
C: V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

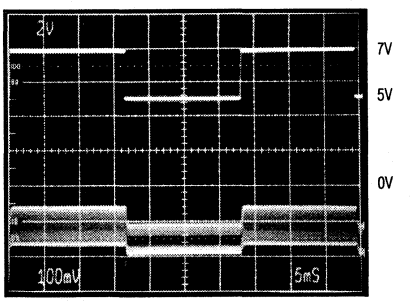
MEDIUM-LOAD SWITCHING WAVEFORMS



10µs/div

V_{IN} = 5V, I_{OUT} = 500mA, V_{OUT} = 12V
A: EXT VOLTAGE, 10V/div
B: INDUCTOR CURRENT, 1A/div
C: V_{OUT} RIPPLE, 50mV/div, AC-COUPLED

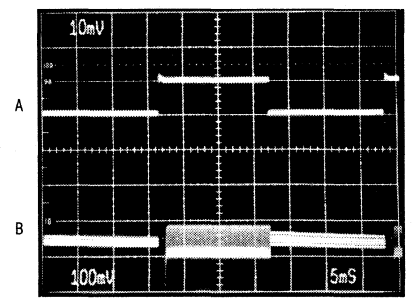
LINE-TRANSIENT RESPONSE



5ms/div

I_{OUT} = 700mA, V_{OUT} = 12V
A: V_{IN}, 5V to 7V, 2V/div
B: V_{OUT} RIPPLE, 100mV/div, AC-COUPLED

LOAD-TRANSIENT RESPONSE



5ms/div

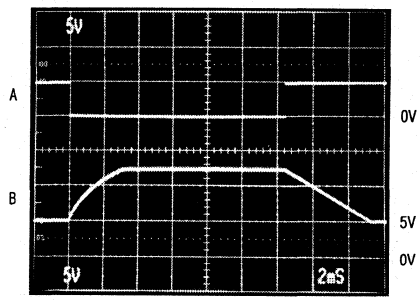
V_{IN} = 6V, V_{OUT} = 12V
A: LOAD CURRENT, 0mA to 500mA, 500mA/div
B: V_{OUT} RIPPLE, 100mV/div, AC-COUPLED

12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, T_A = +25°C, unless otherwise noted.)

ENTERING/EXITING SHUTDOWN



I_{OUT} = 500mA, V_{IN} = 5V
A: SHDN, 5V/div
B: V_{OUT}, 5V/div

Pin Description

PIN	NAME	FUNCTION
1	EXT	Gate Drive for External N-Channel Power Transistor
2	V+	Power-Supply Input. Also acts as a voltage-sense point when in bootstrapped mode.
3	FB	Feedback Input for Adjustable-Output Operation. Connect to ground for fixed-output operation. Use a resistor divider network to adjust the output voltage. See *Setting the Output Voltage* section.
4	SHDN	Active-High TTL/CMOS Logic-Level Shutdown Input. In shutdown mode, V_{OUT} is a diode drop below V+ (due to the DC path from V+ to the output) and the supply current drops to 5µA maximum. Connect to ground for normal operation.
5	REF	1.5V Reference Output that can source 100µA for external loads. Bypass to GND with 0.1µF. The reference is disabled in shutdown.
6	AGND	Analog Ground
7	GND	High-Current Ground Return for the Output Driver
8	CS	Positive Input to the Current-Sense Amplifier. Connect the current-sense resistor between CS and GND.

Detailed Description

The MAX1771 is a BiCMOS, step-up, switch-mode power-supply controller that provides a preset 12V output, in addition to adjustable-output operation. Its unique control scheme combines the advantages of pulse-frequency modulation (low supply current) and pulse-width modulation (high efficiency with heavy loads), providing high efficiency over a wide output current range, as well as increased output current capability over previous PFM devices. In addition, the external sense resistor and power transistor allow the user to tailor the output current capability for each application. Figure 1 shows the MAX1771 functional diagram.

The MAX1771 offers three main improvements over prior pulse-skipping control solutions: 1) the converter operates with miniature (5mm height and less than 9mm diameter) surface-mount inductors due to its 300kHz switching frequency; 2) the current-limited PFM control scheme allows 90% efficiencies over a wide range of load currents; and 3) the maximum supply current is only 110µA.

The device has a shutdown mode that reduces the supply current to 5µA max.

Bootstrapped/Non-Bootstrapped Modes

Figure 2 shows the standard application circuits for bootstrapped and non-bootstrapped modes. In bootstrapped mode, the IC is powered from the output (V_{OUT}, which is connected to V+) and the input voltage range is 2V to V_{OUT}. The voltage applied to the gate of the external power transistor is switched from V_{OUT} to ground, providing more switch gate drive and thus reducing the transistor's on resistance.

In non-bootstrapped mode, the IC is powered from the input voltage (V+) and operates with minimum supply current. In this mode, FB is the output voltage sense point. Since the voltage swing applied to the gate of the external power transistor is reduced (the gate swings from V+ to ground), the power transistor's on resistance

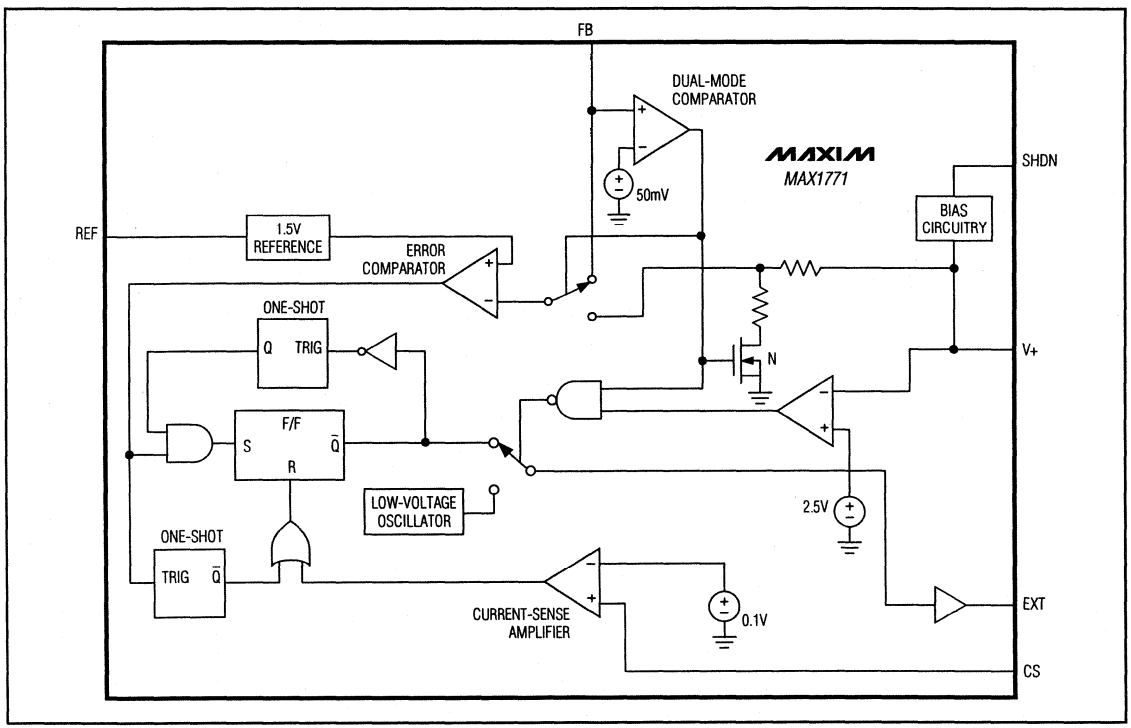


Figure 1. Functional Diagram

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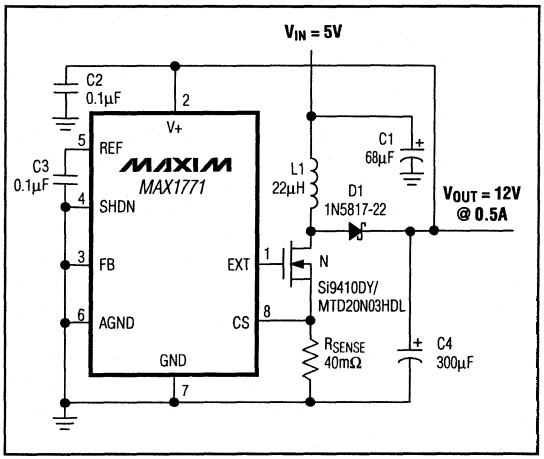

Figure 2a. 12V Preset Output, Bootstrapped

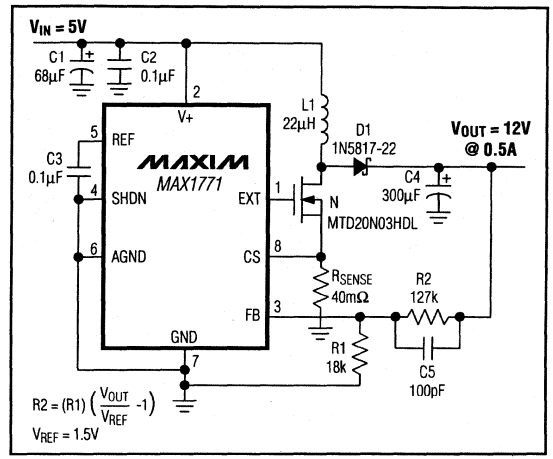

Figure 2b. 12V Output, Non-Bootstrapped

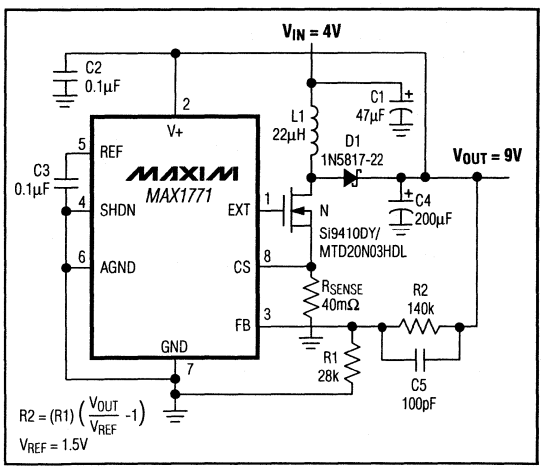

Figure 2c. 9V Output, Bootstrapped

increases at low input voltages. However, the supply current is also reduced because V+ is at a lower voltage, and because less energy is consumed while charging and discharging the external MOSFET's gate capacitance. The minimum input voltage is 3V when using external feedback resistors. With supply voltages below 5V, bootstrapped mode is recommended.

Note: When using the MAX1771 in non-bootstrapped mode, there is no preset output operation because V+ is also the output voltage sense point for fixed-output operation. External resistors must be used to set the output voltage. Use 1% external feedback resistors when operating in adjustable-output mode (Figures 2b, 2c) to achieve an overall output voltage accuracy of ±5%. To achieve highest efficiency, operate in bootstrapped mode whenever possible.

External Power-Transistor Control Circuitry

PFM Control Scheme

The MAX1771 uses a proprietary current-limited PFM control scheme to provide high efficiency over a wide range of load currents. This control scheme combines the ultra-low supply current of PFM converters (or pulse skippers) with the high full-load efficiency of PWM converters.

Unlike traditional PFM converters, the MAX1771 uses a sense resistor to control the peak inductor current. The device also operates with high switching frequencies (up to 300kHz), allowing the use of miniature external components.

As with traditional PFM converters, the power transistor is not turned on until the voltage comparator senses the output is out of regulation. However, unlike traditional PFM converters, the MAX1771 switch uses the combination of a peak current limit and a pair of one-shots that set the maximum on-time (16µs) and minimum off-time (2.3µs); there is no oscillator. Once off, the minimum off-time one-shot holds the switch off for 2.3µs. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The control circuitry allows the IC to operate in continuous-conduction mode (CCM) while maintaining high efficiency with heavy loads. When the power switch is turned on, it stays on until either 1) the maximum on-time one-shot turns it off (typically 16µs later), or 2) the switch current reaches the peak current limit set by the current-sense resistor.

The MAX1771 switching frequency is variable (depending on load current and input voltage), causing variable switching noise. However, the subharmonic noise generated does not exceed the peak current limit times the filter capacitor equivalent series resistance (ESR). For example, when generating a 12V output at 500mA from a 5V input, only 100mV of output ripple occurs using the circuit of Figure 2a.

Low-Voltage Start-Up Oscillator

The MAX1771 features a low input voltage start-up oscillator that guarantees start-up with no load down to 2V when operating in bootstrapped mode and using internal feedback resistors. At these low voltages, the supply voltage is not large enough for proper error-comparator operation and internal biasing. The start-up oscillator has a fixed 50% duty cycle and the MAX1771 disregards the error-comparator output when the supply voltage is less than 2.5V. Above 2.5V, the error-comparator and normal one-shot timing circuitry are used. The low-voltage start-up circuitry is disabled if non-bootstrapped mode is selected (FB is not tied to ground).

Shutdown Mode

When SHDN is high, the MAX1771 enters shutdown mode. In this mode, the internal biasing circuitry is turned off (including the reference) and V_{OUT} falls to a diode drop below V_{IN} (due to the DC path from the input to the output). In shutdown mode, the supply current drops to less than 5µA. SHDN is a TTL/CMOS logic-level input. Connect SHDN to GND for normal operation.

Design Procedure

Setting the Output Voltage

To set the output voltage, first determine the mode of operation, either bootstrapped or non-bootstrapped. Bootstrapped mode provides more output current capability, while non-bootstrapped mode reduces the supply current (see *Typical Operating Characteristics*). If a decaying voltage source (such as a battery) is used, see the additional notes in the *Low Input Voltage Operation* section.

The MAX1771's output voltage can be adjusted from very high voltages down to 3V, using external resistors

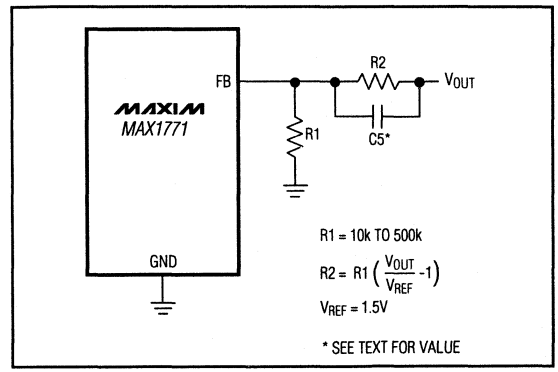

Figure 3. Adjustable Output Circuit

R1 and R2 configured as shown in Figure 3. For adjustable-output operation, select feedback resistor R1 in the 10kΩ to 500kΩ range. R2 is given by:

$$R2 = (R1)\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} equals 1.5V.

For preset-output operation, tie FB to GND (this forces bootstrapped-mode operation.

Figure 2 shows various circuit configurations for bootstrapped/non-bootstrapped, preset/adjustable operation.

Determining R_{SENSE}

Use the theoretical output current curves shown in Figures 4a–4d to select R_{SENSE}. They were derived using the minimum (worst-case) current-limit comparator threshold value over the extended temperature range (-40°C to +85°C). No tolerance was included for R_{SENSE}. The voltage drop across the diode was assumed to be 0.5V, and the drop across the power switch $r_{DS(ON)}$ and coil resistance was assumed to be 0.3V.

Determining the Inductor (L)

Practical inductor values range from 10µH to 300µH. 22µH is a good choice for most applications. In applications with large input/output differentials, the IC's output current capability will be much less when the inductance value is too low, because the IC will always operate in discontinuous mode. If the inductor value is too low, the current will ramp up to a high level before the current-limit comparator can turn off the switch. The minimum on-time for the switch (t_{ON}(min)) is

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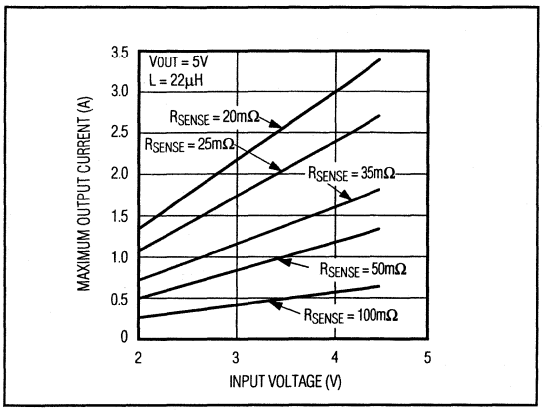

Figure 4a. Maximum Output Current vs. Input Voltage (V_{OUT} = 5V)

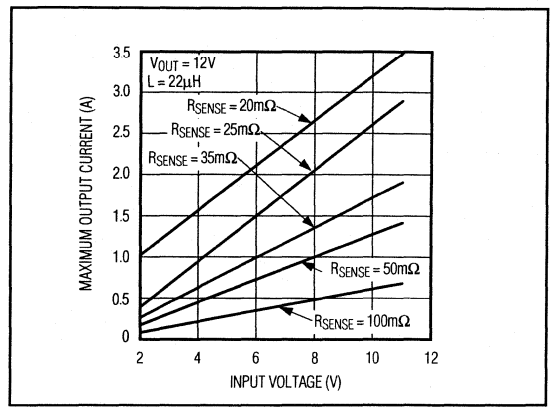

Figure 4b. Maximum Output Current vs. Input Voltage (V_{OUT} = 12V)

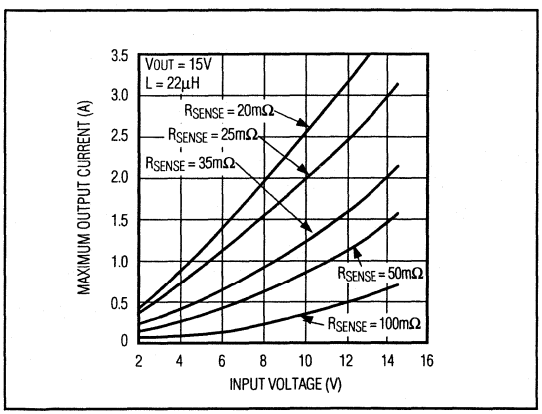

Figure 4c. Maximum Output Current vs. Input Voltage (V_{OUT} = 15V)

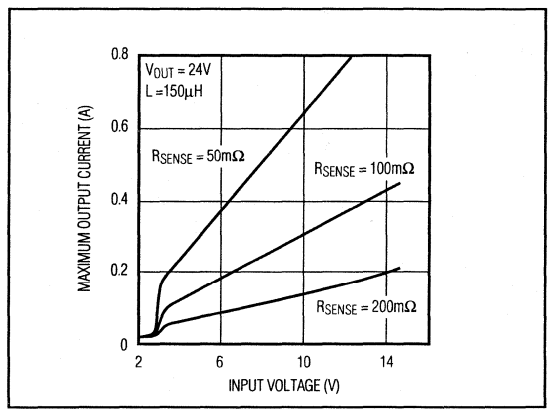

Figure 4d. Maximum Output Current vs. Input Voltage (V_{OUT} = 24V)

approximately 2µs; select an inductor that allows the current to ramp up to I_{LIM}.

The standard operating circuits use a 22µH inductor. If a different inductance value is desired, select L such that:

$$L \geq \frac{V_{IN(max)} \times 2\mu s}{I_{LIM}}$$

Larger inductance values tend to increase the start-up time slightly, while smaller inductance values allow the coil current to ramp up to higher levels before the switch turns off, increasing the ripple at light loads.

Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current rating set by R_{SENSE}. However, it is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, use a coil with low DC resistance, preferably under 20mΩ. To minimize radiated noise, use a toroid, a pot core, or a shielded coil.

Table 1 lists inductor suppliers and specific recommended inductors.

Power Transistor Selection

Use an N-channel MOSFET power transistor with the MAX1771.

To ensure the external N-channel MOSFET (N-FET) is turned on hard, use logic-level or low-threshold N-FETs when the input drive voltage is less than 8V. This applies even in bootstrapped mode, to ensure start-up. N-FETs provide the highest efficiency because they do not draw any DC gate-drive current.

When selecting an N-FET, three important parameters are the total gate charge (Q_G), on resistance ($r_{DS(ON)}$), and reverse transfer capacitance (C_{RSS}).

Q_G takes into account all capacitances associated with charging the gate. Use the typical Q_G value for best results; the maximum value is usually grossly over-specified since it is a guaranteed limit and not the measured value. The typical total gate charge should be 50nC or less. With larger numbers, the EXT pins may not be able to adequately drive the gate. The EXT rise/fall time varies with different capacitive loads as shown in the *Typical Operating Characteristics*.

The two most significant losses contributing to the N-FET's power dissipation are I^2R losses and switching losses. Select a transistor with low $r_{DS(ON)}$ and low C_{RSS} to minimize these losses.

Determine the maximum required gate-drive current from the Q_G specification in the N-FET data sheet.

The MAX1771's maximum allowed switching frequency during normal operation is 300kHz; but at start-up, the maximum frequency can be 500kHz, so the maximum current required to charge the N-FET's gate is f(max) x Q_G(typ). Use the typical Q_G number from the transistor data sheet. For example, the Si9410DY has a Q_G(typ) of 17nC (at V_{GS} = 5V), therefore the current required to charge the gate is:

$$I_{GATE}(max) = (500kHz)(17nC) = 8.5mA.$$

The bypass capacitor on V+ (C2) must instantaneously furnish the gate charge without excessive droop (e.g., less than 200mV):

$$\Delta V+ = \frac{Q_G}{C2}$$

Continuing with the example, $\Delta V+ = 17nC/0.1\mu F = 170mV$.

Figure 2a's application circuit uses an 8-pin Si9410DY surface-mount N-FET that has 50mΩ on-resistance with 4.5V V_{GS}, and a guaranteed V_{TH} of less than 3V. Figure 2b's application circuit uses an MTD20N03HDL logic-level N-FET with a guaranteed threshold voltage (V_{TH}) of 2V.

Diode Selection

The MAX1771's high switching frequency demands a high-speed rectifier. Schottky diodes such as the 1N5817–1N5822 are recommended. Make sure the Schottky diode's average current rating exceeds the peak current limit set by R_{SENSE}, and that its breakdown voltage exceeds V_{OUT}. For high-temperature applications, Schottky diodes may be inadequate due to their high leakage currents; high-speed silicon diodes such as the MUR105 or EC11FS1 can be used instead. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantages of its high leakage current.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor (C4) is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the ripple seen on the output voltage. Two OS-CON 150µF, 16V output filter capacitors in parallel with 35mΩ of ESR each typically provide 75mV ripple when stepping up from 5V to 12V at 500mA (Figure 2a). Smaller-value and/or higher-ESR capacitors are acceptable for light loads or in applications that can tolerate higher output ripple.

Since the output filter capacitor's ESR affects efficiency, use low-ESR capacitors for best performance. See Table 1 for component selection.

Input Bypass Capacitors

The input bypass capacitor (C1) reduces peak currents drawn from the voltage source and also reduces noise at the voltage source caused by the switching action of the MAX1771. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is recommended. For output currents up to 1A, 68µF (C1) is adequate, although smaller bypass capacitors may also be acceptable.

Bypass the IC with a 0.1µF ceramic capacitor (C2) placed as close to the V+ and GND pins as possible.

Reference Capacitor

Bypass REF with a 0.1µF capacitor (C3). REF can source up to 100µA of current for external loads.

Feed-Forward Capacitor

In adjustable output voltage and non-bootstrapped modes, parallel a 47pF to 220pF capacitor across R2, as shown in Figures 2 and 3. Choose the lowest capacitor value that insures stability; high capacitance values may degrade line regulation.

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Table 1. Component Suppliers

PRODUCTION	INDUCTORS	CAPACITORS	TRANSISTORS	DIODES
Surface Mount	Sumida CD54 series CDR125 series Coiltronics CTX20 series Coilcraft DO3316 series DO3340 series	Matsuo 267 series Sprague 595D series AVX TPS series	Siliconix Si9410DY Si9420DY (high voltage) Motorola MTP3055EL MTD20N03HDL MMFT3055ELTI MTD6N1O MMBT8099LTI MMBT8599LTI	Central Semiconductor CMPSH-3 CMPZ5240 Nihon EC11 FS1 series (high-speed silicon) Motorola MBRS1100T3 MMBZ5240BL
Through Hole	Sumida RCH855 series RCH110 series	Sanyo OS-CON series Nichicon PL series		Motorola 1N5817–1N5822 MUR115 (high voltage) MUR105 (high-speed silicon)

SUPPLIER	PHONE	FAX
AVX	USA: (803) 448-9411	(803) 448-1943
Central Semiconductor	USA: (516) 435-1110	(516) 435-1824
Coilcraft	USA: (708) 639-6400	(708) 639-1469
Coiltronics	USA: (407) 241-7876	(407) 241-9339
Matsuo	USA: (714) 969-2491 Japan: 81-6-337-6450	(714) 960-6492 81-6-337-6456
Motorola	USA: (800) 521-6274	(602) 952-4190
Nichicon	USA: (708) 843-7500	(708) 843-2798
Nihon	USA: (805) 867-2555	(805) 867-2556
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-1005	(619) 661-1055 81-7-2070-1174
Siliconix	USA: (800) 554-5565	(408) 970-3950
Sprague	USA: (603) 224-1961	(603) 224-1430
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	(708) 956-0702 81-3-3607-5144

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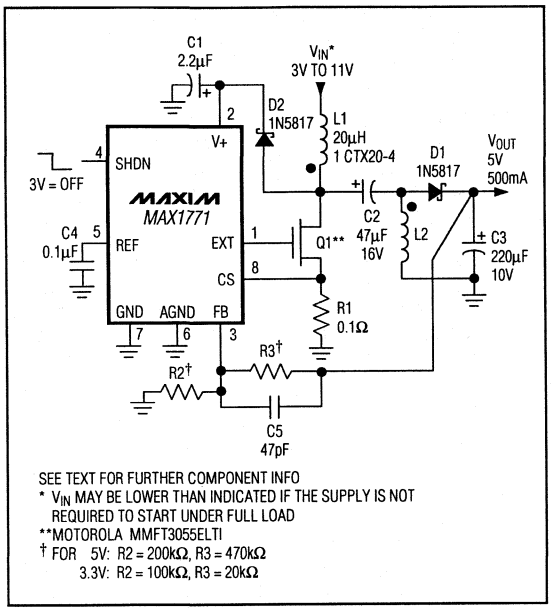

Figure 5. Step-Up/Down for a 5V/3.3V Output

Applications Information

Low Input Voltage Operation

When using a power supply that decays with time (such as a battery), the N-FET transistor will operate in its linear region when the voltage at EXT approaches the threshold voltage of the FET, dissipating excessive power. Prolonged operation in this mode may damage the FET. This effect is much more significant in non-bootstrapped mode than in bootstrapped mode, since bootstrapped mode typically provides much higher V_{GS} voltages. To avoid this condition, make sure V_{EXT} is above the V_{TH} of the FET, or use a voltage detector (such as the MAX8211) to put the IC in shutdown mode once the input supply voltage falls below a predetermined minimum value. Excessive loads with low input voltages can also cause this condition.

Starting Up under Load

The *Typical Operating Characteristics* show the Start-Up Voltage vs. Load Current graph for bootstrapped-mode operation. This graph depends on the type of power switch used. The MAX1771 is not designed to start up under full load in bootstrapped mode with low input voltages.

Layout Considerations

Due to high current levels and fast switching waveforms, which radiate noise, proper PC board layout is essential. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. Place input bypass capacitor C2 as close as possible to V+ and GND.

Excessive noise at the V+ input may falsely trigger the timing circuitry, resulting in short pulses at EXT. If this occurs it will have a negligible effect on circuit efficiency. If desired, place a 4.7µF directly across the V+ and GND pins (in parallel with the 0.1µF C2 bypass capacitor) to reduce the noise at V+.

Other Application Circuits

4 Cells to 5V (or 3 Cells to 3.3V), 500mA Step-Up/Down Converter

The circuit shown in Figure 5 generates 5V (or 3.3V) at 500mA with 85% efficiency, from an input voltage that varies above and below the output. The output couples to the switching circuitry via a capacitor. This configuration offers two advantages over flyback-transformer and step-up linear-regulator circuits: smooth regulation as the input passes through the output, and no output current in shutdown.

This circuit requires two inductors, which can be wound on one core with no regard to coupling since they do not work as a transformer. L1 and L2 can either be wound together (as with the Coiltronics CTX20-4) or kept as two separate inductors; both methods provide equal performance. Capacitors C2 and C3 should be low-ESR types for best efficiency. A 1µF ceramic capacitor will work at C2, but with about 3% efficiency loss. C2's voltage rating must be greater than the maximum input voltage. Also note that the LX switch must withstand a voltage equal to the sum of the input and output voltage; for example, when converting 11V to 5V, the switch must withstand 16V.

LX switch pulses are captured by Schottky diode D2 to boost V+ to (V_{OUT} + V_{IN}). This improves efficiency with a low input voltage, but also limits the maximum input supply to 11V. If the input voltage does not fall below 4V and if a 3V logic threshold FET is used for Q1, you may omit D2 and connect V+ directly to the input supply.

12V Output Buck/Boost

The circuit in Figure 6 generates 12V from a 4.5V to 16V input. Higher input voltages are possible if you

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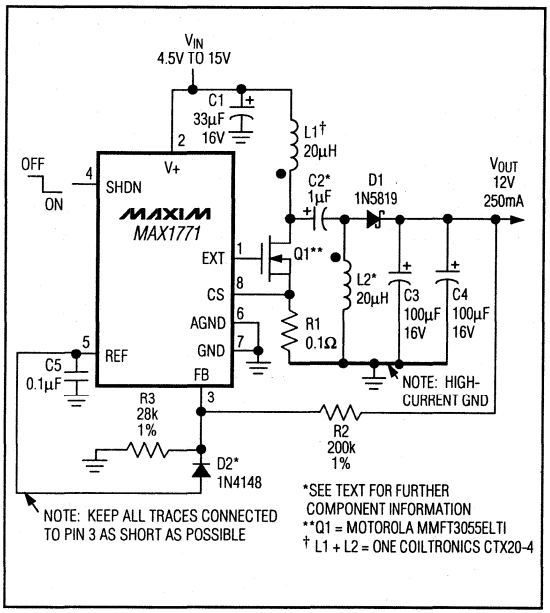


Figure 6. 12V Buck/Boost from a 4.5V to 15V Input

carefully observe the component voltage ratings, since some components must withstand the sum of the input and output voltage (27V in this case). The circuit operates as an AC-coupled boost converter, and does not change operating modes when crossing from buck to boost. There is no instability around a 12V input. Efficiency ranges from 85% at medium loads to about 82% at full load. Also, when shutdown is activated (SHDN high) the output goes to 0V and sources no current. A 1µF ceramic capacitor is used for C2. A larger capacitor value improves efficiency by about 1% to 3%.

D2 ensures start-up for this AC-coupled configuration by overriding the MAX1771's Dual-Mode feature, which allows the use of preset internal or user-set external feedback. When operating in Dual-Mode, the IC first tries to use internal feedback and looks to V+ for its feedback signal. However, since V+ may be greater than the internally set feedback (12V for the MAX1771), the IC may think the output is sufficiently high and not start. D2 ensures start-up by pulling FB above ground and forcing the external feedback mode. In a normal (not AC-coupled) boost circuit, D2 isn't needed, since the output and FB rise as soon as input power is applied.

Transformerless -48V to +5V at 300mA

The circuit in Figure 7 uses a transformerless design to supply 5V at 300mA from a -30V to -75V input supply. The MAX1771 is biased such that its ground connections are made to the -48V input. The IC's supply voltage (at V+) is set to about 9.4V (with respect to -48V) by a zener-biased emitter follower (Q2). An N-channel FET (Q1) is driven in a boost configuration. Output regulation is achieved by a transistor (Q3), which level shifts a feedback signal from the 5V output to the IC's FB input. Conversion efficiency is typically 82%.

When selecting components, be sure that D1, Q1, Q2, Q3, and C6 are rated for the full input voltage plus a reasonable safety margin. Also, if D1 is substituted, it should be a fast-recovery type with a t_{rr} less than 30ns. R7, R9, C8, and D3 are optional and may be used to soft start the circuit to prevent excessive current surges at power-up.

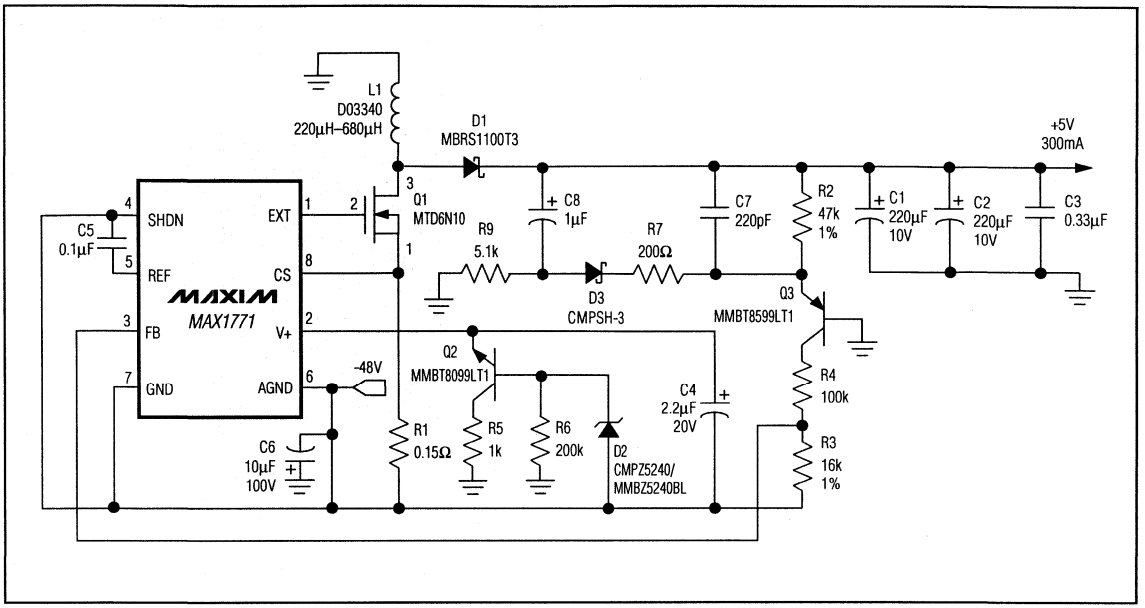
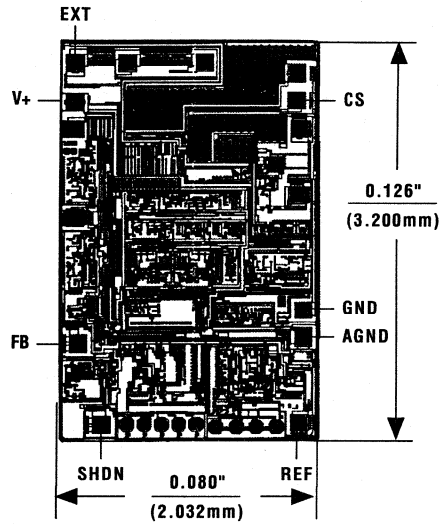


Figure 7. -48V Input to 5V Output at 300mA, Without a Transformer

12V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controller

Chip Topography



TRANSISTOR COUNT: 501
SUBSTRATE CONNECTED TO V+

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Low Dropout, P-Channel, 500mA Linear Regulators

General Description

The MAX603/MAX604 are low-dropout, low quiescent current, linear regulators that supply 5V, 3.3V, or an adjustable output for currents up to 500mA. They are available in a new 1.9W SO package. Typical dropouts are 260mV at 5V and 400mA, or 240mV at 3.3V and 200mA. Quiescent currents are 15µA typical and 35µA maximum. Shutdown turns off all circuitry and puts the regulator in a 2µA off mode. A unique protection scheme limits reverse currents when the input voltage falls below the output. Other features include foldback current limiting and thermal overload protection.

The output is preset at 3.3V for the MAX604 and 5V for the MAX603. In addition, both devices employ Dual Mode™ operation, allowing user-adjustable outputs from 1.3V to 11V using external resistors. The input voltage supply range is 2.7V to 11.5V.

The MAX603/MAX604 feature a 500mA P-channel MOSFET pass transistor. This transistor allows the devices to draw less than 35µA over temperature, independent of output current. The supply current remains low because the P-channel MOSFET pass transistor draws no base currents (unlike the PNP transistors of conventional bipolar linear regulators). And, when the input-to-output voltage differential becomes small, the internal P-channel MOSFET avoids the excessive base-current losses of saturated PNP transistors.

Applications

5V and 3.3V Regulators

1.3V to 11V Adjustable Regulators

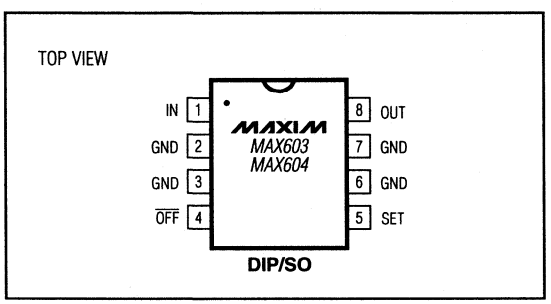
Battery-Powered Devices

Pagers and Radio Control Receivers

Portable Instruments

Solar-Powered Instruments

Pin Configuration



Features

- ♦ **Dual Mode™ Operation: Fixed Output or Adjustable from 1.3V to 11V**
- ♦ **500mA Output Current, with Foldback Current Limiting**
- ♦ **Large Input Range (2.7V to 11.5V)**
- ♦ **Internal 500mA P-Channel Pass Transistor**
- ♦ **High-Power (1.9W) 8-pin SO Package**
- ♦ **15µA Typical Quiescent Current**
- ♦ **2µA Shutdown Mode**
- ♦ **Thermal Overload Protection**
- ♦ **Reverse Current Protection**

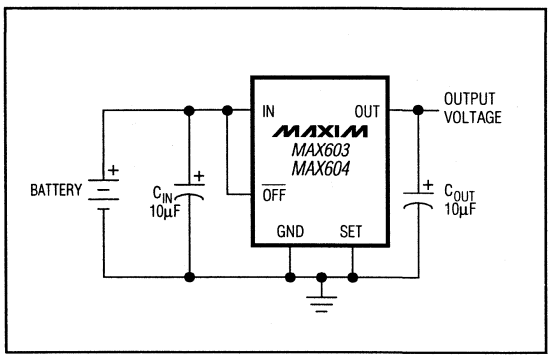
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX603CPA	0°C to +70°C	8 Plastic DIP
MAX603CSA	0°C to +70°C	8 SO
MAX603C/D	0°C to +70°C	Dice*
MAX603ESA	-40°C to +85°C	8 SO
MAX603MJA	-55°C to +125°C	8 CERDIP**
MAX604CPA	0°C to +70°C	8 Plastic DIP
MAX604CSA	0°C to +70°C	8 SO
MAX604C/D	0°C to +70°C	Dice*
MAX604ESA	-40°C to +85°C	8 SO
MAX604MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



™ Dual Mode is a registered trademark of Maxim Integrated Products.

19-0188; Rev 0; 11/93

MAXIM

Dual-Slot PCMCIA Analog Power Controllers

General Description

The MAX613/MAX614 contain switches for the VPP supply-voltage lines for Personal Computer Memory Card International Association (PCMCIA) Release 2.0 card slots. These ICs also contain level-translator outputs to switch the PCMCIA card VCC.

The MAX613 allows digital control of two separate VPP lines that can be switched between 0V, VCC, +12V, and high impedance. It also includes level shifters that allow the control of N-channel power MOSFETs for connecting and disconnecting the slot VCC supply voltage.

The MAX614 controls a single VPP supply-voltage line and includes one level shifter in an 8-pin package.

Applications

Notebook and Palmtop Computers

Personal Organizers

Digital Cameras

Handiterminals

Bar-Code Readers

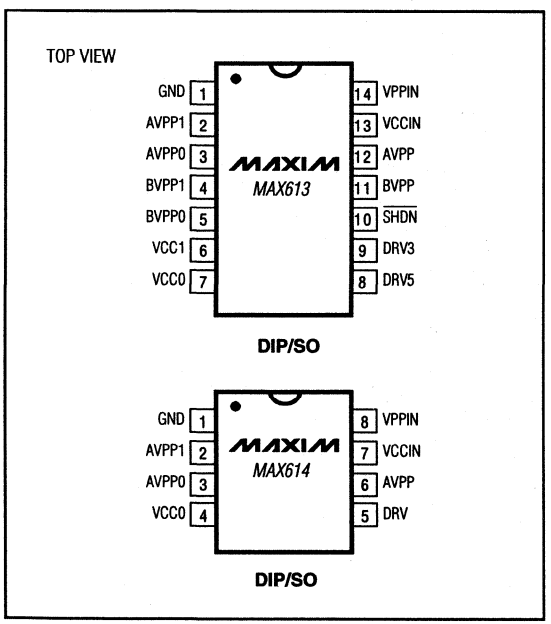
Features

- **Logic Compatible with Industry-Standard PCMCIA Digital Controllers:**
  - **Intel 82365SL**
  - **Intel 82365SL DF**
  - **Vadem VG-365**
  - **Vadem VG-465**
  - **Vadem VG-468**
  - **Cirrus Logic CL-PD6710**
  - **Cirrus Logic CL-PD6720**
- **0V/VCC/+12V/High-Impedance VPP Outputs**
- **Internal 1.6Ω VPP Power Switches**
- **10µA Quiescent Supply Current**
- **Break-Before-Make Switching**
- **VCC Switch Control**

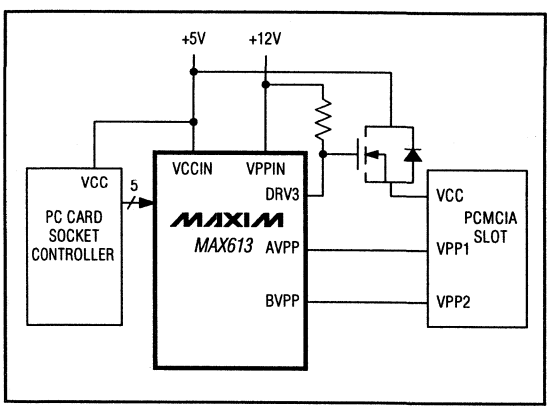
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX613CPD	0°C to +70°C	14 Plastic DIP
MAX613CSD	0°C to +70°C	14 SO
MAX613EPD	-40°C to +85°C	14 Plastic DIP
MAX613ESD	-40°C to +85°C	14 SO
MAX614CPA	0°C to +70°C	8 Plastic DIP
MAX614CSA	0°C to +70°C	8 SO
MAX614EPA	-40°C to +85°C	8 Plastic DIP
MAX614ESA	-40°C to +85°C	8 SO

Pin Configurations



Typical Operating Circuit



Dual-Slot PCMCIA Analog Power Controllers

ABSOLUTE MAXIMUM RATINGS

VCCIN to GND .....+7V, -0.3V
VPPIN to GND .....+13.2V, -0.3V
DRV5, DRV3, DRV to GND .....(VPPIN + 0.3V), -0.3V
AVPP, BVPP to GND .....(VPPIN + 0.3V), -0.3V
All Other Pins to GND .....(VCCIN + 0.3V), -0.3V
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C).....800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW

Operating Temperature Ranges:
MAX61_C__ .....0°C to +70°C
MAX61_E__ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
VCCIN Input Voltage Range				2.85		5.5	V
VPPIN Input Voltage Range				0		12.6	V
VPPIN Supply Current (12V Mode)	AVPP = BVPP = VPPIN = 12.6V	MAX613	$\overline{SHDN}$ = 0V		0.05	1	µA
			$\overline{SHDN}$ = VCCIN		2.25	10	
		MAX614			0.05	1	
VPPIN Supply Current (5V Mode)	VPPIN = 12.6V, AVPP = BVPP= VCCIN	MAX613	$\overline{SHDN}$ = 0V		0.05		µA
			$\overline{SHDN}$ = VCCIN		2		
		MAX614			0.05		
VPPIN Supply Current (0V Mode)	AVPP = BVPP = 0V	MAX613	$\overline{SHDN}$ = 0V		0.05		µA
			$\overline{SHDN}$ = VCCIN		2.25		
		MAX614			0.05		
VCCIN Supply Current (12V Mode)	AVPP = BVPP = VPPIN	MAX613	$\overline{SHDN}$ = 0V		3.5		µA
			$\overline{SHDN}$ = VCCIN		20		
		MAX614			3.5		
VCCIN Supply Current (5V Mode)	AVPP = BVPP = VCCIN	MAX613	$\overline{SHDN}$ = 0V		3.5	10	µA
			$\overline{SHDN}$ = VCCIN		22	50	
		MAX614			3.5	10	
VCCIN Supply Current (0V Mode)	AVPP = BVPP = 0V	MAX613	$\overline{SHDN}$ = 0V		3.5		µA
			$\overline{SHDN}$ = VCCIN		20		
		MAX614			3.5		

ELECTRICAL CHARACTERISTICS (continued)

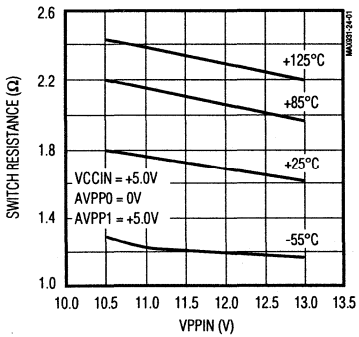
(VCCIN = +5V, VPPIN = +12V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
AVPP, BVPP Switch Resistance	VPPIN = 11.4V, 0mA < I_{LOAD} < 120mA (12V mode)		1.60	2.45	Ω
	VCCIN = 4.5V, 0mA < I_{LOAD} < 1mA (5V mode)		30	50	
	VPPIN = 11.4V, 0mA < I_{LOAD} < 1mA (0V mode)		135	300	
DRV, DRV3, DRV5 Leakage Current	High-impedance mode		1	75	nA
DRV, DRV3, DRV5 Output Voltage Low	I_{LOAD} = 1mA		0.1	0.4	V
LOGIC SECTION					
Logic Input Leakage Current				1	µA
Logic Input High		2.4			V
Logic Input Low				0.8	V
VCC to DRV_ Propagation Delay			50		ns

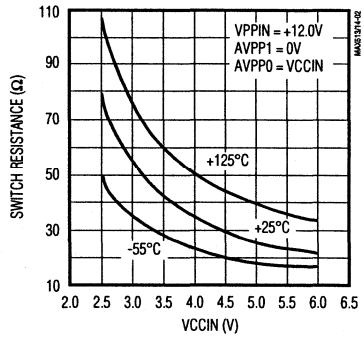
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

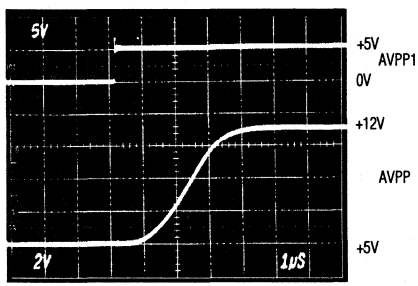
AVPP SWITCH RESISTANCE (12V MODE)



AVPP SWITCH RESISTANCE (5V MODE)



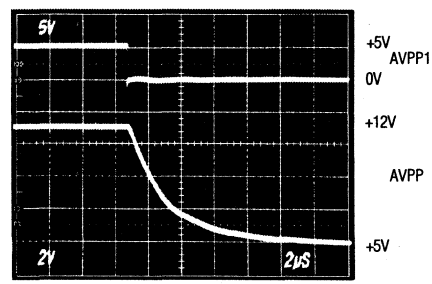
AVPP SWITCHING 5V TO 12V



1µs/div

C_{VPPIN} = 1µF, AVPP0 = $\overline{AVPP1}$, C_{AVPP} = 0.1µF

AVPP SWITCHING 12V TO 5V



2µs/div

C_{VPPIN} = 1µF, AVPP0 = $\overline{AVPP1}$, C_{AVPP} = 0.1µF

Dual-Slot PCMCIA Analog Power Controllers

Pin Description

PIN		NAME	FUNCTION
MAX613	MAX614		
1	1	GND	Ground
2	2	AVPP1	Logic inputs that control the voltage on AVPP (see Table 1 in *Detailed Description*).
3	3	AVPP0	
4	—	BVPP1	Logic inputs that control the voltage on BVPP (see Table 2 in *Detailed Description*).
5	—	BVPP0	
6	—	VCC1	Logic input that controls the state of DRV3 and DRV5 (see Table 3 in *Detailed Description*).
7	4	VCC0	Logic input that controls the state of DRV on the MAX614. On the MAX613, both VCC0 and VCC1 control the state of DRV3 and DRV5 (see Table 3 in *Detailed Description*).
—	5	DRV	Open-drain power MOSFET gate-driver output used to switch the slot VCC supply voltage. DRV sinks current when VCC0 is high and goes high impedance when VCC0 is low.
8	—	DRV5	Open-drain power MOSFET gate-driver output used to switch the slot VCC supply voltage (see Table 3 in *Detailed Description*).
9	—	DRV3	Open-drain power MOSFET gate-driver output used to switch the slot VCC supply voltage (see Table 3 in *Detailed Description*).
10	—	$\overline{SHDN}$	Logic-level shutdown input. When $\overline{SHDN}$ is low, DRV3 and DRV5 sink current regardless of the state of VCC0 and VCC1. When $\overline{SHDN}$ is high, DRV3 and DRV5 are controlled by VCC0 and VCC1.
11	—	BVPP	Switched output, controlled by BVPP1 and BVPP0, that outputs 0V, +5V, or +12V. BVPP can also be programmed to go high impedance (see Table 2 in *Detailed Description*).
12	6	AVPP	Switched output, controlled by AVPP1 and AVPP0, that outputs 0V, +5V, or +12V. AVPP can also be programmed to go high impedance (see Table 1 in *Detailed Description*).
13	7	VCCIN	+5V power input
14	8	VPPIN	+12V power input. VPPIN can have 0V or +5V applied as long as VCCIN > 2.85V.

Detailed Description

VPP Switching

The MAX613/MAX614 allow simple switching of PCMCIA card VPP to 0V, +5V, and +12V. On-chip power MOSFETs connect AVPP and BVPP to either GND, VCCIN, or VPPIN. The AVPP0 and AVPP1 control logic inputs determine AVPP's state. Likewise, BVPP0 and BVPP1 control BVPP. AVPP and BVPP can also be programmed to be high impedance.

Each PCMCIA card slot has two VPP voltage inputs labeled VPP1 and VPP2. Typically, VPP1 supplies the flash chips that store the low-order byte of the 16-bit words, and VPP2 supplies the chips that contain the high-order byte. Programming the high-order bytes separately from the low-order bytes may be necessary to minimize +12V current consumption. A single 8-bit flash chip typically requires at most 30mA of +12V VPP current during erase or programming.

Thus, systems with less than 60mA current capability from +12V cannot program two 8-bit flash chips simultaneously, and need separate controls for VPP1 and VPP2. Figure 1 shows an example of a power-control circuit using the MAX613 to control VPP1 and VPP2 separately. Figure 1's circuit uses a MAX662 charge-pump DC-DC converter to convert +5V to +12V at 30mA output current capability without an inductor. When higher VPP current is required, the MAX734 can supply 120mA.

Use the MAX614 for single-slot applications that do not require a separate VPP1 and VPP2. Figure 2 shows the MAX614 interfaced to the Vadem VG-465 single-slot controller.

To prevent VPP overshoot resulting from parasitic inductance in the +12V supply, the VPPIN bypass capacitor's value must be at least 10 times greater than the capacitance from AVPP or BVPP to GND; the AVPP and BVPP bypass capacitors must be at least 0.01µF.

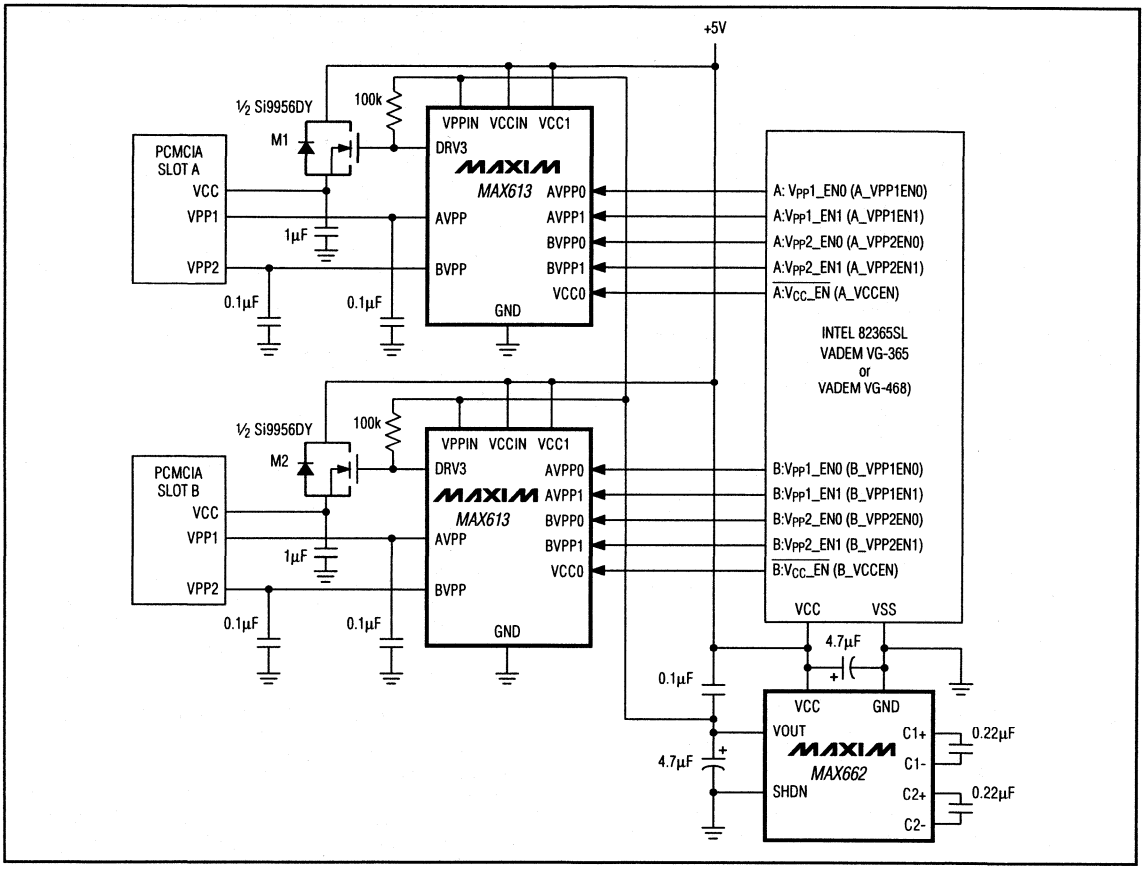


Figure 1. MAX613 Dual Slot, Separate VPP1 and VPP2, 5V Only VCC Operating Circuit

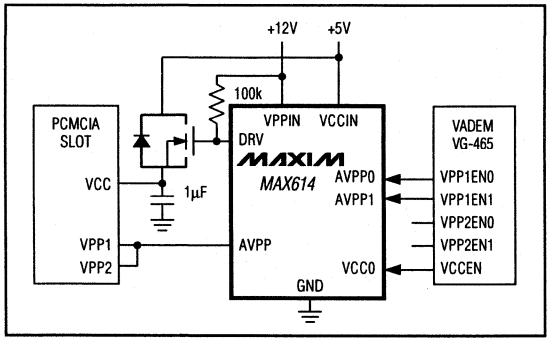


Figure 2. MAX614 Single-Slot Application

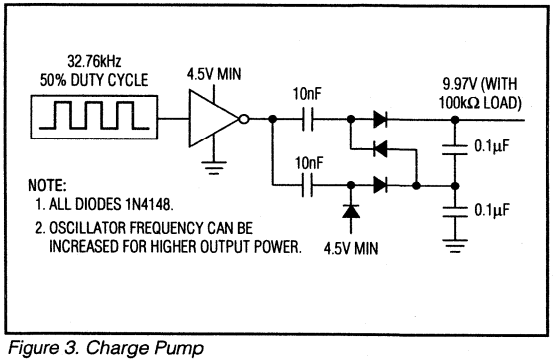


Figure 3. Charge Pump

Dual-Slot PCMCIA Analog Power Controllers

VCC Switching

The MAX613/MAX614 contain level shifters that simplify driving external power MOSFETs to switch PCMCIA card VCC. While a PCMCIA card is being inserted into the socket, the VCC pins on the card edge connector should be powered down to 0V to prevent "hot insertion" that may damage the PCMCIA card. The MAX613/MAX614 MOSFET drivers are open drain. Their rise time is controlled by an external pull-up resistor, allowing slow turn-on of VCC power to the PCMCIA card.

The DRV3 and DRV5 pins on the MAX613 and the DRV pin on the MAX614 are open-drain outputs pulled down with internal N-channel devices. The gate drive to these internal N-channel devices is powered from VCCIN, regardless of VPPIN's voltage. If VCCIN is left unconnected or less than 2V is applied to VCCIN, the DRV3/DRV5/DRV gate drivers will not sink current.

To switch VCC (M1 and M2 in Figure 1), use external N-channel power MOSFETs. M1 and M2 should be logic-level N-channel power MOSFETs with low on resistance. The Motorola MTP3055EL and Siliconix Si9956DY MOSFETs are both good choices. Turn on M1 and M2 by pulling their gates above +5V. With the gates pulled up to VPPIN as shown in Figure 1, VPPIN should be at least 10V so that with VCC = 5.5V, M1 and M2 have at least 4.5V of gate drive.

Table 1. AVPP Control Logic

LOGIC INPUT		OUTPUT
AVPP1	AVPP0	AVPP
0	0	0V
0	1	VCCIN
1	0	VPPIN
1	1	HI-Z

Table 2. BVPP Control Logic

LOGIC INPUT		OUTPUT
BVPP1	BVPP0	BVPP
0	0	0V
0	1	VCCIN
1	0	VPPIN
1	1	HI-Z

Table 3. MAX613 DRV3 and DRV5 Control Logic ($\overline{SHDN}$ = VCCIN)

LOGIC INPUT		OUTPUT	
VCC1	VCC0	DRV3	DRV5
0	0	0V	0V
0	1	HI-Z	0V
1	0	0V	HI-Z
1	1	0V	0V

The gates of M1 and M2 can be pulled up to any 10V to 20V source, and do not need to be pulled up to VPPIN. Typically, the +12V used for VPPIN is supplied from a +5V to +12V switching regulator. To save power, the +5V to +12V switching regulator can be shut down when not using the VPP programming voltage, allowing VPPIN to fall below +5V.

In this case, M1 and M2 should not be pulled up to VPPIN, since M1 and M2 cannot be turned on reliably when VPPIN falls below +10V. Any clock source can be used to generate a high-side gate-drive voltage by using capacitors and diodes to build an inexpensive charge pump. Figure 3 shows a charge-pump circuit that generates 10V from a +5V logic clock source.

Applications Information

The MAX613 contains all the gate drivers and switching circuitry needed to support a +3.3V/+5V VCC PCMCIA slot with minimal external components. Figure 4 shows the analog power control necessary to support two dual voltage PCMCIA slots. The A:VCC and B:VCC pins on the Intel 82365SL DF power the drivers for the control signals that directly connect to the PCMCIA card.

A 3.3V card needs 3.3V logic-level control signals and the capability to program VPP1 and VPP2 to 3.3V. The MAX613's VCCIN is switched with slot VCC, so AVPP0 = 1 and AVPP1 = 0 causes AVPP = slot VCC. Likewise, A:VCC and B:VCC are connected to VCCIN, so the Intel 82365SL DF control signals to the PCMCIA card are the right logic levels.

PCMCIA card interface controllers other than the Intel 82365SL DF can be used with Figure 4's circuit. Table 4 shows the pins on the Cirrus Logic CL-PD6720 that perform the same function as the Intel 82365SL DF pins.

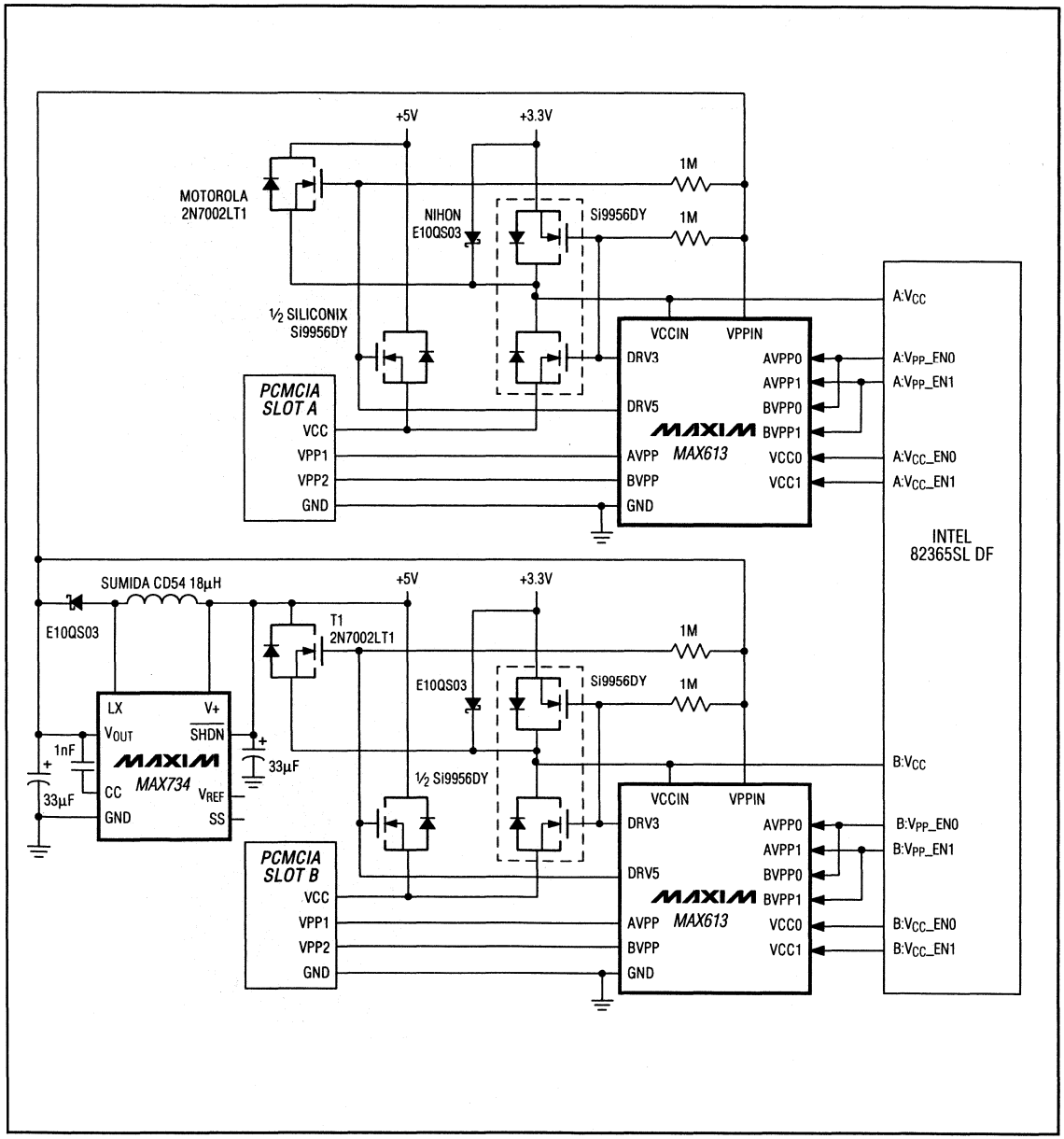


Figure 4. Mixed 3.3V/5V VCC Application Circuit

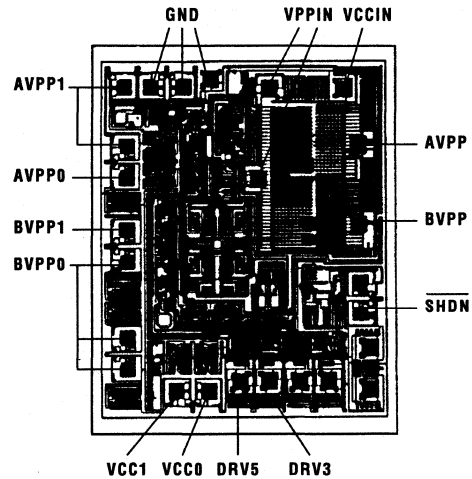
Dual-Slot PCMCIA Analog Power Controllers

Table 4. Interchangeable Interface Controllers

INTEL	CIRRUS LOGIC
82365SL DF	CL-PD6720
A:V_{CC}	A_SLOT_VCC
A:V_{PP}_EN0	A_VPP_VCC
A:V_{PP}_EN1	A_VPP_PGM
A:V_{CC}_EN0	A_-VCC_5
A:V_{CC}_EN1	A_-VCC_3
B:V_{CC}	B_SLOT_VCC
V:V_{PP}_EN0	B_VPP_VCC
B:V_{PP}_EN1	B_VPP_PGM
B:V_{CC}_EN0	B_-VCC_5
B:V_{CC}_EN1	B_-VCC_3

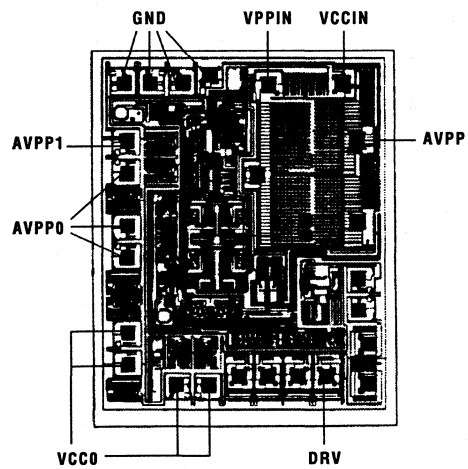
Chip Topographies

MAX613



TRANSISTOR COUNT: 982;
SUBSTRATE CONNECTED TO GND.

MAX614



TRANSISTOR COUNT: 982;
SUBSTRATE CONNECTED TO GND.

19-0227; Rev 0; 2/94

EVALUATION KIT AVAILABLE

MAXIM

Regulated 5V Charge-Pump DC-DC Converter

General Description

The MAX619 step-up charge-pump DC-DC converter delivers a regulated 5V ±4% output at 50mA over temperature. The input voltage range is 2V to 3.6V (two battery cells).

The complete MAX619 circuit fits into less than 0.1in^2 of board space because it requires only four external capacitors: two 0.22µF flying capacitors, and 10µF capacitors at the input and output.

Low operating supply current (150µA max) and low shutdown supply current (1µA max) make this device ideal for small, portable, and battery-powered applications. When shut down, the load is disconnected from the input.

The MAX619 is available in 8-pin DIP and SO packages.

Applications

Two Battery Cells to 5V Conversion

Local 3V-to-5V Conversion

Portable Instruments & Handy-Terminals

Battery-Powered Microprocessor-Based Systems

5V Flash Memory Programmer

Minimum Component DC-DC Converters

Remote Data-Acquisition Systems

Compact 5V Op-Amp Supply

Regulated 5V Supply from Lithium Backup Battery

Switching Drive Voltage for MOSFETs in Low-Voltage Systems

Features

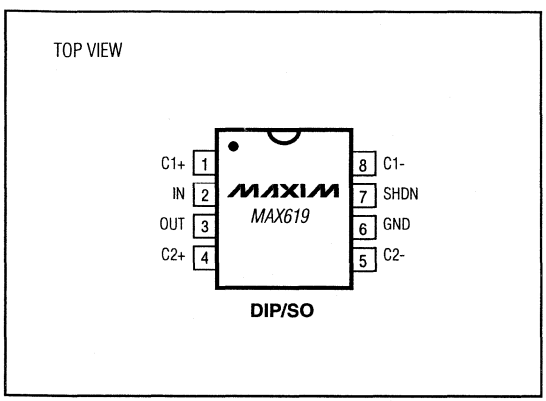
- **Regulated 5V ±4% Charge Pump**
- **Output Current Guaranteed over Temperature**
  20mA (V_{IN} ≥ 2V)
  50mA (V_{IN} ≥ 3V)
- **2V to 3.6V Input Range**
- **No Inductors; Very Low EMI Noise**
- **Ultra-Small Application Circuit (0.1in2)**
- **Uses Small, Inexpensive Capacitors**
- **500kHz Internal Oscillator**
- **Logic-Controlled 1µA Max Shutdown Supply Current**
- **Shutdown Disconnects Load from Input**
- **8-Pin DIP and SO Packages**

Ordering Information

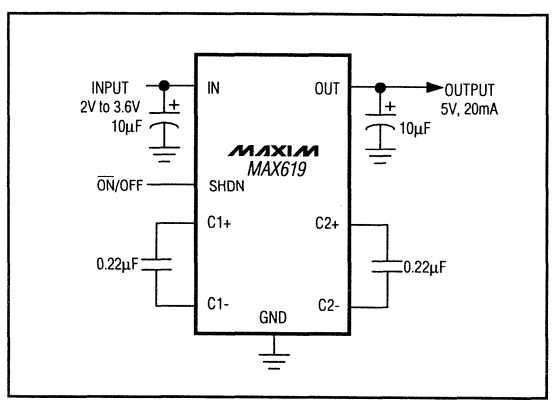
PART	TEMP. RANGE	PIN-PACKAGE
MAX619CPA	0°C to +70°C	8 Plastic DIP
MAX619CSA	0°C to +70°C	8 SO
MAX619C/D	0°C to +70°C	Dice*
MAX619EPA	-40°C to +85°C	8 Plastic DIP
MAX619ESA	-40°C to +85°C	8 SO
MAX619MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at T_A = +25°C.*

Pin Configuration



Typical Operating Circuit



Regulated 5V Charge-Pump DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND .....-0.3V to +5.5V
V_{OUT} to GND .....-0.3V to +5.5V
SHDN to GND .....-0.3V to (V_{IN} + 0.3V)
I_{OUT} Continuous (Note 1).....120mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX619C_ _ .....0°C to +70°C
MAX619E_ _ .....-40°C to +85°C
MAX619MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The MAX619 is not short-circuit protected.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2V to 3.6V, C1 = C2 = 0.22µF, C3 = C4 = 10µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

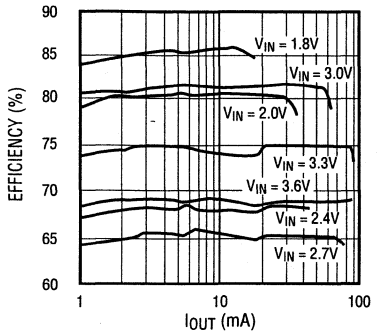
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}			2		3.6	V
Output Voltage	V_{OUT}	2.0V ≤ V_{IN} ≤ 3.6V, 0mA ≤ I_{OUT} ≤ 20mA		4.8	5.0	5.2	V
		3.0V ≤ V_{IN} ≤ 3.6V, 0mA ≤ I_{OUT} ≤ 50mA, MAX619C					
		3.0V ≤ V_{IN} ≤ 3.6V, 0mA ≤ I_{OUT} ≤ 40mA, MAX619E/M					
Output Ripple	V_{RIPPLE}	No load to full load			100		mV
No-Load Supply Current	I_{IN}	2V ≤ V_{IN} ≤ 3.6V, I_{OUT} = 0mA			75	150	µA
Shutdown Supply Current		2V ≤ V_{IN} ≤ 3.6V, I_{OUT} = 0mA, V_{SHDN} = V_{IN}	MAX619C/E		0.02	1	µA
			MAX619M			10	
Efficiency	Eff	V_{IN} = 3V, I_{OUT} = 20mA			82		%
		V_{IN} = 3V, I_{OUT} = 30mA			82		
		V_{IN} = 2V, I_{OUT} = 20mA			80		
Switching Frequency		At full load			500		kHz
SHDN Input Threshold	V_{IH}			0.7 x V_{IN}			V
	V_{IL}					0.4	
SHDN Input Current	I_{IH}	V_{SHDN} = V_{IN}	MAX619C/E			±1	µA
			MAX619M			±10	

Regulated 5V Charge-Pump DC-DC Converter

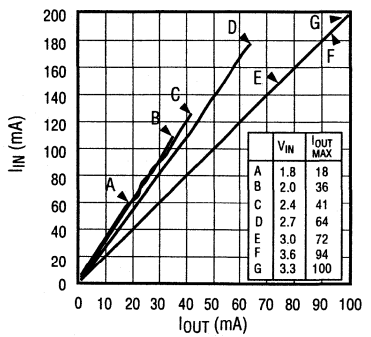
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

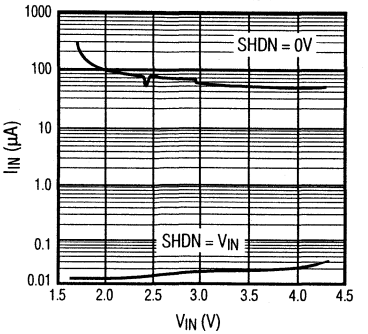
EFFICIENCY vs. OUTPUT CURRENT AND INPUT VOLTAGE



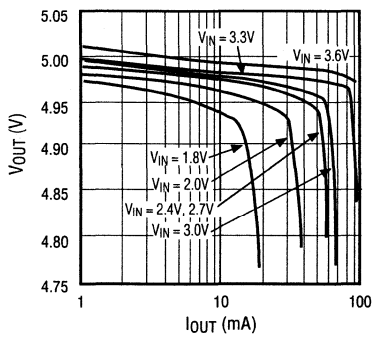
INPUT CURRENT vs. OUTPUT CURRENT



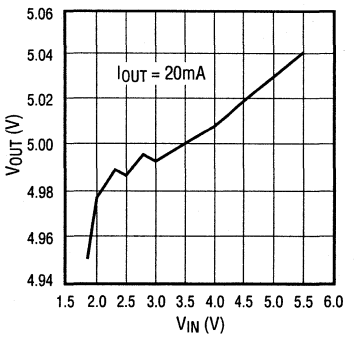
NO-LOAD INPUT CURRENT vs. INPUT VOLTAGE



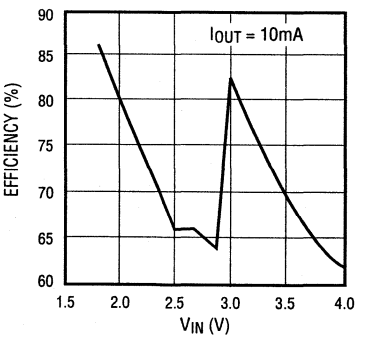
OUTPUT VOLTAGE vs. OUTPUT CURRENT



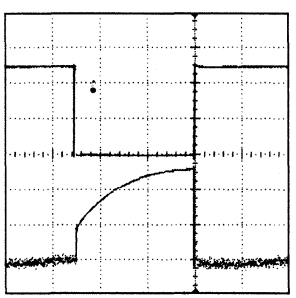
OUTPUT VOLTAGE vs. INPUT VOLTAGE



EFFICIENCY vs. INPUT VOLTAGE

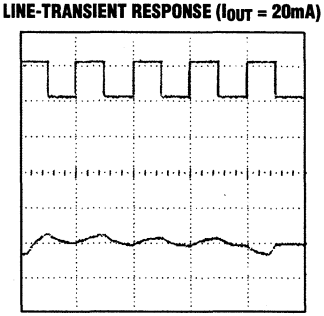


LOAD-TRANSIENT RESPONSE



TOP TRACE: OUTPUT CURRENT, 0mA to 25mA, 10mA/div
BOTTOM TRACE: OUTPUT VOLTAGE, 5mV/div, AC-COUPLED

LINE-TRANSIENT RESPONSE (I_{OUT} = 20mA)



R_{LOAD} = 250Ω, V_{OUT} = 5V, I_{OUT} = 20mA
TOP TRACE: V_{IN} = 2V to 3V, 1V/div
BOTTOM TRACE: OUTPUT VOLTAGE, 50mV/div, AC-COUPLED

Regulated 5V Charge-Pump DC-DC Converter

Pin Description

PIN	NAME	FUNCTION
1	C1+	Positive Terminal for C1
2	IN	Input Supply Voltage
3	OUT	+5V Output Voltage. V_{OUT} = 0V when in shutdown mode.
4	C2+	Positive Terminal for C2
5	C2-	Negative Terminal for C2
6	GND	Ground
7	SHDN	Active-High CMOS Logic-Level Shutdown Input
8	C1-	Negative Terminal for C1

Detailed Description

Operating Principle

The MAX619 provides a regulated 5V output from a 2V to 3.6V (two battery cells) input. Internal charge pumps and external capacitors generate the 5V output, eliminating the need for inductors. The output voltage is regulated to 5V ±4% by a pulse-skipping controller that turns on the charge pump when the output voltage begins to droop.

To maintain the greatest efficiency over the entire input voltage range, the MAX619's internal charge pump operates as a voltage doubler when V_{IN} ranges from 3.0V to 3.6V, and as a voltage tripler when V_{IN} ranges from 2.0V to 2.5V. When V_{IN} ranges from 2.5V to 3.0V, the MAX619 switches between doubler and tripler mode on alternating cycles, making a 2.5 x V_{IN} charge pump. To further enhance efficiency over the input range, an internal comparator selects the higher of V_{IN} or V_{OUT} to run the MAX619's internal circuitry. Efficiency with V_{IN} = 2V and I_{OUT} = 20mA is typically 80%.

Figure 1 shows a detailed block diagram of the MAX619. In tripler mode, when the S1 switches close, the S2 switches open and capacitors C1 and C2 charge up to V_{IN}. On the second half of the cycle, C1 and C2 are connected in series between IN and OUT when the S1 switches open and the S2 switches close, as shown in Figure 1. In doubler mode, only C2 is used.

During one oscillator cycle, energy is transferred from the input to the charge-pump capacitors, and then from the charge-pump capacitors to the output capacitor and load. The number of cycles within a given time frame increases as the load increases or as the input supply voltage decreases. In the limiting case, the charge pumps operate continuously, and the oscillator frequency is nominally 500kHz.

Shutdown Mode

The MAX619 enters low-power shutdown mode when SHDN is a logic high. SHDN is a CMOS-compatible input. In shutdown mode, the charge-pump switching action is halted, OUT is disconnected from IN, and V_{OUT} falls to 0V. Connect SHDN to ground for normal operation. When V_{IN} = 3.6V, V_{OUT} typically reaches 5V in 0.5ms under no-load conditions after SHDN goes low.

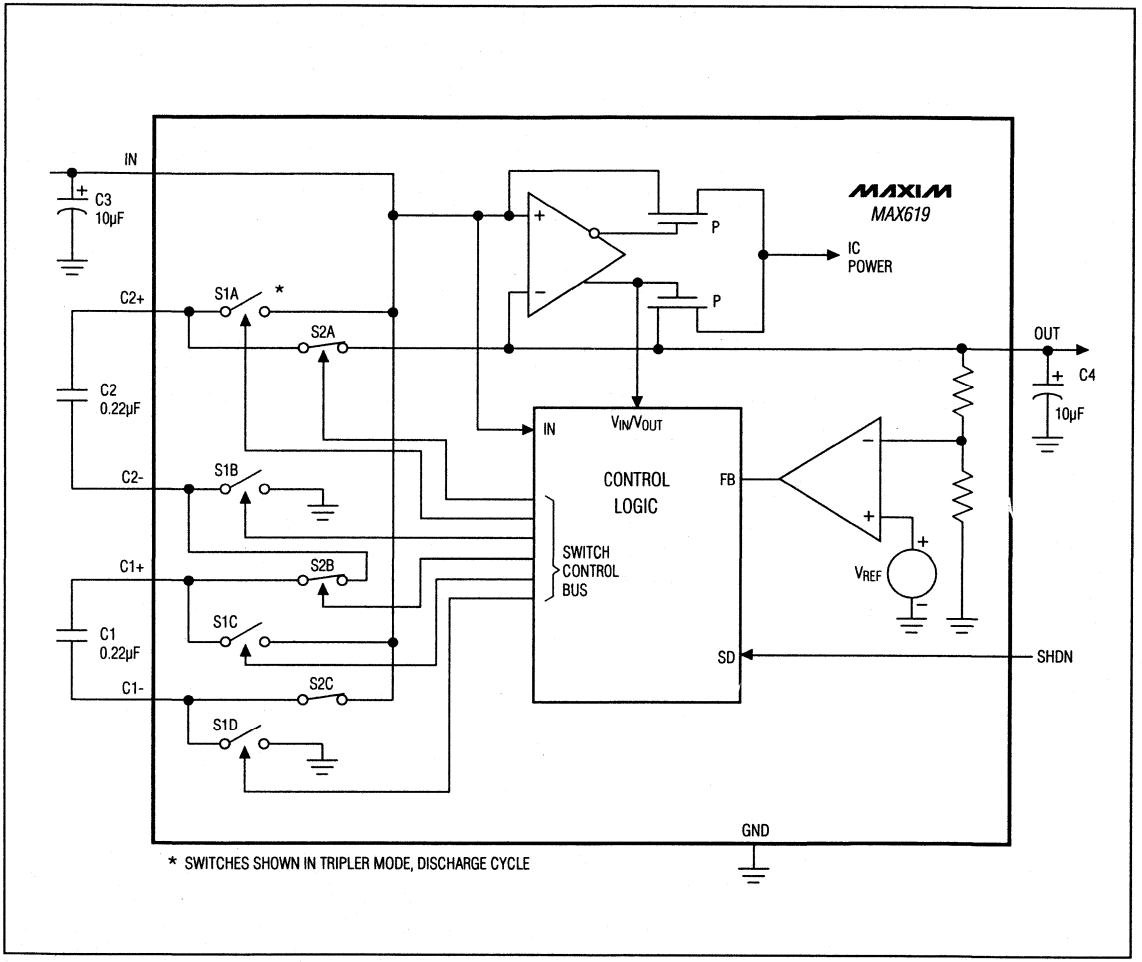


Figure 1. Block Diagram

Regulated 5V Charge-Pump DC-DC Converter

Applications Information

Capacitor Selection

Charge-Pump Capacitors C1 and C2

The values of charge-pump capacitors C1 and C2 are critical to ensure adequate output current and avoid excessive peak currents. Use values in the range of 0.22µF to 1.0µF. Larger capacitors (up to 50µF) can be used, but larger capacitors will increase output ripple. Ceramic or tantalum capacitors are recommended.

Input and Output Capacitors, C3 and C4

The type of input bypass capacitor (C3) and output filter capacitor (C4) used is not critical, but it does affect performance. Tantalums, ceramics, or aluminum electrolytics are suggested. For smallest size, use Sprague 595D106X0010A2 surface-mount capacitors, which measure 3.7mm x 1.8mm (0.146in x 0.072in). For lowest ripple, use large, low effective-series-resistance (ESR) ceramic or tantalum capacitors. For lowest cost, use aluminum electrolytic or tantalum capacitors.

Figure 2 shows the component values for proper operation using minimal board space. The input bypass capacitor (C3) and output filter capacitor (C4) should both be at least 10µF when using aluminum electrolytics or Sprague's miniature 595D series of tantalum chip capacitors.

When using ceramic capacitors, the values of C3 and C4 can be reduced to 2µF and 1µF, respectively. If the input supply source impedance is very low, C3 may not be necessary.

Many capacitors exhibit 40% to 50% variation over temperature. Compensate for capacitor temperature coefficient by selecting a larger nominal value to ensure proper operation over temperature. Table 1 lists capacitor suppliers.

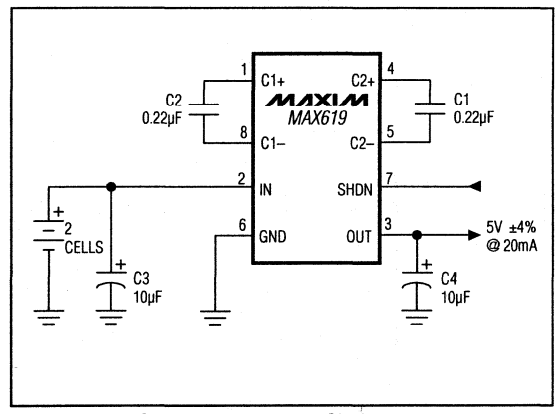


Figure 2. Two-Cell to 5V Application Circuit

Table 1. Capacitor Suppliers

SUPPLIER	PHONE NUMBER	FAX NUMBER	CAPACITOR	CAPACITOR TYPE*
Murata Erie	(814) 237-1431	(814) 238-0490	GRM42-6Z5U10M50	0.1µF ceramic (SM)
			GRM42-6Z5U22M50	0.22µF ceramic (SM)
			RPI123Z5U105M50V	1.0µF ceramic (TH)
			RPE121Z5U104M50V	0.1µF ceramic (TH)
Sprague Electric (smallest size)	(603) 224-1961 (207) 327-4140	(603) 224-1430 (207) 324-7223	595D106X0010A2	10µF tantalum (SM)

* **Note:** (SM) denotes surface-mount component, (TH) denotes through-hole component.

Layout Considerations

The MAX619's high oscillator frequency makes good layout important. A good layout ensures stability and helps maintain the output voltage under heavy loads. For best performance, use very short connections to the capacitors.

Paralleling Devices

Two MAX619s can be placed in parallel to increase output drive capability. The IN, OUT, and GND pins can be paralleled, but C1- and C2 pins cannot. The input bypass capacitor and output filter capacitor are, to some extent, shared when two circuits are paralleled. If the circuits are physically close together, it may be possible to use a single bypass and a single output capacitor, each with twice the value of the single circuit. If the MAX619s cannot be placed close together, use separate bypass and output capacitors. The amount of output ripple observed will determine whether single input bypass and output filter capacitors can be used.

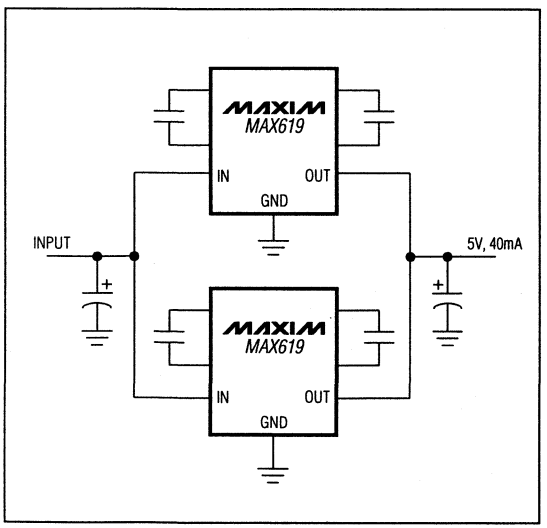
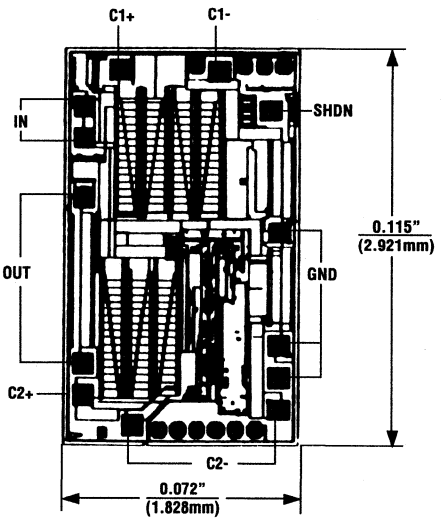


Figure 3. Paralleling Two MAX619s

Chip Topography



TRANSISTOR COUNT: 599;
SUBSTRATE CONNECTED TO GND.

19-4505; Rev 2; 4/94

EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

General Description

The MAX639/MAX640/MAX653 step-down switching regulators provide high efficiency over a wide range of load currents, delivering up to 225mA. A current-limiting pulse-frequency-modulated (PFM) control scheme gives the devices the benefits of pulse-width-modulated (PWM) converters (high efficiency at heavy loads), while using only 10µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

The MAX639/MAX640/MAX653 input range is 4V to 11.5V, and the devices provide lower preset output voltages of 5V, 3.3V, and 3V, respectively. Or, the output can be user-adjusted to any voltage from 1.3V to the input voltage.

The MAX639/MAX640/MAX653 have an internal 1A power MOSFET switch, making them ideal for minimum-component, low- and medium-power applications. For increased output drive capability, use the MAX649/MAX651/MAX652 step-down controllers, which drive an external P-channel FET to deliver up to 5W.

Applications

9V Battery to 5V, 3.3V, or 3V Conversion

High-Efficiency Linear Regulator Replacement

Portable Instruments and Handy-Terminals

5V-to-3.3V Converters

Features

- **High Efficiency for a Wide Range of Load Currents**
- **10µA Quiescent Current**
- **Output Currents Up to 225mA**
- **Preset or Adjustable Output Voltage:**
  - **5.0V (MAX639)**
  - **3.3V (MAX640)**
  - **3.0V (MAX653)**
- **Low-Battery Detection Comparator**
- **Current-Limiting PFM Control Scheme**

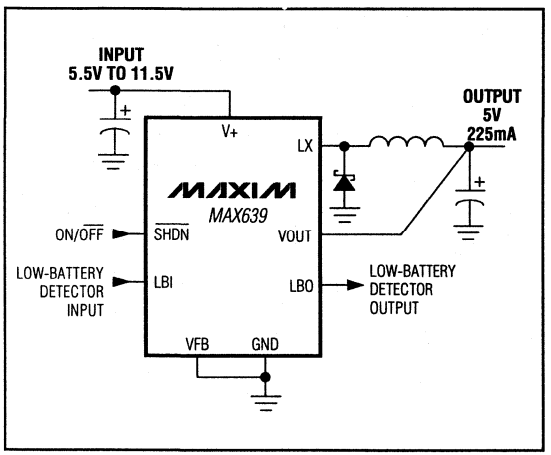
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX639CPA	0°C to +70°C	8 Plastic DIP
MAX639CSA	0°C to +70°C	8 SO
MAX639C/D	0°C to +70°C	Dice*
MAX639EPA	-40°C to +85°C	8 Plastic DIP
MAX639ESA	-40°C to +85°C	8 SO
MAX639MJA	-55°C to +125°C	8 CERDIP

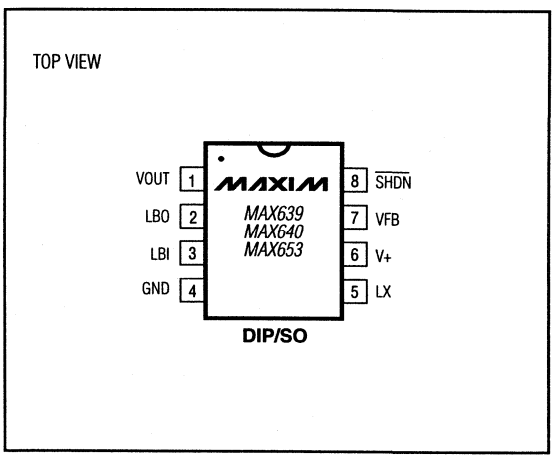
Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

V+ 12V
LX ..... (V+ - 12V) to (V+ + 0.3V)
LBI, LBO, VFB, $\overline{SHDN}$, VOUT ..... -0.3V to (V+ + 0.3V)
LX Output Current (Note 1) 1A
LBO Output Current 10mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX639C_ _ ..... 0°C to +70°C
MAX639E_ _ ..... -40°C to +85°C
MAX639MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Peak inductor current must be limited to 600mA by using an inductor of 100µH or greater.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 9V for the MAX639, V+ = 5V for the MAX640/MAX653, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			4.0		11.5	V
Supply Current	$\overline{SHDN}$ = V+, no load			10	20	µA
Output Voltage (Note 2)	MAX639, V+ = 6.0V to 11.5V, 0mA < I_{OUT} < 100mA		4.80	5.00	5.20	V
	MAX640, V+ = 4.0V to 11.5V, 0mA < I_{OUT} < 100mA		3.17	3.30	3.43	
	MAX653, V+ = 4.0V to 11.5V, 0mA < I_{OUT} < 100mA		2.88	3.00	3.12	
Dropout Voltage	I_{OUT} = 100mA, L = 100µH			0.5		V
Efficiency	MAX639	I_{OUT} = 100mA, L = 100µH		91		%
		I_{OUT} = 25mA, L = 470µH		94		
	MAX640	I_{OUT} = 100mA, L = 100µH		87		
		I_{OUT} = 25mA, L = 470µH		91		
	MAX653	I_{OUT} = 100mA, L = 100µH		85		
		I_{OUT} = 25mA, L = 470µH		89		
Switch On-Time	MAX639	V+ = 9V, V_{OUT} = 5V	10.6	12.5	14.4	µs
		V+ = 6V, V_{OUT} = 3V	14.2	16.7	19.2	
	MAX640	V+ = 9V, V_{OUT} = 3.3V	7.5	8.8	10.1	
		V+ = 4V, V_{OUT} = 3.3V	60.7	71.4	82.1	
	MAX653	V+ = 9V, V_{OUT} = 3V	7.1	8.3	9.5	
		V+ = 4V, V_{OUT} = 3V	42.5	50.0	57.5	
Switch Off-Time	MAX639	V+ = 9V, V_{OUT} = 5V	9.0	11.7	13.5	µs
		V+ = 6V, V_{OUT} = 3V	16.6	19.5	22.4	
	MAX640	V+ = 9V, V_{OUT} = 3.3V	13.3	15.6	17.9	
		V+ = 4V, V_{OUT} = 3.3V	13.3	15.6	17.9	
	MAX653	V+ = 9V, V_{OUT} = 3V	14.6	17.2	19.8	
		V+ = 4V, V_{OUT} = 3V	14.6	17.2	19.8	

ELECTRICAL CHARACTERISTICS (continued)

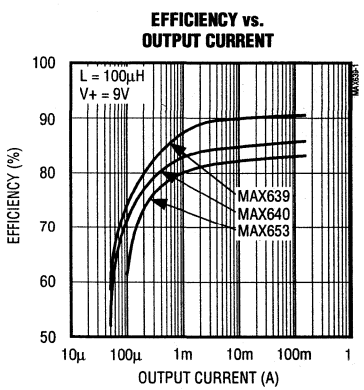
(V+ = 9V for the MAX639, V+ = 5V for the MAX640/MAX653, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

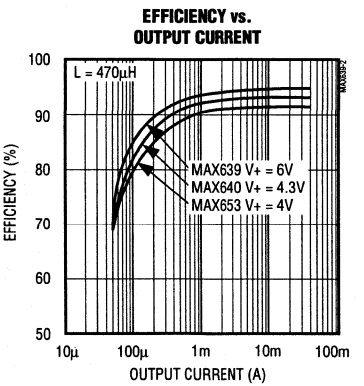
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX Switch On Resistance	V+ = 9V, T_A = +25°C, MAX639/MAX640/MAX653			0.8	1.5	Ω
	V+ = 6V, T_A = T_{MIN} to T_{MAX}, MAX639				2.5	
	V+ = 4V, T_A = T_{MIN} to T_{MAX}, MAX640/MAX653				2.8	
LX Switch Leakage	V+ = 11.5V, V_{LX} = 0V	T_A = +25°C		0.003	1.0	µA
		T_A = T_{MIN} to T_{MAX}			30.0	
VFB Bias Current	VFB = 2V			4.0	15.0	nA
VFB Dual-Mode Trip Point				50		mV
VFB Threshold	MAX6_ _C		1.26	1.28	1.30	V
	MAX6_ _E/M		1.24	1.28	1.32	
LBI Bias Current	V_{LBI} = 2V			2	10	nA
LBI Threshold	MAX6_ _C		1.26	1.28	1.30	V
	MAX6_ _E/M		1.24	1.28	1.32	
LBO Sink Current	V_{LBO} = 0.4V	MAX639	0.8	2.5		mA
		MAX640/MAX653	0.4	1.2		
LBO Leakage Current	V_{LBO} = 11.5V			0.001	0.1	µA
LBO Delay	50mV overdrive			25		µs
$\overline{SHDN}$ Threshold			0.80	1.15	2.00	V
$\overline{SHDN}$ Pull-Up Current	$\overline{SHDN}$ = 0V		0.10	0.20	0.40	µA

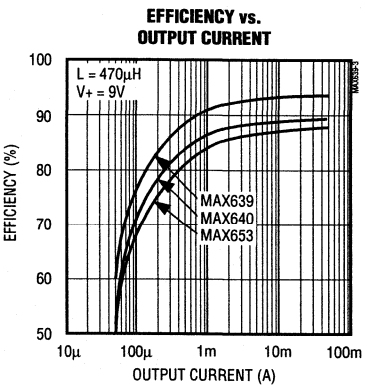
Note 2: Output guaranteed by correlation to measurements of device parameters (i.e., switch ON resistance, on-times, off-times, and output voltage trip points).

Typical Operating Characteristics

(Circuit of Figure 3, internal feedback, L = 100µH, T_A = +25°C, unless otherwise noted.)





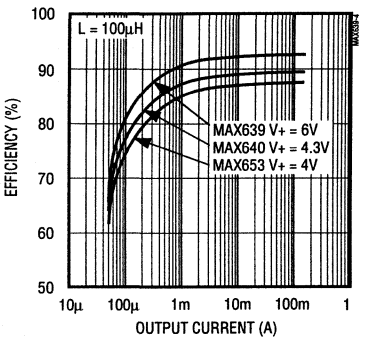


5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

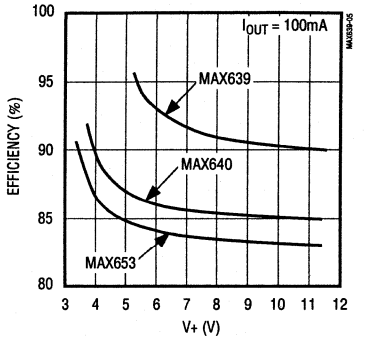
Typical Operating Characteristics (continued)

(Circuit of Figure 3, internal feedback, L = 100µH, T_A = +25°C, unless otherwise noted.)

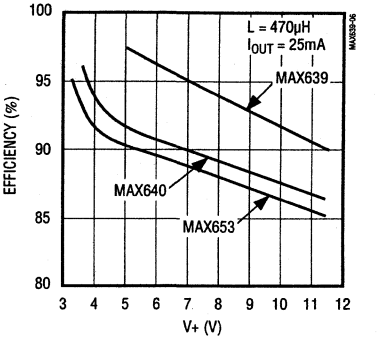
EFFICIENCY vs. OUTPUT CURRENT



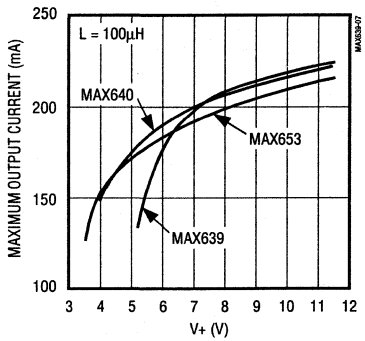
EFFICIENCY vs. INPUT VOLTAGE



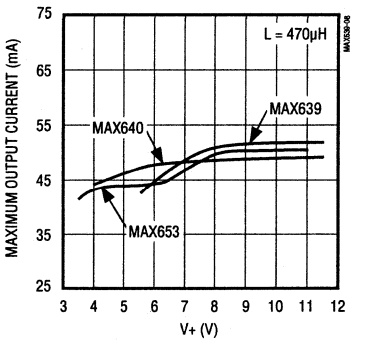
EFFICIENCY vs. INPUT VOLTAGE



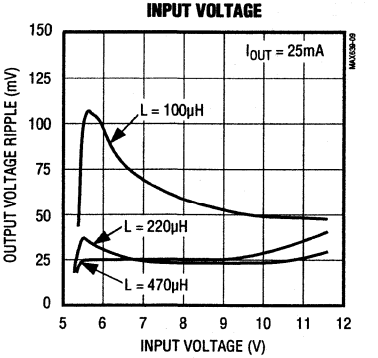
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



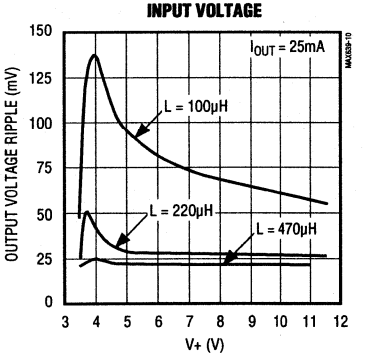
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



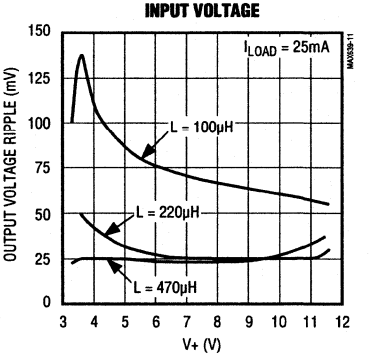
MAX639 OUTPUT VOLTAGE RIPPLE vs. INPUT VOLTAGE



MAX640 OUTPUT VOLTAGE RIPPLE vs. INPUT VOLTAGE



MAX653 OUTPUT VOLTAGE RIPPLE vs. INPUT VOLTAGE

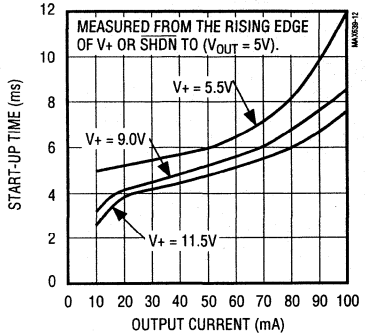


5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

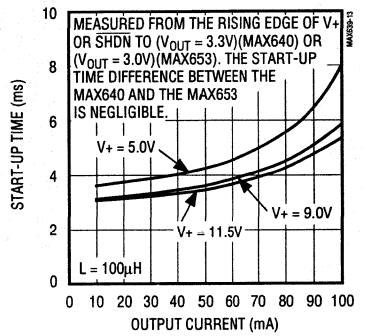
Typical Operating Characteristics (continued)

(Circuit of Figure 3, internal feedback, L = 100µH, T_A = +25°C, unless otherwise noted.)

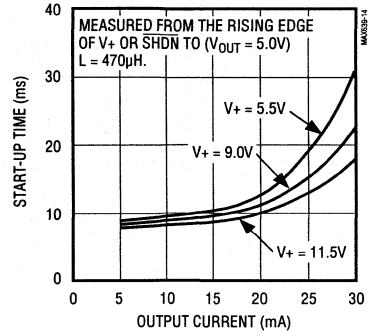
MAX639 START-UP TIME vs. OUTPUT CURRENT



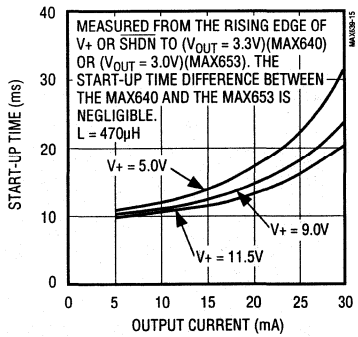
MAX640/MAX653 START-UP TIME vs. OUTPUT CURRENT



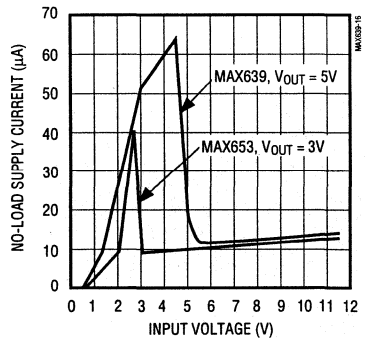
MAX639 START-UP TIME vs. OUTPUT CURRENT



MAX640/MAX653 START-UP TIME vs. OUTPUT CURRENT



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE

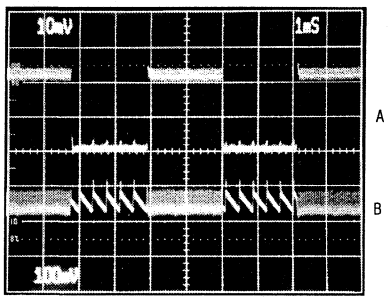


5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

Typical Operating Characteristics (continued)

(Circuit of Figure 3, internal feedback, L = 100µH, T_A = +25°C, unless otherwise noted.)

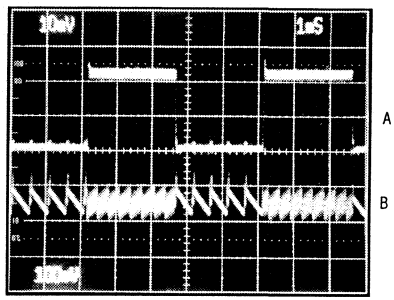
MAX653
LOAD-TRANSIENT RESPONSE



1ms/div

A: I_{LOAD}, 0mA TO 100mA, 50mA/div
B: V_{OUT}, 100mV/div, AC COUPLED
V_{IN} = 5V, V_{OUT} = 3V

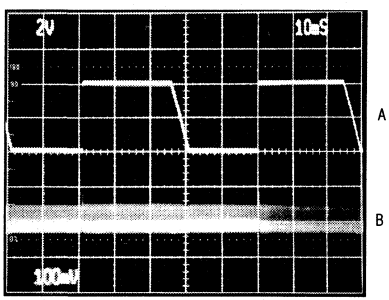
MAX639
LOAD-TRANSIENT RESPONSE



1ms/div

A: I_{LOAD}, 0mA TO 200mA, 100mA/div
B: V_{OUT}, 100mV/div, AC COUPLED
V_{IN} = 9V, V_{OUT} = 5V

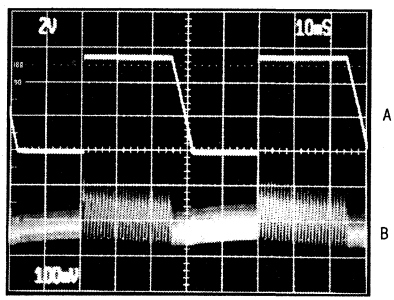
MAX653
LINE-TRANSIENT RESPONSE



10ms/div

A: V_{IN}, 4V TO 8V, 2V/div
B: V_{OUT}, 100mV/div
V_{OUT} = 3V, I_{LOAD} = 100mA

MAX639
LINE-TRANSIENT RESPONSE



10ms/div

A: V_{IN}, 6V TO 11.5V, 2V/div
B: V_{OUT}, 100mV/div
V_{OUT} = 5V, I_{LOAD} = 100mA

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

Pin Description

PIN	NAME	FUNCTION
1	VOUT	Sense Input for regulated-output operation. Internally connected to an on-chip voltage divider and to the variable duty-cycle, on-demand oscillator. It must be connected to the external regulated output.
2	LBO	Low-Battery Output. An open-drain N-channel MOSFET sinks current when the voltage at LBI drops below 1.28V.
3	LBI	Low-Battery Input. When the voltage at LBI drops below 1.28V, LBO sinks current.
4	GND	Ground
5	LX	Drain of a PMOS power switch that has its source connected to V+. LX drives the external inductor, which provides current to the load.
6	V+	Positive Supply-Voltage Input. Should not exceed 11.5V
7	VFB	Dual-Mode Feedback Pin. When VFB is grounded, the internal voltage divider sets the output to 5V (MAX639), 3.3V (MAX640) or 3V (MAX653). For adjustable operation, connect VFB to an external voltage divider.
8	$\overline{SHDN}$	Shutdown Input — active low. When pulled below 0.8V, the LX power switch stays off, shutting down the regulator. When the shutdown input is above 2V, the regulator stays on. Tie $\overline{SHDN}$ to V+ if shutdown mode is not used.

Getting Started

Designing power supplies with the MAX639/MAX640/MAX653 is easy. The few required external components are readily available. The most general applications use the following components:

(1) Capacitors: For the input and output filter capacitors, try using electrolytics in the 100µF range, or use low-ESR capacitors to minimize output ripple. Capacitor values are not critical.

(2) Diode: Use the popular 1N5817 or equivalent Schottky diode.

(3) Inductor: For the highest output current, choose a 100µH inductor with an incremental saturation current rating of at least 600mA. To obtain the highest efficiencies and smallest size, refer to the *Inductor Selection* section.

Detailed Description

Figure 1 shows a simplified, step-down DC-DC converter. When the switch is closed, a voltage equal to (V+ - V_{OUT}) is applied to the inductor. The current through the inductor ramps up, storing energy in the inductor's magnetic field. This same current also flows into the output filter capacitor and load. When the switch opens, the current continues to flow through the inductor in the same direction, but must also flow through the diode. The inductor alone supplies current to the load when the switch is open. This current decays to zero as the energy stored in the inductor's magnetic field is transferred to the output filter capacitor and the load.

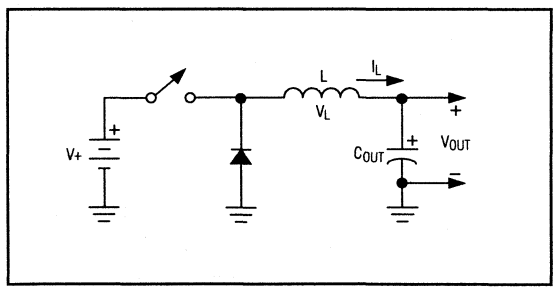


Figure 1. Simplified Step-Down Converter

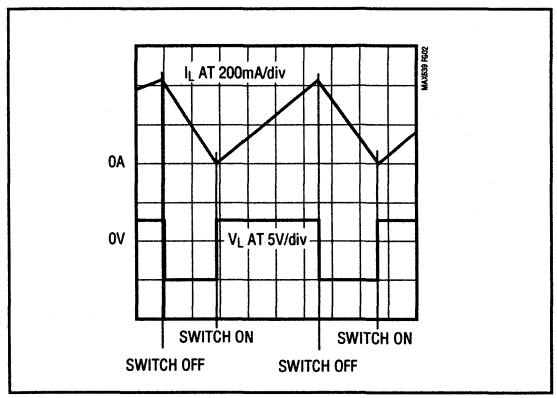


Figure 2. Simplified Step-Down Converter Operation

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

Figure 2 shows what happens to the ideal circuit of Figure 1 if the switch turns on with a 66% duty cycle and V+ = 3/2 VOUT. The inductor current rises more slowly than it falls because the magnitude of the voltage applied during tON is less than that applied during tOFF. Varying the duty cycle and switching frequency keeps the peak current constant as input voltage varies. The MAX639/MAX640/MAX653 control the switch (tON and tOFF) according to the following equations:

Equation (1) $t_{ON} = 50\mu sV / (V+ - V_{OUT})$

Equation (2) $t_{OFF} \geq 50\mu sV / V_{OUT}$

Equation (3) $I_{PEAK} = 50\mu sV / L$

These three equations ensure constant peak currents for a given inductor value, across all input voltages (ignoring the voltage drop across the diode (D1) and the resistive losses in the switch and inductor). The variable duty cycle also ensures that the current through the inductor discharges to zero at the end of each pulse.

Figure 3 shows the MAX639/MAX640/MAX653 block diagram and a typical connection in which 9V is converted to 5V (MAX639), 3.3V (MAX640), or 3.0V (MAX653). The sequence of events in this application is as follows:

When the output dips:

(1) The error comparator switches high.

(2) The internal oscillator starts (15µs start-up time) and connects to the gate of the LX output driver.

(3) LX turns on and off according to tON and tOFF, charging and discharging the inductor, and supplying current to the output (as described above).

When the output voltage recovers:

(1) The comparator switches low.

(2) LX turns off.

(3) The oscillator shuts down to save power.

Fixed or Adjustable Output

For operation at the preset output voltage, connect VFB to GND; no external resistors are required. For other output voltages, use an external voltage divider. Set the output voltage using R3 and R4 as determined by the following formula:

$$R3 = R4\ [(V_{OUT} / VFB\ Threshold) - 1]$$

where R4 is any resistance in the 10kΩ to 1MΩ range (typically 100kΩ), and the VFB threshold is typically 1.28V.

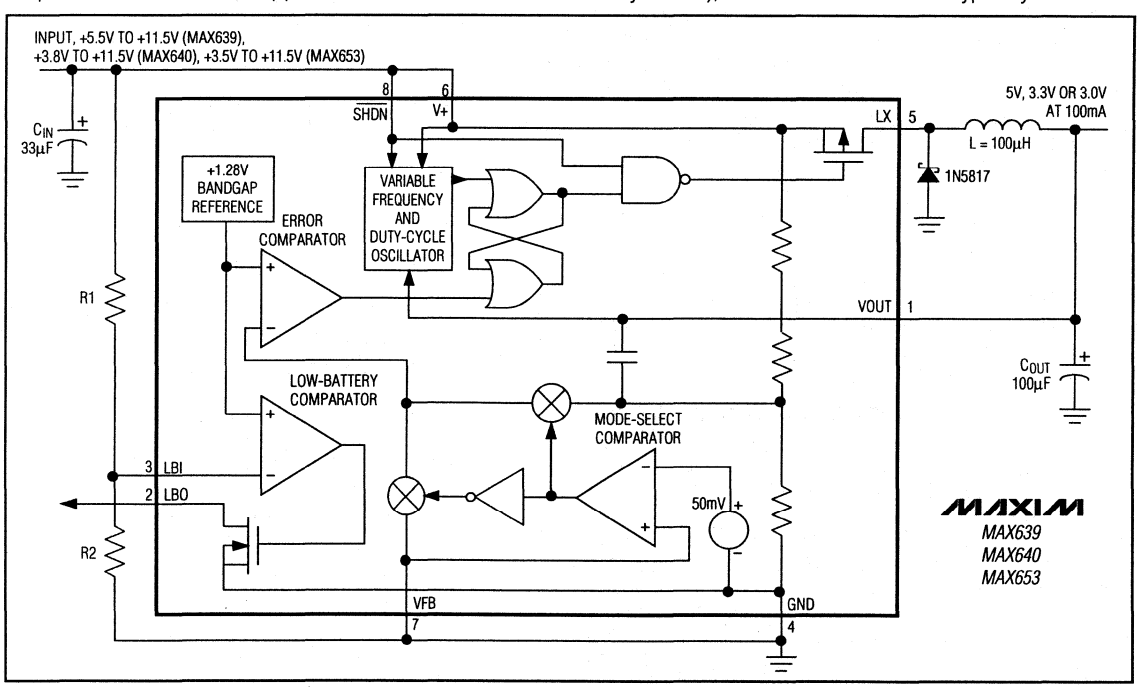


Figure 3. Block Diagram

Low-Battery Detector

The low-battery detector compares the voltage on the LBI input with the internal 1.28V reference. LBO goes low whenever the input voltage at LBI is less than 1.28V. Set the low-battery detection voltage with resistors R1 and R2 (Figure 3) as determined by the following formula:

$$R1 = R2\ [(VLB / LBI\ Threshold) - 1]$$

where R2 is any resistance in the 10kΩ to 1MΩ range (typically 100kΩ), the LBI threshold is typically 1.28V, and VLB is the desired low-battery detection voltage.

The low-battery comparator remains active in shutdown mode.

Shutdown Mode

Bringing $\overline{SHDN}$ below 0.8V places the MAX639/MAX640/MAX643 in shutdown mode. LX becomes high impedance, and the voltage at VOUT falls to zero. The time required for the output to rise to its nominal regulated voltage when brought out of shutdown (start-up time) depends on the inductor value, input voltage, and load current (see the Start-Up Time vs. Output Current graph in the *Typical Operating Characteristics*). The low-battery comparator remains active in shutdown mode.

Applications Information

Inductor Selection

When selecting an inductor, consider these four factors: peak-current rating, inductance value, series resistance, and size. It is important not to exceed the inductor's peak-current rating. A saturated inductor will pull excessive currents through the MAX639/MAX640/MAX653's switch, and may cause damage. Avoid using RF chokes or air-core inductors since they have very low peak-current ratings. Electromagnetic interference must not upset nearby circuitry or the regulator IC. Ferrite-bobbin types work well for most digital circuits; toroids or pot cores work well for EMI-sensitive analog circuits.

Recall that the inductance value determines I_{PEAK} for all input voltages (Equation 3). If there are no resistive losses and the diode is ideal, the maximum average current that can be drawn from the MAX639/MAX640/MAX653 will be one-half I_{PEAK}. With the real losses in the switch, inductor, and diode taken into account, the real maximum output current typically varies from 90% to 50% of the ideal. The following steps describe a conservative way to pick an appropriate inductor.

Step 1: Decide on the maximum required output current, in amperes: I_{OUTMAX}.

Step 2: $I_{PEAK} = 4 \times I_{OUTMAX}$.

Table 1. Component Suppliers

INDUCTORS — THROUGH HOLE

PART NUMBER	SIZE (inches)	VALUE (µH)	I_{MAX} (A)	SERIES R (Ω)
MAXL001*	0.65 x 0.33 dia.	100	1.75	0.2
7300-13**	0.63 x 0.26 dia.	100	0.89	0.27
7300-15**	0.63 x 0.26 dia.	150	0.72	0.36
7300-17**	0.63 x 0.26 dia.	220	0.58	0.45
7300-19**	0.63 x 0.26 dia.	330	0.47	0.58
7300-21**	0.63 x 0.26 dia.	470	0.39	0.86
7300-25**	0.63 x 0.26 dia.	1000	0.27	2.00

* Maxim Integrated Products
**Caddell-Burns
258 East Second Street
Mineola, NY 11501-3508
(516) 746-2310

INDUCTORS — SURFACE MOUNT

PART NUMBER	SIZE (mm)	VALUE (µH)	I_{MAX} (A)	SERIES R (Ω)
CD54	5.2 x 5.8 x 4.5	100	0.52	0.63
CD54	5.2 x 5.8 x 4.5	220	0.35	1.50
CDR74	7.1 x 7.7 x 4.5	100	0.52	0.51
CDR74	7.1 x 7.7 x 4.5	220	0.35	0.98
CDR105	9.2 x 10.0 x 5.0	100	0.80	0.35
CDR105	9.2 x 10.0 x 5.0	220	0.54	0.69

Sumida Electric (USA)
637 East Golf Road
Arlington Heights, IL 60005
(708) 956-0666

CAPACITORS — LOW ESR

PART NUMBER	SIZE (inches)	VALUE (µF)	ESR (Ω)	V_{MAX} (V)
MAXC001*	0.49 x 0.394 dia.	150	0.2	35
267 Series**	D SM packages	47	0.2	10
267 Series**	E SM packages	100	0.2	6.3

* Maxim Integrated Products
**Matsuo Electronics
2134 Main Street
Huntington Beach, CA 92648
(714) 969-2491

SCHOTTKY DIODES — SURFACE MOUNT

PART NUMBER	SIZE	V_F (V)	I_{MAX} (A)
SE014	SOT89	0.55	1
SE024	SOT89	0.55	0.95

Collmer Semiconductor
14368 Proton Road
Dallas, TX 75244
(214) 233-1589

NOTE: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

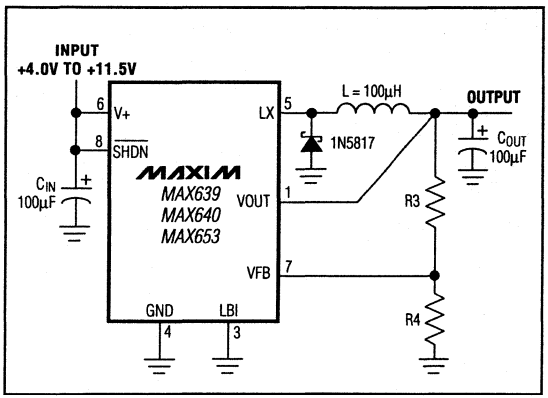


Figure 4. Adjustable-Output Operation

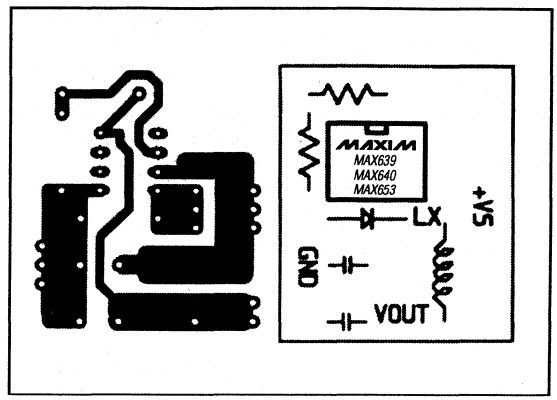


Figure 5. Through-Hole PC Layout and Component Placement Diagram for Standard Step-Down Application (Top-Side View)

Step 3: L = 50 / I_{PEAK}. L will be in µH. Do not use an inductor of less than 100µH.

Step 4: Make sure that I_{PEAK} does not exceed 0.6A or the inductor's maximum current rating, whichever is lower.

Inductor series resistance affects both efficiency and dropout voltage. A high series resistance severely limits the maximum current available at lower input voltages. Output currents up to 225mA are possible if the inductor has low series resistance. Inductor and series switch resistance form an LR circuit during t_{ON}. If the L/R time constant is less than the oscillator t_{ON}, the inductor's peak current will fall short of the desired I_{PEAK}.

To maximize efficiency, choose the highest-value inductor that will provide the required output current over the whole range of your input voltage (see *Typical Operating Characteristics*). Inductors with peak currents in the 600mA range do not need to be very large. They are about the size of a 1W resistor, with surface-mount versions less than 5mm in diameter. Table 1 lists suppliers of inductors suitable for use with the MAX639/MAX640/MAX653.

Output Filter Capacitor

The MAX639/MAX640/MAX653's output ripple has two components. One component results from the variation in stored charge on the filter capacitor with each LX pulse. The other is the product of the current into the capacitor and the capacitor's equivalent series resistance (ESR).

The amount of charge delivered in each oscillator pulse is determined by the inductor value and input voltage. It decreases with larger inductance, but increases as the input voltage lessens. As a general rule, a smaller amount of charge delivered in each pulse results in less output ripple.

With low-cost aluminum electrolytic capacitors, the ESR-induced ripple can be larger than that caused by the charge variation. Consequently, high-quality aluminum-electrolytic or tantalum filter capacitors will minimize output ripple. Best results at reasonable cost are typically achieved with an aluminum-electrolytic capacitor in the 100µF range, in parallel with a 0.1µF ceramic capacitor (Table 1).

External Diode

In most MAX639/MAX640/MAX653 circuits, the current in the external diode (D1, Figure 3) changes abruptly from zero to its peak value each time LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low-power circuits with peak currents less than 100mA, signal diodes such as the 1N4148 perform well. The 1N5817 diode works well for high-power circuits, or for maximum efficiency at low power. 1N5817 equivalent diodes are also available in surface-mount packages (Table 1). Although the 1N4001 and other general-purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-off times result in excessive losses.

Minimum Load

Under no-load conditions, because of leakage from the PMOS power switch (see the LX Leakage Current vs. Temperature graph in the *Typical Operating Characteristics*) and from the internal resistor from V+ to V_{OUT}, leakage current may be supplied to the output

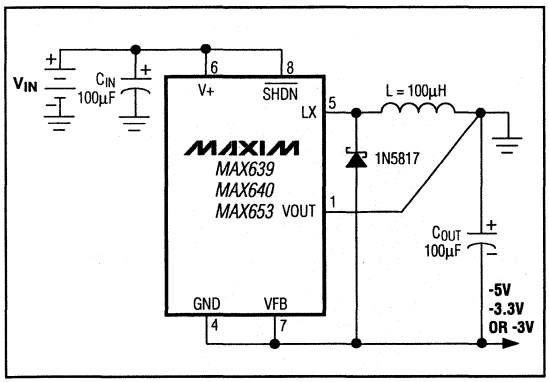


Figure 6. Inverting Configuration

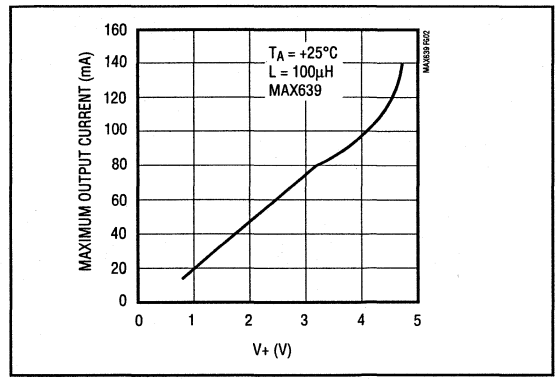


Figure 7. Maximum Current Capability of Figure 6 Circuit

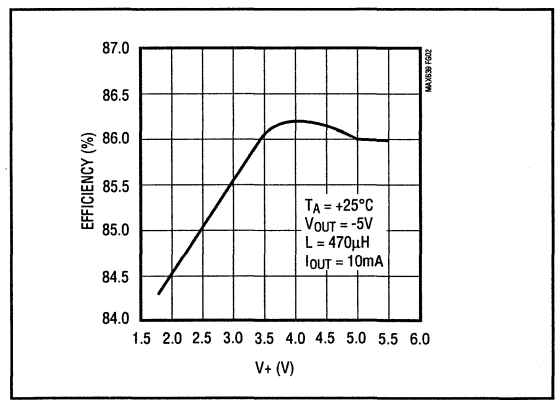


Figure 8. Efficiency of Figure 6 Circuit

capacitor, even when the switch is off. This will usually not be a problem for a 5V output at room temperature, since the diode's reverse leakage current and the feedback resistors' current typically drain the excess. However, if the diode leakage is very low (which can occur at low temperatures and/or small output voltages), charge may build up on the output capacitor, making VOUT rise above its set point. If this happens, add a small load resistor (typically 1MΩ) to the output to pull a few extra microamps of current from the output capacitor.

Layout

Several of the external components in a MAX639/MAX640/MAX653 circuit experience peak currents up to 600mA. Wherever one of these components connects to ground, there is a potential for ground bounce. Ground bounce occurs when high currents flow through the parasitic resistances of PC board traces. What one component interprets as ground can differ from the IC's ground by several millivolts. This may increase the MAX639/MAX640/MAX653's output ripple, since the error comparator (which is referenced to ground) will generate extra switching pulses when they are not needed. It is essential that the input filter capacitor's ground lead, the MAX639/MAX640/MAX653's GND pin, the diode's anode, and the output filter capacitor's ground lead are as close together as possible, preferably at the same point. Figure 5 shows a suggested through-hole printed circuit layout that minimizes ground bounce.

Inverter Configuration

Figure 6 shows the MAX639/MAX640/MAX653 in a floating ground configuration. By tying what would normally be the output to the supply-voltage ground, the IC's GND pin is forced to a regulated -5V (MAX639), -3.3V (MAX640), or -3V (MAX653). Avoid exceeding the maximum differential voltage of 11.5V from V+ to VOUT. Other negative voltages can be generated by placing a voltage divider across COUT and connecting the tap point to VFB in the same manner as the normal step-down configuration.

Two AA Batteries to 5V, 3.3V, or 3V

For battery-powered applications, where the signal ground does not have to correspond to the power-supply ground, the circuit in Figure 6 generates 5V (MAX639), 3.3V (MAX640), or 3V (MAX653) from a pair of AA batteries. Connect the VIN ground point to your system's input, and connect the output to your system's ground input. This configuration has the added advantage of reduced on resistance, since the IC's internal power FET has VIN + VOUT of gate drive (Figures 7 and 8).

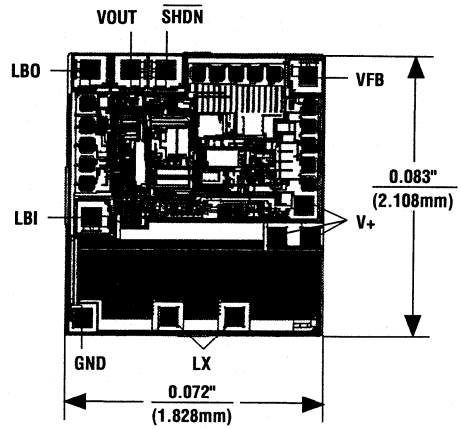
5V/3.3V/3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converters

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX640CPA	0°C to +70°C	8 Plastic DIP
MAX640CSA	0°C to +70°C	8 SO
MAX640C/D	0°C to +70°C	Dice*
MAX640EPA	-40°C to +85°C	8 Plastic DIP
MAX640ESA	-40°C to +85°C	8 SO
MAX640MJA	-55°C to +125°C	8 CERDIP
MAX653CPA	0°C to +70°C	8 Plastic DIP
MAX653CSA	0°C to +70°C	8 SO
MAX653C/D	0°C to +70°C	Dice*
MAX653EPA	-40°C to +85°C	8 Plastic DIP
MAX653ESA	-40°C to +85°C	8 SO
MAX653MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

_____Chip Topography



TRANSISTOR COUNT: 221
SUBSTRATE CONNECTED TO V+

19-0225; Rev 1; 7/94

EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

General Description

The MAX649/MAX651/MAX652 BiCMOS, step-down DC-DC switching controllers provide high efficiency over three decades of load current. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using only 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over loads ranging from 10mA to more than 2.5A.

These devices use miniature external components. Their high switching frequency (up to 300kHz) allows for less than 9mm diameter surface-mount inductors.

The MAX649/MAX651/MAX652 have dropout voltages less than 1V and accept input voltages up to 16.5V. Output voltages are preset at 5V (MAX649), 3.3V (MAX651), and 3V (MAX652). These controllers can also be adjusted to any voltage from 1.5V to the input voltage by using two resistors.

These step-down controllers drive external P-channel MOSFETs at loads greater than 10W. If less power is required, use the MAX639/MAX640/MAX653 step-down converters with on-chip FETs, which allow up to a 225mA load current.

Applications

5V-to-3.3V Green PC Applications

High-Efficiency Step-Down Regulation

Minimum-Component DC-DC Converters

Battery-Powered Applications

Features

- **More than 90% Efficiency (10mA to 1.5A Loads)**
- **More than 12.5W Output Power**
- **100µA Max Quiescent Supply Current**
- **5µA Max Shutdown Supply Current**
- **Less than 1.0V Dropout Voltage**
- **16.5V Max Input Voltage**
- **5V (MAX649), 3.3V (MAX651), 3V (MAX652), or Adjustable Output Voltage**
- **Current-Limited Control Scheme**
- **Up to 300kHz Switching Frequency**

Ordering Information

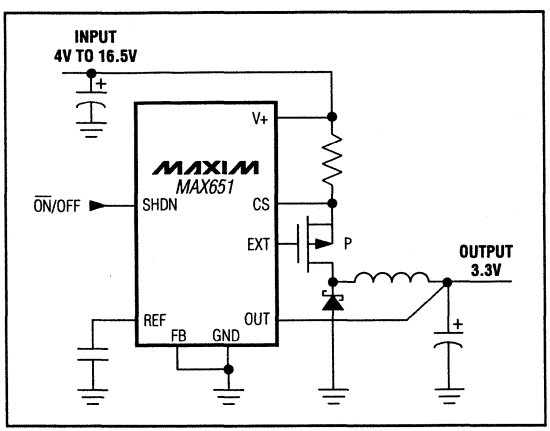
PART	TEMP. RANGE	PIN-PACKAGE
MAX649CPA	0°C to +70°C	8 Plastic DIP
MAX649CSA	0°C to +70°C	8 SO
MAX649C/D	0°C to +70°C	Dice*
MAX649EPA	-40°C to +85°C	8 Plastic DIP
MAX649ESA	-40°C to +85°C	8 SO
MAX649MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

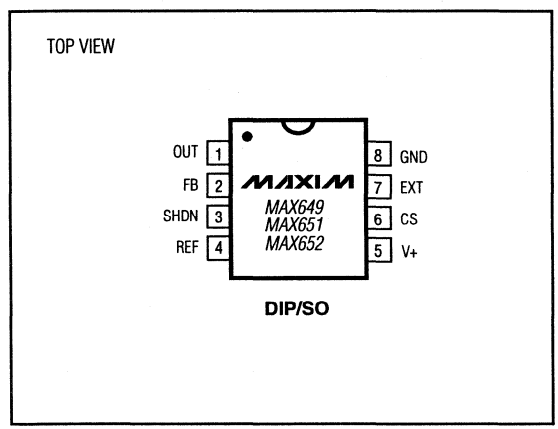
** Dice are tested at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to GND .....-0.3V, +17V
REF, SHDN, FB, CS, EXT, OUT .....-0.3V, (V+ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX649C_A, MAX65_C_A .....0°C to +70°C
MAX649E_A, MAX65_E_A .....-40°C to +85°C
MAX649MJA, MAX65_MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+			4.0		16.5	V
Supply Current	I_Q	V+ = 16.5V, SHDN ≤ 0.4V (operating, switch off)			80	100	µA
		V+ = 16.5V, SHDN ≥ 1.6V (shutdown)			4		
		V+ = 10V, SHDN ≥ 1.6V (shutdown)			2	5	
FB Trip Point		MAX649C, MAX65_C		1.470	1.5	1.530	V
		MAX649E, MAX65_E		1.4625	1.5	1.5375	
		MAX649M, MAX65_M		1.455	1.5	1.545	
FB Input Current	I_{FB}	MAX649C, MAX65_C				±50	nA
		MAX649E, MAX65_E				±70	
		MAX649M, MAX65_M				±90	
Output Voltage	V_{OUT}	Circuit of Figure 1	MAX649, V+ = 6V to 16.5V	4.80	5.0	5.20	V
			MAX651, V+ = 4V to 16.5V	3.17	3.3	3.43	
			MAX652, V+ = 4V to 16.5V	2.88	3.0	3.12	
Reference Voltage	V_{REF}	MAX649C, MAX65_C, I_{REF} = 0µA		1.470	1.5	1.530	V
		MAX649E, MAX65_E, I_{REF} = 0µA		1.4625	1.5	1.5375	
		MAX649M, MAX65_M, I_{REF} = 0µA		1.455	1.5	1.545	
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA, sourcing only	MAX649C/E, MAX65_C/E		4	10	mV
			MAX649M, MAX65_M		4	15	
REF Line Regulation		4V ≤ V+ ≤ 16.5V			40	100	µV/V
Output Voltage Line Regulation		Circuit of Figure 1	MAX649, 6V ≤ V+ ≤ 16V, I_{LOAD} = 1A		2.6		mV/V
			MAX651, 4.5V ≤ V+ ≤ 16V, I_{LOAD} = 1A		1.7		
			MAX652, 4V ≤ V+ ≤ 16V, I_{LOAD} = 1A		1.9		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

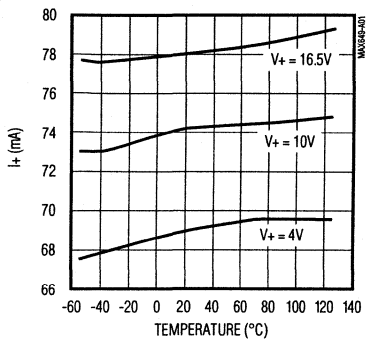
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Load Regulation		Circuit of Figure 1	MAX649, 0A ≤ I_{LOAD} ≤ 1.5A, V_{IN} = 10V		-47		mV/A
			MAX651, 0A ≤ I_{LOAD} ≤ 1.5A, V_{IN} = 5V		-45		
			MAX652, 0A ≤ I_{LOAD} ≤ 1.5A, V_{IN} = 5V		-45		
Efficiency		Circuit of Figure 1	MAX649, V+ = 10V, I_{LOAD} = 1A		92		%
			MAX651, V+ = 5V, I_{LOAD} = 1A		89		
			MAX652, V+ = 5V, I_{LOAD} = 1A		88		
SHDN Input Current		V+ = 16.5V, SHDN = 0V or V+				1	µA
SHDN Input Voltage High	V_{IH}	4V ≤ V+ ≤ 16.5V		1.6			V
SHDN Input Voltage Low	V_{IL}	4V ≤ V+ ≤ 16.5V				0.4	V
Current-Limit Trip Level (V+ to CS)	V_{CS}	4V ≤ V+ ≤ 16.5V	MAX649C/E, MAX65_C/E	180	210	240	mV
			MAX649M, MAX65_M	160	210	260	
CS Input Current		4V ≤ V+ ≤ 16.5V				±1	µA
Switch Maximum On-Time	t_{ON} (max)	V+ = 12V		12	16	20	µs
Switch Minimum Off-Time	t_{OFF} (min)	V+ = 12V		1.8	2.3	2.8	µs
EXT Rise Time		C_{EXT} = 0.001µF, V+ = 12V			50		ns
EXT Fall Time		C_{EXT} = 0.001µF, V+ = 12V			50		ns

5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

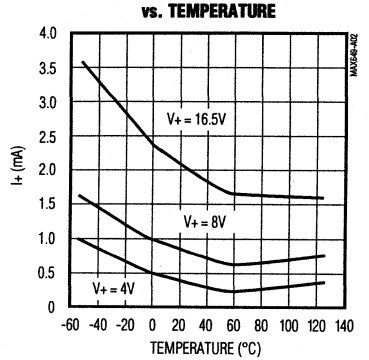
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

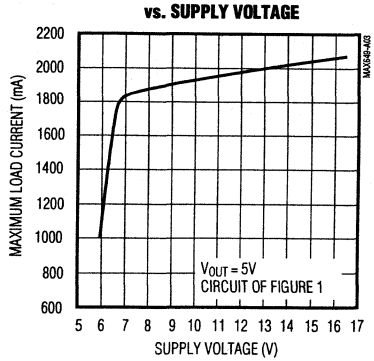
SUPPLY CURRENT vs. TEMPERATURE



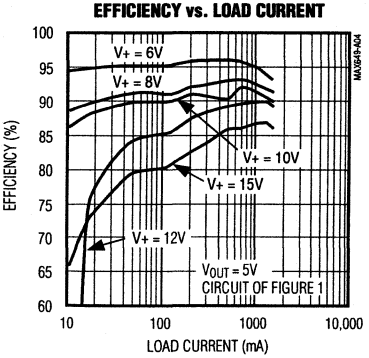
SHUTDOWN CURRENT vs. TEMPERATURE



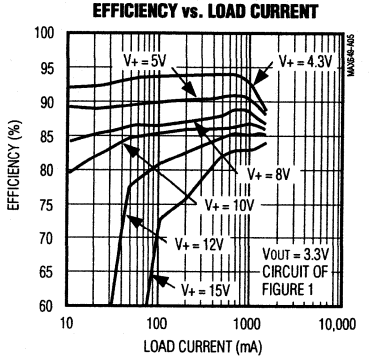
MAXIMUM LOAD CURRENT vs. SUPPLY VOLTAGE



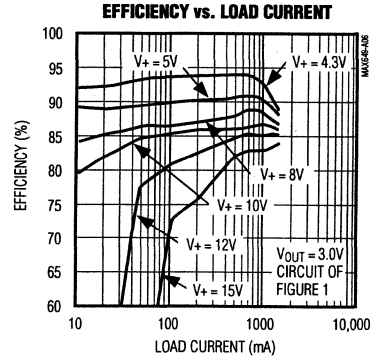
MAX649 EFFICIENCY vs. LOAD CURRENT



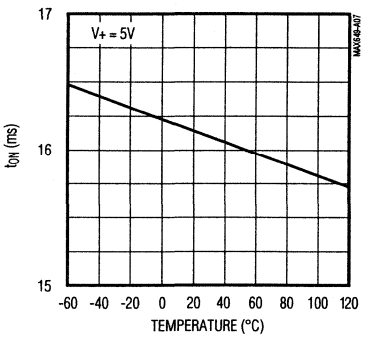
MAX651 EFFICIENCY vs. LOAD CURRENT



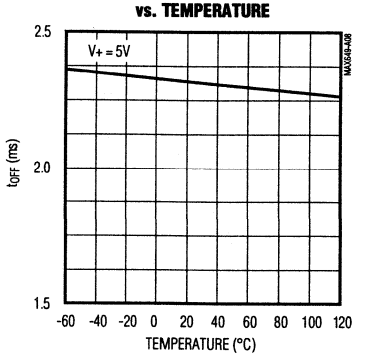
MAX652 EFFICIENCY vs. LOAD CURRENT



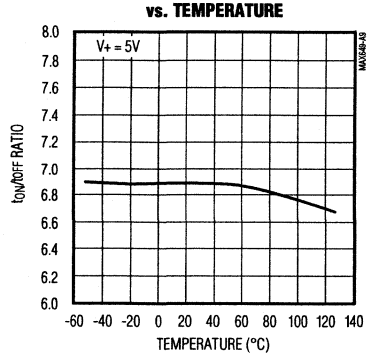
SWITCH ON-TIME vs. TEMPERATURE



SWITCH OFF-TIME vs. TEMPERATURE



SWITCH ON-TIME/OFF-TIME RATIO vs. TEMPERATURE

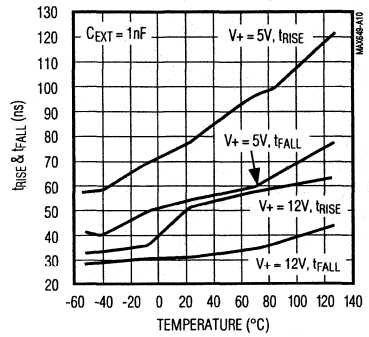


5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

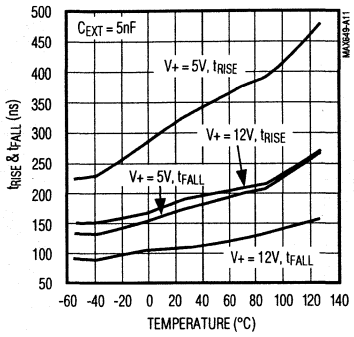
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

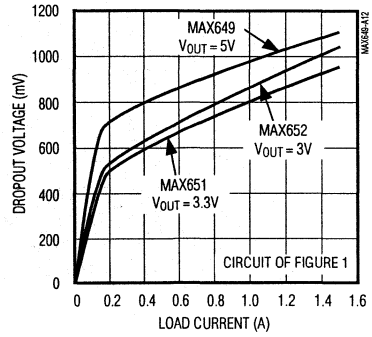
EXT RISE AND FALL TIMES vs. TEMPERATURE (1nF)



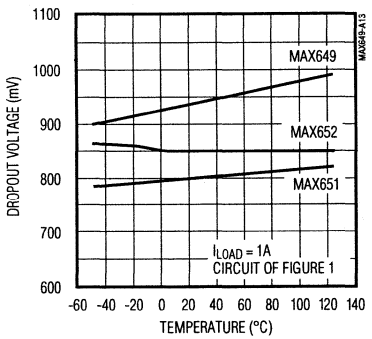
EXT RISE AND FALL TIMES vs. TEMPERATURE (5nF)



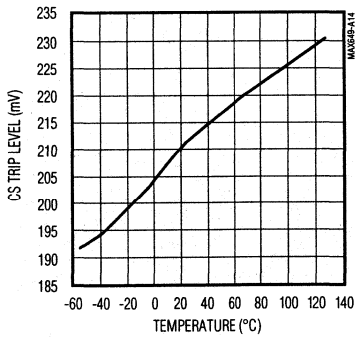
DROPOUT VOLTAGE vs. LOAD CURRENT



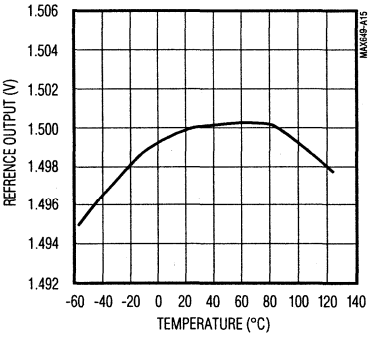
DROPOUT VOLTAGE vs. TEMPERATURE



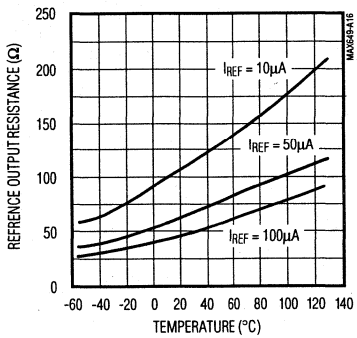
CS TRIP LEVEL vs. TEMPERATURE



REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE

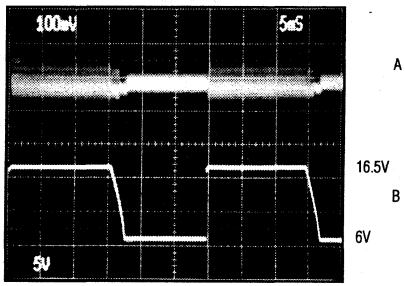


5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

Typical Operating Characteristics (continued)

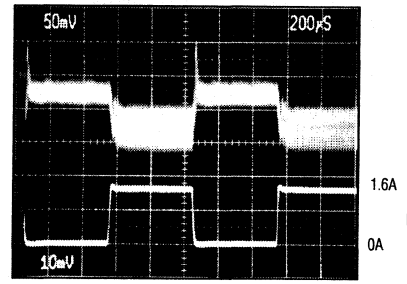
(T_A = +25°C, unless otherwise noted.)

MAX649
LINE-TRANSIENT RESPONSE



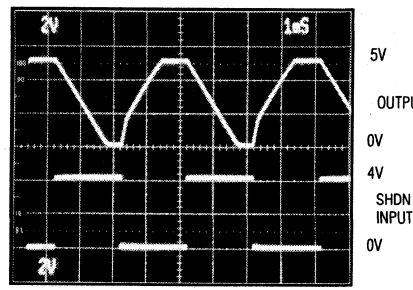
5ms/div
CIRCUIT OF FIGURE 1, I_{LOAD} = 1A
A: V_{OUT} = 5V, 100mV/div, AC-COUPLED
B: V+ = 6V TO 16.5V, 5V/div

MAX649
LOAD-TRANSIENT RESPONSE



200µs/div
CIRCUIT OF FIGURE 1, V+ = 10V
A: V_{OUT} = 5V, 100mV/div, AC-COUPLED
B: I_{LOAD} = 30mA TO 1.6A, 1A/div

MAX649
SHDN RESPONSE TIME



1ms/div
CIRCUIT OF FIGURE 1, V+ = 10V, I_{LOAD} = 1A

Pin Description

PIN	NAME	FUNCTION
1	OUT	Sense input for fixed 5V, 3.3V, or 3V output operation. OUT is internally connected to the on-chip voltage divider. Although it is connected to the output of the circuit, the OUT pin does not supply current.
2	FB	Feedback input. Connect to GND for fixed-output operation. Connect a resistor divider between OUT, FB, and GND for adjustable-output operation. See *Setting the Output Voltage* section.
3	SHDN	Active-high TTL/CMOS logic-level input. Part is placed in shutdown when SHDN is driven high. In shutdown mode, the reference and the external MOSFET are turned off, and OUT = 0V. Connect to GND for normal operation.
4	REF	1.5V reference output that can source 100µA. Bypass with 0.1µF.
5	V+	Positive power-supply input
6	CS	Current-sense input. Connect current-sense resistor between V+ and CS. When the voltage across the resistor equals the current-limit trip level, the external MOSFET is turned off.
7	EXT	Gate drive for external P-channel MOSFET. EXT swings between V+ and GND.
8	GND	Ground

5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

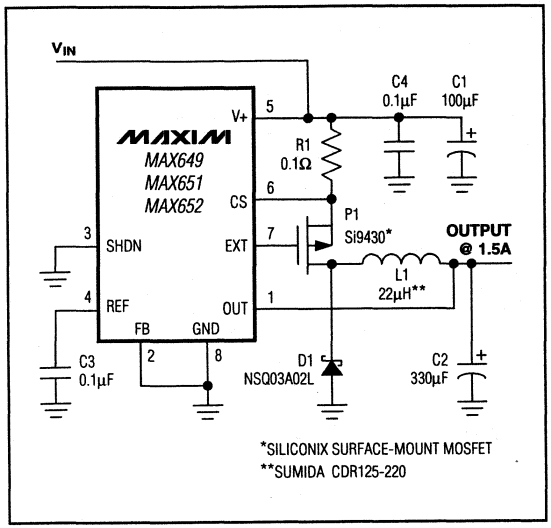


Figure 1. Test Circuit

Detailed Description

The MAX649/MAX651/MAX652 are BiCMOS, step-down, switch-mode power-supply controllers that provide fixed outputs of 5V, 3.3V, and 3V, respectively. Their unique control scheme combines the advantages of pulse-frequency-modulation (low supply current) and pulse-width-modulation (high efficiency at high loads). An external P-channel power MOSFET allows peak currents in excess of 3A, increasing the output current capability over previous PFM devices. Figure 2 is the block diagram.

The MAX649/MAX651/MAX652 offer three main improvements over prior solutions:

1) The converters operate with tiny (less than 9mm diameter) surface-mount inductors, due to their 300kHz switching frequency.
2) The current-limited PFM control scheme allows greater than 90% efficiencies over a wide range of load currents (1.0mA to 1.5A).
3) The maximum supply current is only 100µA.

PFM Control Scheme

The MAX649/MAX651/MAX652 use a proprietary, current-limited PFM control scheme. As with traditional PFM converters, the external power MOSFET is turned on when the voltage comparator senses that the output is out of regulation. However, unlike traditional PFM converters, switching is accomplished through the combination of a peak current limit and a pair of one-shots that set the maximum switch on-time (16µs) and minimum switch off-time (2.3µs). Once off, the minimum off-time one-shot holds the switch off for 2.3µs. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The MAX649/MAX651/MAX652 also limit the peak inductor current, which allows them to run in continuous-conduction mode and maintain high efficiency with heavy loads (Figure 3a). This current-limiting feature is a key component of the control circuitry. Once turned on, the switch stays on until either 1) the maximum on-time one-shot turns it off (16µs later), or 2) the current limit is reached.

To increase light-load efficiency, the current limit for the first two pulses is set to half the peak current limit. If those pulses bring the output voltage into regulation, the voltage comparator holds the MOSFET off and the current limit remains at half its peak. If the output voltage is still out of regulation after two pulses, the current limit for the next pulse is raised to its peak (Figure 3b). Calculate the peak current limit by dividing the Current-Limit Trip Level (see *Electrical Characteristics*) by the value of the current-sense resistor.

Shutdown Mode

When SHDN is high, the MAX649/MAX651/MAX652 enter shutdown mode. In this mode, the internal biasing circuitry is turned off (including the reference) and the supply current drops to less than 5µA. EXT goes high, turning off the external MOSFET. SHDN is a TTL/CMOS logic-level input. Connect SHDN to GND for normal operation.

Quiescent Current

In normal operation, the quiescent current is less than 100µA. However, this current is measured by forcing the external transistor switch off. In an actual application, even with no load, additional current is drawn to supply external feedback resistors (if used) and the diode and capacitor leakage currents. In the circuit of Figure 1, with V+ at 5V and V_{OUT} at 3.3V, the typical quiescent current is 90µA.

EXT Drive Voltage Range

EXT swings from V+ to GND and provides the drive output for an external P-channel power MOSFET.

Modes of Operation

When delivering high output currents, the MAX649/MAX651/MAX652 operate in continuous-conduction mode (CCM). In this mode, current always flows in the

5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

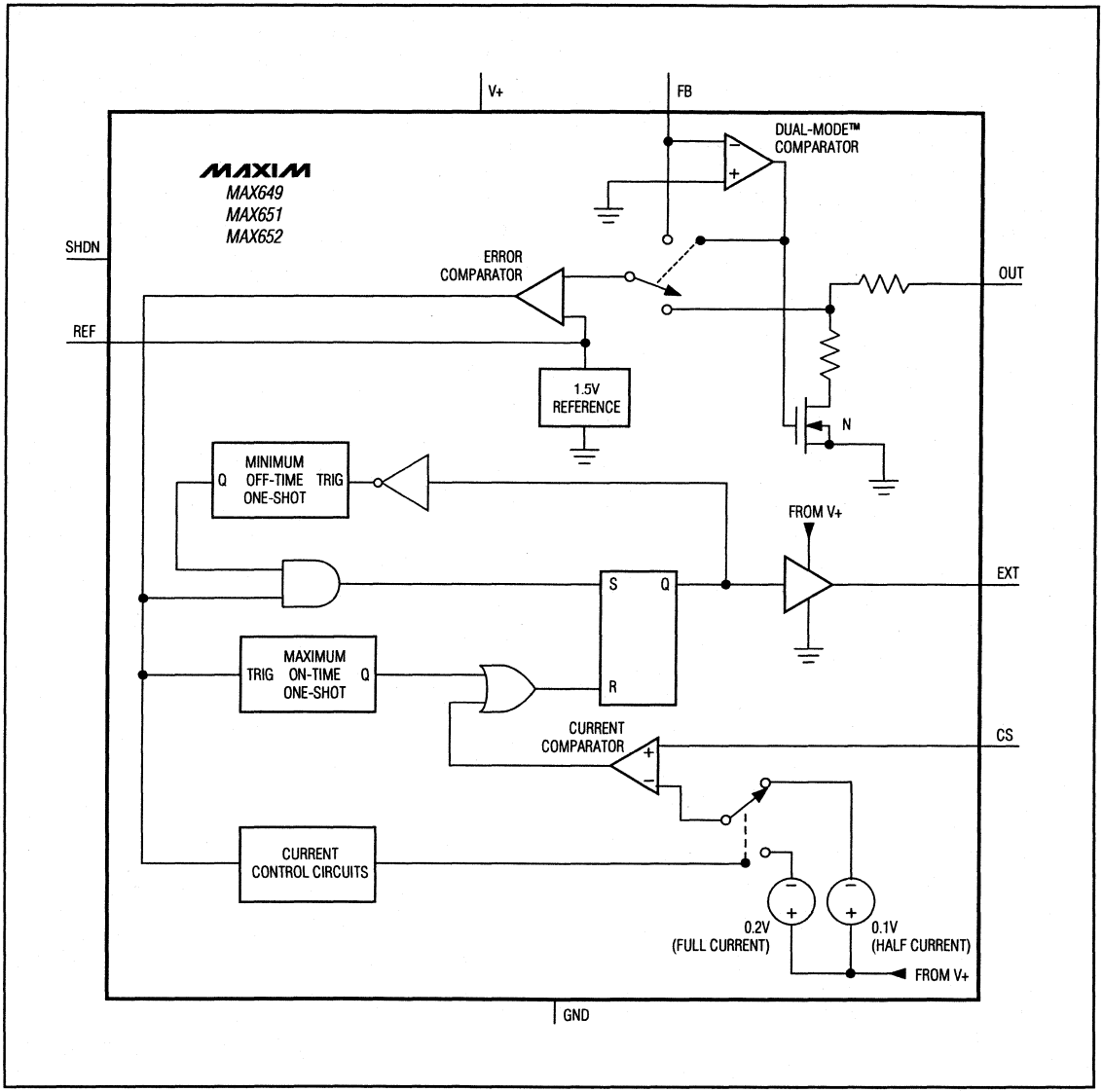


Figure 2. Block Diagram

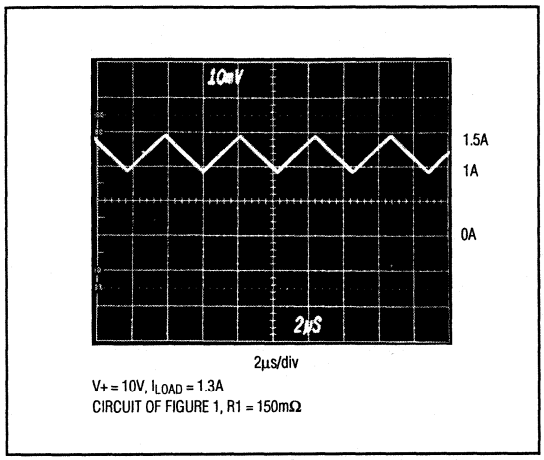


Figure 3a. MAX649 Continuous-Conduction Mode, Heavy Load-Current Waveform (500mA/div)

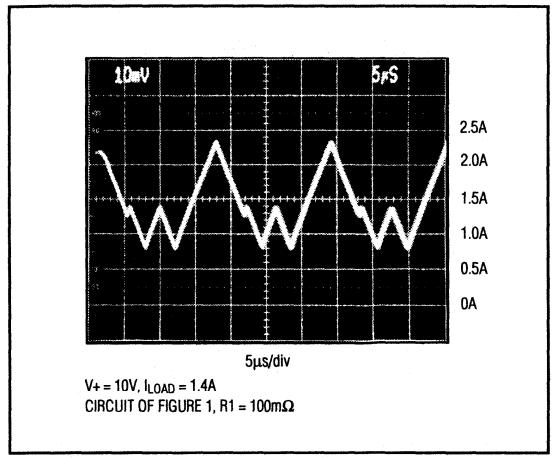


Figure 3b. MAX649 Light/Medium Load-Current Waveform (500mA/div)

inductor, and the control circuit adjusts the switch duty cycle to maintain regulation without exceeding the switch current capability (Figure 3a). This provides excellent load-transient response and high efficiency.

In discontinuous-conduction mode (DCM), current through the inductor starts at zero, rises to a peak value, then ramps down to zero. Although efficiency is still excellent, the output ripple increases slightly, and the switch waveforms exhibit ringing (the self-resonant frequency of the inductor). This ringing is to be expected and poses no operational problems.

Dropout

The MAX649/MAX651/MAX652 are said to be in dropout when the input voltage (V+) is low enough that the output drops below the minimum output voltage specification (see *Electrical Characteristics*). The dropout voltage is the difference between the input and output voltage when dropout occurs. See the *Typical Operating Characteristics* for the Dropout Voltage vs. Load Current and Dropout Voltage vs. Temperature graphs.

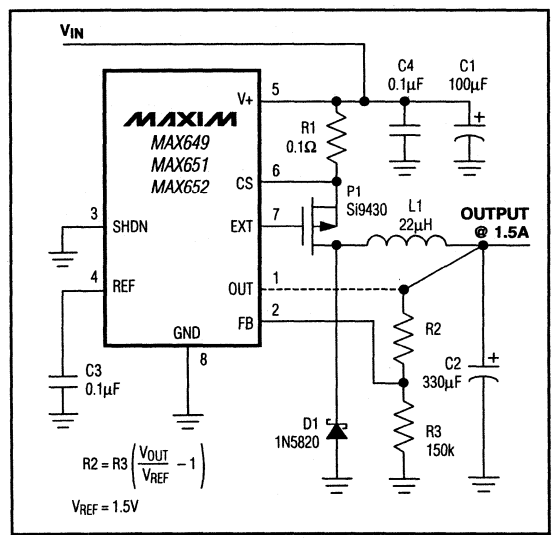


Figure 4. Adjustable-Output Operation

5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

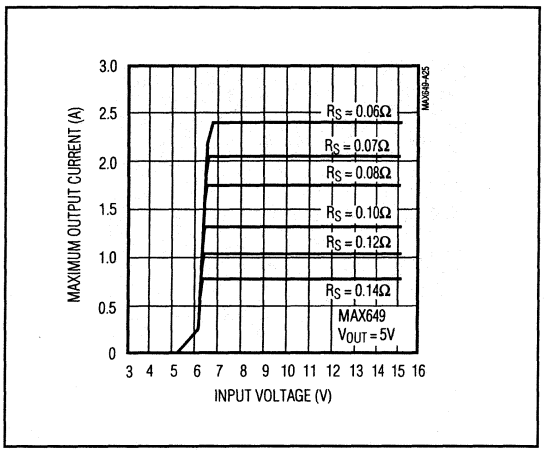


Figure 5a. MAX649 Current-Sense Resistor Graph

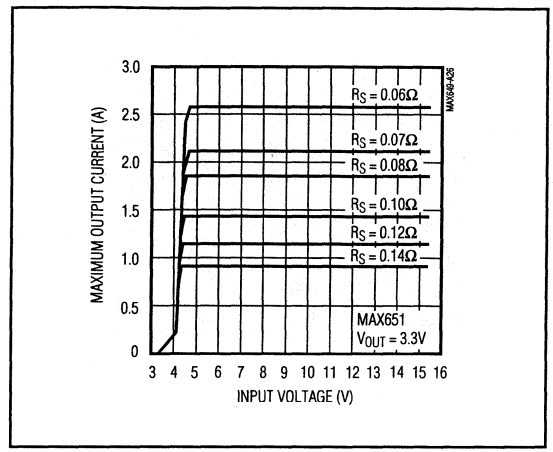


Figure 5b. MAX651 Current-Sense Resistor Graph

Design Procedure

Setting the Output Voltage

The MAX649/MAX651/MAX652 are preset for 5V, 3.3V, and 3V output voltages, respectively. Tie FB to GND for fixed-output operation. They may also be adjusted from 1.5V (the reference voltage) to the input voltage, using external resistors R2 and R3 configured as shown in Figure 4. For adjustable-output operation, 150kΩ is recommended for resistor R3. 150kΩ is a good value—high enough to avoid wasting energy, yet low enough to avoid RC delays caused by parasitic capacitance at FB. R2 is given by:

$$R2 = R3 \times \left[\frac{V_{OUT}}{V_{REF}} - 1\right]$$

where V_{REF} = 1.5V.

When using external resistors, it does no harm to connect OUT and the output together, or to leave OUT unconnected.

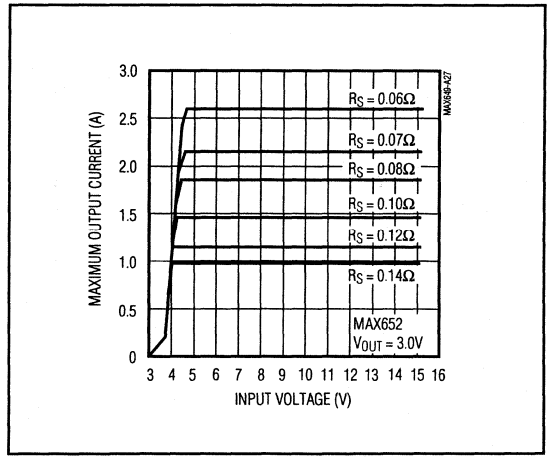


Figure 5c. MAX652 Current-Sense Resistor Graph

Current-Sense Resistor Selection

The current-sense resistor limits the peak switch current to 210mV/RSENSE, where RSENSE is the value of the current-sense resistor, and 210mV is the current-limit trip level (see *Electrical Characteristics*).

To maximize efficiency and reduce the size and cost of external components, minimize the peak current. However, since the available output current is a function of the peak current, the peak current must not be too low.

To choose the proper current-sense resistor for a particular output voltage, determine the minimum input voltage and the maximum load current. Next, referring to Figures 5a, 5b, or 5c, using the minimum input voltage, find the curve with the largest sense resistor that provides sufficient output current. It is not necessary to perform worst-case calculations. These curves take into account the worst-case values for sense resistor (±5%), inductor (22µH ±10%), diode drop (0.6V), and

the IC's current-sense trip level; an external MOSFET on-resistance of 0.13Ω is assumed for V_{GS} = -4.5V.

Standard wire-wound and metal-film resistors have an inductance high enough to degrade performance. Surface-mount (chip) resistors have very little inductance and are well suited for use as current-sense resistors. A wire resistor made by IRC works well in through-hole applications. Because this resistor is a band of metal shaped as a "U", its inductance is less than 10nH (an order of magnitude less than metal film resistors). Resistance values between 5mΩ and 0.1Ω are available (see Table 1).

Inductor Selection

Practical inductor values range from 10µH to 50µH or more. The circuit operates in discontinous-conduction mode if:

$$V+ \leq \frac{V_{OUT} \times (R + 1)}{R} + \frac{V_D}{R} + V_{SW}$$

R, the switch on-time/off-time ratio, equals 6.7. V_D is the diode's drop, and V_{SW} is the voltage drop across the P-channel FET. To get the full output capability in discontinuous-conduction mode, choose an inductor value no larger than:

$$L(max) = \frac{R_{SENSE} \times 12\mu s \times (V+ - V_{SW} - V_{OUT})}{V_{CS}}$$

where V_{CS} is the current-sense voltage.

In both the continuous and discontinuous modes, the lower limit of the inductor is more important. With a small inductor value, the current rises faster and overshoots the desired peak current limit because the current-limit comparator cannot respond fast enough. This reduces efficiency slightly and, more importantly, could cause the current rating of the external components to be exceeded. Calculate the minimum inductor value as follows:

$$L(min) = \frac{(V+(max) - V_{SW} - V_{OUT}) \times 0.3\mu s}{\Delta I \times I_{LIM}(min)}$$

where ΔI is the percentage of inductor-current overshoot, where $I_{LIM} = V_{CS}/R_{SENSE}$ and 0.3µs is the time it takes the comparator to switch. An overshoot of 10% is usually not a problem. Inductance values above the minimum work well if the maximum value defined above is not exceeded. Smaller inductance values cause higher output ripple because of overshoot. Larger values tend to produce physically larger coils.

For highest efficiency, use a coil with low DC resistance; a value smaller than $0.1V/I_{LIM}$ works best. To minimize radiated noise, use a toroid, pot core, or shielded-bobbin inductor. Inductors with a ferrite core or equivalent are recommended. Make sure the inductor's saturation-current rating is greater than I_{LIM}(max). However, it is generally acceptable to bias the inductor into saturation by about 20% (the point where the inductance is 20% below its nominal value).

The peak current of Figure 1 is 2.35A for a 1.5A output. The inductor used in this circuit is specified to drop by 10% at 2.2A (worst case); a curve provided by the manufacturer shows that the inductance typically drops by 20% at 3.1A. Using a slightly underrated inductor can sometimes reduce size and cost, with only a minor impact on efficiency. The MAX649/MAX651/MAX652 current limit prevents any damage from an underrated inductor's low inductance at high currents.

Table 1 lists inductor types and suppliers for various applications. The efficiencies of the listed surface-mount inductors are nearly equivalent to those of the larger size through-hole versions.

Diode Selection

The MAX649/MAX651/MAX652's high switching frequency demands a high-speed rectifier (commonly called a catch diode when used in switching-regulator circuits). Schottky diodes, such as the 1N5817 through 1N5822 families (and their surface-mount equivalents), are recommended. Choose a diode with an average current rating equal to or greater than I_{LIM}(max) and a voltage rating higher than V+(max). For high-temperature applications, where Schottky diodes can be inadequate because of high leakage currents, use high-speed silicon diodes instead. At heavy loads and high temperatures, the disadvantages of a Schottky diode's high leakage current may outweigh the benefits of its low forward voltage. Table 1 lists diode types and suppliers for various applications.

External Switching Transistor

The MAX649/MAX651/MAX652 drive P-channel enhancement-mode MOSFET transistors only. The choice of power transistor is primarily dictated by the input voltage and the peak current. The transistor's on-resistance, gate-source threshold, and gate capacitance must also be appropriately chosen. The drain-to-source and gate-to-source breakdown voltage ratings must be greater than V+. The total gate-charge specification is normally not critical, but values should be less than 100nC for best efficiency. The MOSFET should be capable of handling the peak current and, for maximum efficiency, have a very low on-resistance at that current. Also, the on-resistance must be low for the minimum available V_{GS}, which equals V+(min). Select a transistor with an on-resistance between 50%

5V/3.3V/3V or Adjustable, High-Efficiency, Low IQ, Step-Down DC-DC Controllers

and 100% of the current-sense resistor. The Si9430 transistor chosen for the *Typical Operating Circuit* has a drain-to-source rating of -20V and a typical on-resistance of 0.115Ω at 2A with V_{GS} = -4.5V. Tables 1 and 2 list suppliers of switching transistors suitable for use with these devices.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR), rather than high capacitance. An electrolytic capacitor with low enough ESR will automatically have high enough capacitance. The product of the inductor-current variation and the ESR of the output filter capacitor determines the amplitude of the high-frequency ripple seen on the output voltage. When a 330µF, 10V Sprague surface-mount capacitor (595D series) with ESR = 0.15Ω is used, 40mV of output ripple is typically observed when stepping down from 10V to 5V at 1A.

The output filter capacitor's ESR also affects efficiency. Use low-ESR capacitors for best performance. The smallest low-ESR SMT tantalum capacitors currently available are from the Sprague 595D series. Sanyo OS-CON organic semiconductor through-hole capacitors and the Nichicon PL series also exhibit very low ESR. Table 1 lists some suppliers of low-ESR capacitors.

Input Bypass Capacitor

The input bypass capacitor reduces peak currents drawn from the voltage source, and also reduces the amount of noise at the voltage source caused by the switching action of the MAX649/MAX651/MAX652. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is recommended. Bypass the IC separately with a 0.1µF ceramic capacitor placed close to the V+ and GND pins.

Reference Capacitor

Bypass REF with a 0.1µF or larger capacitor. REF can source at least 100µA.

Layout Considerations

Proper PC board layout is essential because of high current levels and fast switching waveforms that radiate noise. Minimize ground noise by connecting the anode of the catch diode, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point ("star" ground configuration). A ground plane is recommended. Also minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. In particular, the traces connected to FB (if an external resistor divider is used) and EXT must be short. Place the 0.1µF ceramic bypass capacitor as close as possible to V+ and GND.

Table 1. Component Selection Guide

PRODUCTION METHOD	INDUCTORS	CAPACITORS	DIODES	CURRENT-SENSE RESISTORS	MOSFETS
Surface Mount	Sumida CDR125-220 (22µH) Coiltronics CTX 100 series	Matsuo 267 series Sprague 595D series	Nihon NSQ series	IRC LRC series	Siliconix Little Foot series Motorola medium-power surface-mount products
Miniature Through-Hole	Sumida RCH855-220M	Sanyo OS-CON series low-ESR organic semiconductor		IRC OAR series	Motorola
Low-Cost Through-Hole	Renco RL 1284-22	Nichicon PL series low-ESR electrolytics United Chemi-Con LXF series	Motorola 1N5820, 1N5823		Motorola TMOS power MOSFETs

Table 2. Component Suppliers

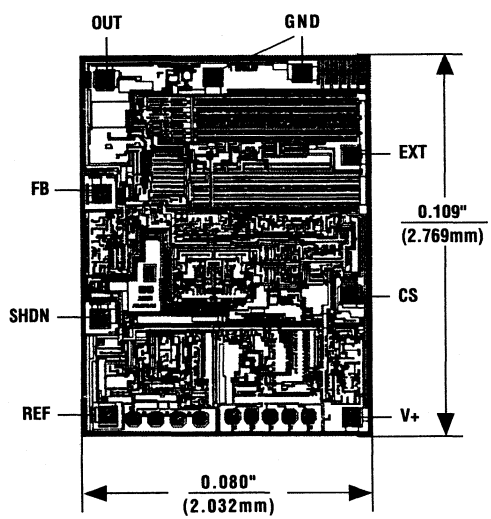
COMPANY		PHONE	FAX
Coiltronics	USA	(407) 241-7876	(407) 241-9339
Harris	USA	(800) 442-7747	(407) 724-3937
International Rectifier	USA	(310) 322-3331	(310) 322-3332
IRC	USA	(704) 264-8861	(704) 264-8866
Matsuo	USA Japan	(714) 969-2491 81-6-337-6450	(714) 960-6492 81-6-337-6456
Motorola	USA	(800) 521-6274	(602) 244-4015
Nichicon	USA Japan	(708) 843-7500 81-7-5231-8461	(708) 843-2798 81-7-5256-4158
Nihon	USA Japan	(805) 867-2555 81-3-3494-7411	(805) 867-2556 81-3-3494-7414
Renco	USA	(516) 586-5566	(516) 586-5562
Sanyo	USA Japan	(619) 661-6835 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Siliconix	USA	(408) 988-8000	(408) 970-3950
Sprague	USA	(603) 224-1961	(603) 224-1430
Sumida	USA Japan	(708) 956-0666 81-3-3607-5111	(708) 956-0702 81-3-3607-5144
United Chemi-Con	USA	(714) 255-9500	(714) 255-9400

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX651CPA	0°C to +70°C	8 Plastic DIP
MAX651CSA	0°C to +70°C	8 SO
MAX651C/D	0°C to +70°C	Dice*
MAX651EPA	-40°C to +85°C	8 Plastic DIP
MAX651ESA	-40°C to +85°C	8 SO
MAX651MJA	-55°C to +125°C	8 CERDIP**
MAX652CPA	0°C to +70°C	8 Plastic DIP
MAX652CSA	0°C to +70°C	8 SO
MAX652C/D	0°C to +70°C	Dice*
MAX652EPA	-40°C to +85°C	8 Plastic DIP
MAX652ESA	-40°C to +85°C	8 SO
MAX652MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 442;
SUBSTRATE CONNECTED TO V+.

19-3293; Rev. 1; 7/93

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

CMOS Monolithic Voltage Converter

General Description

The MAX660 monolithic, charge-pump voltage inverter converts a +1.5V to +5.5V input to a corresponding -1.5V to -5.5V output. Using only two low-cost capacitors, the charge pump's 100mA output replaces switching regulators, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of its load-current range combined with a typical operating current of only 120µA provides ideal performance for both battery-powered and board-level voltage conversion applications. The MAX660 can also double the output voltage of an input power supply or battery, providing +9.35V at 100mA from a +5V input.

A frequency control (FC) pin selects either 10kHz typ or 80kHz typ (40kHz min) operation to optimize capacitor size and quiescent current. The oscillator frequency can also be adjusted with an external capacitor or driven with an external clock. The MAX660 is a pin-compatible high-current upgrade of the ICL7660.

The MAX660 is available in both 8-pin DIP and small-outline packages in commercial, extended, and military temperature ranges.

Features

- **0.65V Typ Loss at 100mA Load**
- **6.5Ω Typ Output Impedance**
- **Pin-Compatible High-Current ICL7660 Upgrade**
- **Inverts or Doubles Input Supply Voltage**
- **Selectable Oscillator Frequency: 10kHz/80kHz**
- **88% Typ Conversion Efficiency at 100mA (I_L to GND)**
- **120µA Operating Current**

Ordering Information

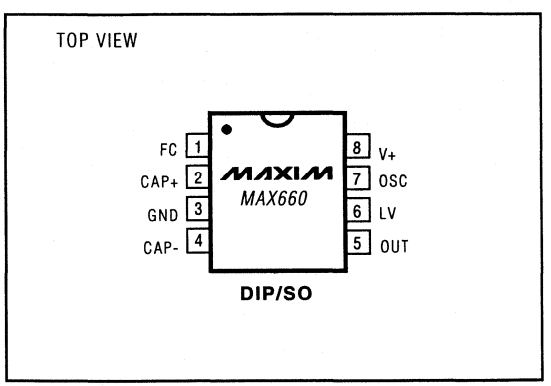
PART	TEMP. RANGE	PIN-PACKAGE
MAX660CPA	0°C to +70°C	8 Plastic DIP
MAX660CSA	0°C to +70°C	8 SO
MAX660C/D	0°C to +70°C	Dice*
MAX660EPA	-40°C to +85°C	8 Plastic DIP
MAX660ESA	-40°C to +85°C	8 SO
MAX660EJA	-40°C to +85°C	8 CERDIP
MAX660MJA	-55°C to +125°C	8 CERDIP

* *Contact factory for dice specifications.*

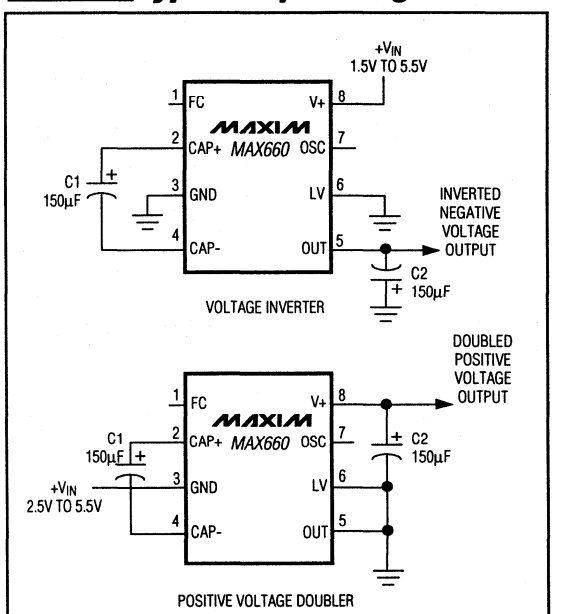
Applications

Laptop Computers
Medical Instruments
Interface Power Supplies
Hand-Held Instruments
Operational-Amplifier Power Supplies

Pin Configuration



Typical Operating Circuits



4

CMOS Monolithic Voltage Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to OUT) ..... +6V
LV Input Voltage ..... (OUT - 0.3V) to V+ + 0.3V
FC and OSC Input Voltages ..... The least negative of (OUT - 0.3V) or (V+ - 6V) to (V+ + 0.3V)
OUT and V+ Continuous Output Current 120mA
Output Short-Circuit Duration to GND (Note 1) 1sec
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above + 70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX660C_ _ ..... 0°C to +70°C
MAX660E_ _ ..... -40°C to +85°C
MAX660MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: OUT may be shorted to GND for 1sec without damage, but shorting OUT to V+ may damage the device and should be avoided. Also, for temperatures above +85°C, OUT must not be shorted to GND or V+, even instantaneously, or device damage may result.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, C1 = C2 = 150µF, test circuit of Figure 1, FC = open, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	R_L = 1kΩ	Inverter, LV = open	3.0		5.5	V
		Inverter, LV = GND	1.5		5.5	
		Doubler, LV = OUT	2.5		5.5	
Supply Current	No Load	FC = open, LV = open		0.12	0.5	mA
		FC = V+, LV = open		1	3	
Output Current	$T_A \le$ +85°C, OUT more negative than -4V		100			mA
	$T_A >$ +85°C, OUT more negative than -3.8V		100			
Output Resistance (Note 3)	I_L = 100mA	$T_A \le$ +85°C		6.5	10.0	Ω
		$T_A >$ +85°C			12	
Oscillator Frequency	FC = open		5	10		kHz
	FC = V+		40	80		
OSC Input Current	FC = open			±1		µA
	FC = V+			±8		
Power Efficiency	R_L = 1kΩ connected between V+ and OUT		96	98		%
	R_L = 500Ω connected between OUT and GND		92	96		
	I_L = 100mA to GND			88		
Voltage Conversion Efficiency	No load		99.00	99.96		%

Note 2: In the test circuit, capacitors C1 and C2 are 150µF, 0.2Ω maximum ESR, aluminum electrolytics (Maxim part # MAXC001). Capacitors with higher ESR may reduce output voltage and efficiency. See *Capacitor Selection* section.

Note 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. See *Capacitor Selection* section.

19-0253; Rev 1; 8/94

EVALUATION KIT AVAILABLE

MAXIM

+12V, 30mA Flash Memory Programming Supply

General Description

The MAX662A is a regulated +12V, 30mA-output, charge-pump DC-DC converter. It provides the necessary +12V ±5% output to program byte-wide flash memories, and requires no inductors to deliver a guaranteed 30mA output from inputs as low as 4.75V. It fits into less than 0.1in^2 of board space. The MAX662A is a pin-compatible upgrade to the MAX662, and is recommended for new designs. The MAX662A offers lower quiescent and shutdown currents, and guarantees the output current over all temperature ranges.

The MAX662A is the first charge-pump boost converter to provide a regulated +12V output. It requires only a few inexpensive capacitors, and the entire circuit is completely surface-mountable.

A logic-controlled shutdown pin that interfaces directly with microprocessors reduces the supply current to only 0.5µA. The MAX662A comes in 8-pin narrow SO and DIP packages.

For higher-current flash memory programming solutions, refer to the data sheets for the MAX734 (120mA output current, guaranteed) and MAX732 (200mA output current, guaranteed) PWM, switch-mode DC-DC converters. Or, refer to the MAX761 data sheet for a 150mA, PFM switch-mode DC-DC converter that operates from inputs as low as 2V.

Applications

+12V Flash Memory Programming Supplies
Compact +12V Op-Amp Supplies
Switching MOSFETs in Low-Voltage Systems
Dual-Output +12V and +20V Supplies

Features

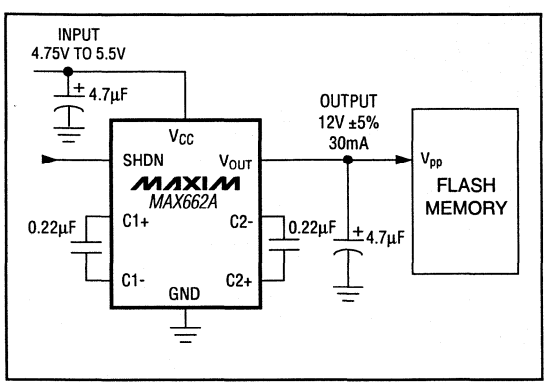
- **Regulated +12V ±5% Output Voltage**
- **4.5V to 5.5V Supply Voltage Range**
- **Fits in 0.1in^2**
- **Guaranteed 30mA Output**
- **No Inductor—Uses Only 4 Capacitors**
- **185µA Quiescent Current**
- **Logic-Controlled 0.5µA Shutdown**
- **8-Pin Narrow SO and DIP Packages**

Ordering Information

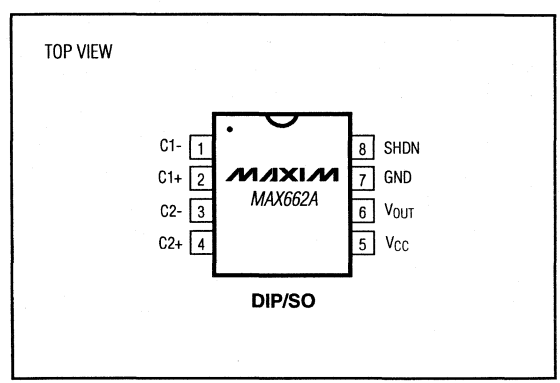
PART	TEMP. RANGE	PIN-PACKAGE
MAX662ACPA	0°C to +70°C	8 Plastic DIP
MAX662ACSA	0°C to +70°C	8 SO
MAX662AC/D	0°C to +70°C	Dice*
MAX662AEPA	-40°C to +85°C	8 Plastic DIP
MAX662AESA	-40°C to +85°C	8 SO
MAX662AMJA	-55°C to +125°C	8 CERDIP**

* *Dice are tested at T_A = +25°C.*
** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



+12V, 30mA Flash Memory Programming Supply

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to 6V
SHDN.....-0.3V to (V_{CC} + 0.3V)
I_{OUT} Continuous.....50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX662AC_A .....0°C to +70°C
MAX662AE_A .....-40°C to +85°C
MAX662AMJA.....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

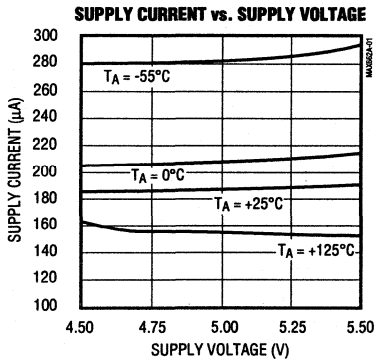
ELECTRICAL CHARACTERISTICS

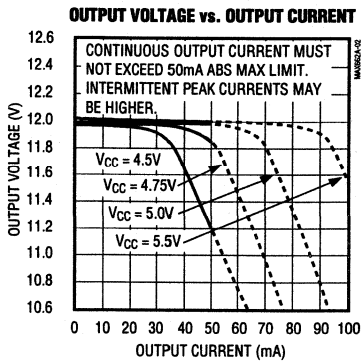
(Circuit of Figure 3a, V_{CC} = 4.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

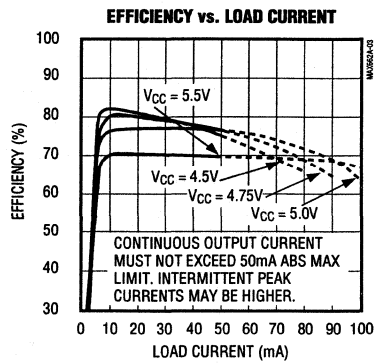
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	MAX662AC/E	0mA ≤ I_{OUT} ≤ 30mA, V_{CC} = 4.75V to 5.5V	11.4	12	12.6	V
			0mA ≤ I_{OUT} ≤ 20mA	11.4	12	12.6	
		MAX662AM	0mA ≤ I_{OUT} ≤ 24mA, V_{CC} = 4.75V to 5.5V	11.4	12	12.6	
			0mA ≤ I_{OUT} ≤ 16mA	11.4	12	12.6	
Supply Current	I_{CC}	No load, V_{SHDN} = 0V			185	500	µA
Shutdown Current		No load, V_{SHDN} = V_{CC}			0.5	10	µA
Oscillator Frequency	f_{OSC}	V_{CC} = 5V, I_{OUT} = 30mA			500		kHz
Power Efficiency		V_{CC} = 5V, I_{OUT} = 30mA			76		%
V_{CC}-to-V_{OUT} Switch Impedance	R_{SW}	V_{CC} = V_{SHDN} = 5V, I_{OUT} = 30mA	MAX662AC/E		1	2	kΩ
			MAX662AM		1	2.5	
Shutdown Input Threshold	V_{IH}			2.4			V
	V_{IL}					0.4	
SHDN Pin Current		V_{CC} = 5V, V_{SHDN} = 0V		-50	-15	-5	µA
		V_{CC} = V_{SHDN} = 5V			0		

Typical Operating Characteristics

(Circuit of Figure 3a, T_A = +25°C, unless otherwise noted.)





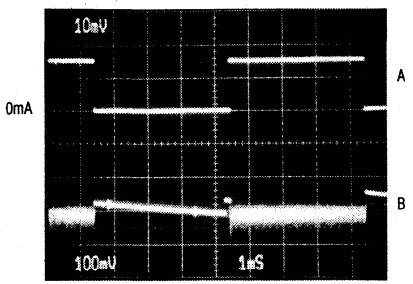


+12V, 30mA Flash Memory Programming Supply

Typical Operating Characteristics (continued)

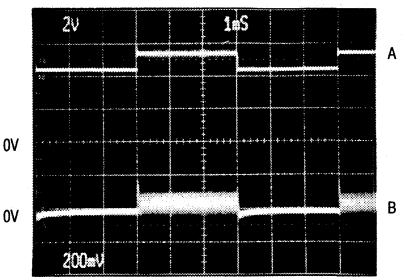
(Circuit of Figure 3a, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



A: OUTPUT CURRENT, 20mA/div, I_{OUT} = 0mA to 30mA
B: OUTPUT VOLTAGE RIPPLE, 100mV/div, V_{CC} = 5.0V

LINE-TRANSIENT RESPONSE



A: SUPPLY VOLTAGE, 2V/div, V_{CC} = 4.5V to 5.5V, I_{OUT} = 30mA
B: OUTPUT VOLTAGE RIPPLE, 200mV/div

Pin Description

PIN	NAME	FUNCTION
1	C1-	Negative terminal for the first charge-pump capacitor
2	C1+	Positive terminal for the first charge-pump capacitor
3	C2-	Negative terminal for the second charge-pump capacitor
4	C2+	Positive terminal for the second charge-pump capacitor
5	V_{CC}	Supply Voltage
6	V_{OUT}	+12V Output Voltage. V_{OUT} = V_{CC} when in shutdown mode.
7	GND	Ground
8	SHDN	Active-high CMOS-logic level Shutdown Input. SHDN is internally pulled up to V_{CC}. Connect to GND for normal operation. In shutdown mode, the charge pumps are turned off and V_{OUT} = V_{CC}.

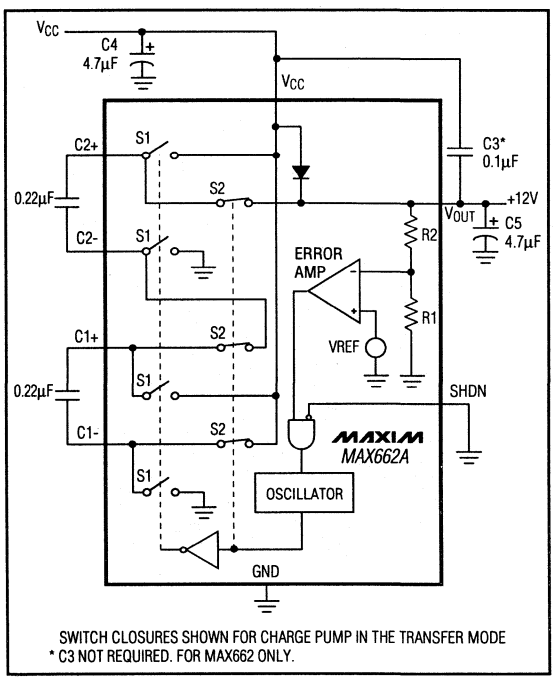


Figure 1. Block Diagram

+12V, 30mA Flash Memory Programming Supply

Detailed Description

Operating Principle

The MAX662A provides a regulated 12V output voltage at 30mA from a 5V ±5% power supply, making it ideal for flash EEPROM programming applications. It uses internal charge pumps and external capacitors to generate +12V, eliminating inductors. Regulation is provided by a pulse-skipping scheme that monitors the output voltage level and turns on the charge pumps when the output voltage begins to droop.

Figure 1 shows a simplified block diagram of the MAX662A. When the S1 switches are closed and the S2 switches are open, capacitors C1 and C2 are charged up to V_{CC}. The S1 switches are then opened and the S2 switches are closed so that capacitors C1 and C2 are connected in series between V_{CC} and V_{OUT}. This performs a voltage tripling function. A pulse-skipping feedback scheme adjusts the output voltage to 12V ±5%. The efficiency of the MAX662A with V_{CC} = 5V and I_{OUT} = 30mA is typically 76%. See the Efficiency vs. Load Current graph in the *Typical Operating Characteristics*.

During one oscillator cycle, energy is transferred from the charge-pump capacitors to the output filter capacitor and the load. The number of cycles within a given time frame increases as the load current increases or as the input supply voltage decreases. In the limiting case, the charge pumps operate continuously, and the oscillator frequency is nominally 500kHz.

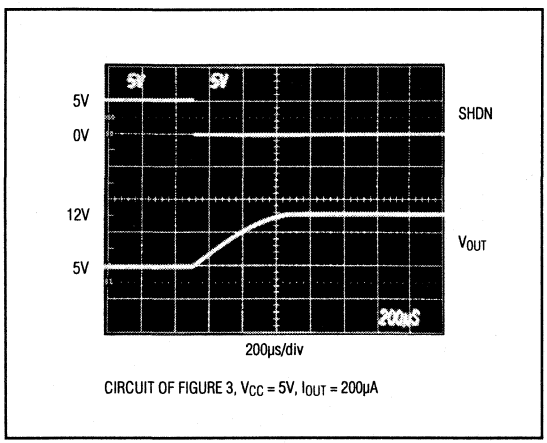


Figure 2. MAX662A Exiting Shutdown

Shutdown Mode

The MAX662A enters shutdown mode when SHDN is a logic high. SHDN is a TTL/CMOS-compatible input signal that is internally pulled up to V_{CC}. In shutdown mode, the charge-pump switching action is halted and V_{IN} is connected to V_{OUT} through a 1kΩ switch. When entering shutdown, V_{OUT} declines to V_{CC} in typically 13ms. Connect SHDN to ground for normal operation. When V_{CC} = 5V, it takes typically 400µs for the output to reach 12V after SHDN goes low (Figure 2).

Applications Information

Compatibility with MAX662

The MAX662A is a 100%-compatible upgrade of the MAX662. The MAX662A does not require capacitor C3, although its presence does not affect performance.

Capacitor Selection

Charge-Pump Capacitors, C1 and C2

The capacitance values of the charge-pump capacitors C1 and C2 are critical. Use ceramic or tantalum capacitors in the 0.22µF to 1.0µF range. For applications requiring operation over extended and/or military temperature ranges, use 1.0µF tantalum capacitors for C1 and C2 (Figure 3b).

Input and Output Capacitors, C4 and C5

The type of input bypass capacitor (C4) and output filter capacitor (C5) affects performance. Tantalums, ceramics or aluminum electrolytics are suggested. For smallest size, use Sprague 595D475X9016A7 surface-mount capacitors, which are 3.51mm x 1.81mm. For lowest ripple, use low-ESR through-hole ceramic or tantalum capacitors. For lowest cost, use aluminum electrolytic or tantalum capacitors.

Figure 3a shows the component values for proper operation over the commercial temperature range using minimum board space. The input bypass capacitor (C4) and output filter capacitor (C5) should both be at least 4.7µF when using Sprague's miniature 595D series of tantalum chip capacitors. Figure 3b shows the suggested component values for applications over extended and/or military temperature ranges.

The values of C4 and C5 can be reduced to 2µF and 1µF, respectively, when using ceramic capacitors. If using aluminum electrolytics, choose capacitance values of 10µF or larger for C4 and C5. Note that as V_{CC} increases above 5V and the output current decreases, the amount of ripple at V_{OUT} increases due to the slower oscillator frequency combined with the higher input voltage. Increase the input and output bypass capacitance to reduce output ripple.

Table 1 lists various capacitor suppliers.

+12V, 30mA Flash Memory Programming Supply

Table 1. Capacitor Suppliers

Supplier	Phone Number	Fax Number	Capacitor	Capacitor Type*
Murata Erie	(814) 237-1431	(814) 238-0490	GRM42-6Z5U224M50	0.22µF Ceramic (SM)
			RPE123Z5U105M50V	1.0µF Ceramic (TH)
Sprague Electric	(603) 224-1961 (207) 324-4140	(603) 224-1430 (207) 324-7223	595D475X9016A7	4.7µF Tantalum (SM)
			595D105X9016A7	1.0µF Tantalum (SM)

**Note: (SM) denotes surface-mount component, (TH) denotes through-hole component.*

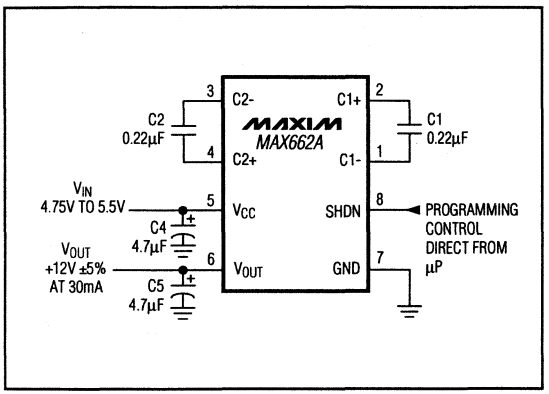


Figure 3a. Flash EEPROM Programming Power Supply for Commercial Temperature Range Applications

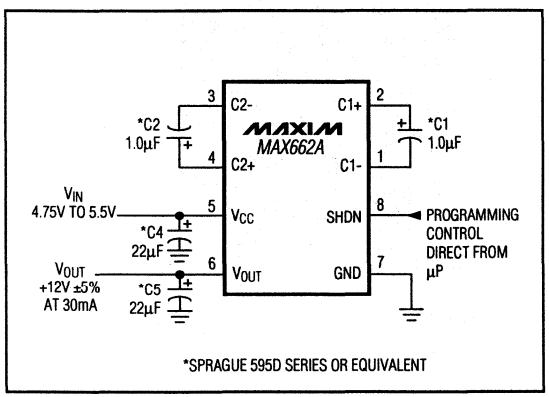


Figure 3b. Flash EEPROM Programming Power Supply for Extended and/or Military Temperature Range Applications

Layout Considerations

Layout is critical, due to the MAX662A's high oscillator frequency. Good layout ensures stability and helps maintain the output voltage under heavy loads. For best performance, use very short connections to the capacitors. The order of importance is: C4, C5, C1, C2.

Flash EEPROM Applications

The circuit of Figure 3a is a +12V ±5% 30mA flash EEPROM programming power supply. A microprocessor controls the programming voltage via the SHDN pin. When SHDN is low, the output voltage (which is connected to the flash memory V_{PP} supply-voltage pin) rises to +12V to facilitate programming the flash memory. When SHDN is high, the output voltage is connected to V_{IN} through an internal 1kΩ resistor.

Paralleling Devices

Two MAX662As can be placed in parallel to increase output drive capability. The V_{CC}, V_{OUT}, and GND pins can be paralleled, reducing pin count. Use a single bypass capacitor and a single output filter capacitor with twice the capacitance value if the two devices can be placed close to each other. If the MAX662As cannot be placed close together, use separate bypass and output capacitors. The amount of output ripple observed will determine whether single input bypass and output filter capacitors can be used. Under certain conditions, one device may supply the total output current. Therefore, regardless of the number of devices in parallel, the maximum continuous current must not exceed 50mA.

12V and 20V Dual-Output Power Supply

Using the charge-pump voltage-doubler circuit of Figure 4, the MAX662A can produce a +20V supply from a single +5V supply. Figure 5 shows the current capability of the +20V supply.

+12V, 30mA Flash Memory Programming Supply

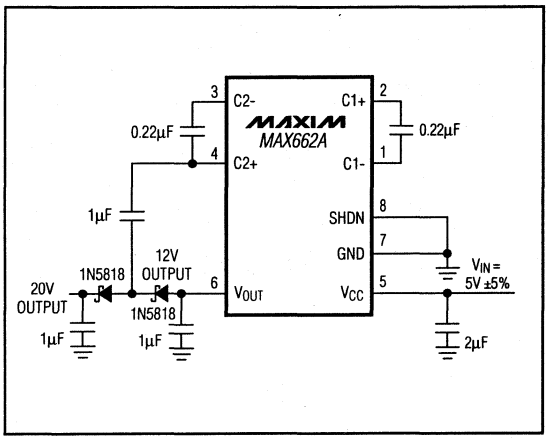


Figure 4. +12V and +20V Dual Supply from a +5V Input

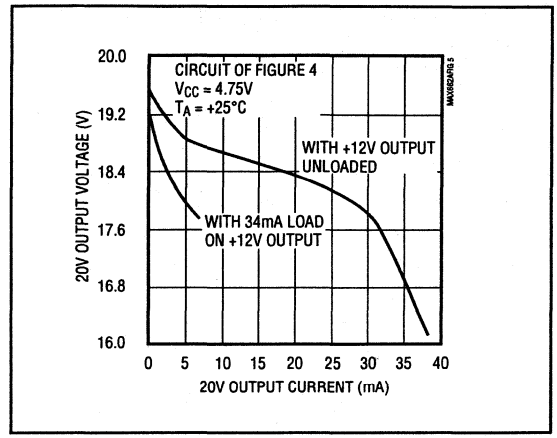
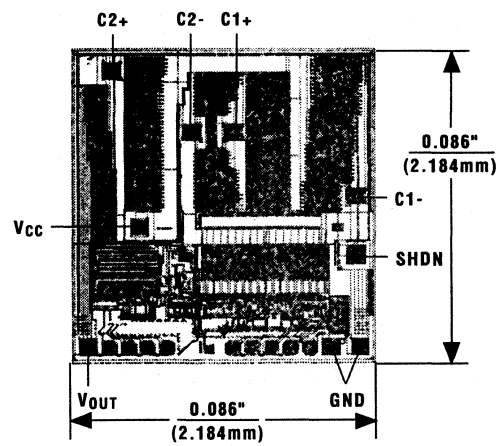


Figure 5. +20V Supply Output Current Capability

Chip Topography



TRANSISTOR COUNT: 225

SUBSTRATE CONNECTED TO VOUT

19-3894; Rev 3; 10/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

+5V/Programmable Low-Dropout Voltage Regulator

General Description

The MAX667 low-dropout, positive, linear voltage regulator supplies up to 250mA of output current. With no load, it has a typical quiescent current of 20µA. At 200mA of output current, the input/output voltage differential is typically 150mV. Other features include a low-voltage detector to indicate power failure, as well as early-warning and low-dropout detectors to indicate an imminent loss of output voltage regulation. A shutdown control disables the output and puts the circuit into a low quiescent-current mode.

The MAX667 employs Dual Mode™ operation. One mode uses internally trimmed feedback resistors to produce +5V. In the other mode, the output may be varied from +1.3V to +16V by connecting two external resistors.

The MAX667 is a pin-compatible upgrade to the MAX666 in most applications where the input voltages are above +3.5V. Choose the MAX667 when high output currents and/or low dropout voltages are desired, as well as for improved performance at higher temperatures.

Applications

Battery-Powered Devices

Pagers and Radio Control Receivers

Portable Instruments

Solar-Powered Instruments

Features

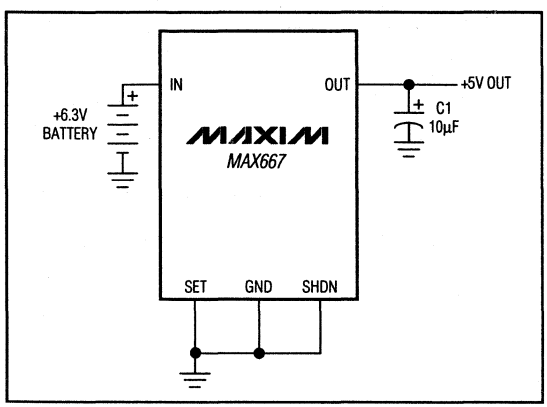
- ♦ **350mV Max Dropout at 200mA**
- ♦ **250mA Output Current**
- ♦ **Normal Mode: 20µA Typ Quiescent Current**
  Shutdown Mode: 0.2µA Typ Quiescent Current
- ♦ **Low-Battery Detector**
- ♦ **Fixed +5V (Min Component Count) or Adjustable Output**
- ♦ **+3.5V to +16.5V Input**
- ♦ **Dropout Detector Output**
- ♦ **10µF Output Capacitor**

Ordering Information

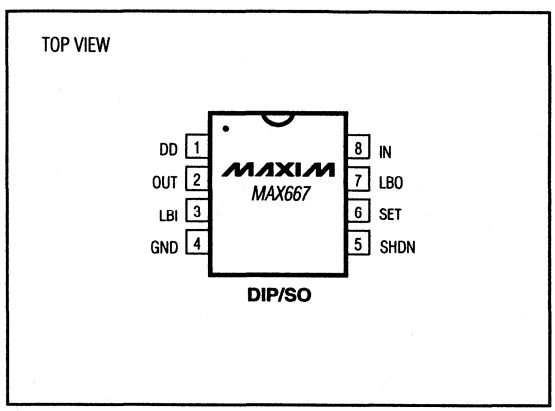
PART	TEMP. RANGE	PIN-PACKAGE
MAX667CPA	0°C to +70°C	8 Plastic DIP
MAX667CSA	0°C to +70°C	8 SO
MAX667C/D	0°C to +70°C	Dice*
MAX667EPA	-40°C to +85°C	8 Plastic DIP
MAX667ESA	-40°C to +85°C	8 SO
MAX667MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



™ Dual Mode is a trademark of Maxim Integrated Products.

+5V/Programmable Low-Dropout Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage .....+18V
Output Short Circuited to Ground.....1sec
LBO Output Sink Current 50mA
LBO Output Voltage .....GND to V_{OUT}
SHDN Input Voltage .....-0.3V to (V_{IN} + 0.3V)
Input Voltages LBI, SET.....-0.3V to (V_{IN} - 1.0V)
Continuous Power Dissipation
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Ranges
MAX667C_A.....0°C to +70°C
MAX667E_A.....-40°C to +85°C
MAX667MJA.....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($GND = 0V$, $V_{IN} = +9V$, $V_{OUT} = +5V$, $C1 = 10\mu F$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		$T_A = +25°C$ MIN	TYP	MAX	$T_A = T_{MIN}$ to T_{MAX} MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}						3.5		16.5	V
Output Voltage	V_{OUT}	$V_{SET} = 0V$, $V_{IN} = 6V$, $I_{OUT} = 10mA$, $T_A = -40°C$ to $+85°C$			5		4.8		5.2	V
		$V_{SET} = 0V$, $V_{IN} = 6V$, $I_{OUT} = 10mA$, $T_A = -55°C$ to $+125°C$			5		4.75		5.25	
Maximum Output Current	I_{OUT}	$V_{IN} = 6V$, $4.5V < V_{OUT} < 5.5V$		250			250			mA
Quiescent Current	I_Q	$V_{SHDN} = 2V$			0.2	1			2	µA
		$V_{SHDN} = 0V$, $V_{SET} = 0V$	$I_{OUT} = 0\mu A$		20	25			35	µA
			$I_{OUT} = 100\mu A$		20	30			50	µA
			$I_{OUT} = 200mA$		5	15			20	mA
Dropout Voltage (Note1)		$I_{OUT} = 100\mu A$			5	60			75	mV
		$I_{OUT} = 200mA$			150	250			350	mV
Load Regulation		$I_{OUT} = 10mA$ to $200mA$			50	100			250	mV
Line Regulation		$V_{IN} = 6V$ to $10V$, $I_{OUT} = 10mA$			5	10			15	mV
SET Reference Voltage	V_{SET}				1.225		1.20		1.25	V
SET Input Leakage Current	I_{SET}	$V_{SET} = 1.5V$			0.01	±10			±1000	nA
Output Leakage Current	I_{OUT}	$V_{SHDN} = 2V$			0.1				1	µA
Short-Circuit Current	I_{OUT}	(Note 2)				400			450	mA
Low-Battery Detector Reference Voltage	V_{LBI}				1.225		1.195		1.255	V
Low-Battery Detector Input Leakage Current	I_{LBI}	$V_{LBI} = 1.5V$			0.01	±10			±1000	nA
Low-Battery Detector Output Voltage	V_{LBO}	$V_{IN} = 9V$, $V_{LBI} = 2V$, $I_{LBO} = 10mA$				0.25			0.4	V
SHDN Threshold	V_{SHDN}	V_{IH}		1.5			1.5			V
		V_{IL}				0.3			0.3	V
SHDN Leakage Current	I_{SHDN}	$V_{SHDN} = 0V$ to V_{IN}			0.01	±10			±1000	nA
Dropout Detector Output Voltage	V_{DD}	$V_{SET} = 0V$, $V_{SHDN} = 0V$, $R_{DD} = 100k\Omega$, $I_{OUT} = 10mA$	$V_{IN} = 7V$						0.25	V
			$V_{IN} = 4.5V$				3.5			V

Note 1: Dropout Voltage is V_{IN}-V_{OUT} when V_{OUT} falls to 0.1V below its value at $V_{IN} = V_{OUT} + 2V$.
Note 2: Short-Circuit Current is pulse tested to maintain junction temperature. Short-circuit duration is limited by package dissipation.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

High-Accuracy Low-Dropout Linear Regulators

General Description

The MAX687/MAX688/MAX689 low-dropout linear regulators operate with an input-to-output voltage differential limited only by an external PNP transistor. Outputs are fixed at 3.3V (MAX687/MAX688) or 3.0V (MAX689). Base drive to the external transistor is at least 10mA, permitting output currents to exceed 1A when high-gain (ß > 100) transistors are used. Output current limiting is implemented by limiting the base current of the external transistor. Output voltage monitoring and shutdown functions are included.

The 3.3V MAX687 automatically shuts down whenever the output voltage drops below 2.96V. An internal power-fail comparator also monitors the output and provides an early warning of low output voltage before the device shuts down. When shut down, the output is latched off until the ON input is pulsed. Turning off the power supply in this way prevents battery damage due to excessive discharge or cell reversal, and can provide a mechanism for "self-backup" of volatile memory. Typical applications for these devices include portable telephones and other battery-powered equipment where the power supply must be disabled when the battery voltage is low.

The MAX688/MAX689 do not have an automatic shutdown feature, and are identical except for their output voltages. Each device has an active-low shutdown-control input, used to turn its output on or off at any time. As $\overline{SHDN}$ falls, the device enters a standby mode before fully shutting down. When in standby, the reference and comparators are fully operational, permitting the transition from normal mode to standby mode to occur at a precise voltage level on $\overline{SHDN}$.

Applications

High-Efficiency Linear Regulator

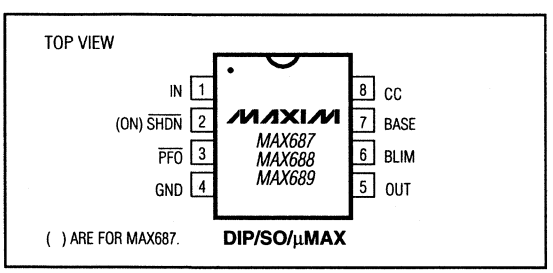
Battery-Powered Devices

Portable Instruments

Portable Telephones

Power Supply or Backup Supply for Memory

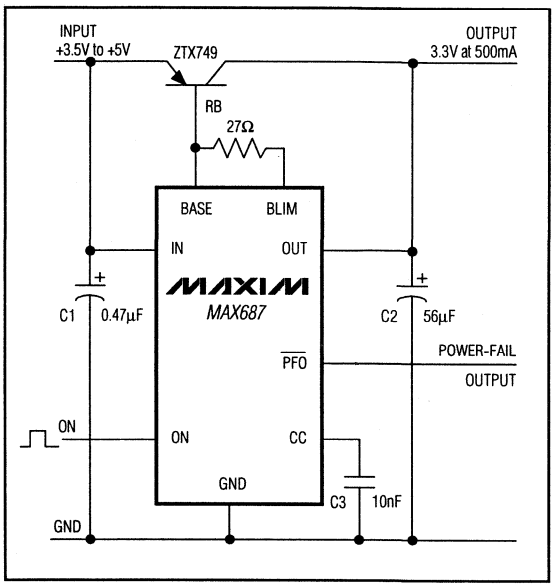
Pin Configuration



Features

- **Fixed Outputs:**
  3.3V (MAX687/MAX688)
  3.0V (MAX689)
- **Directly Drives External PNP Transistor**
- **10mA Min Base-Current Drive for >1A Output**
- **Low Dropout Voltage:**
  <200mV Dropout at 500mA Output (ZTX749)
  <200mV Dropout at 200mA Output (2N2907A)
  <100mV Dropout at 150mA Output (ZTX749)
- **±2% Accurate Power-Fail Monitor**
- **Automatic, Latched Shutdown when Output Falls Out of Regulation (MAX687)**
- **Precision Threshold Shutdown Control (MAX688/MAX689)**
- **Low Supply Current:**
  < 250µA Operating
  <1µA Shutdown
- **2.7V to 11.0V Supply Range**
- **8-Pin DIP/SO/µMAX Packages**

Typical Operating Circuit



19-0165; Rev 1; 8/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

5V, Step-Down, Current-Mode PWM DC-DC Converters

General Description

The MAX730A/MAX738A/MAX744A are 5V-output CMOS, step-down switching regulators. The MAX738A/MAX744A accept inputs from 6V to 16V and deliver 750mA. The MAX744A guarantees 500mA load capability for inputs above 6V and has tighter oscillator frequency limits for low-noise (radio) applications. The MAX730A accepts inputs between 5.2V and 11V and delivers 450mA for inputs above 6V. Typical efficiencies are 85% to 96%. Quiescent supply current is 1.7mA and only 6µA in shutdown.

Pulse-width modulation (PWM) current-mode control provides precise output regulation and excellent transient responses. Output voltage accuracy is guaranteed to be ±5% over line, load, and temperature variations. Fixed-frequency switching allows easy filtering of output ripple and noise, as well as the use of small external components. These regulators require only a single inductor value to work in most applications, so no inductor design is necessary.

The MAX730A/MAX738A/MAX744A also feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection.

Applications

Portable Instruments
Cellular Phones and Radios
Personal Communicators
Distributed Power Systems
Computer Peripherals

Features

- **750mA Load Currents (MAX738A/MAX744A)**
- **High-Frequency, Current-Mode PWM**
- **159kHz to 212.5kHz Guaranteed Oscillator Frequency Limits (MAX744A)**
- **85% to 96% Efficiencies**
- **1.7mA Quiescent Current**
- **6µA Shutdown Supply Current**
- **Single Preselected Inductor Value, No Component Design Required**
- **Overcurrent, Soft-Start, and Undervoltage Lockout Protection**
- **Cycle-by-Cycle Current Limiting**
- **8-Pin DIP/SO Packages (MAX730A)**

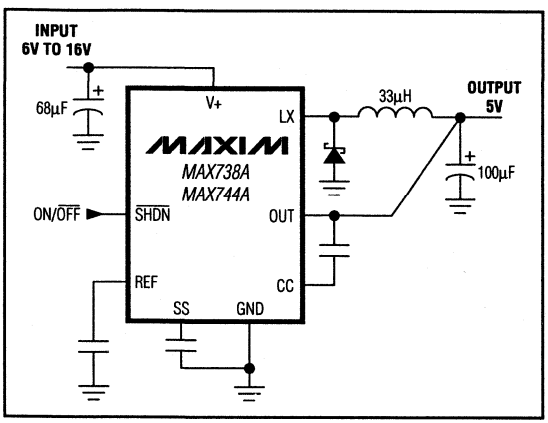
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX730ACPA	0°C to +70°C	8 Plastic DIP
MAX730ACSA	0°C to +70°C	8 SO
MAX730AC/D	0°C to +70°C	Dice*
MAX730AEPA	-40°C to +85°C	8 Plastic DIP
MAX730AESA	-40°C to +85°C	8 SO
MAX730AMJA	-55°C to +125°C	8 CERDIP

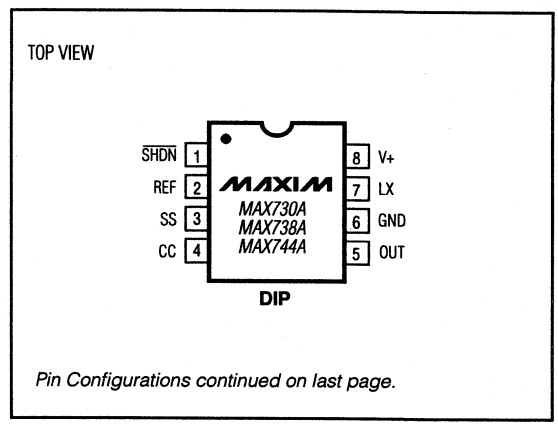
Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configurations



Pin Configurations continued on last page.

5V, Step-Down, Current-Mode PWM DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V+ (MAX730A) ..... +12V, -0.3V
- V+ (MAX738A/MAX744A) ..... +18V, -0.3V
- LX (MAX730A) ..... (V+ - 12V) to (V+ + 0.3V)
- LX (MAX738A/MAX744A) ..... (V+ - 21V) to (V+ + 0.3V)
- OUT ..... ±25V
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)

Peak Switch Current (I_{LX}) 2A
Reference Current (I_{REF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
- 8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX7_ _AC_ _ ..... 0°C to +70°C
- MAX7_ _AE_ _ ..... -40°C to +85°C
- MAX7_ _AMJA ..... -55°C to +125°C

Junction Temperatures:
- MAX7_ _AC_ _/AE_ _ ..... +150°C
- MAX7_ _AMJA ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 3, V+ = 9V for the MAX730A, V+ = 12V for the MAX738A/MAX744A, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MAX730A MIN	MAX730A TYP	MAX730A MAX	MAX738A MIN	MAX738A TYP	MAX738A MAX	MAX744A MIN	MAX744A TYP	MAX744A MAX	UNITS
Output Voltage	V+ = 6.0V to 11.0V	0mA < I_{LOAD} < 450mA, MAX730AC	4.75	5.00	5.25							V
		0mA < I_{LOAD} < 450mA, MAX730AE										
		0mA < I_{LOAD} < 300mA, MAX730AM										
	V+ = 6.0V to 16.0V	0mA < I_{LOAD} < 450mA, MAX738AC/AE				4.75	5.00	5.25	4.75	5.00	5.25	
		0mA < I_{LOAD} < 350mA, MAX738AM										
		0mA < I_{LOAD} < 500mA, MAX744AC/AE										
		0mA < I_{LOAD} < 375mA, MAX744AM										
	V+ = 10.2V to 16.0V, 0mA < I_{LOAD} < 750mA					4.75	5.00	5.25				
	V+ = 9.0V to 16.0V	0mA < I_{LOAD} < 750mA, MAX744AC/AE							4.75	5.00	5.25	
		0mA < I_{LOAD} < 600mA, MAX744AM										
Input Voltage Range			5.2		11.0	6.0		16.0	6.0		16.0	V
Line Regulation	V+ = 5.2V to 11.0V			0.15								%/V
	V+ = 6.0V to 16.0V						0.15			0.15		

19-0190; Rev 0; 9/93

MAXIM

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

General Description

The MAX748A/MAX763A are 3.3V-output CMOS, step-down switching regulators. The MAX748A accepts inputs from 3.3V to 16V and delivers up to 500mA. The MAX763A accepts inputs between 3.3V and 11V and delivers up to 500mA. Typical efficiencies are 85% to 90%. Quiescent supply current is 1.4mA (MAX763A), and only 0.2µA in shutdown.

Pulse-width-modulation (PWM) current-mode control provides precise output regulation and excellent transient responses. Output voltage accuracy is guaranteed to be ±5% over line, load, and temperature variations. Fixed-frequency switching allows easy filtering of output ripple and noise, as well as the use of small external components. A 22µH inductor works in most applications, so no magnetics design is necessary.

The MAX748A/MAX763A also feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection. The MAX748A is available in 8-pin DIP and 16-pin wide SO packages; the MAX763A comes in 8-pin DIP and SO packages.

Applications

5V-to-3.3V Converters
Cellular Phones
Portable Instruments
Hand-Held Computers
Computer Peripherals

Features

- **Up to 500mA Load Currents**
- **Guaranteed 159kHz to 219.5kHz Current-Mode PWM**
- **85% to 90% Efficiencies**
- **1.7mA Quiescent Current (MAX748A)**
  1.4mA Quiescent Current (MAX763A)
- **0.2µA Shutdown Supply Current**
- **22µH Preselected Inductor Value;**
  No Component Design Required
- **Overcurrent, Soft-Start, and Undervoltage Lockout Protection**
- **Cycle-by-Cycle Current Limiting**
- **8-Pin DIP/SO Packages (MAX763A)**

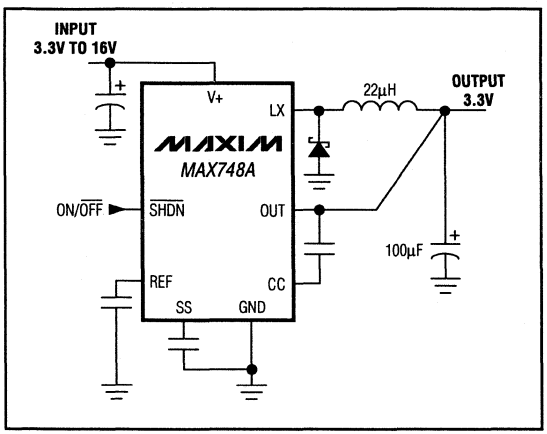
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX748ACPA	0°C to +70°C	8 Plastic DIP
MAX748ACWE	0°C to +70°C	16 Wide SO
MAX748AC/D	0°C to +70°C	Dice*
MAX748AEPA	-40°C to +85°C	8 Plastic DIP
MAX748AEWE	-40°C to +85°C	16 Wide SO
MAX748AMJA	-55°C to +125°C	8 CERDIP

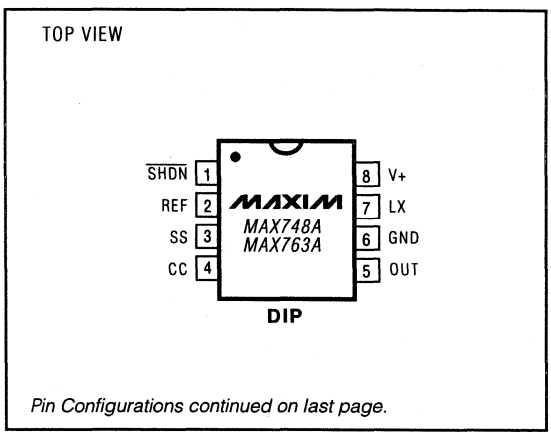
Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configurations



Pin Configurations continued on last page.

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Pin Voltages:
- V+ (MAX748A) ..... +17V, -0.3V
- V+ (MAX763A) ..... +12V, -0.3V
- LX (MAX748A) ..... (V+ - 21V) to (V+ + 0.3V)
- LX (MAX763A) ..... (V+ - 12V) to (V+ + 0.3V)
- OUT ..... ±25V
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)

Peak Switch Current (I_{LX}) 2.0A
Reference Current (I_{REF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 6.90mW/°C above +70°C) ... 552mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
- 8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX7__AC__ ..... 0°C to +70°C
- MAX7__AE__ ..... -40°C to +85°C
- MAX7__AMJA__ ..... -55°C to +125°C

Junction Temperatures:
- MAX7__AC/E ..... +150°C
- MAX7__AM ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 3, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MAX748A			MAX763A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range		3.3		16.0	3.3		11.0	V
Output Voltage	C/E temp. ranges, V+ = 4.0V to 16V, 0mA < I_{LOAD} < 300mA	3.135	3.3	3.465				V
	M temp. range, V+ = 4.0V to 16V, 0mA < I_{LOAD} < 250mA	3.135	3.3	3.465				
	C/E temp. ranges, V+ = 4.75V to 16V, 0mA < I_{LOAD} < 500mA	3.135	3.3	3.465				
	M temp. range, V+ = 4.75V to 16V, 0mA < I_{LOAD} < 400mA	3.135	3.3	3.465				
	C/E temp. ranges, V+ = 4.0V to 11V, 0mA < I_{LOAD} < 300mA				3.135	3.3	3.465	
	M temp. range, V+ = 4.0V to 11V, 0mA < I_{LOAD} < 250mA				3.135	3.3	3.465	
	C/E temp. ranges, V+ = 4.75V to 11V, 0mA < I_{LOAD} < 500mA				3.135	3.3	3.465	
	M temp. range, V+ = 4.75V to 11V, 0mA < I_{LOAD} < 400mA				3.135	3.3	3.465	
Line Regulation			0.13			0.13		%/V
Load Regulation	I_{LOAD} = 0mA to 500mA		0.001			0.001		%/mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 3, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

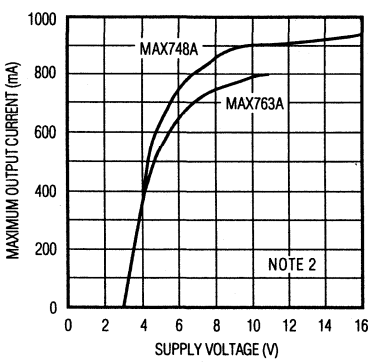
PARAMETER	CONDITIONS		MAX748A MIN	MAX748A TYP	MAX748A MAX	MAX763A MIN	MAX763A TYP	MAX763A MAX	UNITS
Efficiency	V+ = 5V	I_{LOAD} = 300mA		88			88		%
		I_{LOAD} = 100mA		90			90		
Supply Current	Includes switch current			1.7	3.0		1.4	2.5	mA
Shutdown Current	$\overline{SHDN}$ = 0V (Note 1)			0.2	100.0		0.2	100.0	µA
Shutdown Input Threshold	V_{IH}		2.0			2.0			V
	V_{IL}				0.25			0.25	
Shutdown Input Leakage Current					1.0			1.0	µA
Short-Circuit Current				1.2			1.2		A
Undervoltage Lockout	V+ falling			2.7	3.0		2.7	3.0	V
LX On Resistance	I_{LX} = 500mA			1.0			1.0		Ω
LX Leakage Current	V+ = 12V, LX = 0			10			10		nA
Reference Voltage	T_A = +25°C		1.15	1.22	1.30	1.15	1.22	1.30	V
Reference Drift	T_A = T_{MIN} to T_{MAX}			50			50		ppm/°C
Oscillator Frequency			159	180	212.5	159	200	212.5	kHz
Compensation Pin Impedance				7500			7500		Ω

Note 1: The standby current typically settles to 10µA (over temperature) within 2 seconds; however, to decrease test time, the part is guaranteed at a 100µA maximum value.

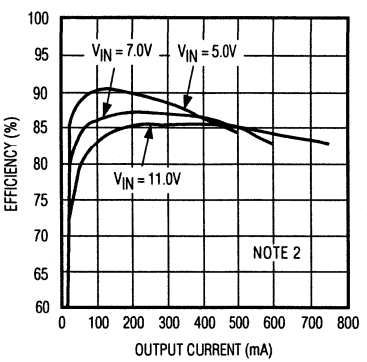
Typical Operating Characteristics

(Circuit of Figure 3, T_A = +25°C, V_{OUT} = 3.3V, unless otherwise noted.)

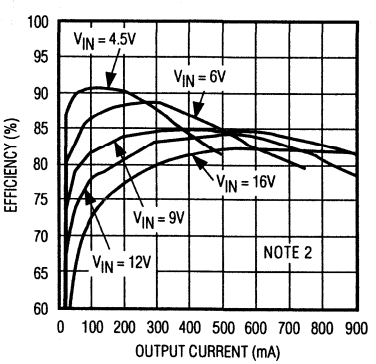
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



MAX763A EFFICIENCY vs. OUTPUT CURRENT



MAX748A EFFICIENCY vs. OUTPUT CURRENT

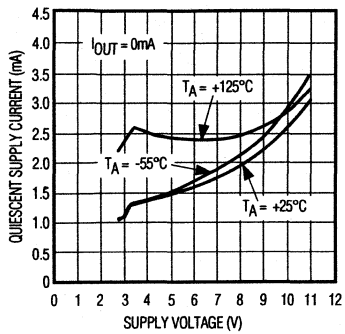


3.3V, Step-Down, Current-Mode PWM DC-DC Converters

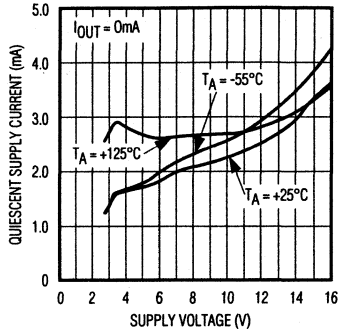
Typical Operating Characteristics (continued)

(Circuit of Figure 3, T_A = +25°C, V_{OUT} = 3.3V, unless otherwise noted.)

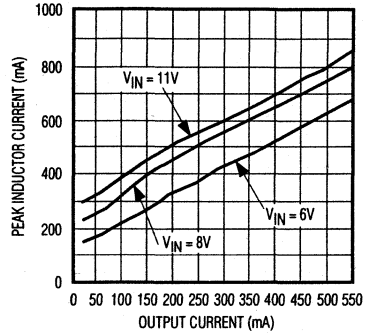
MAX763A QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



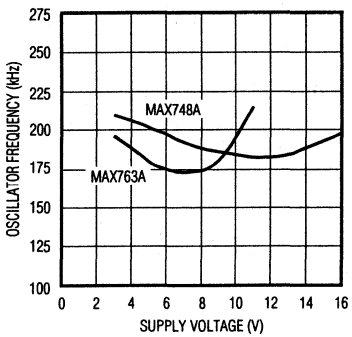
MAX748A QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



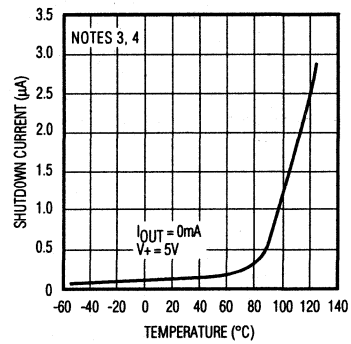
PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



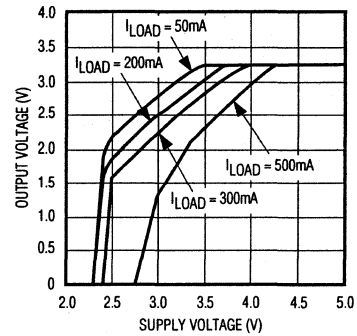
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



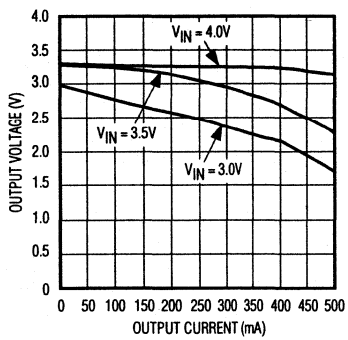
SHUTDOWN CURRENT vs. TEMPERATURE



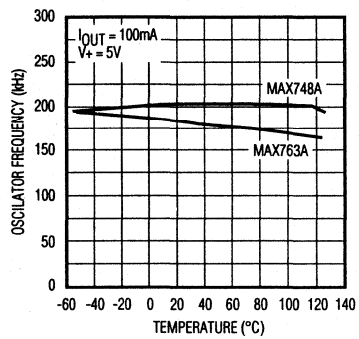
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE vs. OUTPUT CURRENT



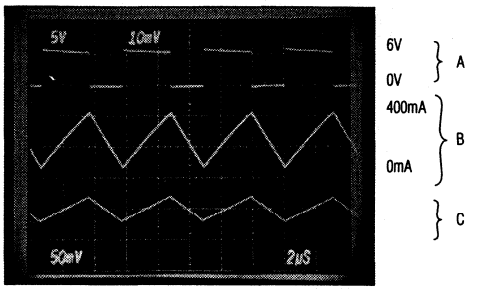
OSCILLATOR FREQUENCY vs. TEMPERATURE



Typical Operating Characteristics (continued)

(Circuit of Figure 3, T_A = +25°C, V_{OUT} = 3.3V, unless otherwise noted.)

SWITCHING WAVEFORMS, CONTINUOUS CONDUCTION

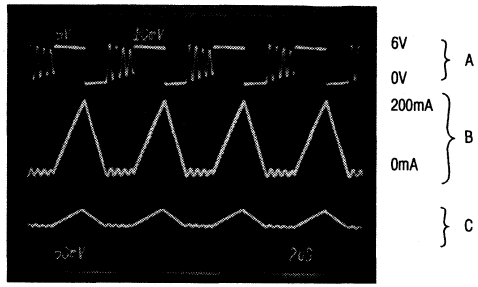


2µs/div

A: SWITCH VOLTAGE (LX PIN), 5V/div, 0V TO +6V
B: INDUCTOR CURRENT, 200mA/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div

V+ = 6V, I_{OUT} = 250mA

SWITCHING WAVEFORMS, DISCONTINUOUS CONDUCTION

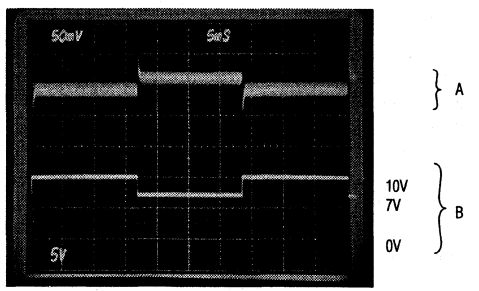


2µs/div

A: SWITCH VOLTAGE (LX PIN), 5V/div, 0V TO +6V
B: INDUCTOR CURRENT, 100mA/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div

V+ = 6V, I_{OUT} = 75mA

LINE-TRANSIENT RESPONSE

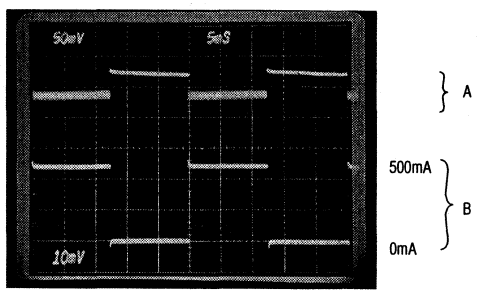


5ms/div

A: V_{OUT}, 50mV/div
B: V+, 5V/div, 7.0V TO 10.0V

I_{OUT} = 350mA

LOAD-TRANSIENT RESPONSE



5ms/div

A: V_{OUT}, 50mV/div
B: I_{OUT}, 200mA/div, 0mA TO 500mA

V+ = 6V

Note 2: Operation beyond the specifications listed in the *Electrical Characteristics* may exceed the power dissipation ratings of the device.

Note 3: Wide temperature range circuit of Figure 5 using Sprague surface-mount capacitors.

Note 4: Standby current includes all external component leakage currents. Capacitor leakage currents dominate at T_A = +85°C.

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

Pin Description

PIN #		NAME	FUNCTION
8-PIN DIP/SO	16-PIN WIDE SO (MAX748A)		
1	2	$\overline{SHDN}$	Shutdown—active low. Connect to ground to power down chip; tie to V+ for normal operation. Output voltage falls to 0V when $\overline{SHDN}$ is low.
2	3	REF	Reference Voltage Output (+1.23V) supplies up to 100µA for external loads. Bypass to GND with a 0.047µF capacitor.
3	7	SS	Soft-Start. Capacitor between SS and GND provides soft-start and short-circuit protection.
4	8	CC	Compensation Capacitor Input externally compensates the outer (voltage) feedback loop. Connect to OUT with a 330pF capacitor.
5	9	OUT	Output-Voltage Sense Input provides regulation feedback sensing. Connect to +3.3V output.
6	10, 11	GND	Ground*
7	12, 13, 14	LX	Drain of internal P-channel power MOSFET*
8	1,15,16	V+	Supply Voltage Input. Bypass to GND with 1µF ceramic and large-value electrolytic capacitor in parallel. The 1µF capacitor must be as close to the GND and V+ pins as possible.*
	4, 5, 6	N.C.	No Connect—no internal connections to these pins.

**16-pin wide SO package: All pins sharing the same name must be connected together externally.*

Detailed Description

The MAX748A/MAX763A switch-mode regulators use a current-mode pulse-width-modulation (PWM) control system in a step-down (buck) regulator topography. They convert an unregulated DC input voltage from 4V to 11V (MAX763A) or from 4V to 16V (MAX748A) to a regulated 3.3V output at 300mA. For loads less than 300mA, V+ may be less than 4.0V (see the Output Voltage vs. Supply Voltage graph in the *Typical Operating Characteristics*). The current-mode PWM architecture provides cycle-by-cycle current limiting, improved load-transient response, and simpler outerloop design.

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor and amplifier, and an outer (voltage) loop that monitors the output voltage through the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the power transistor on-time when the switch current reaches a predetermined threshold. This threshold is determined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

Programmable Soft-Start

Figure 2 shows a capacitor connected to the soft-start (SS) pin to ensure orderly power-up. A typical value is 0.047µF. SS controls both the SS timing and the maximum output current that can be delivered while maintaining regulation.

The charging capacitor slowly raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold. Table 1 lists timing characteristics for selected capacitor values and circuit conditions.

The overcurrent comparator trips when the load exceeds approximately 1.2A. When either an undervoltage or overcurrent fault condition is detected, an SS cycle is actively initiated, which triggers an internal transistor to discharge the SS capacitor to ground. An SS cycle is also enabled at power-up and when coming out of shutdown mode.

Overcurrent Limiting

The overcurrent comparator triggers when the load current exceeds approximately 1.2A. On each clock cycle, the output FET turns on and attempts to deliver current until cycle-by-cycle or overcurrent limits are exceeded. Note that the SS capacitor must be greater than 0.01µF for overcurrent protection to function properly. A typical value is 0.047µF.

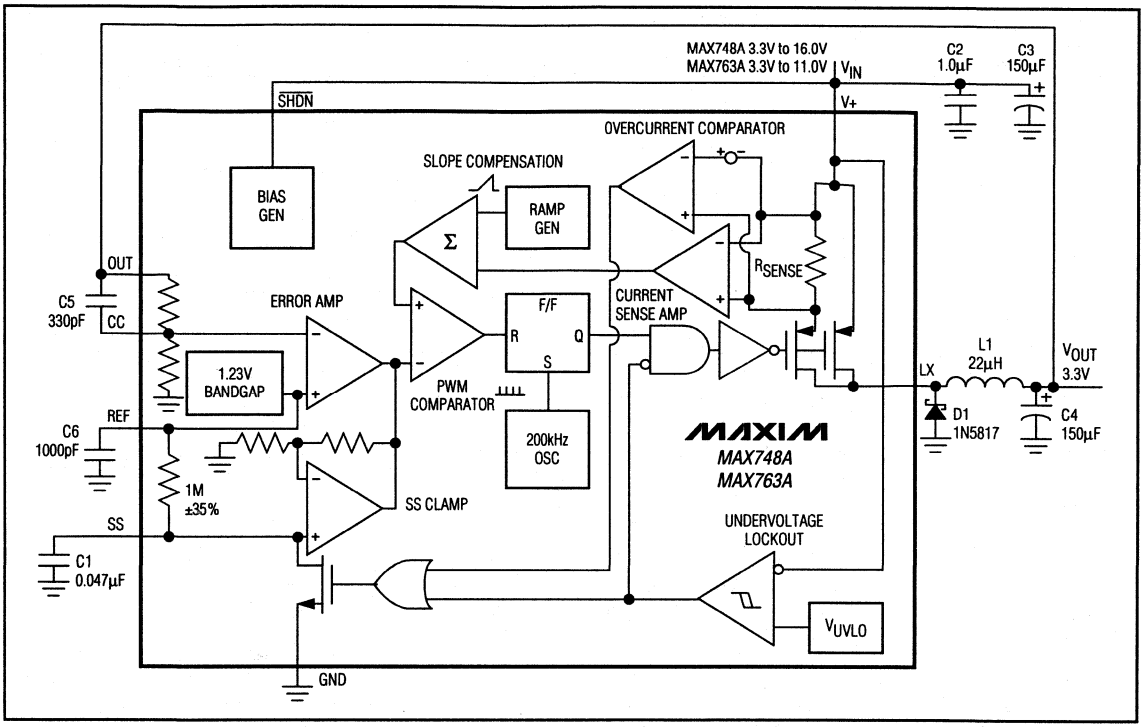


Figure 1. Detailed Block Diagram with External Components

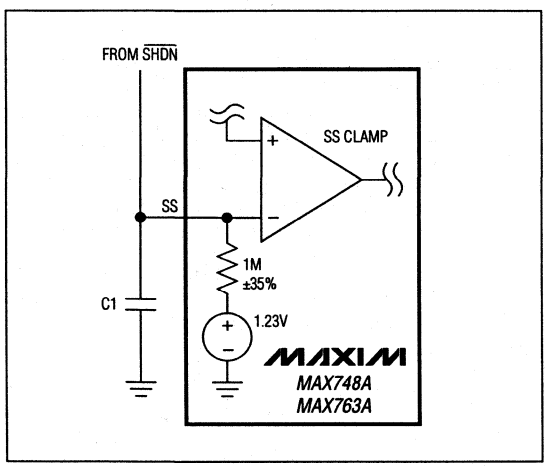


Figure 2. Soft-Start Circuitry Block Diagram

Table 1. Typical Soft-Start Times

(Circuit of Figure 3, C4 = 150µF)

Circuit Cond.		Soft-Start Time (ms) vs. C1 (µF)			
V+ (V)	I_{OUT} (mA)	C1 = 0.01	C1 = 0.047	C1 = 0.1	C1 = 0.47
8	0	1	4	7	12
12*	0	1	2	3	6
8	200	10	33	50	200
12*	200	7	17	20	80
8	300	13	44	65	325
12*	300	8	25	35	140

** MAX748A only*

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

Table 3. External Component Suppliers

Production Method	Inductors	Capacitors
Surface Mount	Sumida CD105 series Coiltronics CTX series Coilcraft DT series	Matsuo 267 series Sprague 595D/293D series
High Performance/ Miniature Through-Hole	Sumida RCH895 series	Sanyo OS-CON series (very low ESR)
Through-Hole	Renco RL1284 series	Nichicon PL series (low ESR)

Phone and FAX Numbers:

Coilcraft	USA:	(708) 639-6400, FAX: (708) 639-1469	Renco	USA:	(516) 586-5566, FAX: (516) 586-5562
Coiltronics	USA:	(305) 781-8900, FAX: (305) 782-4163	Sanyo	USA:	(0720) 70-1005, FAX: (0720) 70-1174
Matsuo	USA:	(714) 969-2491, FAX: (714) 960-6492	Sprague Elec. Co.	USA:	(603) 224-1961, FAX: (603) 224-1430
	Japan:	(06) 332-0871	Sumida	USA:	(708) 956-0666, FAX: (708) 956-0702
Nichicon	USA:	(708) 843-7500, FAX: (708) 843-2798			
	Japan:	(03) 3607-5111, FAX: (03) 3607-5428			

Undervoltage Lockout

The undervoltage lockout feature monitors the supply voltage at V+ and allows operation to start when V+ rises above 2.95V. When V+ falls, operation continues until the supply voltage falls below 2.7V (typ). When an undervoltage condition is detected, control logic turns off the output power FET and discharges the SS capacitor to ground. This prevents partial turn-on of the power MOSFET and avoids excessive power dissipation. The control logic holds the output power FET off until the supply voltage rises above approximately 2.95V, at which time an SS cycle begins. When the input voltage exceeds the undervoltage lockout threshold, switching action will occur, but the output will not be regulated until the input voltage exceeds 3.3V (no load). The exact input voltage required for regulation depends on load conditions (see the Output Voltage vs. Supply Voltage graph in the *Typical Operating Characteristics*).

Shutdown Mode

The MAX748A/MAX763A are held in shutdown mode by keeping $\overline{SHDN}$ at ground. In shutdown mode, the output drops to 0V and the output power FET is held in an off state. The internal reference also turns off, which causes the SS capacitor to discharge. Typical supply current in shutdown mode is 0.2µA. The actual design limit for shutdown current is much less than the 100µA specified in the *Electrical Characteristics*. However, testing to tighter limits is prohibitive because the current takes several seconds to settle to a final value. For normal operation, connect $\overline{SHDN}$ to V+. Coming out of shutdown mode initiates an SS cycle.

Continuous-/Discontinuous-Conduction Modes

The input voltage, output voltage, load current, and inductor value determine whether the IC operates in continuous or discontinuous mode. As the inductor value or load current decreases, or the input voltage increases, the MAX748A/MAX763A tend to operate in discontinuous-conduction mode (DCM). In DCM, the inductor current slope is steep enough so it decays to zero before the end of the transistor off-time. In continuous-conduction mode (CCM), the inductor current never decays to zero, which is typically more efficient than DCM. CCM allows the MAX748A/MAX763A to deliver maximum load current, and is also slightly less noisy than DCM, because it doesn't exhibit the ringing that occurs when the inductor current reaches zero.

Internal Reference

The +1.23V bandgap reference supplies up to 100µA at REF. A 1000pF bypass capacitor from REF to GND is required.

Oscillator

The MAX748A/MAX763A's internal oscillator is guaranteed to operate in the 159kHz to 212.5 kHz range over temperature for V+ = 5V. Temperature stability over the military temperature range is about 0.04%/°C.

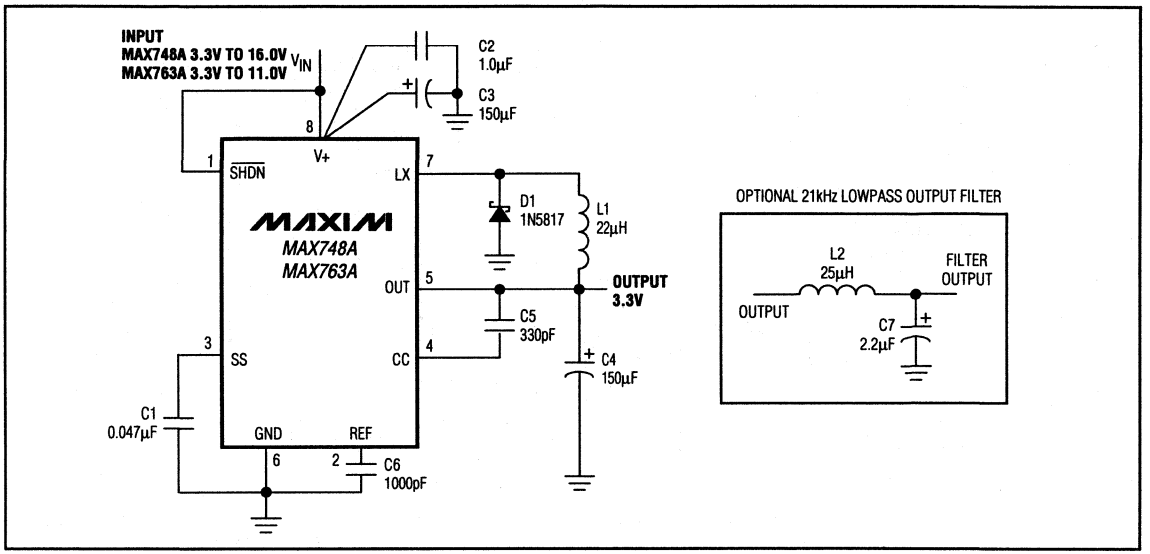


Figure 3. Standard 3.3V Step-Down Application Circuit Using Through-Hole Components (commercial temperture range)

Table 2. Component Table for Wide Temperature Applications

	C1(µF)	C2(µF)	C3(µF)	C4(µF)	C5(pF)	C6(pF)	L1(µH)
Through-Hole	0.047	1.0	150*	220*	330	1000	22
SO	0.047	1.0	68**	100***	330	1000	22

** Sanyo OS-CON Series (very low ESR)*

*** 16V or greater maximum voltage rating.*

**** 6.3V or greater maximum voltage rating.*

Applications Information

Fixed +3.3V Step-Down Converter Application

Figure 3 shows the standard 3.3V step-down circuit with components shown for commercial temperature range applications. Figures 4, 5, and Table 2 suggest external component values for both SO and through-hole wide temperature range applications. These circuits are useful in systems that require high current and high efficiency and are powered by an unregulated supply, such as a battery or wall-plug AC-DC adapter.

The MAX748A delivers a guaranteed 300mA for input voltages of 4V to 16V, and a guaranteed 500mA for input voltages of 4.75V to 16V with 800mA typical output currents. The MAX763A delivers a guaranteed 300mA for input voltages of 4V to 11V, a guaranteed 500mA for input voltages of 4.75V to 11V, and has 700mA typical output currents. The MAX748A/MAX763A operate from an input down to 3V (the upper limit of undervoltage lockout), but with some reduction in output voltage and maximum output current.

Inductor Selection

The MAX748A/MAX763A require no inductor design because they are tested in-circuit, and are guaranteed to deliver the power specified in the *Electrical Characteristics* with high efficiency using a single 22µH inductor. The 22µH inductor's incremental saturation current rating should be greater than 1A for 500mA load operation. Table 3 lists inductor types and suppliers for various applications. The surface-mount inductors have nearly equivalent efficiencies to the larger through-hole inductors.

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the inductor-current variation and the output capacitor's ESR determines the amplitude of the sawtooth ripple seen on the output voltage. Minimize the output filter capacitor's ESR to maintain AC stability.

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

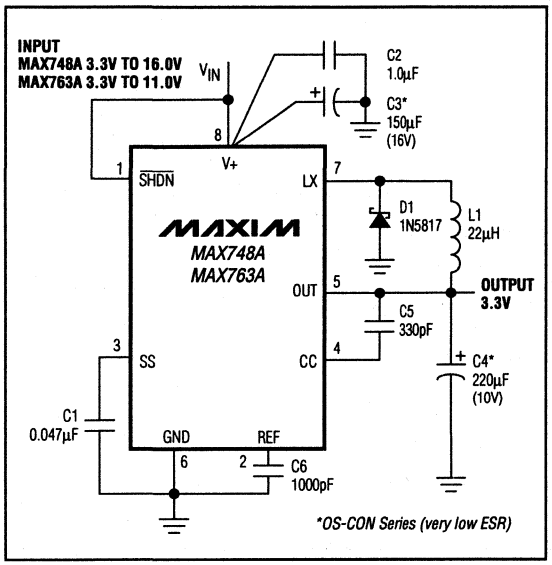


Figure 4. Standard 3.3V Step-Down Application Circuit Using Through-Hole Components (all temperature ranges)

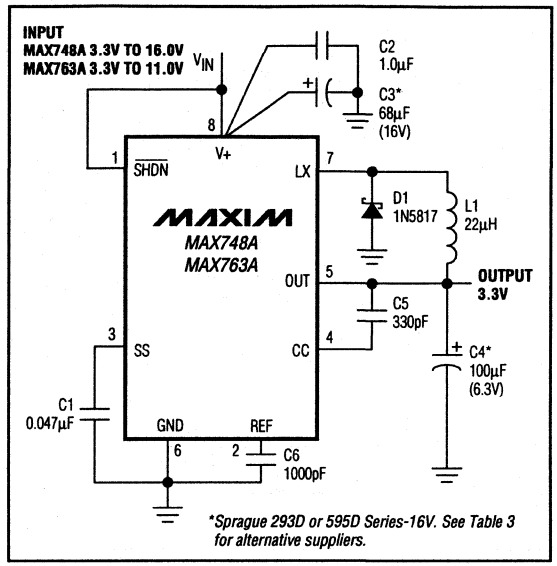


Figure 5. Standard 3.3V Step-Down Application Circuit Using Surface-Mount Components (Commercial and Extended Industrial Temperature Ranges)

The capacitor's ESR should be less than 0.25Ω to keep the output ripple less than 50mVP-P over the entire current range (using a 22µH inductor). Capacitor ESR usually rises at low temperatures, but OS-CON capacitors provide very low ESR below 0°C. Table 3 lists capacitor suppliers.

Other Components

The catch diode should be a Schottky or high-speed silicon rectifier with a peak current rating of at least 1.0A for full-load (500mA) operation. The 1N5817 is a good choice. The 330pF outer-loop compensation capacitor provides the widest input voltage range and best transient characteristics.

Printed Circuit Layouts

A good layout is essential for stable, low-noise operation. The layouts and component placement diagrams in Figures 6-9 have been tested successfully over a wide range of operating conditions. **The 1µF input bypass capacitor must be positioned as close to the V+ and GND pins as possible.** Also, place the output capacitor as close to the OUT and GND pins as possible. The traces connecting ground to the input and output filter capacitors and to the catch diode must be short to reduce inductance. Use an uninterrupted ground plane if possible.

Output-Ripple Filtering

A simple lowpass pi-filter (Figure 3) can be added to the output to reduce output ripple to about 5mVP-P. The cutoff frequency shown is 21kHz. Since the filter inductor is in series with the circuit output, minimize the filter inductor's resistance so the voltage drop across it is not excessive.

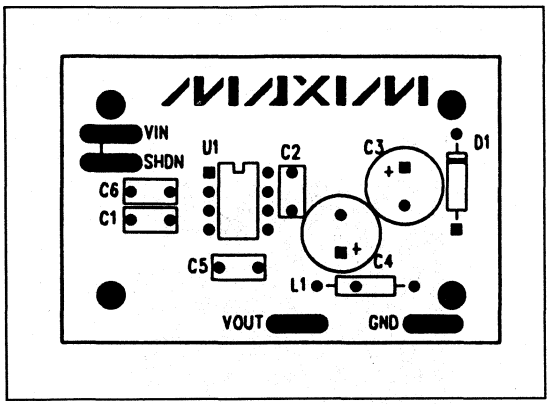


Figure 6. DIP PC Layout, Through-Hole Component Placement Diagram (1X Scale)

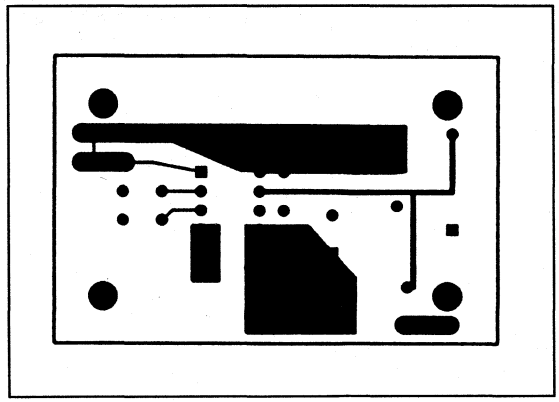


Figure 7. DIP PC Layout, Component Side (1X Scale)

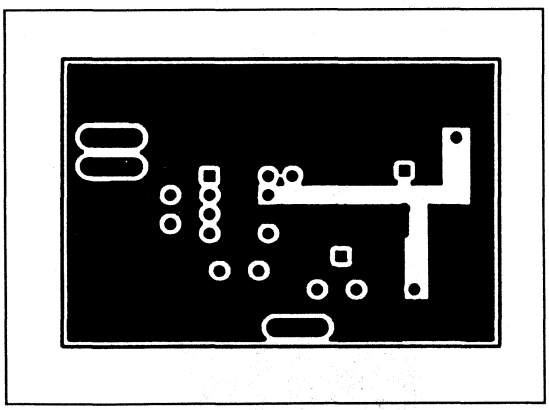


Figure 8. DIP PC Layout, Solder Side (1X Scale)

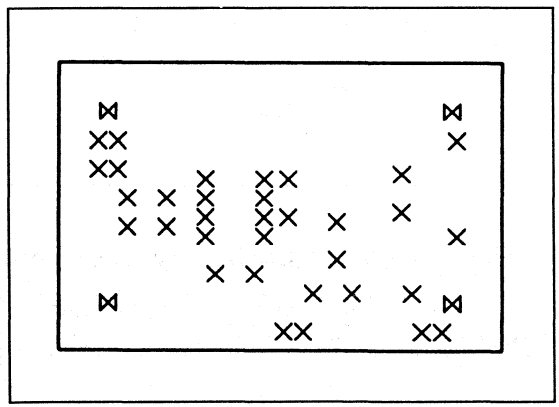
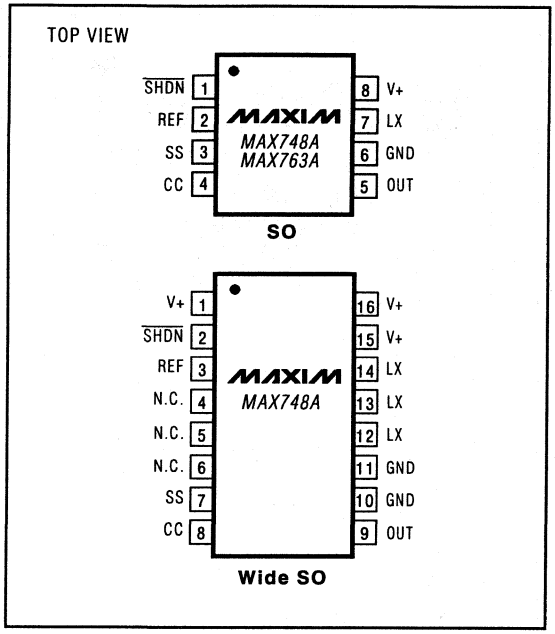


Figure 9. DIP PC Layout, Drill Guide (1X Scale)

3.3V, Step-Down, Current-Mode PWM DC-DC Converters

Pin Configurations (continued)

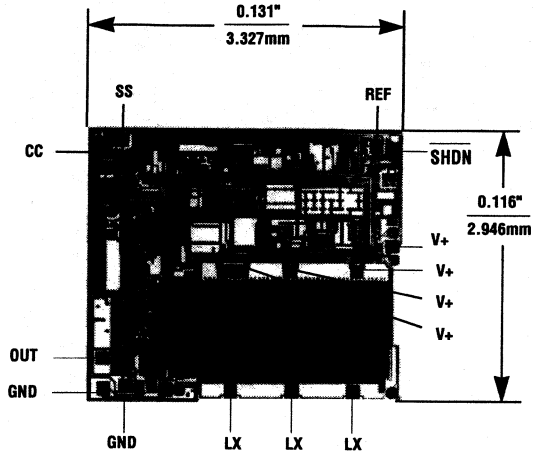


Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX763ACPA	0°C to +70°C	8 Plastic DIP
MAX763ACSA	0°C to +70°C	8 SO
MAX763AC/D	0°C to +70°C	Dice*
MAX763AEPA	-40°C to +85°C	8 Plastic DIP
MAX763AESA	-40°C to +85°C	8 SO
MAX763AMJA	-55°C to +125°C	8 CERDIP

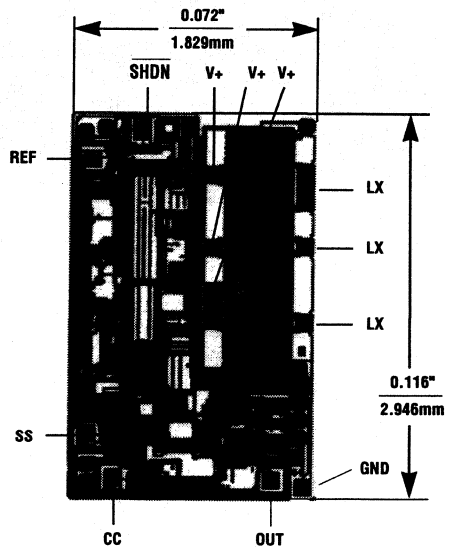
** Contact factory for dice specifications.*

Chip Topographies



MAX748A

TRANSISTOR COUNT: 298
SUBSTRATE CONNECTION: V+



MAX763A

TRANSISTOR COUNT: 281
SUBSTRATE CONNECTION: V+

19-0195; Rev 0; 10/93

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Adjustable, Step-Down, Current-Mode PWM Regulators

General Description

The MAX750A/MAX758A are adjustable-output, CMOS, step-down, DC-DC switching regulators. The MAX758A accepts inputs from 4V to 16V and delivers 750mA, while the MAX750A accepts inputs from 4V to 11V and delivers 450mA. Typical efficiencies are 85% to 90%. Typical quiescent current is 1.7mA, or only 6µA in shutdown mode. The output does not exhibit any ripple at subharmonics of the switching frequency over its specified range.

Pulse-width-modulation (PWM) current-mode control provides precise output regulation and excellent transient responses. Output voltage accuracy is guaranteed to be ±4.5% plus feedback-resistor tolerance over line, load, and temperature variations. Fixed-frequency switching and absence of subharmonic ripple allows easy filtering of output ripple and noise, as well as the use of small external components. These regulators require only a single inductor value to work in most applications, so no inductor design is necessary.

Applications

Cellular Phones & Radios
Portable Communications Equipment
Portable Instruments
Computer Peripherals

Features

- ♦ **Up to 750mA Load Currents**
- ♦ **160kHz High-Frequency, Current-Mode PWM**
- ♦ **85% to 96% Efficiencies**
- ♦ **33µH or 100µH Pre-Selected Inductor Value, No Component Design Required**
- ♦ **1.7mA Quiescent Supply Current**
- ♦ **6µA Shutdown Supply Current**
- ♦ **Adjustable Output Voltage**
- ♦ **Overcurrent, Soft-Start, and Undervoltage Lockout Protection**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **8-Pin DIP/SO Packages (MAX750A)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX750ACPA	0°C to +70°C	8 Plastic DIP
MAX750ACSA	0°C to +70°C	8 SO
MAX750AC/D	0°C to +70°C	Dice*
MAX750AEPA	-40°C to +85°C	8 Plastic DIP
MAX750AESA	-40°C to +85°C	8 SO
MAX750AMJA	-55°C to +125°C	8 CERDIP**

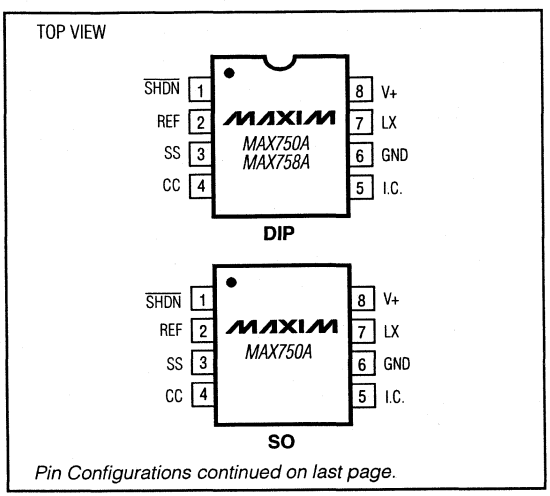
Ordering Information continued on last page.

** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883.*

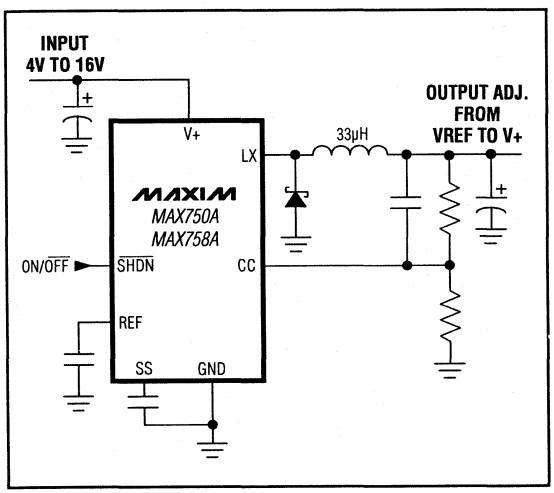
4

Pin Configurations



Pin Configurations continued on last page.

Typical Operating Circuit



Adjustable, Step-Down, Current-Mode PWM Regulators

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V+ (MAX750A) ..... +12V, -0.3V
- V+ (MAX758A) ..... +18V, -0.3V
- LX (MAX750A) ..... (V+ - 12V) to (V+ + 0.3V)
- LX (MAX758A) ..... (V+ - 21V) to (V+ + 0.3V)
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)

Peak Switch Current (I_{LX}) 2A
Reference Current (I_{REF}) 2.5mA
Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
- 8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX75_AC_ _ ..... 0°C to +70°C
- MAX75_AE_ _ ..... -40°C to +85°C
- MAX75_AMJA ..... -55°C to +125°C

Junction Temperatures:
- MAX75_AC_ _/AE_ _ ..... +150°C
- MAX75_AMJA ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 3, V+ = 9V for the MAX750A, V+ = 12V for the MAX758A, V_{OUT} = 5V, R2 = 40.20kΩ, R3 = 13.0kΩ, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MAX750A			MAX758A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage (Note 1)	V+ = 6.0V to 11.0V; 0mA < I_{LOAD} < 450mA for MAX750AC, 0mA < I_{LOAD} < 450mA for MAX750AE, 0mA < I_{LOAD} < 300mA for MAX750AM	4.75	5.00	5.25				V
	V+ = 6.0V to 16.0V; 0mA < I_{LOAD} < 450mA for MAX758AC/AE, 0mA < I_{LOAD} < 350mA for MAX758AM				4.75	5.00	5.25	
	V+ = 10.2V to 16.0V, 0mA < I_{LOAD} < 750mA				4.75	5.00	5.25	
Input Voltage Range		4.0		11.0	4.0		16.0	V
Line Regulation	V+ = 4.0V to 11.0V		0.15					%/V
	V+ = 4.0V to 16.0V					0.15		
Load Regulation	I_{LOAD} = 0mA to 450mA		0.0005					%/mA
	I_{LOAD} = 0mA to 750mA					0.0005		
Efficiency	V+ = 9.0V, I_{LOAD} = 300mA		92			90		%
	V+ = 12V, I_{LOAD} = 750mA					87		
Supply Current			1.7	3.0		1.7	3.0	mA
Shutdown Supply Current (Note 2)	$\overline{SHDN}$ = 0V		6.0	100.0		6.0	100.0	µA
Shutdown Input Threshold	V_{IH}	2.0			2.0			V
	V_{IL}			0.25			0.25	
Shutdown Input Leakage Current				1.0			1.0	µA
Short-Circuit Current			1.5			1.5		A

19-0201; Rev 0; 11/93

EVALUATION KIT AVAILABLE

MAXIM

12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

General Description

The MAX761/MAX762 step-up switching regulators provide high efficiency over a wide range of load currents, delivering up to 150mA. A unique, current-limited pulse-frequency-modulated (PFM) control scheme gives the devices the benefits of pulse-width-modulated (PWM) converters (high efficiency with heavy loads), while using less than 110µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

The MAX761/MAX762 input voltage range is 2V to 16.5V. Output voltages are preset to 12V (MAX761) and 15V (MAX762), or they can be set with two external resistors. With a 5V input, the MAX761 guarantees a 12V, 150mA output. Its high efficiency, low supply current, fast start-up time, SHDN controlling capability, and small size make the MAX761 ideal for powering flash memory.

The MAX761/MAX762 have an internal 1A power MOSFET, making them ideal for minimum-component, low- and medium-power applications. These devices use tiny external components, and their high switching frequencies (up to 300kHz) allow for small surface-mount magnetics.

For increased output drive capability or higher output voltages, use the MAX770–MAX773, which are similar in design to the MAX761/MAX762, but drive external power MOSFETs. For stepping up to 5V, see the MAX756/MAX757 and MAX856-MAX859 data sheets.

Applications

Flash Memory Programming
PCMCIA Cards
Battery-Powered Applications
High-Efficiency DC-DC Converters

Features

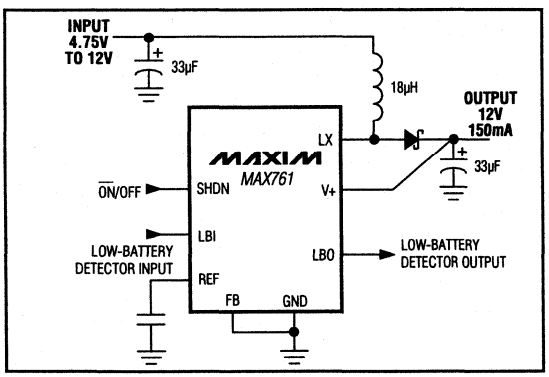
- ♦ **High Efficiency for a Wide Range of Load Currents**
- ♦ **12V/150mA Flash Memory Programming Supply**
- ♦ **110µA Max Supply Current**
- ♦ **5µA Max Shutdown Supply Current**
- ♦ **2V to 16.5V Input Voltage Range**
- ♦ **12V (MAX761), 15V (MAX762) or Adjustable Output**
- ♦ **Current-Limited PFM Control Scheme**
- ♦ **300kHz Switching Frequency**
- ♦ **Internal, 1A, N-Channel Power FET**
- ♦ **LBI/LBO Low-Battery Comparator**

Ordering Information

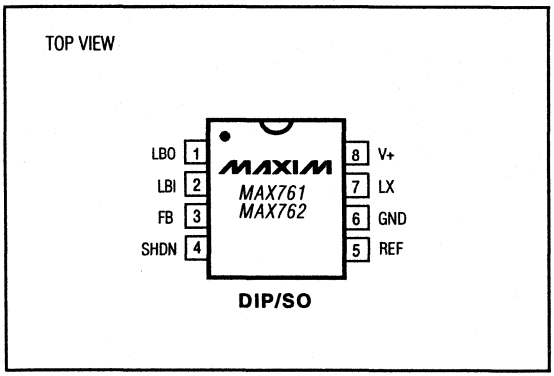
PART	TEMP. RANGE	PIN-PACKAGE
MAX761CPA	0°C to +70°C	8 Plastic DIP
MAX761CSA	0°C to +70°C	8 SO
MAX761C/D	0°C to +70°C	Dice*
MAX761EPA	-40°C to +85°C	8 Plastic DIP
MAX761ESA	-40°C to +85°C	8 SO
MAX761MJA	-55°C to +125°C	8 CERDIP**
MAX762CPA	0°C to +70°C	8 Plastic DIP
MAX762CSA	0°C to +70°C	8 SO
MAX762C/D	0°C to +70°C	Dice*
MAX762EPA	-40°C to +85°C	8 Plastic DIP
MAX762ESA	-40°C to +85°C	8 SO
MAX762MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+ to GND ..... -0.3V to 17V
REF, LBO, LBI, SHDN, FB ..... -0.3V to (V+ + 0.3V)
LX ..... -0.3V to 17V
LX Peak Current 1.5A
LBO Current 5mA
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
  SO (derate 5.88mW/°C above +70°C) 471mW
  CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
  MAX76_C_A ..... 0°C to +70°C
  MAX76_E_A ..... -40°C to +85°C
  MAX76_MJA ..... -55°C to +125°C
Junction Temperatures:
  MAX76_C_A/E_A ..... +150°C
  MAX76_MJA ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V+	Figure 2, bootstrapped		2		16.5	V
		Figure 3 or 5 with external resistors.	MAX76_C/E	3		16.5	
			MAX76_M	3.1		16.5	
Minimum Operating Voltage		Figure 2, bootstrapped			1.7		V
Minimum Start-Up Voltage		Figure 2, bootstrapped			1.7	2.0	V
Supply Current		V+ = 16.5V, normal operation, SHDN = 0V, non-bootstrapped			88	110	µA
		Figure 2, MAX761, V_{IN} = 5V, SHDN = 0V, normal operation			300		
Shutdown Current		V+ = 10.0V, shutdown mode, SHDN = V+			1	5	µA
Output Voltage (Note 1)	V_{OUT}	Figure 2, MAX761, bootstrapped	0mA ≤ I_{LOAD} ≤ 75mA, 3V ≤ V+ ≤ 12V	11.52	12.0	12.48	V
			0mA ≤ I_{LOAD} ≤ 150mA, 4.75V ≤ V+ ≤ 12V	11.52	12.0	12.48	
		Figure 2, MAX762, bootstrapped	0mA ≤ I_{LOAD} ≤ 50mA, 3V ≤ V+ ≤ 15V	14.4	15.0	15.6	
			0mA ≤ I_{LOAD} ≤ 100mA, 4.75V ≤ V+ ≤ 15V	14.4	15.0	15.6	
Peak Current at LX	I_{PEAK}	See Figure 4b		0.75	1.0	1.25	A
Maximum Switch-On Time	t_{ON}			6	8	10	µs
Minimum Switch-Off Time	t_{OFF}			1.0	1.3	1.6	µs
Load Regulation		Figure 2, 0mA ≤ I_{LOAD} ≤ 200mA, bootstrapped			0.0042		%/mA
Line Regulation		Figure 2, 4V ≤ V_{IN} ≤ 6V, bootstrapped			0.08		%/V
Efficiency		Figure 2, bootstrapped, V_{OUT} = 12V, 60mA ≤ I_{LOAD} ≤ 120mA			86		%
Reference Voltage	V_{REF}	MAX76_C		1.4700	1.50	1.5300	V
		MAX76_E		1.4625	1.50	1.5375	
		MAX76_M		1.4550	1.50	1.5450	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Load Regulation		0µA ≤ I_{LOAD} ≤ 100µA	MAX76_C/E			10	mV
			MAX76_M			15	
Reference Line Regulation		3.0V ≤ V+ ≤ 16.5V			30	100	µV/V
LX Leakage Current		V+ = 16.5V, LX = 17V	MAX76_C	-5		5	µA
			MAX76_E	-10		10	
			MAX76_M	-30		30	
FB Leakage Current	I_{FB}	MAX76_C		-20		20	nA
		MAX76_E		-40		40	
		MAX76_M		-60		60	
Voltage Trip Point	V_{FB}	MAX76_C		1.4700	1.50	1.5300	V
		MAX76_E		1.4625	1.50	1.5375	
		MAX76_M		1.4550	1.50	1.5450	
LX On Resistance		V+ > 5.0V			1.0	2.2	Ω
SHDN Input High Voltage	V_{IH}	2.0V ≤ V+ ≤ 16.5V		1.6			V
SHDN Input Low Voltage	V_{IL}	2.0V ≤ V+ ≤ 16.5V				0.4	V
SHDN Leakage Current		V+ = 16.5V, SHDN = 0V or V+		-1		1	µA
LBI Threshold Voltage		LBI falling	MAX76_C	1.4700	1.50	1.5300	V
			MAX76_E	1.4625	1.50	1.5375	
			MAX76_M	1.4550	1.50	1.5450	
LBI Hysteresis					20		mV
LBI Leakage Current		V+ = 16.5V, V_{LBI} = 1.5V		-20		20	nA
LBO Leakage Current		V+ = 16.5V, V_{LBO} = 16.5V		-1		1	µA
LBO Voltage	V_{OL}	V+ = 5.0V, I_{SINK} = 1mA				0.4	V
LBI to LBO Delay		Overdrive = 5mV			2.5		µs

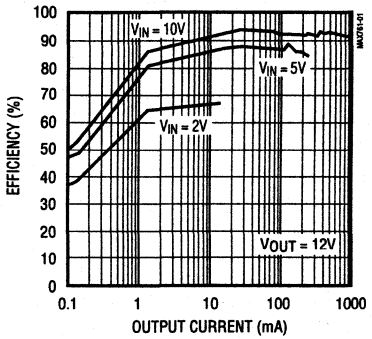
Note 1: See *Typical Operating Characteristics* for output current capability versus input voltage. Guarantees based on correlation to switching on and off times, on-resistance, and peak-current ratings.

12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

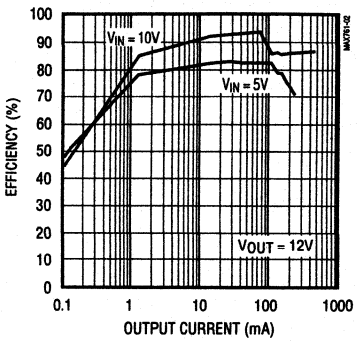
Typical Operating Characteristics

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

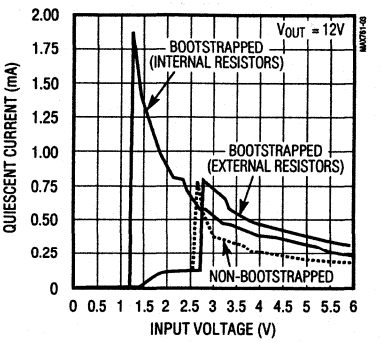
EFFICIENCY vs. OUTPUT CURRENT BOOTSTRAPPED



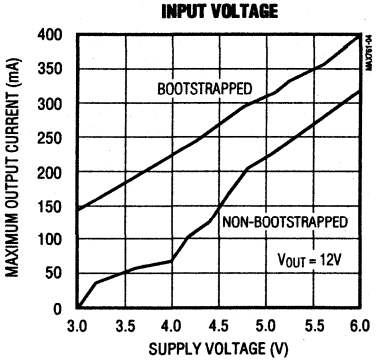
EFFICIENCY vs. OUTPUT CURRENT NON-BOOTSTRAPPED



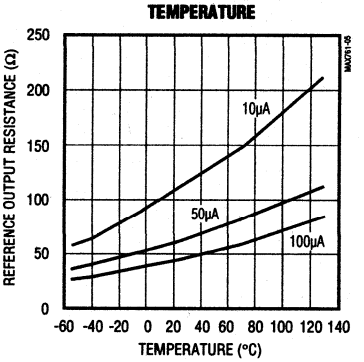
QUIESCENT CURRENT vs. INPUT VOLTAGE



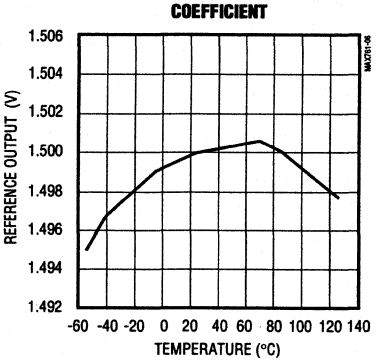
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



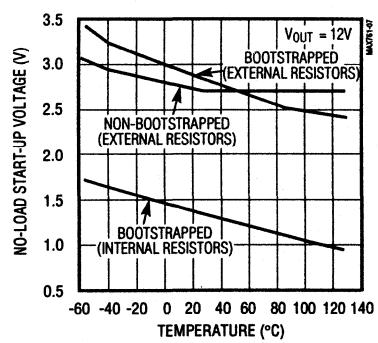
REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE



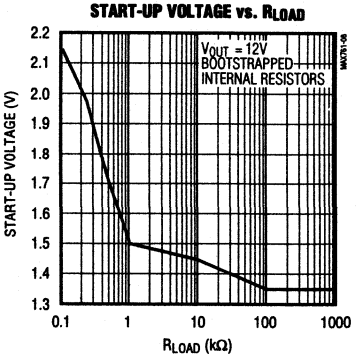
REFERENCE vs. TEMPERATURE COEFFICIENT



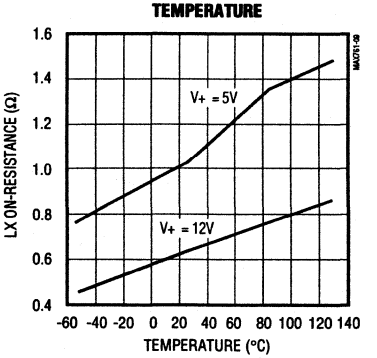
NO-LOAD START-UP VOLTAGE



MAX761 START-UP VOLTAGE vs. R_{LOAD}



LX ON-RESISTANCE vs. TEMPERATURE

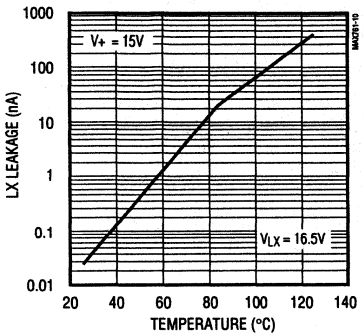


12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

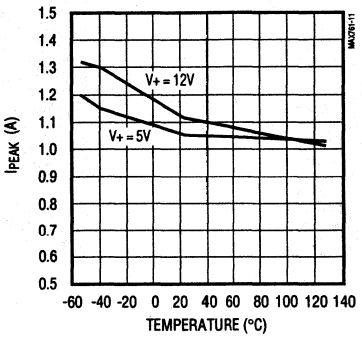
Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

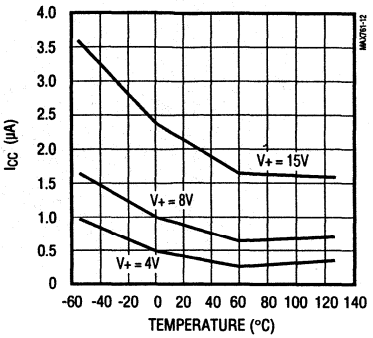
LX LEAKAGE vs. TEMPERATURE



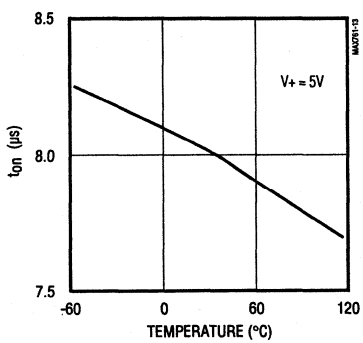
PEAK CURRENT AT LX vs. TEMPERATURE



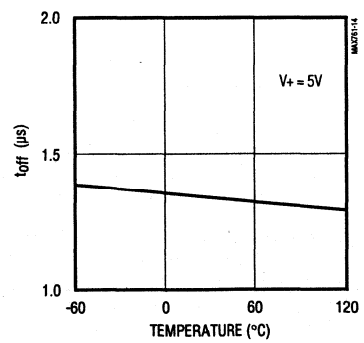
SHUTDOWN CURRENT vs. TEMPERATURE



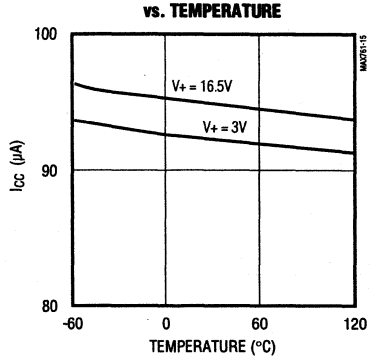
SWITCH-ON TIME vs. TEMPERATURE



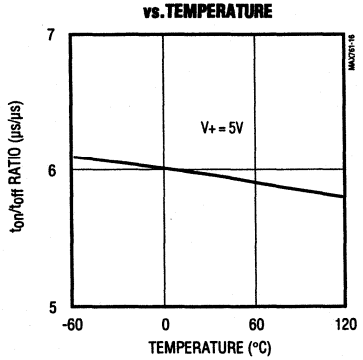
SWITCH-OFF TIME vs. TEMPERATURE



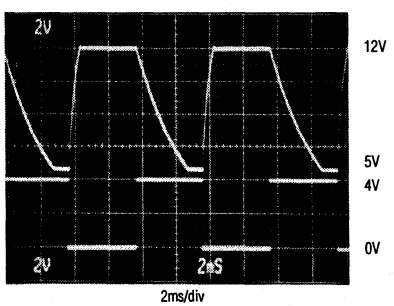
POWER-SUPPLY CURRENT vs. TEMPERATURE



SWITCH-ON/SWITCH-OFF TIME RATIO vs. TEMPERATURE



SHDN RESPONSE TIME



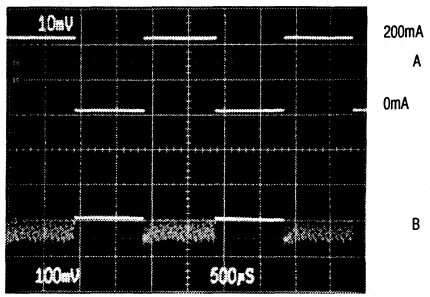
I_{LOAD} = 100mA, V_{IN} = 5V
A: V_{OUT}, 2V/div
B: SHDN (0V to 4V)

12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

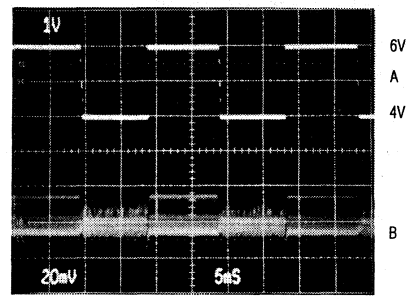
LOAD-TRANSIENT RESPONSE



5µs/div

A: I_{LOAD}, (0mA to 200mA)
B: V_{OUT}, AC COUPLED, 100mV/div
V_{IN} = 5V, V_{OUT} = 12V

LINE-TRANSIENT RESPONSE



5ms/div

A: V_{IN} (4V to 6V)
B: V_{OUT}, AC COUPLED, 20mV/div
I_{OUT} = 50mA, V_{OUT} = 12V

Pin Description

PIN	NAME	FUNCTION
1	LBO	Low-battery output is an open-drain output that goes low when LBI is less than 1.5V. Connect to V+ through a pull-up resistor. Leave LBO floating if not used.
2	LBI	Input to the internal low-battery comparator. Tie to GND or V+ if not used.
3	FB	Feedback input. For fixed-output bootstrapped operation, connect FB to GND. For adjustable-output bootstrapped operation, connect a resistor divider between V+, FB and GND. For non-bootstrapped operation, there is no fixed-output option. Connect a resistor divider network between V_{OUT}, FB and GND. See *Bootstrapped/Non-Bootstrapped Modes* section.
4	SHDN	Active-high TTL/CMOS logic-level input. In shutdown mode (SHDN = V+), the internal switch is turned off and the output voltage equals V+ minus a diode drop (due to the DC path from the input to the output). Tie to GND for normal operation.
5	REF	1.5V reference output that can source 100µA for external loads. Bypass with 0.1µF or larger capacitor.
6	GND	Ground
7	LX	Drain of the internal N-channel FET. LX has an output resistance of 1Ω and a peak current limit of 1A.
8	V+	Power-supply input. In bootstrapped mode, V+ is also the output voltage sense input.

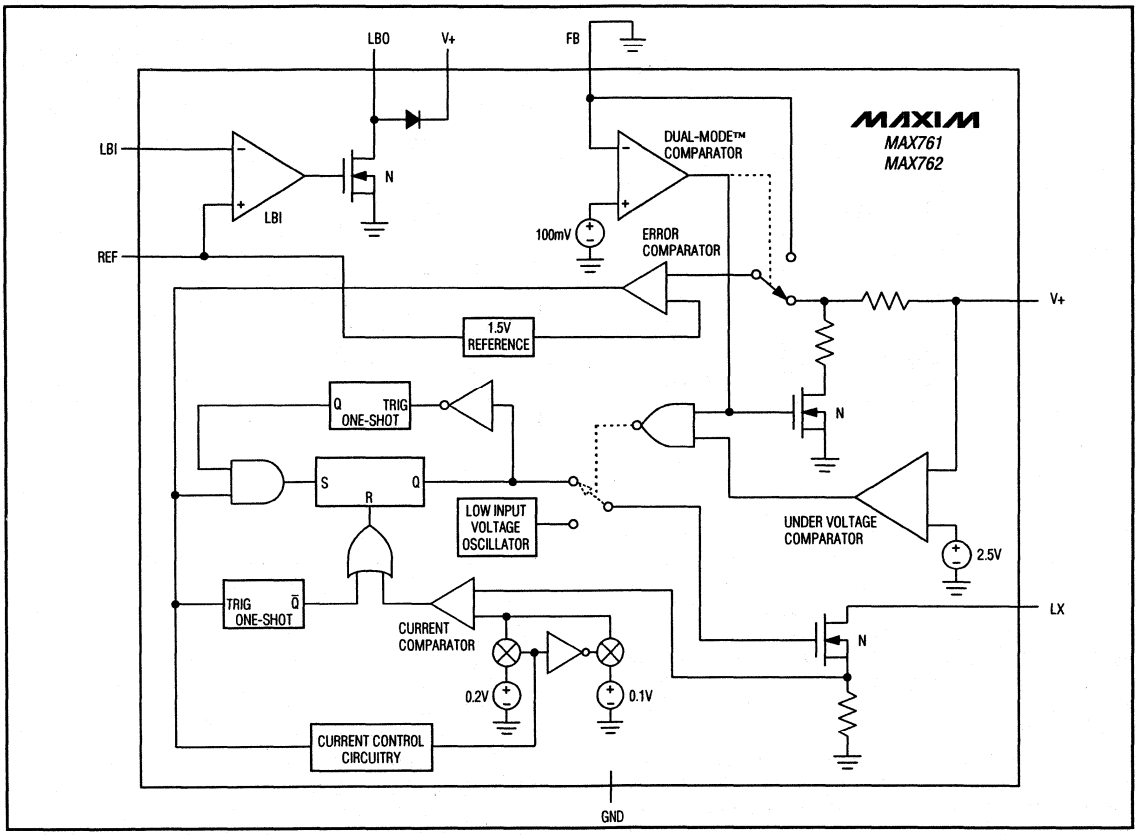


Figure 1. Simple Block Diagram

Detailed Description

Operating Principle

The MAX761/MAX762 BiCMOS step-up switch-mode power supplies provide fixed outputs of 12V and 15V, respectively. They have a unique control scheme that combines the advantages of pulse-frequency modulation (low supply current) and pulse-width modulation (high efficiency at high loads). The internal N-channel power MOSFET allows 1A peak currents, increasing the output current capability over previous pulse-frequency-modulation (PFM) devices. Figure 1 shows the MAX761/MAX762 block diagram.

The MAX761/MAX762 offer three main improvements over prior solutions: (1) the converters operate with tiny surface-mount inductors (less than 5mm diameter) because of their 300kHz switching frequency, (2) the current-limited PFM control scheme allows 86% efficiencies over a wide range of load currents, and (3) the maximum supply current is only 110µA.

Bootstrapped/Non-Bootstrapped Modes

Figures 2 and 3 show the standard application circuits for bootstrapped and non-bootstrapped modes. In bootstrapped mode, the IC is powered from the output (V_{OUT}). In other words, the current needed to power the bootstrapped circuit is different from the V+ current the chip consumes. The voltage applied to the gate of the internal N-channel FET is switched from V_{OUT} to ground, providing more switch-gate drive and increasing the efficiency of the DC-DC converter compared with non-bootstrapped operation.

12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

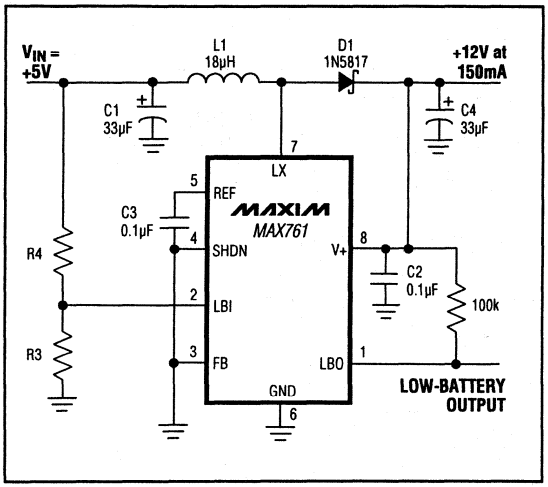


Figure 2. Bootstrapped Operating Circuit

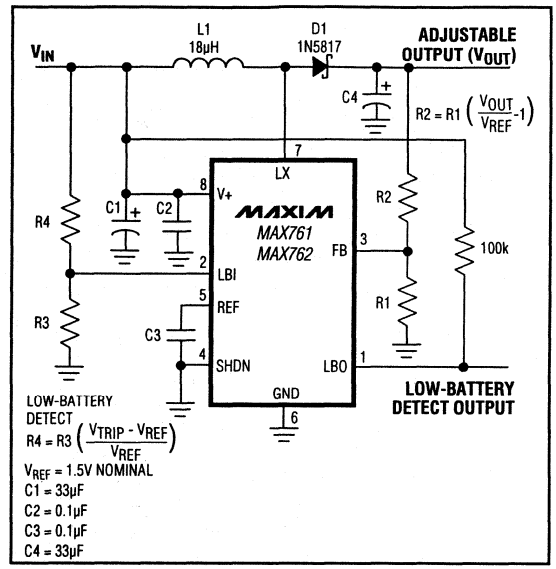


Figure 3. Non-Bootstrapped Operating Circuit

In non-bootstrapped mode, the IC is powered from the supply voltage, V_{IN}, and operates with minimum supply current. Since the voltage applied to the gate of the internal FET is reduced, efficiency declines with low input voltages. **Note: In non-bootstrapped mode, there is no fixed-output operation; external resistors must be used to set the output voltage.** Use 1% external feedback resistors when operating in non-bootstrapped mode (Figure 3).

Use bootstrapped mode when V_{IN} is below approximately 4V. For V_{IN} between 4V and 6V, the trade-off is lower supply current in non-bootstrapped mode versus higher output current in bootstrapped mode (see *Typical Operating Characteristics*).

Pulse-Frequency Modulation (PFM) Control Scheme

The MAX761/MAX762 use a proprietary current-limited PFM control scheme. This control scheme combines the ultra-low supply current of pulse-skipping PFM converters with the high full-load efficiency characteristic of current-mode pulse-width-modulation (PWM) converters. It allows the devices to achieve high efficiency over a wide range of loads, while the current-sense function and high operating frequency allow the use of tiny external components.

As with traditional PFM converters, the internal power MOSFET is turned on when the voltage comparator senses the output is out of regulation (Figure 1). However, unlike traditional PFM converters, switching is accomplished through the combination of a peak current limit and a pair of one-shots that set the maximum on-time (8µs) and minimum off-time (1.3µs) for the switch. Once off, the minimum off-time one-shot holds the switch off for 1.3µs. After this minimum time, the switch either (1) stays off if the output is in regulation, or (2) turns on again if the output is out of regulation.

The MAX761/MAX762 also limit the peak inductor current, allowing the devices to run in continuous-conduction mode (CCM) and maintain high efficiency with heavy loads (Figure 4a). This current-limiting feature is a key component of the control circuitry. Once turned on, the switch stays on until either (1) the maximum on-time one-shot turns it off (8µs later), or (2) the current limit is reached.

To increase light-load efficiency, the current limit for the first two pulses is set to half the peak current limit. If those pulses bring the output voltage into regulation, the voltage comparator holds the MOSFET off, and the current limit remains at half the peak current limit. If the output voltage is still out of regulation after two pulses, the current limit for the next pulse is raised to the full current limit of 1A (Figure 4b).

Internal vs. External Resistors

When external feedback resistors are used, an internal undervoltage lockout system prevents start-up until V+ rises to about 2.7V. When external feedback resistors are

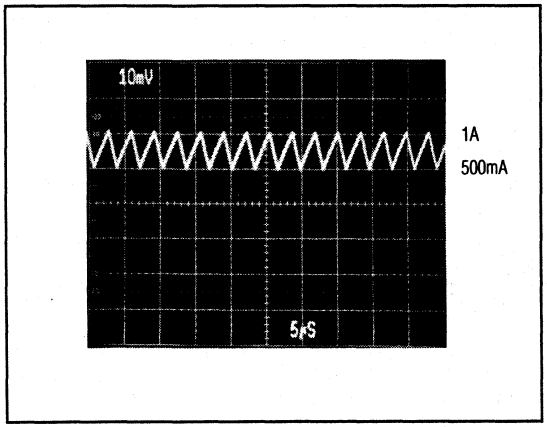


Figure 4a. CCM, Heavy Load Current Waveform (500mA/div)

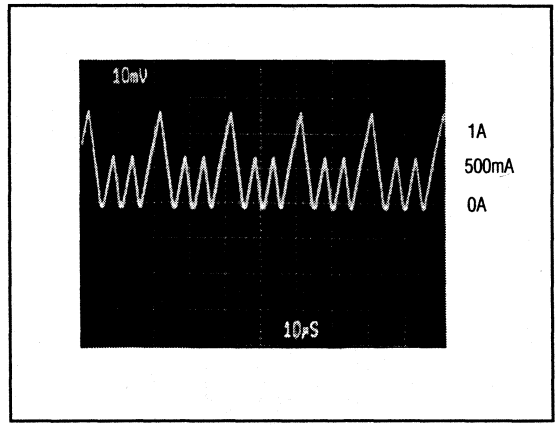


Figure 4b. Light/Medium Load Current Waveform (500mA/div)

used in a bootstrapped circuit (Figure 5), undervoltage lockout prevents start-up at low input voltages; but once started, operation can continue down to a lower voltage that depends on the load.

There is no undervoltage lockout when the internal feedback resistors are used (Figure 2), and special circuitry guarantees start-up at 2.0V. The start-up circuitry fixes the duty cycle at 50% until V+ is driven to 2.5V, above which the normal control system takes over.

Shutdown Mode

The MAX761/MAX762 enter shutdown mode when SHDN is high. In this mode, the internal biasing circuitry is turned off (including the reference) and V_{OUT} equals V+ minus a diode drop (due to the DC path from the input to the output). In shutdown mode, the supply current drops to less than 5µA. SHDN is a TTL/CMOS logic level input. Connect SHDN to GND for normal operation. LBO is high impedance during shutdown.

Modes of Operation

When delivering high output currents, the MAX761/MAX762 operate in CCM. In this mode, current always flows in the inductor, and the control circuit adjusts the switch's duty cycle on a cycle-by-cycle basis to maintain regulation without exceeding the switch-current capability. This provides excellent load-transient response and high efficiency.

In discontinuous-conduction mode (DCM), current through the inductor starts at zero, rises to a peak value, then ramps down to zero on each cycle. Although efficiency is still excellent, the switch waveforms contain ringing (the inductor's self-resonant frequency). This ringing is normal and poses no operational problems.

Low-Battery Detector

The MAX761/MAX762 provide a low-battery comparator that compares the voltage on LBI to the 1.5V reference voltage. When the LBI voltage is below V_{REF}, LBO (an open-drain output) goes low. The low-battery comparator's 20mV of hysteresis adds noise immunity, preventing repeated triggering of LBO. Use a resistor-divider network between V+, LBI, and GND to set the desired trip voltage V_{TRIP} (Figure 3). When SHDN is high, LBI is ignored and LBO is high impedance. The value of resistor R3 should be no larger than 500kΩ to ensure the LBI leakage current does not cause inaccuracies in V_{TRIP}.

Design Procedure

Setting the Output Voltage

The MAX761/MAX762's output voltage can be adjusted from 5V to 16.5V using external resistors R1 and R2 configured as shown in Figures 3 and 5. For adjustable-output operation, select feedback resistor R1 in the 10kΩ to 250kΩ range. Higher R1 values within this range give lowest supply current and best light-load efficiency. R2 is given by:

$$R2 = (R1)\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} = 1.5V.

Note: Tie FB to GND for fixed-output operation (bootstrapped mode only).

12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

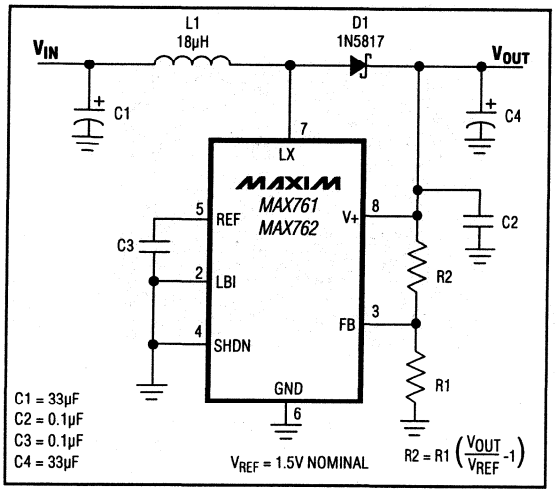


Figure 5. Bootstrapped Operation with Adjustable Output

Selecting the Inductor (L)

In both CCM and DCM, practical inductor values range from 10µH to 50µH. If the inductor value is too low, the current in the coil will ramp up to a high level before the current-limit comparator can turn off the switch. The minimum on-time for the switch ($t_{ON(min)}$) is approximately 2.5µs, so select an inductance that allows the current to ramp up to $I_{LIM}/2$ in no less than 2.5µs. Choosing a value of $I_{LIM}/2$ allows the half-size pulses to occur, giving higher light-load efficiency and minimizing ripple. Hence, calculate the minimum inductance value as:

$$L \geq \frac{(V_{IN(max)})(t_{ON(min)})}{I_{LIM}/2}$$

OR

$$L \geq (V_{IN(max)})(5)$$

where $V_{IN(max)}$ is in volts and L is in microhenries.

The coil's inductance need not satisfy this criterion exactly, as the circuit can tolerate a wide range of values. Larger inductance values tend to produce physically larger coils and increase the start-up time, but are otherwise acceptable. Smaller inductance values allow the coil current to ramp up to higher levels before the switch can turn off, producing higher ripple at light loads. In general, an 18µH inductor is sufficient for most applications ($V_{IN} \leq 5V$). An 18µH inductor is appropriate for input voltages up to 3.6V, as calculated above. However, the same 18µH coil can be used with input voltages up to 5V with only small increases in peak current, as shown in Figures 4a and 4b.

Inductors with a ferrite core or equivalent are recommended. The inductor's incremental saturation-current rating should be greater than the 1A peak current limit. It is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, use a coil with low DC resistance, preferably under 100mΩ. To minimize radiated noise, use a toroid, a pot core, or a shielded coil.

Table 1 lists inductor types and suppliers for various applications. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger through-hole inductors.

Diode Selection

The MAX761/MAX762's high switching frequency demands a high-speed rectifier. Use a Schottky diode with a 1A average current rating, such as a 1N5817. For high-temperature applications, use a high-speed silicon diode, such as the MUR105 or the EC11FS1. These diodes have lower high-temperature leakage than Schottky diodes (Table 1).

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor (C4) is low effective series resistance (ESR). The product of the inductor current variation and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. A 33µF, 16V Sanyo OS-CON capacitor with 100mΩ ESR typically provides 100mV ripple when stepping up from 5V to 12V at 150mA.

Because the output filter capacitor's ESR affects efficiency, use low-ESR capacitors for best performance. The smallest low-ESR SMT tantalum capacitors currently available are the Sprague 595D series. Sanyo OS-CON organic semiconductor through-hole capacitors and Nichicon PL series also exhibit very low ESR. Table 1 lists some suppliers of low-ESR capacitors.

Input Bypass Capacitors

The input bypass capacitor, C1, reduces peak currents drawn from the voltage source, and also reduces noise at the voltage source caused by the MAX761/MAX762's switching action. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is recommended. For output currents up to 250mA, 33µF (C1) is adequate, although smaller bypass capacitors may also be acceptable. Bypass the IC separately with a 0.1µF ceramic capacitor, C2, placed close to the V+ and GND pins.

Reference Capacitor

Bypass REF with a 0.1µF capacitor. REF can source up to 100µA.

Setting the Low-Battery Detector Voltage

To set the low-battery detector's falling trip voltage (V_{TRIP}), select R3 between 10kΩ and 500kΩ (Figures 2 and 3), and calculate R4 as follows:

$$R4 = R3 \left[\frac{(V_{TRIP} - V_{REF})}{V_{REF}} \right]$$

where V_{REF} = 1.5V.

The rising trip voltage is higher because of the comparator's hysteresis of approximately 20mV, and can be calculated by:

$$V_{TRIP}(rising) = (V_{REF} + 20mV)(1 + R4/R3).$$

Connect a high-value resistor (larger than R3 + R4) between LBI and LBO if additional hysteresis is required.

Connect a pull-up resistor (e.g., 100kΩ) between LBO and V_{OUT}. Tie LBI to GND or V+ and leave LBO floating if the low-battery detector is not used.

Applications Information

Layout Considerations

Proper PC board layout is essential because of high current levels and fast switching waveforms that radiate noise. Minimize ground noise by connecting GND, the input bypass-capacitor ground lead, and the output filter-capacitor ground lead to a single point (star ground configuration). Also minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. The traces connected to FB and LX, in particular, must be short. Place bypass capacitor C2 as close as possible to V+ and GND.

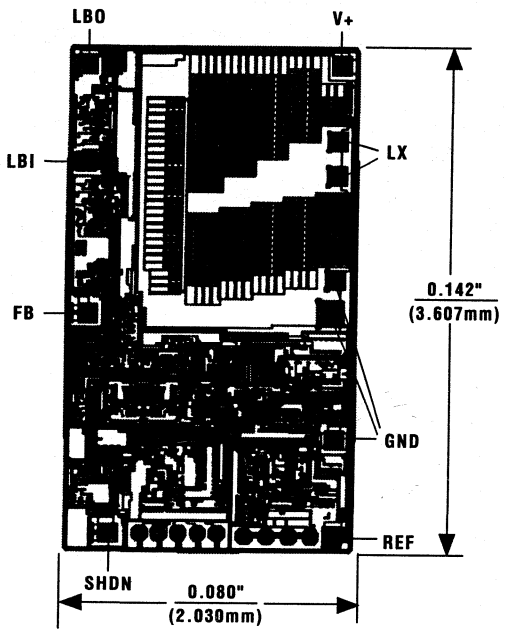
Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CD54-180 (22µH) Coiltronics CTX 100-series	Matsuo 267 series	Nihon EC10 series
Miniature Through-Hole	Sumida RCH855-180M	Sanyo OS-CON series Low-ESR organic semiconductor	Motorola 1N5817, MUR105
Low-Cost Through-Hole	Renco RL 1284-18	Nichicon PL series Low-ESR electrolytics United Chemi-Con LXF series	

Coiltronics	(USA)	(407) 241-7876	FAX (407) 241-9339
Matsuo	(USA)	(714) 969-2491	FAX (714) 960-6492
Matsuo	(Japan)	81-6-337-6450	FAX 81-6-337-6456
Nichicon	(USA)	(708) 843-7500	FAX (708) 843-2798
Nihon	(USA)	(805) 867-2555	FAX (805) 867-2556
Renco	(USA)	(516) 586-5566	FAX (516) 586-5562
Sanyo	(USA)	(619) 661-6835	FAX (619) 661-1055
Sanyo	(Japan)	(0720) 70-1005	FAX (0720) 70-1174
Sumida	(USA)	(708) 956-0666	
Sumida	(Japan)	81-3-607-5111	FAX 81-3-607-5144
United Chem-Con	(USA)	(714) 255-9500	FAX (714) 255-9400

12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converters

Chip Topography



TRANSISTOR COUNT: 492;
SUBSTRATE CONNECTED TO V+.

19-0176; Rev 0; 6/94

EVALUATION KIT AVAILABLE

-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

General Description

The MAX764/MAX765/MAX766 inverting switching regulators are highly efficient over a wide range of load currents, delivering up to 1.5W. A unique, current-limited, pulse-frequency-modulated (PFM) control scheme combines the benefits of traditional PFM converters with the benefits of pulse-width-modulated (PWM) converters. Like PWM converters, the MAX764/MAX765/MAX766 are highly efficient at heavy loads. Yet because they are PFM devices, they use less than 120µA of supply current (vs. 2mA to 10mA for a PWM device).

The input voltage range is 3V to 16V. The output voltage is preset at -5V (MAX764), -12V (MAX765), or -15V (MAX766); it can also be adjusted from -1V to -16V using two external resistors (Dual Mode™). The maximum operating V_{IN} - V_{OUT} differential is 20V.

These devices use miniature external components; their high switching frequencies (up to 300kHz) allow for less than 5mm diameter surface-mount magnetics. A standard 47µH inductor is ideal for most applications, so no magnetics design is necessary.

An internal power MOSFET makes the MAX764/MAX765/MAX766 ideal for minimum component count, low- and medium-power applications. For increased output drive capability or higher output voltages, use the MAX774/MAX775/MAX776 or MAX1774, which drive an external power P-channel MOSFET for loads up to 5W.

Applications

LCD-Bias Generators
Portable Instruments
LAN Adapters
Remote Data-Acquisition Systems
Battery-Powered Applications

Features

- ♦ **High Efficiency for a Wide Range of Load Currents**
- ♦ **250mA Output Current**
- ♦ **120µA Max Supply Current**
- ♦ **5µA Max Shutdown Current**
- ♦ **3V to 16V Input Voltage Range**
- ♦ **-5V (MAX764), -12V (MAX765), -15V (MAX766), or Adjustable Output from -1V to -16V**
- ♦ **Current-Limited PFM Control Scheme**
- ♦ **300kHz Switching Frequency**
- ♦ **Internal, P-Channel Power MOSFET**

Ordering Information

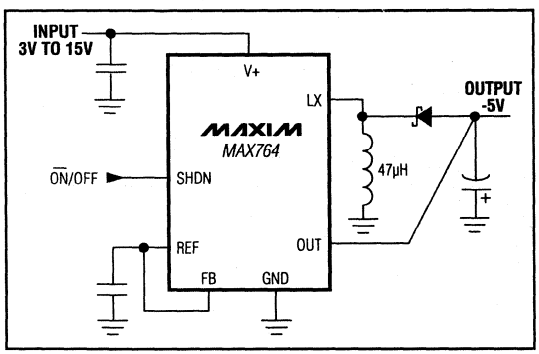
PART	TEMP. RANGE	PIN-PACKAGE
MAX764CPA	0°C to +70°C	8 Plastic DIP
MAX764CSA	0°C to +70°C	8 SO
MAX764C/D	0°C to +70°C	Dice*
MAX764EPA	-40°C to +85°C	8 Plastic DIP
MAX764ESA	-40°C to +85°C	8 SO
MAX764MJA	-55°C to +125°C	8 CERDIP**
MAX765CPA	0°C to +70°C	8 Plastic DIP
MAX765CSA	0°C to +70°C	8 SO
MAX765C/D	0°C to +70°C	Dice*
MAX765EPA	-40°C to +85°C	8 Plastic DIP
MAX765ESA	-40°C to +85°C	8 SO
MAX765MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

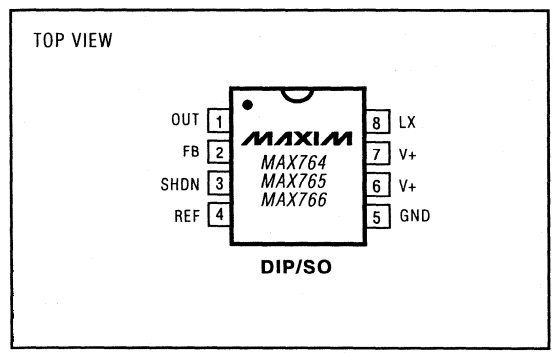
** Dice are tested at T_A = +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +17V
OUT to GND .....+0.5V to -17V
Maximum Differential (V+ to OUT) .....+21V
REF, SHDN, FB to GND .....-0.3V to (V+ + 0.3V)
LX to V+ .....+0.3V to -21V
LX Peak Current 1.5A
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
MAX76_C_A .....0°C to +70°C
MAX76_E_A .....-40°C to +85°C
MAX76_MJA .....-55°C to +125°C
Maximum Junction Temperatures
MAX76_C_A/E_A .....+150°C
MAX76_MJA .....+175°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+	MAX76_C/E		3.0		16.0	V
		MAX76_M		3.5			
Supply Current	I_S	V+ = 16V, SHDN < 0.4V			90	120	µA
Shutdown Current	I_{SHDN}	V+ = 16V, SHDN > 1.6V			2		
		V+ = 10V, SHDN > 1.6V			1	5	
FB Trip Point		3V ≤ V+ ≤ 16V		-10		10	mV
FB Input Current	I_{FB}	MAX76_C				±50	nA
		MAX76_E				±70	
		MAX76_M				±90	
Output Current and Voltage (Note 1)	I_{OUT}	MAX764, -4.8V ≤ V_{OUT} ≤ 5.2V		150	260		mA
		MAX765C/E, -11.52V ≤ V_{OUT} ≤ 12.48V		68	120		
		MAX765M, -11.52V ≤ V_{OUT} ≤ 12.48V		50	120		
		MAX766, -14.40V ≤ V_{OUT} ≤ -15.60V		35	105		
Reference Voltage	V_{REF}	MAX76_C		1.4700	1.5	1.5300	V
		MAX76_E		1.4625	1.5	1.5375	
		MAX76_M		1.4550	1.5	1.5450	
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA	MAX76_C/E		4	10	mV
			MAX76_M		4	15	
REF Line Regulation		3V ≤ V+ ≤ 16V			40	100	µV/V
Load Regulation (Note 2)		0mA ≤ I_{LOAD} ≤ 100mA			0.008		%/mA
Line Regulation (Note 2)		4V ≤ V+ ≤ 6V			0.12		%/V
Efficiency (Note 2)		10mA ≤ I_{LOAD} ≤ 100mA, V_{IN} = 5V	V_{OUT} = -5V		80		%
			V_{OUT} = -15V		82		
SHDN Leakage Current		V+ = 16V, SHDN = 0V or V+				±1	µA
SHDN Input Voltage High	V_{IH}	3V ≤ V+ ≤ 16V		1.6			V
SHDN Input Voltage Low	V_{IL}	3V ≤ V+ ≤ 16V				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

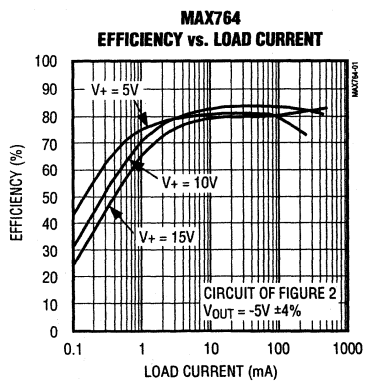
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Leakage Current		|LX| + (V+) ≤ 20V	MAX76_C			±5	µA
			MAX76_E			±10	
			MAX76_M			±30	
LX On-Resistance		|V_{OUT}| + (V+) ≥ 10V			1.4	2.5	Ω
Peak Current at LX	I_{PEAK}	|V_{OUT}| + (V+) ≥ 10V		0.5	0.75		A
Maximum Switch On-Time	t_{ON}			12	16	20	µs
Minimum Switch Off-Time	t_{OFF}			1.8	2.3	2.8	µs

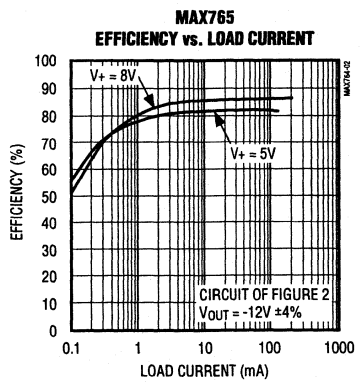
Note 1: See Maximum Output Current vs. Supply Voltage graph in the *Typical Operating Characteristics*. Guarantees are based on correlation to switch on-time, switch off-time, on-resistance, and peak current rating.

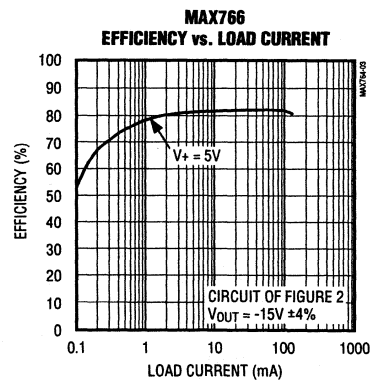
Note 2: Circuit of Figure 2.

Typical Operating Characteristics

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)





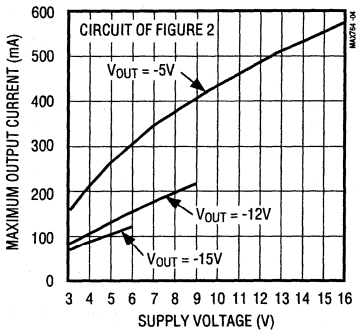


-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

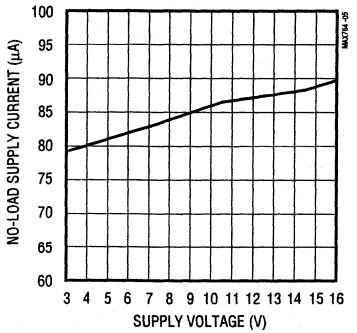
Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

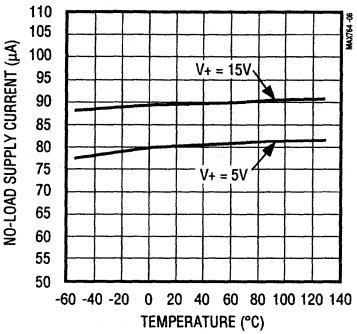
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



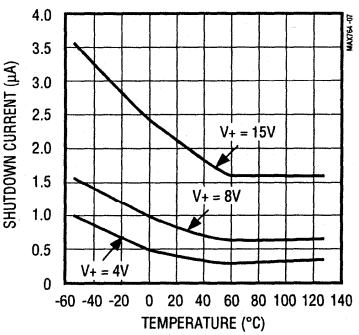
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



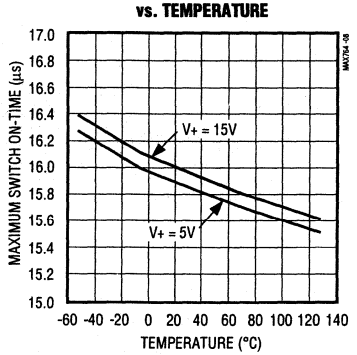
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



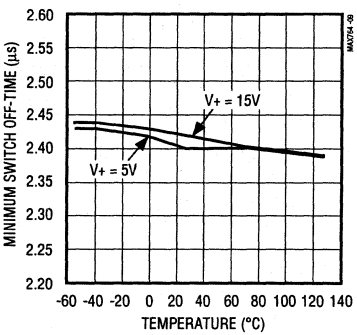
SHUTDOWN CURRENT vs. TEMPERATURE



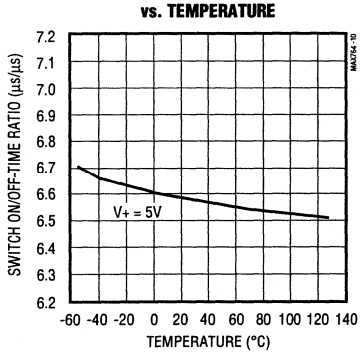
MAXIMUM SWITCH ON-TIME vs. TEMPERATURE



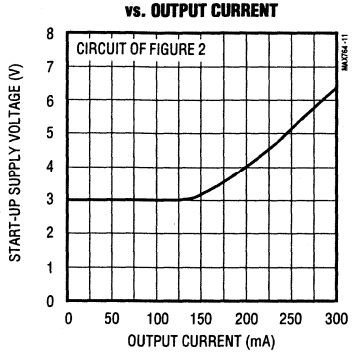
MINIMUM SWITCH OFF-TIME vs. TEMPERATURE



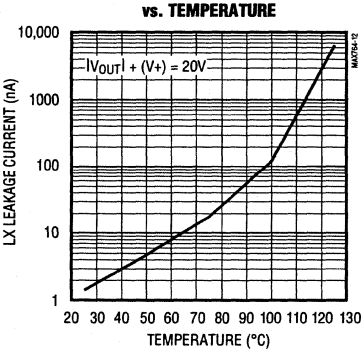
SWITCH ON/OFF-TIME RATIO vs. TEMPERATURE



START-UP SUPPLY VOLTAGE vs. OUTPUT CURRENT



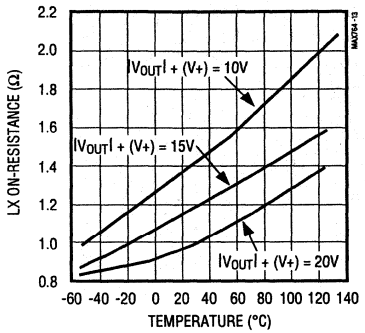
LX LEAKAGE CURRENT vs. TEMPERATURE



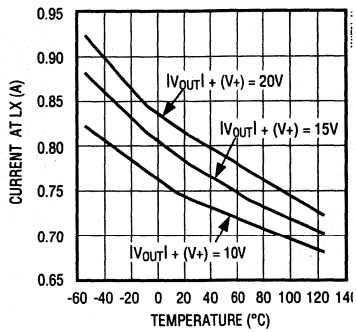
Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

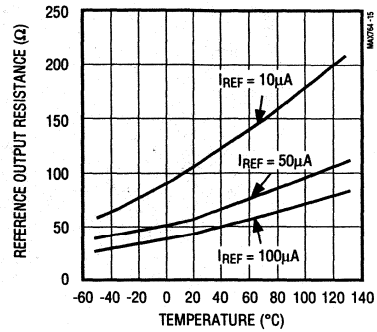
LX ON-RESISTANCE vs. TEMPERATURE



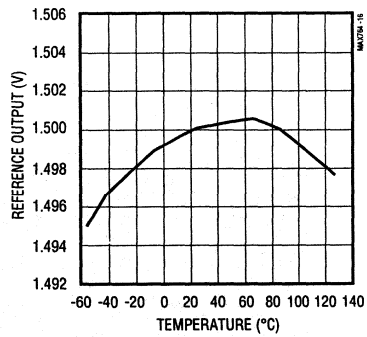
PEAK CURRENT AT LX vs. TEMPERATURE



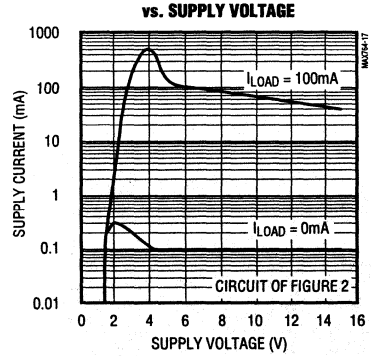
REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE



REFERENCE OUTPUT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

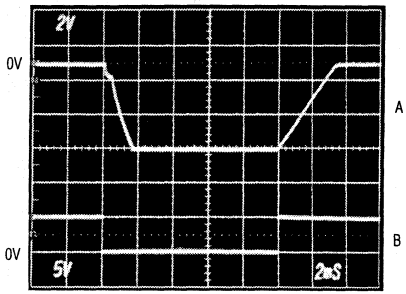


-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

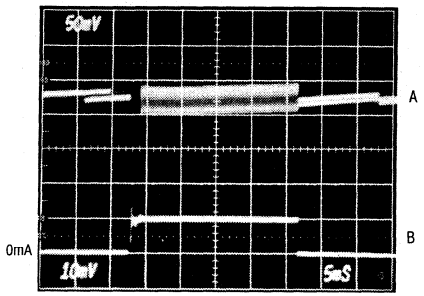
TIME TO ENTER/EXIT SHUTDOWN



2ms/div

CIRCUIT OF FIGURE 2, V+ = 5V, I_{LOAD} = 100mA, V_{OUT} = -5V
A: V_{OUT}, 2V/div
B: SHUTDOWN PULSE, 0V TO 5V, 5V/div

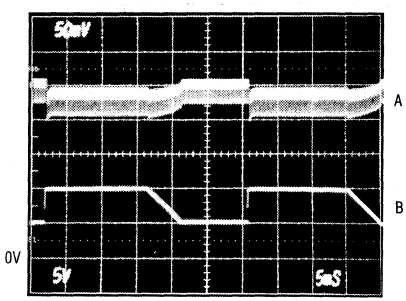
LOAD-TRANSIENT RESPONSE



5ms/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V
A: V_{OUT}, 50mV/div, AC-COUPLED
B: I_{LOAD}, 0mA TO 100mA, 100mA/div

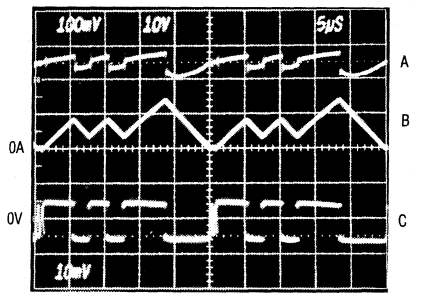
LINE-TRANSIENT RESPONSE



5ms/div

CIRCUIT OF FIGURE 2, V_{OUT} = -5V, I_{LOAD} = 100mA
A: V_{OUT}, 50mV/div, AC-COUPLED
B: V+, 5V TO 10V, 5V/div

DISCONTINUOUS CONDUCTION AT HALF AND FULL CURRENT LIMIT



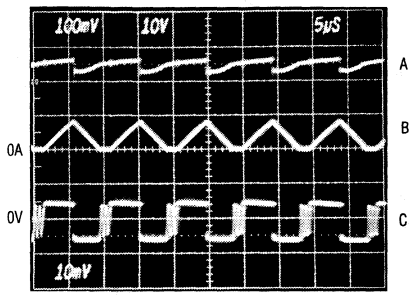
5µs/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V, I_{LOAD} = 140mA
A: OUTPUT RIPPLE, 100mV/div
B: INDUCTOR CURRENT, 500mA/div
C: LX WAVEFORM, 10V/div

Typical Operating Characteristics (continued)

(V+ = 5V, V_{OUT} = -5V, T_A = +25°C, unless otherwise noted.)

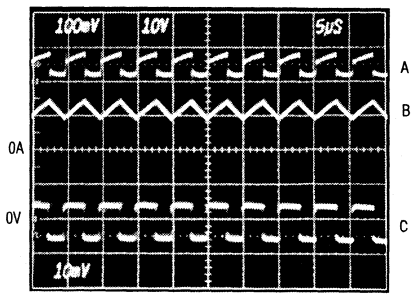
DISCONTINUOUS CONDUCTION AT HALF CURRENT LIMIT



5µs/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V, I_{LOAD} = 80mA
A: OUTPUT RIPPLE, 100mV/div
B: INDUCTOR CURRENT, 500mA/div
C: LX WAVEFORM, 10V/div

CONTINUOUS CONDUCTION AT FULL CURRENT LIMIT



5µs/div

CIRCUIT OF FIGURE 2, V+ = 5V, V_{OUT} = -5V, I_{LOAD} = 240mA
A: OUTPUT RIPPLE, 100mV/div
B: INDUCTOR CURRENT, 500mA/div
C: LX WAVEFORM, 10V/div

Pin Description

PIN	NAME	FUNCTION
1	OUT	Sense Input for Fixed-Output Operation (V_{FB} = V_{REF}). OUT must be connected to V_{OUT}.
2	FB	Feedback Input. Connect FB to REF to use the internal voltage divider for a preset output. For adjustable-output operation, use an external voltage divider, as described in the section *Setting the Output Voltage.*
3	SHDN	Active-High Shutdown Input. With SHDN high, the part is in shutdown mode and the supply current is less than 5µA. Connect to ground for normal operation.
4	REF	1.5V Reference Output that can source 100µA for external loads. Bypass to ground with a 0.1µF capacitor.
5	GND	Ground
6, 7	V+	Positive Power-Supply Input. Must be tied together. **Place a 0.1µF input bypass capacitor as close to the V+ and GND pins as possible.**
8	LX	Drain of the Internal P-Channel Power MOSFET. LX has a peak current limit of 0.75A.

-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

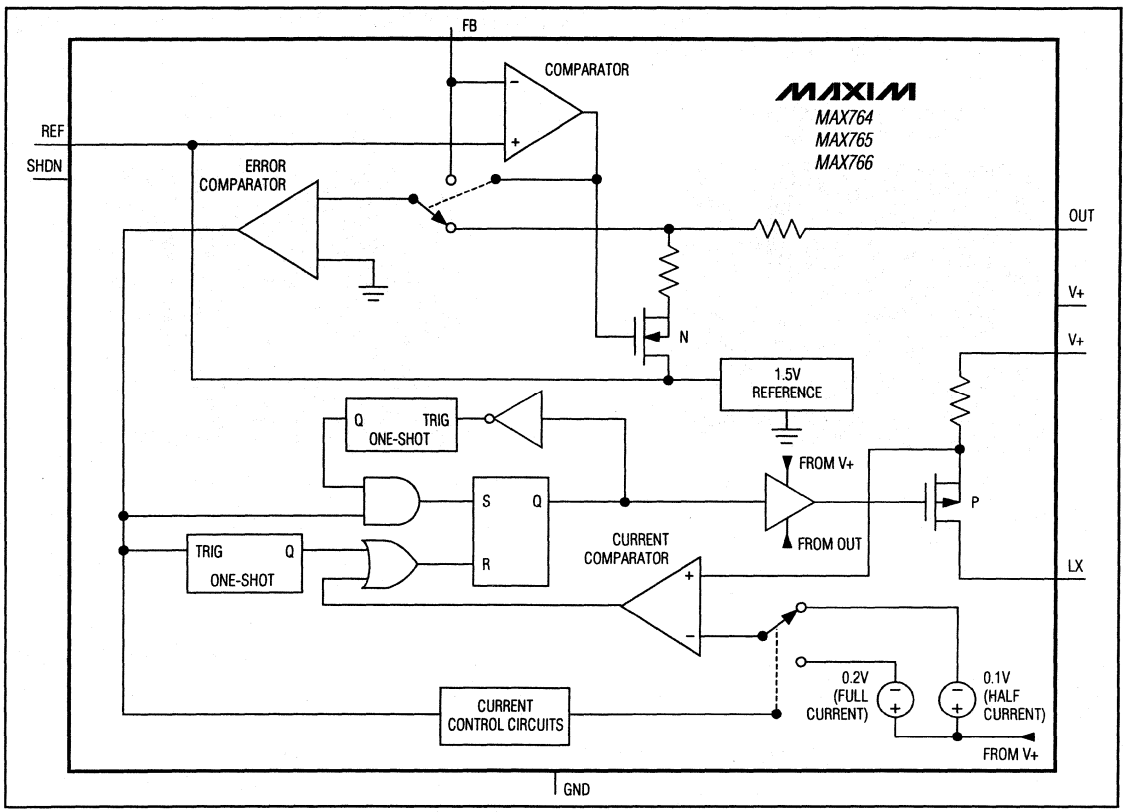


Figure 1. Block Diagram

Detailed Description

Operating Principle

The MAX764/MAX765/MAX766 are BiCMOS, inverting, switch-mode power supplies that provide fixed outputs of -5V, -12V, and -15V, respectively; they can also be set to any desired output voltage using an external resistor divider. Their unique control scheme combines the advantages of pulse-frequency modulation (pulse skipping) and pulse-width modulation (continuous pulsing). The internal P-channel power MOSFET allows peak currents of 0.75A, increasing the output current capability over previous pulse-frequency-modulation (PFM) devices. Figure 1 shows the MAX764/MAX765/MAX766 block diagram.

The MAX764/MAX765/MAX766 offer three main improvements over prior solutions:

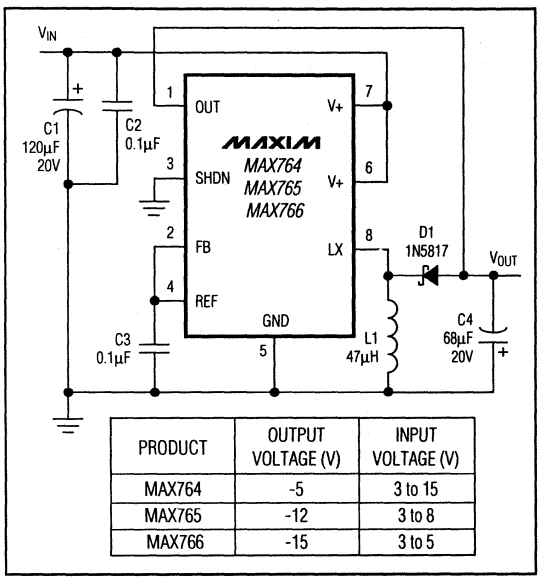
1) They can operate with miniature (less than 5mm diameter) surface-mount inductors, because of their 300kHz switching frequency.
2) The current-limited PFM control scheme allows efficiencies exceeding 80% over a wide range of load currents.
3) Maximum quiescent supply current is only 120µA.

Figures 2 and 3 show the standard application circuits for these devices. In these configurations, the IC is powered from the total differential voltage between the input (V+) and output (V_{OUT}). The principal benefit of this arrangement is that it applies the largest available signal to the gate of the internal P-channel power MOSFET. This increased gate drive lowers switch on-resistance and increases DC-DC converter efficiency.

Since the voltage on the LX pin swings from V+ (when the switch is ON) to $|V_{OUT}|$ plus a diode drop (when the

switch is OFF), the range of input and output voltages is limited to a 21V absolute maximum differential voltage.

When output voltages more negative than -16V are required, substitute the MAX764/MAX765/MAX766 with Maxim's MAX774/MAX775/MAX776 or MAX1774, which use an external switch.



PRODUCT	OUTPUT VOLTAGE (V)	INPUT VOLTAGE (V)
MAX764	-5	3 to 15
MAX765	-12	3 to 8
MAX766	-15	3 to 5

Figure 2. Fixed Output Voltage Operation

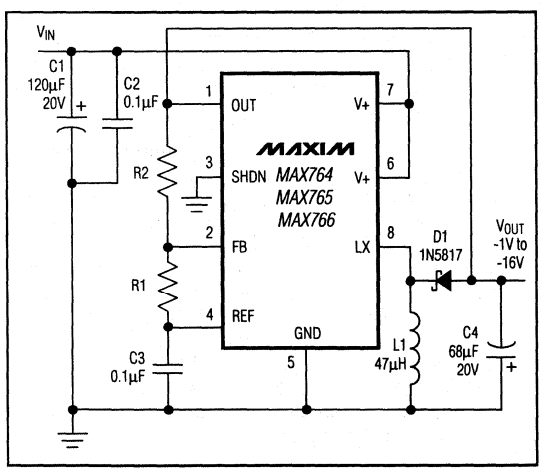


Figure 3. Adjustable Output Voltage Operation

PFM Control Scheme

The MAX764/MAX765/MAX766 use a proprietary, current-limited PFM control scheme that blends the best features of PFM and PWM devices. It combines the ultra-low supply currents of traditional pulse-skipping PFM converters with the high full-load efficiencies of current-mode pulse-width modulation (PWM) converters. This control scheme allows the devices to achieve high efficiencies over a wide range of loads, while the current-sense function and high operating frequency allow the use of miniature external components.

As with traditional PFM converters, the internal power MOSFET is turned on when the voltage comparator senses that the output is out of regulation (Figure 1). However, unlike traditional PFM converters, switching is accomplished through the combination of a peak current limit and a pair of one-shots that set the maximum on-time (16µs) and minimum off-time (2.3µs) for the switch. Once off, the minimum off-time one-shot holds the switch off for 2.3µs. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The MAX764/MAX765/MAX766 limit the peak inductor current, which allows them to run in continuous-conduction mode and maintain high efficiency with heavy loads. (See the photo Continuous Conduction at Full Current Limit in the *Typical Operating Characteristics*.) This current-limiting feature is a key component of the control circuitry. Once turned on, the switch stays on until either 1) the maximum on-time one shot turns it off (16µs later), or 2) the current limit is reached.

To increase light-load efficiency, the current limit is set to half the peak current limit for the first two pulses. If those pulses bring the output voltage into regulation, the voltage comparator holds the MOSFET off and the current limit remains at half the peak current limit. If the output voltage is still out of regulation after two pulses, the current limit is raised to its 0.75A peak for the next pulse. (See the photo Discontinuous Conduction at Half and Full Current Limit in the *Typical Operating Characteristics*.)

Shutdown Mode

When SHDN is high, the MAX764/MAX765/MAX766 enter a shutdown mode in which the supply current drops to less than 5µA. In this mode, the internal biasing circuitry (including the reference) is turned off and OUT discharges to ground. SHDN is a TTL/CMOS-logic level input. Connect SHDN to GND for normal operation. With a current-limited supply, power-up the device while unloaded or in shutdown mode (hold SHDN high until V+ exceeds 3.0V) to save power and reduce power-up current surges. (See the Supply Current vs. Supply Voltage graph in the *Typical Operating Characteristics*.)

-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

Modes of Operation

When delivering high output currents, the MAX764/MAX765/MAX766 operate in continuous-conduction mode. In this mode, current always flows in the inductor, and the control circuit adjusts the duty-cycle of the switch on a cycle-by-cycle basis to maintain regulation without exceeding the switch-current capability. This provides excellent load-transient response and high efficiency.

In discontinuous-conduction mode, current through the inductor starts at zero, rises to a peak value, then ramps down to zero on each cycle. Although efficiency is still excellent, the output ripple may increase slightly.

Design Procedure

Setting the Output Voltage

The MAX764/MAX765/MAX766's output voltage can be adjusted from -1.0V to -16V using external resistors R1 and R2, configured as shown in Figure 3. For adjustable-output operation, select feedback resistor R1 = 150kΩ. R2 is given by:

$$R2 = (R1)\left|\frac{V_{OUT}}{V_{REF}}\right|$$

where V_{REF} = 1.5V.

For fixed-output operation, tie FB to REF.

Inductor Selection

In both continuous- and discontinuous-conduction modes, practical inductor values range from 22µH to 68µH. If the inductor value is too low, the current in the coil will ramp up to a high level before the current-limit comparator can turn off the switch, wasting power and reducing efficiency. The maximum inductor value is not critical. A 47µH inductor is ideal for most applications.

For highest efficiency, use a coil with low DC resistance, preferably under 100mΩ. To minimize radiated noise, use a toroid, pot core, or shielded coil. Inductors with a ferrite core or equivalent are recommended. The inductor's incremental saturation-current rating should be greater than the 0.75A peak current limit. It is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value).

Table 1 lists inductor types and suppliers for various applications. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger-size through-hole inductors.

Diode Selection

The MAX764/MAX765/MAX766's high switching frequency demands a high-speed rectifier. Use a Schottky diode with a 0.75A average current rating, such as the 1N5817 or 1N5818. High leakage currents may make Schottky diodes inadequate for high-temperature and light-load applications. In these cases you can use high-speed silicon diodes, such as the MUR105 or the EC11FS1. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantages of its high leakage current.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor (C4) is low effective series resistance (ESR). The product of the inductor-current variation and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. A 68µF, 20V Sanyo OS-CON capacitor with ESR = 45mΩ (SA series) typically provides 50mV ripple when converting from 5V to -5V at 150mA.

Output filter capacitor ESR also affects efficiency. To obtain optimum performance, use a 68µF or larger, low-ESR capacitor with a voltage rating of at least 20V. The smallest low-ESR surface-mount tantalum capacitors currently available are from the Sprague 595D series. Sanyo OS-CON series organic semiconductors and AVX TPS series tantalum capacitors also exhibit very low ESR. OS-CON capacitors are particularly useful at low temperatures. Table 1 lists some suppliers of low-ESR capacitors.

For best results when using capacitors other than those suggested in Table 1 (or their equivalents), increase the output filter capacitor's size or use capacitators in parallel to reduce ESR.

Input Bypass Capacitor

The input bypass capacitor, C1, reduces peak currents drawn from the voltage source and reduces the amount of noise at the voltage source caused by the switching action of the MAX764–MAX766. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is highly recommended. For output currents up to 250mA, a 100µF to 120µF capacitor with a voltage rating of at least 20V (C1) in parallel with a 0.1µF capacitor (C2) is adequate in most applications. **C2 must be placed as close as possible to the V+ and GND pins.**

Reference Capacitor

Bypass REF with a 0.1µF capacitor (C3). The REF output can source up to 100µA for external loads.

Layout Considerations

Proper PC board layout is essential to reduce noise generated by high current levels and fast switching waveforms. Minimize ground noise by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. In particular, keep the traces connected to FB and LX short. **C2 must be placed as close as possible to the V+ and GND pins.** If an external resistor divider is used (Figure 3), the trace from FB to the resistors must be extremely short.

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CD75/105 series Coiltronics CTX series Coilcraft DT/D03316 series	Matsuo 267 series Sprague 595D/293D series AVX TPS series	Nihon EC10QS02L (Schottky) EC11FS1 (high-speed silicon)
Miniature Through-Hole	Sumida RCH895 series	Sanyo OS-CON series (very low ESR)	Motorola 1N5817, 1N5818, (Schottky) MUR105 (high-speed silicon)
Low-Cost Through-Hole	Renco RL1284 series	Nichicon PL series	

SUPPLIER	PHONE	FAX
AVX	USA: (803) 448-9411	(803) 448-1943
Coilcraft	USA: (708) 639-6400	(708) 639-1469
Coiltronics	USA: (407) 241-7876	(407) 241-9339
Matsuo	USA: (714) 969-2491 Japan: 81-6-337-6450	(714) 960-6492 81-6-337-6456
Motorola	USA: (800) 521-6274	(602) 952-4190
Nichicon	USA: (708) 843-7500 Japan: 81-7-5231-8461	(708) 843-2798 81-7-5256-4158
Nihon	USA: (805) 867-2555 Japan: 81-3-3494-7411	(805) 867-2556 81-3-3494-7414
Renco	USA: (516) 586-5566	(516) 586-5562
Sanyo OS-CON	USA: (619) 661-6835 Japan: 81-7-2070-1005	(619) 661-1055 81-7-2070-1174
Sprague Electric Co.	USA: (603) 224-1961	(603) 224-1430
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	(708) 956-0702 81-3-3607-5144

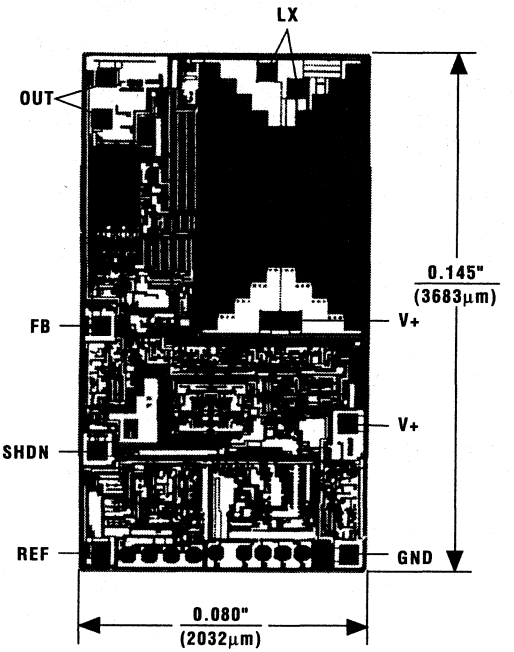
-5V/-12V/-15V or Adjustable, High-Efficiency, Low IQ DC-DC Inverters

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX766CPA	0°C to +70°C	8 Plastic DIP
MAX766CSA	0°C to +70°C	8 SO
MAX766C/D	0°C to +70°C	Dice*
MAX766EPA	-40°C to +85°C	8 Plastic DIP
MAX766ESA	-40°C to +85°C	8 SO
MAX766MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

_____Chip Topography



TRANSISTOR COUNT: 443
SUBSTRATE CONNECTED TO V+

19-0224; Rev 1; 5/94

EVALUATION KIT AVAILABLE

MAXIM

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

General Description

The MAX767 is a high-efficiency, synchronous buck controller IC dedicated to converting a fixed 5V supply into a tightly regulated 3.3V output. Two key features set this device apart from similar, low-voltage step-down switching regulators: high operating frequency and all N-channel construction in the application circuit. The 300kHz operating frequency results in very small, low-cost external surface-mount components.

The inductor, at 3.3µH for 5A, is physically at least five times smaller than inductors found in competing solutions. All N-channel construction and synchronous rectification result in reduced cost and highest efficiency. Efficiency exceeds 90% over a wide range of loading, eliminating the need for heatsinking. Output capacitance requirements are low, reducing board space and cost.

The MAX767 is a monolithic BiCMOS IC available in 20-pin SSOP packages. For other fixed output voltages and package options, please consult the factory.

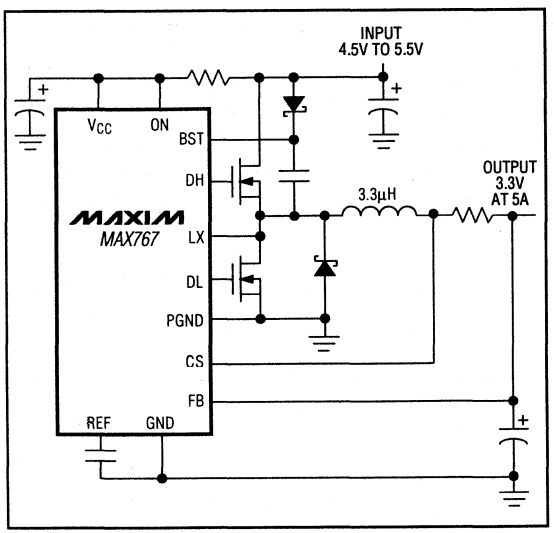
Applications

Local 5V-to-3.3V DC-DC Conversion

Microprocessor Daughterboards

Power Supplies up to 10A or More

Typical Application Circuit



Features

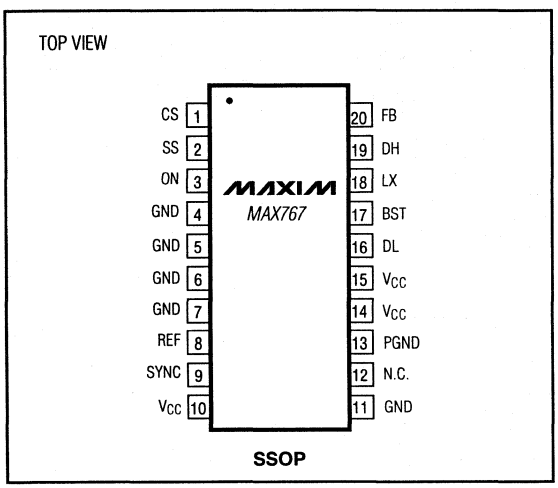
- ♦ **>90% Efficiency**
- ♦ **700µA Quiescent Supply Current**
- ♦ **120µA Standby Supply Current**
- ♦ **4.5V-to-5.5V Input Range**
- ♦ **Low-Cost Application Circuit**
- ♦ **All N-Channel Switches**
- ♦ **Small External Components**
- ♦ **Tiny Shrink-Small-Outline Package (SSOP)**
- ♦ **Predesigned Applications**
- ♦ **Fixed Output Voltages Available:**
  3.3V (Standard)
  3.45V (High-Speed Pentium™)
  3.6V (PowerPC™)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	VOUT
MAX767CAP	0°C to +70°C	20 SSOP	3.3V
MAX767RCAP	0°C to +70°C	20 SSOP	3.45V
MAX767SCAP	0°C to +70°C	20 SSOP	3.6V
MAX767C/D	0°C to +70°C	Dice*	–
MAX767EAP	-40°C to +85°C	20 SSOP	3.3V
MAX767REAP	-40°C to +85°C	20 SSOP	3.45V
MAX767SEAP	-40°C to +85°C	20 SSOP	3.6V

** Contact factory for dice specifications.*

Pin Configuration



™ Pentium is a trademark of Intel. PowerPC is a trademark of IBM.

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V, +7V
PGND to GND .....±2V
BST to GND .....-0.3V, +15V
LX to BST .....-7V, +0.3V
Inputs/Outputs to GND
(ON, REF, SYNC, CS, FB, SS) .....-0.3V, V_{CC} + 0.3V
DL to PGND .....-0.3V, V_{CC} + 0.3V
DH to LX .....-0.3V, BST + 0.3V

REF Short to GND .....Momentary
REF Current 20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges:
MAX767CAP/MAX767_CAP .....0°C to +70°C
MAX767EAP/MAX767_EAP .....-40°C to +85°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = ON = 5V, GND = PGND = SYNC = 0V, I_{REF} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

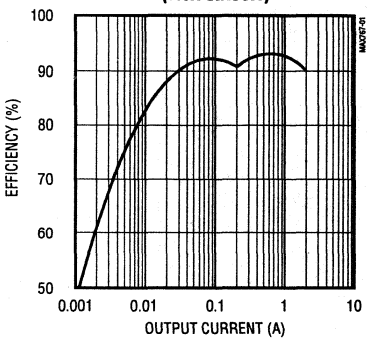
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Input Supply Range			4.5		5.5	V
Output Voltage (FB)	0mV < (CS - FB) < 80mV, 4.5V < V_{CC} < 5.5V (includes load and line regulation)	MAX767	3.17	3.35	3.46	V
		MAX767R	3.32	3.50	3.60	
		MAX767S	3.46	3.65	3.75	
Load Regulation	(CS - FB) = 0mV to 80mV			2.5		%
Line Regulation	V_{CC} = 4.5V to 5.5V			0.1		%
V_{CC} Fault Lockout Voltage	Falling edge, hysteresis = 1%		3.80		4.20	V
Current-Limit Voltage	CS - FB		80	100	120	mV
SS Source Current			2.50	4	6.5	µA
SS Fault Sink Current			2			mA
REF Output Voltage	No external load		3.24	3.30	3.36	V
V_{CC} Standby Current	ON = 0V, V_{CC} = 5.5V			120	200	µA
V_{CC} Quiescent Current	FB = CS = 3.5V			0.7	1.0	mA
Oscillator Frequency	SYNC = 3.3V		260	300	340	kHz
	SYNC = 0V or 5V			200		
Oscillator SYNC Range			240		350	kHz
SYNC High Pulse Width			200			ns
SYNC Low Pulse Width			200			ns
SYNC Rise/Fall Time	Not tested				200	ns
Oscillator Maximum Duty Cycle	SYNC = 3.3V		89	92		%
	SYNC = 0V			95		
Input Low Voltage	SYNC, ON				0.8	V
Input High Voltage	ON		2.40			V
	SYNC		V_{CC} - 0.5			
Input Current	SYNC, ON = 0V or 5V				±1	µA
DL Sink/Source Current	DL = 2V			1		A
DH Sink/Source Current	(BST - LX) = 4.5V, DH = 2V			1		A
DL On Resistance	High or low				7	Ω
DH On Resistance	High or low, (BST - LX) = 4.5V				7	Ω

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

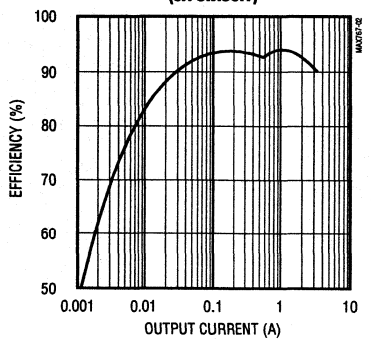
Typical Operating Characteristics

(Circuit of Figure 1 (5A configuration), V_{IN} = 5V, oscillator frequency = 300kHz, T_A = +25°C, unless otherwise noted.)

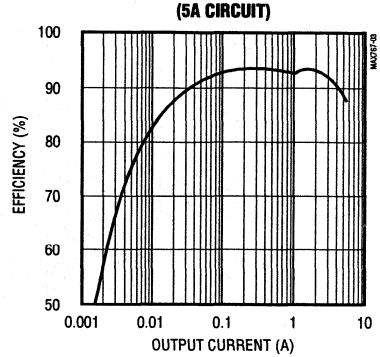
EFFICIENCY vs. OUTPUT CURRENT (1.5A CIRCUIT)



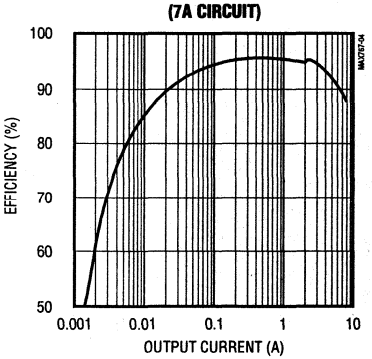
EFFICIENCY vs. OUTPUT CURRENT (3A CIRCUIT)



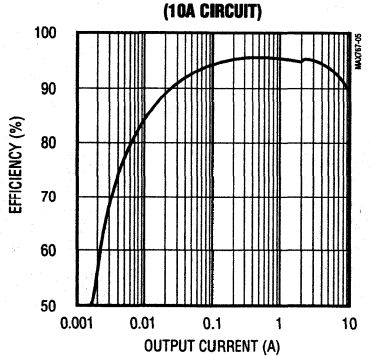
EFFICIENCY vs. OUTPUT CURRENT (5A CIRCUIT)



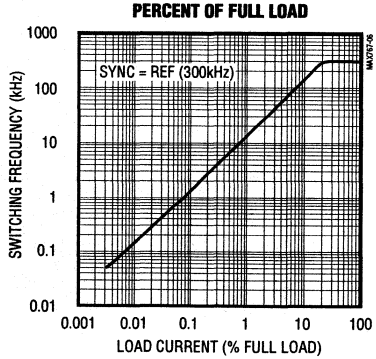
EFFICIENCY vs. OUTPUT CURRENT (7A CIRCUIT)



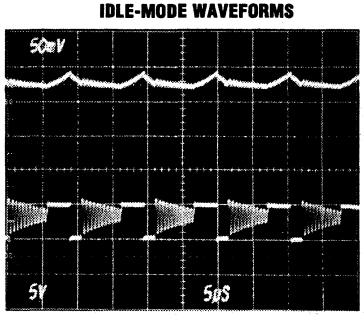
EFFICIENCY vs. OUTPUT CURRENT (10A CIRCUIT)



SWITCHING FREQUENCY vs. PERCENT OF FULL LOAD



IDLE-MODE WAVEFORMS

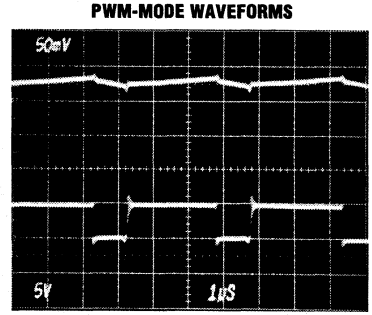


3.3V OUTPUT
50mV/div, AC COUPLED

LX
5V/div

5µs/div
I_{LOAD} = 300mA

PWM-MODE WAVEFORMS



3.3V OUTPUT
50mV/div, AC COUPLED

LX
5V/div

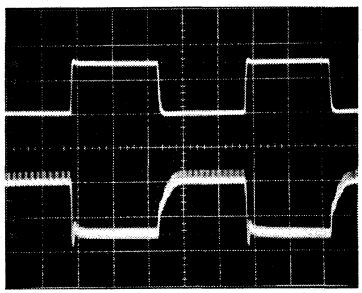
1µs/div
I_{LOAD} = 5A

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

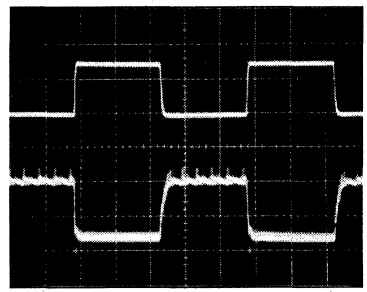
Typical Operating Characteristics (continued)

(Circuit of Figure 1 (5A configuration), V_{IN} = 5V, oscillator frequency = 300kHz, T_A = +25°C, unless otherwise noted.)

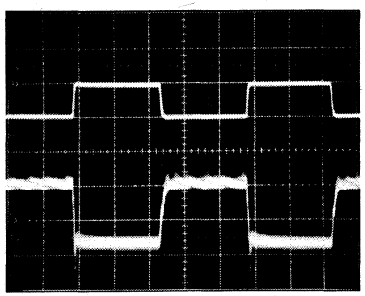
1.5A CIRCUIT LOAD-TRANSIENT RESPONSE



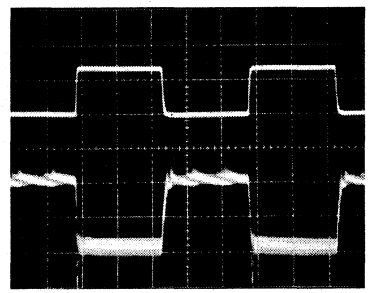
3A CIRCUIT LOAD-TRANSIENT RESPONSE



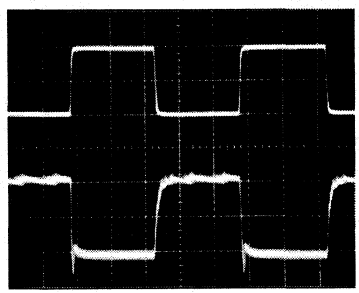
5A CIRCUIT LOAD-TRANSIENT RESPONSE



7A CIRCUIT LOAD-TRANSIENT RESPONSE



10A CIRCUIT LOAD-TRANSIENT RESPONSE



5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

Pin Description

PIN	NAME	FUNCTION
1	CS	Current-sense input: +100mV = nominal current-limit level referred to FB.
2	SS	Soft-start input. Ramp time to full current limit is 1ms/nF of capacitance to GND.
3	ON	ON/$\overline{OFF}$ control input to disable the PWM. Tie directly to V_{CC} for automatic start-up.
4–7, 11	GND	Low-current analog ground. Feedback reference point for the output.
8	REF	3.3V internal reference output. Bypass to GND with 0.22µF minimum capacitor.
9	SYNC	Oscillator control/synchronization input. Connect to V_{CC} or GND for 200kHz; connect to REF for 300kHz. For external clock synchronization in the 240kHz to 350kHz range, a high-to-low transition causes a new cycle to start.
10, 14, 15	V_{CC}	Supply voltage input: 4.5V to 5.5V
12	N.C.	No internal connection
13	PGND	Power ground
16	DL	Gate-drive output for the low-side synchronous rectifier MOSFET
17	BST	Boost capacitor connection (0.1µF)
18	LX	Inductor connection. Can swing 2V below GND without latchup.
19	DH	Gate-drive output for the high-side MOSFET
20	FB	Feedback and current-sense input for the PWM

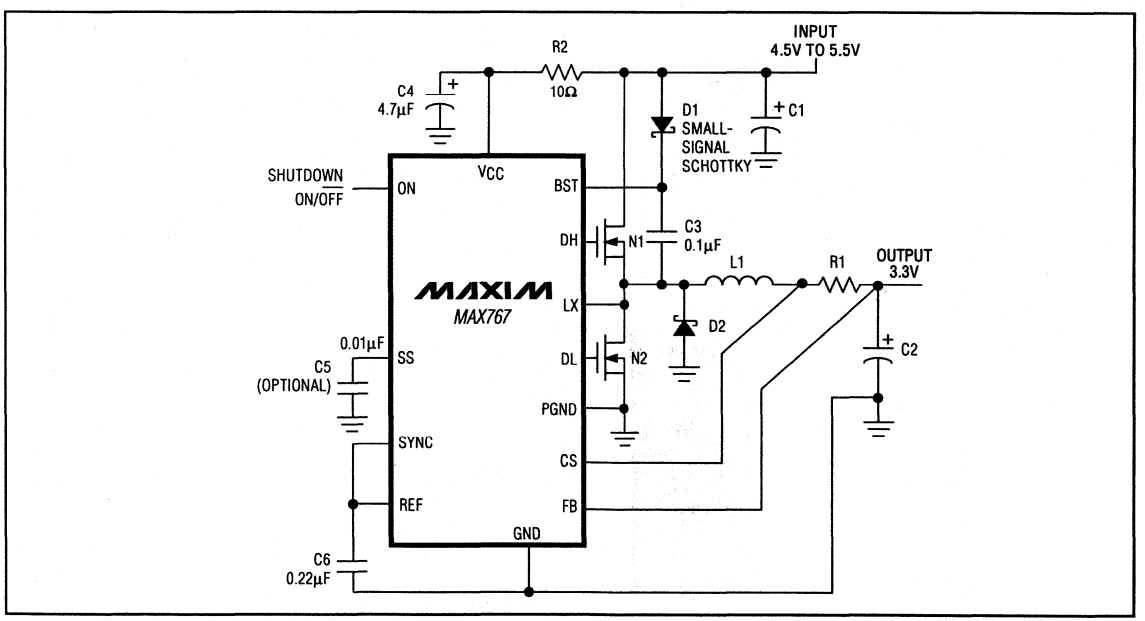


Figure 1. Standard Application Circuit

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

Standard Application Circuits

This data sheet shows five predesigned circuits with output current capabilities from 1.5A to 10A. Many users will find one of these standard circuits appropriate for their needs. If a standard circuit is used, the remainder of this data sheet (*Detailed Description* and *Applications Information and Design Procedure*) can be bypassed.

Figure 1 shows the Standard Application Circuit. Table 1 gives component values and part numbers for five different implementations of this circuit: 1.5A, 3A, 5A, 7A, and 10A output currents.

Each of these circuits is designed to deliver the full rated output load current over the temperature range listed. In addition, each will withstand a short circuit of several seconds duration from the output to ground. If the circuit must withstand a continuous short circuit, refer to the *Short-Circuit Duration* section for the required changes.

Layout and Grounding

Good layout is necessary to achieve the designed output power, high efficiency, and low noise. Good layout includes the use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths. The following points are in order of decreasing importance.

1. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multilayer board and full use of the four or more copper layers is recommended. Use the top and bottom layers for interconnections and the inner layers for an uninterrupted ground plane.
2. Because the sense resistance values are similar to a few centimeters of narrow traces on a printed circuit board, trace resistance can contribute significant errors. To prevent this, Kelvin connect CS and FB to the sense resistor; i.e., use separate traces not carrying any of the inductor or load current, as shown in Figure 2. These signals must be carefully shielded from DH, DL, BST, and the LX node. **Important: place the sense resistor as close as possible to and no further than 10mm from the MAX767.**
3. Place the LX node components N1, N2, L1, and D2 as close together as possible. This reduces resistive and switching losses and confines noise due to ground inductance.
4. The input filter capacitor C1 should be less than 10mm away from N1's drain. The connecting copper trace carries large currents and must be at least 2mm wide, preferably 5mm.
5. Keep the gate connections to the MOSFETs short for low inductance (less than 20mm long and more than 0.5mm wide) to ensure clean switching.
6. To achieve good shielding, it is best to keep all switching signals (MOSFET gate drives DH and DL, BST, and the LX node) on one side of the board and all sensitive nodes (CS, FB, and REF) on the other side.
7. Connect the GND and PGND pins directly to the ground plane, which should ideally be an inner layer of a multilayer board.

Detailed Description

Note: *The remainder of this document contains the detailed information necessary to design a circuit that differs substantially from the five standard application circuits. If you are using one of the predesigned standard circuits, the following sections are provided only for your reading pleasure.*

The MAX767 converts a 4.5V to 5.5V input to a 3.3V output. Its load capability depends on external components and can exceed 10A. The 3.3V output is generated by a current-mode, pulse-width-modulation (PWM) step-down regulator. The PWM regulator operates at either 200kHz or 300kHz, with a corresponding tradeoff between somewhat higher efficiency (200kHz) and smaller external component size (300kHz). The MAX767 also has a 3.3V, 5mA reference voltage. Fault-protection circuitry shuts off the output should the reference lose regulation or the input voltage go below 4V (nominally).

External components for the MAX767 include two N-channel MOSFETs, a rectifier, and an LC output filter. The gate-drive signal for the high-side MOSFET, which must exceed the input voltage, is provided by a boost circuit that uses a 0.1µF capacitor. The synchronous rectifier keeps efficiency high by clamping the voltage across the rectifier diode. An external low-value current-sense resistor sets the maximum current limit, preventing excessive inductor current during start-up or under short-circuit conditions. An optional external capacitor sets the programmable soft-start, reducing in-rush surge currents upon start-up and providing adjustable power-up time.

The PWM regulator is a direct-summing type, lacking a traditional integrator-type error amplifier and the phase shift associated with it. It therefore does not require external feedback-compensation components, as long as you follow the ESR guidelines in the *Applications Information and Design Procedure* sections.

Table 1. Component Values

Part	1.5A Circuit	3A Circuit	5A Circuit	7A Circuit	10A Circuit
L1	10µH Sumida CDR74B-100	5µH Sumida CDR125 DRG# 4722-JPS-001	3.3µH CoilCraft DO3316-332	2.1µH, 5mΩ Coiltronics CTX03-12338-1	1.5µH, 3.5mΩ Coiltronics CTX03-12357-1
R1	0.04Ω IRC LR2010-01-R040 or Dale WSL-2512-R040	0.02Ω IRC LR2010-01-R020 or Dale WSL-2512-R020	0.012Ω Dale WSL-2512-R012 or 2 x 0.025Ω IRC LR2010-01-R025 (in parallel)	3 x 0.025Ω IRC LR2010-01-R025 or Dale WSL-2512-R025 (in parallel)	3 x 0.020Ω IRC LR2010-01-R020 or 2 x 0.012Ω Dale WSL-2512-R012 (in parallel)
N1, N2	International Rectifier IRF7101, Siliconix Si9936DY or Motorola MMDF3N03HD (dual N-channel)	Siliconix Si9410DY, International Rectifier IRF7101 or Motorola MMDF3N03HD (both FETs in parallel)	Motorola MTD20N03HDL	Motorola MTD20N03HDL (N1 = 2 in parallel, N2 = 1 FET)	Motorola MTD20N03HDL (N1 = 3 in parallel, N2 = 2 in parallel)
C1	47µF, 20V AVX TPSD476K020R	2 x 47µF, 20V AVX TPSD476K020R	220µF, 10V Sanyo OS-CON 10SA220M	2 x 100µF, 10V Sanyo OS-CON 10SA100M	2 x 220µF, 10V Sanyo OS-CON 10SA220M
C2	220µF, 6.3V Sprague 595D227X06R3D2B	2 x 150µF, 10V Sprague 595D157X0010D7T	2 x 220µF, 10V Sanyo OS-CON 10SA220M	2 x 220µF, 10V Sanyo OS-CON 10SA220M	4 x 220µF, 10V Sanyo OS-CON 10SA220M
D2	1N5817 Nihon EC10QS02, or Motorola MBRS120T3	1N5817 Nihon EC10QS02, or Motorola MBRS120T3	1N5820 Nihon NSQ03A02, or Motorola MBRS340T3	1N5820 Nihon NSQ03A02, or Motorola MBRS340T3	1N5820 Nihon NSQ03A02, or Motorola MBRS340T3
Temp. Range	to +85°C	to +85°C	to +85°C	to +85°C	to +85°C

Table 2. Component Suppliers

Company	Factory Fax [Country Code]	USA Telephone
AVX	[1] (207) 283-1941	(800) 282-4975
CoilCraft	[1] (708) 639-1469	(708) 639-6400
Coiltronics	[1] (407) 241-9339	(407) 241-7876
Dale	[1] (402) 563-6418	(402) 563-6582
IRC	[1] (512) 992-3377	(512) 992-7900
International Rectifier	[1] (310) 322-3332	(310) 322-3331
Motorola	[1] (602) 244 4015	(602) 244- 3576
Nihon	[81] 3-3494-7414	(805) 867-2555
Sanyo	[81] 7-2070-1174	(619) 661-6835
Siliconix	[1] (408) 970-3950	(408) 988-8000
Sprague	[1] (603) 224-1430	(603) 224-1961
Sumida	[81] 3-3607-5144	(708) 956-0666

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

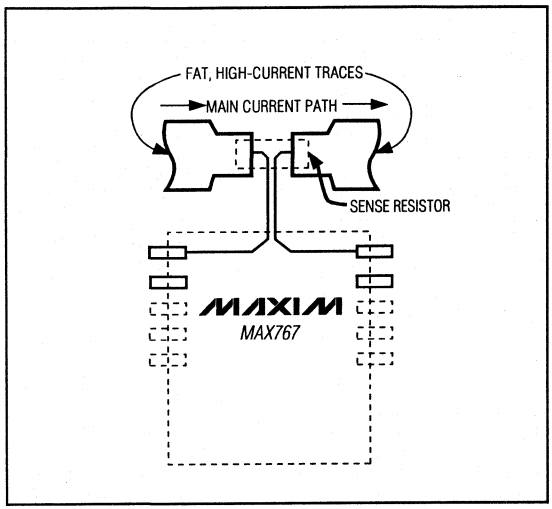


Figure 2. Kelvin Connections for the Current-Sense Resistor

The main gain block is an open-loop comparator that sums four signals: output voltage error signal, current-sense signal, slope-compensation ramp, and the 3.3V reference. This direct-summing method approaches the ideal of cycle-by-cycle control of the output voltage. Under heavy loads, the controller operates in full PWM mode. Every pulse from the oscillator sets the output latch and turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}).

As the high-side switch turns off, the synchronous rectifier latch is set; 60ns later, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle (in continuous-conduction mode) or until the inductor current reaches zero (in discontinuous-conduction mode). Under fault conditions where the inductor current exceeds the 100mV current-limit threshold, the high-side latch resets and the high-side switch turns off.

At light loads, the inductor current fails to exceed the 25mV threshold set by the minimum-current comparator. When this occurs, the PWM goes into Idle-Mode™, skipping most of the oscillator pulses to reduce the switching frequency and cut back switching losses. The oscillator is effectively gated off at light loads because the minimum-current comparator immediately resets the high-side latch at the beginning of each cycle, unless the FB signal falls below the reference voltage level.

Soft-Start

Connecting a capacitor from the soft-start pin (SS) to ground allows a gradual build-up of the 3.3V output after power is applied or ON is driven high. When ON is low, the soft-start capacitor is discharged to GND. When ON is driven high, a 4µA constant current source charges the capacitor up to 4V. The resulting ramp voltage on SS linearly increases the current-limit comparator set-point, increasing the duty cycle to the external power MOSFETs. With no soft-start capacitor, the full output current is available within 10µs (see *Applications Information and Design Procedure* section).

Synchronous Rectifier

Synchronous rectification allows for high efficiency by reducing the losses associated with the Schottky rectifier. Also, the synchronous-rectifier MOSFET is necessary for correct operation of the MAX767's boost gate-drive supply.

When the external power MOSFET (N1) turns off, energy stored in the inductor causes its terminal voltage to reverse instantly. Current flows in the loop formed by the inductor (L1), Schottky diode (D2), and the load—an action that charges up the output filter capacitor (C2). The Schottky diode has a forward voltage of about 0.5V which, although small, represents a significant power loss and degrades efficiency. The synchronous-rectifier MOSFET parallels the diode and is turned on by DL shortly after the diode conducts. Since the synchronous rectifier's on resistance ($r_{DS(ON)}$) is very low, the losses are reduced. The synchronous-rectifier MOSFET is turned off when the inductor current falls to zero.

The MAX767's internal break-before-make timing ensures that shoot-through (both external switches turned on at the same time) does not occur. The Schottky rectifier conducts during the time that neither MOSFET is on, which improves efficiency by preventing the synchronous-rectifier MOSFET's lossy body diode from conducting.

The synchronous rectifier works under all operating conditions, including discontinuous-conduction mode and idle-mode.

™ Idle-Mode is a trademark of Maxim Integrated Products.

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

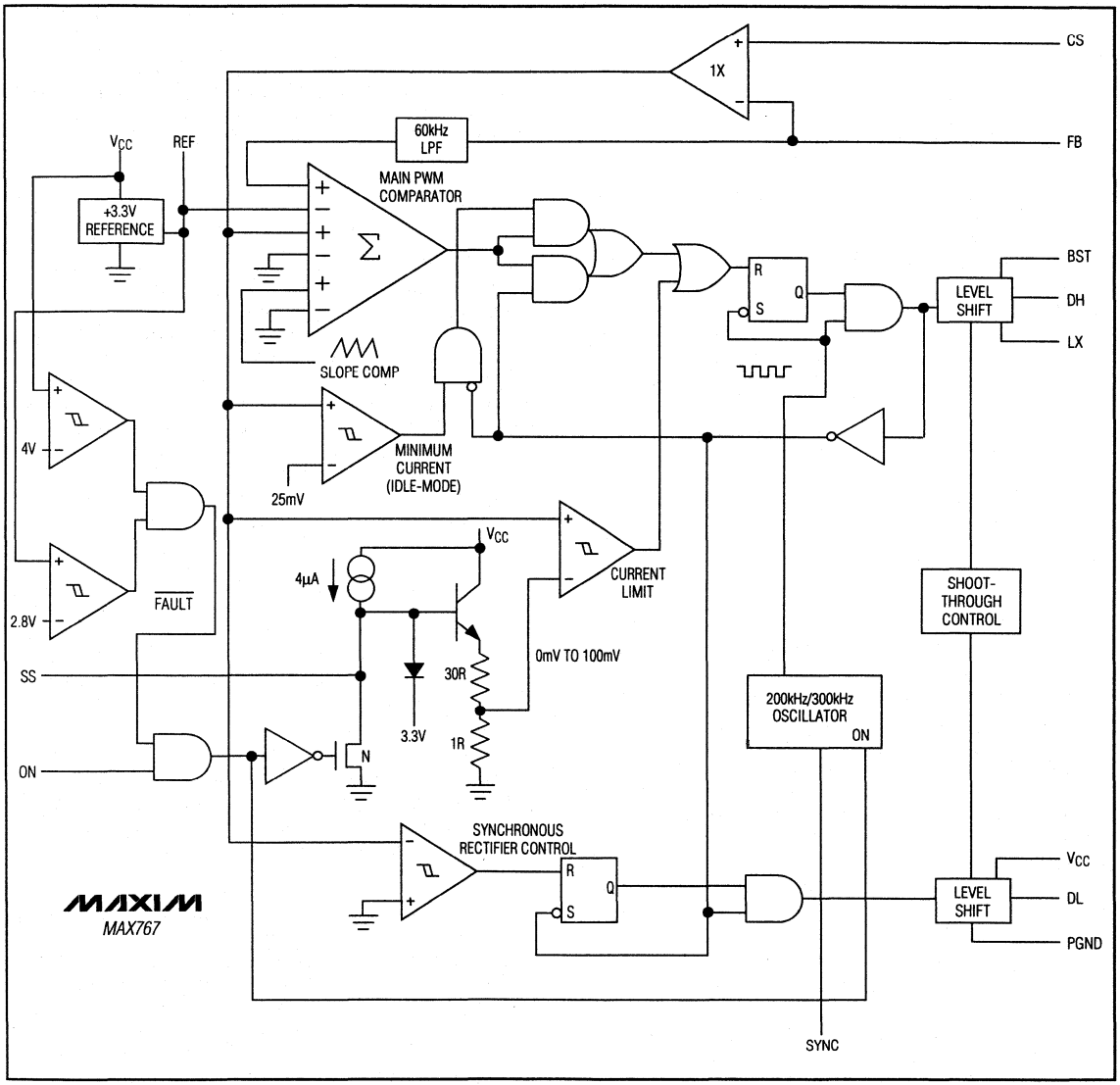


Figure 3. MAX767 Block Diagram

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

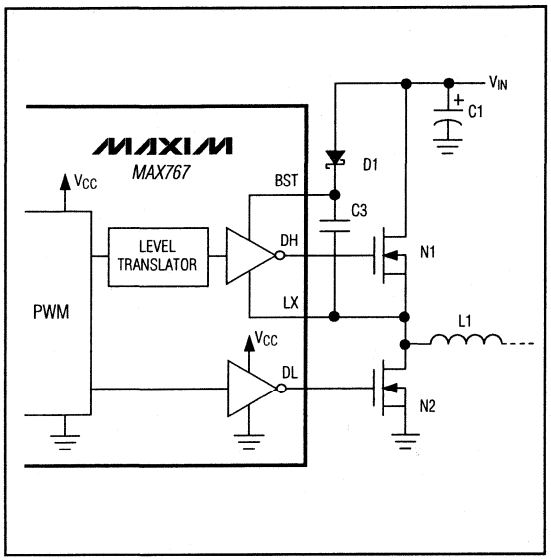


Figure 4. Boost Supply for High-Side Gate Driver

Gate-Driver Boost Supply

Gate-drive voltage for the high-side N-channel switch is generated with the flying-capacitor boost circuit shown in Figure 4. The capacitor (C3) is alternately charged from the 5V input via the diode (D1) and placed in parallel with the high-side MOSFET's gate-source terminals. On start-up, the synchronous rectifier (low-side) MOSFET (N2) forces LX to 0V and charges the BST capacitor to 5V. On the second half-cycle, the PWM turns on the high-side MOSFET (N1); it does this by closing an internal switch between BST and DH, which connects the capacitor to the MOSFET gate. This provides the necessary enhancement voltage to turn on the high-side switch, an action that "boosts" the 5V gate-drive signal above the input voltage.

Ringing seen at the high-side MOSFET gates (DH) in discontinuous-conduction mode (light loads) is a natural operating condition. It is caused by the residual energy in the tank circuit, formed by the inductor and stray capacitance at the LX node. The gate-driver negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive supply.

Modes of Operation

PWM Mode

Under heavy loads—over approximately 25% of full load—the supply operates as a continuous-current PWM supply (see *Typical Operating Characteristics*). The duty cycle, %ON, is approximately:

$$\%ON = \frac{V_{OUT}}{V_{IN}}$$

Current flows continuously in the inductor: first, it ramps up when the power MOSFET conducts; second, it ramps down during the flyback portion of each cycle as energy is put into the inductor and then discharged into the load. Note that the current flowing into the inductor when it is being charged is also flowing into the load, so the load is continuously receiving current from the inductor. This minimizes output ripple and maximizes inductor use, allowing very small physical and electrical sizes. Output ripple is primarily a function of the filter capacitor's effective series resistance (ESR), and is typically under 50mV (see *Design Procedure* section).

Idle-Mode

Under light loads (<25% of full load), the MAX767 enhances efficiency by turning the drive voltage on and off for only a single clock period, skipping most of the clock pulses entirely. Asynchronous switching, seen as "ghosting" on an oscilloscope, is thus a normal operating condition whenever the load current is less than approximately 25% of full load.

At certain input voltage and load conditions, a transition region exists where the controller can pass back and forth from idle-mode to PWM mode. In this situation, short pulse bursts occur, which make the current waveform look erratic but do not materially affect the output ripple. Efficiency remains high.

Current Limiting

The voltage between CS and FB is continuously monitored. An external, low-value shunt resistor is connected between these pins, in series with the inductor, allowing the inductor current to be continuously measured throughout the switching cycle. Whenever this voltage exceeds 100mV, the drive voltage to the external high-side MOSFET is cut off. This protects the MOSFET, the load, and the input supply in case of short circuits or temporary load surges. The current-limiting resistance is typically 20mΩ for 3A.

Oscillator Frequency

The SYNC input controls the oscillator frequency. Connecting SYNC to GND or to V_{CC} selects 200kHz operation; connecting it to REF selects 300kHz operation. SYNC can also be driven with an external 240kHz to 350kHz CMOS/TTL source to synchronize the internal oscillator. Normally, 300kHz operation is chosen to minimize the inductor and output filter capacitor sizes, but 200kHz operation may be chosen for a small (about 1%) increase in efficiency at heavy loads.

Internal Reference

The internal 3.3V bandgap reference (REF) remains active, even when the switching regulator is turned off. It can furnish up to 5mA, and can be used to supply memory keep-alive power or for other purposes. Bypass REF to GND with 0.22µF, plus 1µF/mA of load current.

Applications Information and Design Procedure

Most users will be able to work with one of the standard application circuits; others may want to implement a circuit with an output current rating that lies between or beyond the standard values.

If you want an output current level that lies between two of the standard application circuits, you can interpolate many of the component values from the values given for the two circuits. These components include the input and output filter capacitors, the inductor, and the sense resistor. The capacitors must meet ESR and ripple current requirements (see *Input Filter Capacitor* and *Output Filter Capacitor* sections). The inductor must meet the required current rating (see *Inductor* section).

You may use the rectifier and MOSFETs specified for the circuit with the greater output current capability, or choose a new rectifier and MOSFETs according to the requirements detailed in the *Rectifier* and *MOSFET Switches* sections. For more complete information, or for output currents in excess of 10A, refer to the design information in the following sections.

Inductor, L1

Three inductor parameters are required: the inductance value (L), the peak inductor current (I_{LPEAK}), and the coil resistance (R_L). The inductance is:

$$L1 = \frac{1.32}{f \times I_{OUT} \times LIR}$$

where:

f = switching frequency, normally 300kHz

I_{OUT} = maximum 3.3V DC load current (A)

LIR = ratio of inductor peak-to-peak AC current to average DC load current, typically 0.3.

A higher LIR value allows smaller inductance, but results in higher losses and ripple.

The highest peak inductor current (I_{LPEAK}) equals the DC load current (I_{OUT}) plus half the peak-to-peak AC inductor current (I_{LPP}). The peak-to-peak AC inductor current is typically chosen as 30% of the maximum DC load current, so the peak inductor current is 1.15 x I_{OUT}.

The peak inductor current at any load is given by:

$$I_{LPEAK} = I_{OUT} + \frac{1.32}{2 \times f \times L1}$$

The coil resistance should be as low as possible, preferably in the low milliohms. The coil is effectively in series with the load at all times, so the wire losses alone are approximately:

$$\text{Power Loss} = I_{OUT}^2 \times R_L$$

In general, select a standard inductor that meets the L, I_{LPEAK}, and R_L requirements. If a standard inductor is unavailable, choose a core with an LI^2 parameter greater than $L \times I_{LPEAK}^2$, and use the largest wire that will fit the core.

Current-Sense Resistor, R1

The current-sense resistor must carry the peak current in the inductor, which exceeds the full DC load current. The internal current limiting starts when the voltage across the sense resistors exceeds 100mV nominally, 80mV minimum. Use the minimum value to ensure adequate output current capability: R1 = 80mV / I_{LPEAK}.

The low V_{IN}/V_{OUT} ratio creates a potential problem with start-up under full load or with load transients from no-load to full load. If the supply is subjected to these conditions, reduce the sense resistor:

$$R1 = \frac{70mV}{I_{LPEAK}}$$

Since the sense-resistance values are similar to a few centimeters of narrow traces on a printed circuit board, trace resistance can contribute significant errors. To prevent this, Kelvin connect the CS and FB pins to the sense resistors; i.e., use separate traces not carrying any of the inductor or load current, as shown in Figure 2.

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

Place R1 as close as possible to the MAX767, preferably less than 10mm. Run the traces at minimum spacing from one another. If they are longer than 20mm, bypass CS to FB with a 1nF capacitor placed as close as possible to these pins. The wiring layout for these traces is critical for stable, low-ripple outputs (see *Layout and Grounding* section).

Input Filter Capacitor, C1

Use at least 6µF per watt of output power for C1. If the 5V input is some distance away or comes through a PC bus, greater capacitance may be desirable to improve the load-transient response. Use a low-ESR capacitor located no further than 10mm from the MOSFET switch (N1) to prevent ringing. The ripple current rating must be at least $I_{RMS} = 0.5 \times I_{OUT}$. For high-current applications, two or more capacitors in parallel may be needed to meet these requirements.

The ESR of C1 is effectively in series with the input. The resistive dissipation of C1, $I_{RMS}^2 \times ESR_{C1}$, can significantly impact the circuit's efficiency.

Output Filter Capacitor, C2

The output filter capacitor determines the loop stability, output voltage ripple, and output load-transient response.

Stability

To ensure stability, stay above the minimum capacitance value and below the maximum ESR value. These values are:

$$C2 > \frac{3\Omega}{R1}\ \mu F$$

and

$$ESR_{C2} < R1$$

Be sure to satisfy both these requirements. To achieve the low ESR required, it may be appropriate to parallel two or more capacitors and/or use a total capacitance 2 or 3 times larger than the calculated minimum.

Output Ripple

The output ripple in continuous-conduction mode is:

$$V_{OUT(RPL)} = I_{OUT(max)} \times LIR \times \left(ESR_{C2} + \frac{1}{2 \times \pi \times f \times C2}\right)$$

where f is the switching frequency (200kHz or 300kHz).

In idle-mode, the ripple has a capacitive and a resistive component:

$$V_{OUT(RPL)}(C) = \frac{0.0004 \times L}{R1^2 \times C2} \times 0.89\ Volts$$

$$V_{OUT(RPL)}(R) = \frac{0.02 \times ESR_{C2}}{R1}$$

The total ripple, $V_{OUT(RPL)}$, can be approximated as follows:

if

$$V_{OUT(RPL)}(R) < 0.5\ V_{OUT(RPL)}(C)$$

then

$$V_{OUT(RPL)} = V_{OUT(RPL)}(C)$$

otherwise

$$V_{OUT(RPL)} = 0.5\ V_{OUT(RPL)}(C) + V_{OUT(RPL)}(R)$$

Load-Transient Performance

In response to a large step increase in load current, the output voltage will sag for several microseconds unless C2 is increased beyond the values that satisfy the above requirements. Note that an increase in capacitance is all that's required to improve the transient response, and that the ESR requirements don't change. Therefore, the added capacitance can be supplied by an additional low-cost bulk capacitor in parallel with the normal low-ESR switching-regulator capacitor. The equation for voltage sag under a step load change is:

$$V_{SAG} = \frac{I_{STEP}^2 \times L}{2 \times C2 \times (V_{IN(min)} \times DMAX - 3.3V)}$$

where DMAX is the maximum duty cycle. Higher duty cycles are possible when the oscillator frequency is reduced to 200kHz, since fixed propagation delays through the PWM comparator become a lesser part of the whole period. The tested worst-case limit for DMAX is 92% at 200kHz or 89% at 300kHz. Lower inductance values can reduce the filter capacitance requirement, but only at the expense of increased output ripple (due to higher peak currents).

RC Filter for VCC

R2 and C4 form a lowpass filter to remove switching noise from the V_{CC} input to the MAX767. C4 must have fairly low ESR (<5Ω). Switching noise can interfere with proper output voltage regulation, resulting in an excessive output voltage decrease (>100mV) at full load.

Overheating during soldering can damage the surface-mount capacitors specified for C4, causing the regulation problems described above. Take care to heat the capacitor for as short a time as possible, especially if it is soldered by hand.

Rectifier, D2

Use a 1N5817 or similar Schottky diode for applications up to 3A, or a 1N5820 for up to 10A. Surface-mount equivalents are available from N.I.E.C. with part numbers EC10QS02 and NSQ03A02, or from Motorola with part numbers MBRS120T3 and MBRS320T3. D2 must be a Schottky diode to prevent the lossy MOSFET body diode from turning on.

Soft-Start

A capacitor connected from GND to SS causes the supply's current-limit level to ramp up slowly. The ramp time to full current limit is approximately 1ms for every nF of capacitance on SS, with a minimum value of 10µs. Typical values for the soft-start capacitor are in the 10nF to 100nF range; a 5V rating is sufficient.

The time required for the output voltage to ramp up to its rated value depends upon the output load, and is not necessarily the same as the time it takes for the current limit to reach full capacity.

Duty Cycle

The duty cycle for the high-side MOSFET (N1) in continuous-conduction mode is:

$$\frac{100\% \times (V_{OUT} + V_{N2})}{V_{IN} - V_{N1}}$$

where:

V_{OUT} = 3.3V

V_{IN} = 5V

V_{N1} and V_{N2} = $I_{LOAD} \times r_{DS(ON)}$ for each MOSFET.

It is apparent that, in continuous-conduction mode, N1 will conduct for about twice the time as N2. Under short-circuit conditions, however, N2 can conduct as much 90% of the time. If there is a significant chance of short circuiting the output, select N2 to handle the resulting duty cycle (see *Short-Circuit Duration* section).

MOSFET Switches, N1 and N2

The two N-channel MOSFETs must be "logic-level" FETs; that is, they must be fully on (have low $r_{DS(ON)}$) with only 4V gate-source drive voltage. For high-current applications, FETs with low gate-threshold voltage specifications (i.e., maximum $V_{GS(TH)}$ = 2V rather than 3V) are preferred. In addition, they should have low total gate charge (<70nC) to minimize switching losses.

For output currents in excess of the five standard application circuits, placing MOSFETs with very low gate charge in parallel increases output current and lowers resistive losses. This approach has been used for the 7A and 10A circuits. N2 does not normally require the same current capacity as N1 because it conducts only about 33% of the time, while N1 conducts about 66% of the time.

Short-Circuit Duration

At their highest rated temperatures (+70°C or +85°C), each of the five standard application circuits will withstand a short circuit of several seconds duration. In most cases, the MAX767 will be used in applications where long-term short circuiting of the output is unlikely.

If it is desirable for the circuit to withstand a continuous short circuit, the MOSFETs must be able to dissipate the required power. This depends on physical factors such as the mounting of the transistor, any heat-sinking used, and ventilation provided, as well as the actual current the transistor must deliver. The short-circuit current is approximately 100mV / R1, but may vary by ±20%.

Cautious design requires that the transistors withstand the maximum possible current, which is I_{SC} = 120mV / R1. N1 and N2 must withstand this current scaled by their maximum duty factors. The maximum duty factor for N1 occurs under high-load (but not short-circuit) conditions, and is approximately V_{OUT} / $V_{IN(min)}$ or about 0.7. The maximum duty factor for N2 occurs during short-circuit conditions and is:

$$1 - \frac{I_{SC} \times r_{DS(ON)N2}}{V_{IN(max)} - I_{SC} \times r_{DS(ON)N1}}$$

which can exceed 0.9. The total power dissipated in both MOSFETs together is $I_{SC}^2 \times r_{DS(ON)}$.

5V-to-3.3V, Synchronous, Step-Down Power-Supply Controller

Proper circuit operation requires that the short-circuit current be at least I_{LOAD} x (1 + LIR / 2). However, the standard application circuits are designed for a short-circuit current slightly in excess of this amount. This excess design current guarantees proper start-up under constant full-load conditions and proper full-load transient response, and is particularly necessary with low input voltages. If the circuit will not be subjected to full-load transients or to loads approaching the full-load at start-up, you can decrease the short-circuit current by increasing R1, as described in the *Current-Sense Resistor* section. This may allow use of MOSFETs with a lower current-handling capability.

Heavy-Load Efficiency

Losses due to parasitic resistances in the switches, coil, and sense resistor dominate at high load-current levels. Under heavy loads, the MAX767 operates deep in the continuous-conduction mode, where there is a large DC offset to the inductor current (plus a small sawtooth AC component) (see *Inductor* section). This DC current is exactly equal to the load current, a fact which makes it easy to estimate resistive losses via the simplifying assumption that the total inductor current is equal to this DC offset current. The major loss mechanisms under heavy loads, in usual order of importance, are:

- I^2R losses
- gate-charge losses
- diode-conduction losses
- transition losses
- capacitor-ESR losses
- losses due to the operating supply current of the IC.

Inductor-core losses, which are fairly low at heavy loads because the AC component of the inductor current is small, are not accounted for in this analysis.

$$\text{Efficiency} = \frac{P_{OUT}}{P_{IN}} \times 100\% =$$

$$\frac{P_{OUT}}{P_{OUT} + PD_{TOTAL}} \times 100\%$$

$$PD_{TOTAL} = PD_{(I^2R)} + PD_{GATE} + PD_{DIODE} + PD_{TRAN} + PD_{CAP} + PD_{IC}$$

I^2R Losses

$$PD_{(I^2R)} = \text{resistive loss} = (I_{LOAD}^2) \times (R_{COIL} + r_{DS(ON)} + R1)$$

where R_{COIL} is the DC resistance of the coil and $r_{DS(ON)}$ is the drain-source on resistance of the MOSFET. Note that the $r_{DS(ON)}$ term assumes that identical MOSFETs are employed for both the synchronous rectifier and high-side switch, because they time-share the inductor current. If the MOSFETs are not identical, estimate losses by averaging the two individual $r_{DS(ON)}$ terms according to their duty factors: 0.66 for N1 and 0.34 for N2.

Gate-Charge Losses

$$PD_{GATE} = \text{gate driver loss} = q_G \times f \times 5V$$

where q_G is the sum of the gate charge for low- and high-side switches. Note that gate-charge losses are dissipated in the IC, not the MOSFETs, and therefore contribute to package temperature rise. For a pair of matched MOSFETs, q_G is simply twice the gate capacitance of a single MOSFET (a data sheet specification).

Diode Conduction Losses

$$PD_{DIODE} = \text{diode conduction losses} = I_{LOAD} \times V_D \times t_D \times f$$

where V_D is the forward voltage of the Schottky diode at the output current, t_D is the diode's conduction time (typically 110ns), and f is the switching frequency.

Transition Losses

$$PD_{TRAN} = \text{transition loss} = \frac{V_{IN}^2 \times C_{RSS} \times I_{LOAD} \times f}{I_{DRIVE}}$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data sheet parameter), f is the switching frequency, and I_{DRIVE} is the peak current available from the high-side gate driver output (approximately 1A).

Additional switching losses are introduced by other sources of stray capacitance at the switching node, including the catch-diode capacitance, coil interwinding capacitance, and low-side switch drain capacitance, and are given as $PD_{SW} = V_{IN}^2 \times C_{STRAY} \times f$, but these are usually negligible compared to C_{RSS} losses. The low-side switch introduces only tiny switching losses, since its drain-source voltage is already low when it turns on.

Capacitor ESR Losses

PD_{CAP} = capacitor ESR loss = I_{RMS}^2 x ESR

where I_{RMS} = RMS AC input current, approximately I_{LOAD} / 2.

Note that losses in the output filter capacitors are small when the circuit is heavily loaded, because the current into the capacitor is not chopped. The output capacitor sees only the small AC sawtooth ripple current. Ensure that the input bypass capacitor has a ripple current rating that exceeds the value of I_{RMS}.

IC Supply-Current Losses

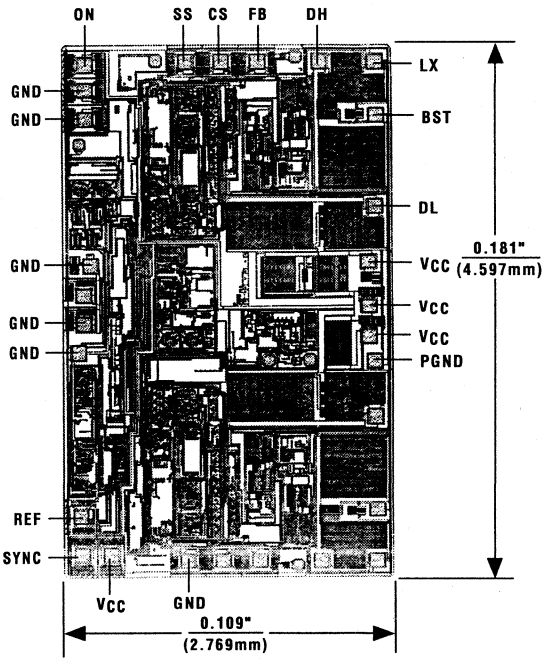
PD_{IC} is the quiescent power dissipation of the IC and is 5V times the quiescent supply current (a data sheet parameter), or about 5mW.

Light-Load Efficiency

Under light loads, the PWM will operate in discontinuous-conduction mode, where the inductor current discharges to zero at some point during each switching cycle. New loss mechanisms, insignificant at heavy loads, begin to become important. The basic difference is that in discontinuous mode, the AC component of the inductor current is large compared to the load current. This increases losses in the core and in the output filter capacitors. Ferrite cores are recommended over powdered-material types for best light-load efficiency.

At light loads, the inductor delivers triangular current pulses rather than the nearly square waves found in continuous-conduction mode. These pulses ramp up to a point set by the idle-mode current comparator, which is internally fixed at approximately 25% of the full-scale current-limit level. This 25% threshold provides an optimum balance between low-current efficiency and output voltage noise (the efficiency curve would actually look better with this threshold set at about 45%, but the output noise would be too high).

Chip Topography



TRANSISTOR COUNT: 1294

SUBSTRATE CONNECTED TO GND

19-0202; Rev 0; 1/94

EVALUATION KIT AVAILABLE

MAXIM

5V/12V/15V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controllers

General Description

The MAX770–MAX773 step-up switching controllers provide 90% efficiency over a 10mA to 1A load. A unique current-limited pulse-frequency-modulation (PFM) control scheme gives these devices the benefits of pulse-width-modulation (PWM) converters (high efficiency at heavy loads), while using less than 110µA of supply current (vs. 2mA to 10mA for PWM converters).

These ICs use tiny external components. Their high switching frequencies (up to 300kHz) allow surface-mount magnetics of 5mm height and 9mm diameter.

The MAX770/MAX771/MAX772 accept input voltages from 2V to 16.5V. Output voltages are preset at 5V, (MAX770), 12V (MAX771), and 15V (MAX772); they can also be adjusted using two resistors.

The MAX773 accepts inputs from 3V to 16.5V. For a wider input range, it features an internal shunt regulator that allows unlimited higher input voltages. The MAX773's output can be set to 5V, 12V, or 15V, or it can be adjusted with two resistors.

The MAX770–MAX773 drive external N-channel MOSFET switches, allowing them to power loads up to 15W. If less power is required, use the MAX756/MAX757 or MAX761/MAX762 step-up switching regulators with on-board MOSFETs.

Applications

Palmtops/Handy-Terminals
High-Efficiency DC-DC Converters
Battery-Powered Applications
Positive LCD-Bias Generators
Portable Communicators
Flash Memory Programmers

Features

- **90% Efficiency for 10mA to 1A Load Currents**
- **Up to 15W Output Power**
- **110µA Max Supply Current**
- **5µA Max Shutdown Current**
- **2V to 16.5V Input Range (MAX770/MAX771/MAX772)**
- **Internal Shunt Regulator for High Input Voltages (MAX773)**
- **Preset or Adjustable Output Voltages**
  MAX770: 5V or Adjustable
  MAX771: 12V or Adjustable
  MAX772: 15V or Adjustable
  MAX773: 5V, 12V, 15V, or Adjustable
- **Current-Limited PFM Control Scheme**
- **300kHz Switching Frequency**

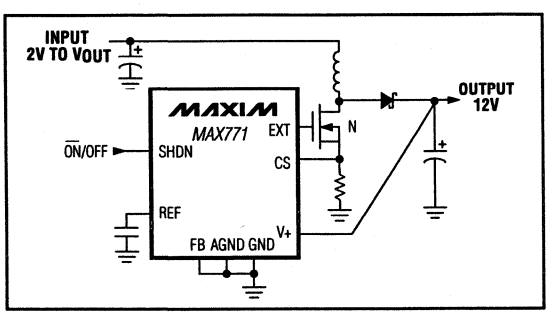
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX770CPA	0°C to +70°C	8 Plastic DIP
MAX770CSA	0°C to +70°C	8 SO
MAX770C/D	0°C to +70°C	Dice*
MAX770EPA	-40°C to +85°C	8 Plastic DIP
MAX770ESA	-40°C to +85°C	8 SO
MAX770MJA	-55°C to +125°C	8 CERDIP**

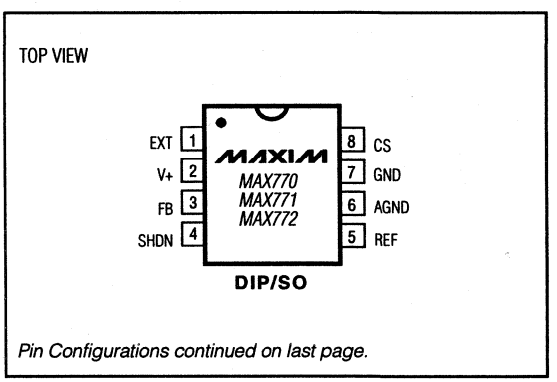
Ordering Information continued on last page.

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883B.*

Typical Operating Circuit



Pin Configurations



Pin Configurations continued on last page.

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V+ to GND ..... -0.3V, 17V
- V+ to SGND ..... -0.3V, 7V
- SGND ..... -0.3V, (V+ + 0.3V)

EXT, CS, REF, LBO, LBI, SHDN, FB ..... -0.3V, (V+ + 0.3V)
EXTH, EXTL ..... -0.3V, (V+ + 0.3V)
V5, V12, V15 ..... -0.3V, 17V
GND to AGND ..... 0.1V, -0.1V
I_{SGND} 50mA
Continuous Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
- 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
- 14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
- 14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW

Operating Temperature Ranges
- MAX77_C_ _ ..... 0°C to +70°C
- MAX77_E_ _ ..... -40°C to +85°C
- MAX77_MJ_ ..... -55°C to +125°C

Junction Temperatures
- MAX77_C_ _/E_ _ ..... +150°C
- MAX77_MJ_ ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		MAX770–772 (internal feedback resistors)		2.0		16.5	V
		MAX770–772C/E (external resistors)		3.0		16.5	
		MAX770–772MJA (external resistors)		3.1		16.5	
		MAX773C/E		3.0		16.5	
		MAX773MJD		3.1		16.5	
Minimum Start-Up Voltage		MAX770/MAX771/MAX772			1.8	2.0	V
Supply Current		V+ = 16.5V, SHDN = 0V (normal operation)			85	110	µA
Standby Current		V+ = 10.0V, SHDN ≥ 1.6V (shutdown)			2	5	µA
		V+ = 16.5V, SHDN ≥ 1.6V (shutdown)			4		
Output Voltage (Note 1)		V+ = 2.0V to 5.0V, over full load range		4.80	5.0	5.20	V
		V+ = 2.0V to 12.0V, over full load range		11.52	12.0	12.48	
		V+ = 2.0V to 15.0V, over full load range		14.40	15.0	15.60	
Output Voltage Line Regulation (Note 2)		Figure 2a, V+ = 2.7V to 4.5V, I_{LOAD} = 700mA, V_{OUT} = 5V			5		mV/V
Output Voltage Load Regulation (Note 2)		Figure 2a, V+ = 3V, I_{LOAD} = 30mA to 1A, V_{OUT} = 5V			20		mV/A
Maximum Switch On-Time	t_{ON}(max)			12	16	20	µs
Minimum Switch Off-Time	t_{OFF}(min)			1.8	2.3	2.8	µs
Efficiency		V+ = 4V, I_{LOAD} = 500mA, V_{OUT} = 5V			87		%
Reference Voltage	V_{REF}	I_{REF} = 0µA	MAX77_C	1.4700	1.5	1.5300	V
			MAX77_E	1.4625	1.5	1.5375	
			MAX77_M	1.4550	1.5	1.5450	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA	MAX77_C/E		4	10	mV
			MAX77_M		4	15	
REF Line Regulation		3V ≤ V+ ≤ 16.5V			40	100	µV/V
FB Trip-Point Voltage	V_{FB}	MAX77_C		1.4700	1.50	1.5300	V
		MAX77_E		1.4625	1.50	1.5375	
		MAX77_M		1.4550	1.50	1.5450	
FB Input Current	I_{FB}	MAX77_C				±20	nA
		MAX77_E				±40	
		MAX77_M				±60	
SHDN Input High Voltage	V_{IH}	V+ = 2.0V to 16.5V		1.6			V
SHDN Input Low Voltage	V_{IL}	V+ = 2.0V to 16.5V				0.4	V
SHDN Input Current		V+ = 16.5V, SHDN = 0V or V+				±1	µA
LBI Input Current		MAX773, V+ = 16.5V, LBI = 1.5V				±20	nA
LBI Hysteresis		MAX773			20		mV
LBI Delay		5mV overdrive			2.5		µs
LBI Threshold Voltage		MAX773, LBI falling	MAX77_C	1.4700	1.50	1.5300	V
			MAX77_E	1.4625	1.50	1.5375	
			MAX77_M	1.4550	1.50	1.5450	
LBO Leakage Current		MAX773, V+ = 16.5V, V_{LBO} = 16.5V			0.01	1.00	µA
LBO Output Voltage Low	V_{OL}	MAX773, V+ = 5V, LBO sinking 1mA			0.1	0.4	V
Current-Limit Trip Level	V_{CS}	V+ = 5V to 16.5V		170	200	230	mV
CS Input Current					0.01	±1	µA
EXT Rise Time		V+ = 5V, 1nF from EXT to ground (Note 3)			55		ns
EXT Fall Time		V+ = 5V, 1nF from EXT to ground (Note 3)			55		ns
Supply Voltage in Shunt Mode	V_{SHUNT}	MAX773, I_{SHUNT} = 1mA to 20mA, SGND = 0V, C_{SHUNT} = 0.1µF		5.5		6.3	V

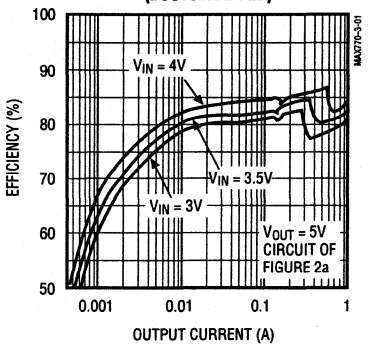
Note 1: Output voltage guaranteed using preset voltages. See Figures 7a–7d for output current capability versus input voltage.
Note 2: Output voltage line and load regulation depend on external circuit components.
Note 3: For the MAX773, EXT is EXTH and EXTL shorted together.

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

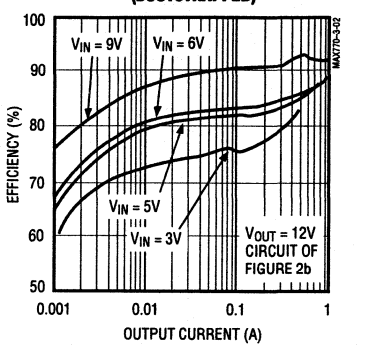
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

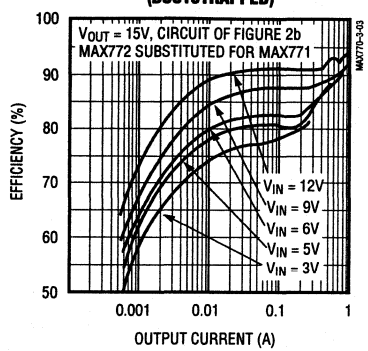
MAX770
EFFICIENCY vs. OUTPUT CURRENT
(BOOTSTRAPPED)



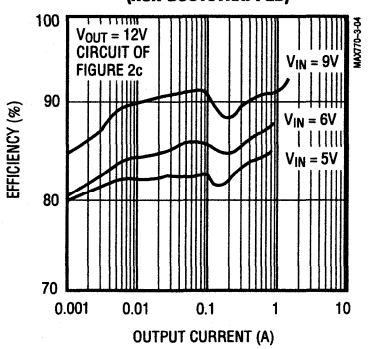
MAX771
EFFICIENCY vs. OUTPUT CURRENT
(BOOTSTRAPPED)



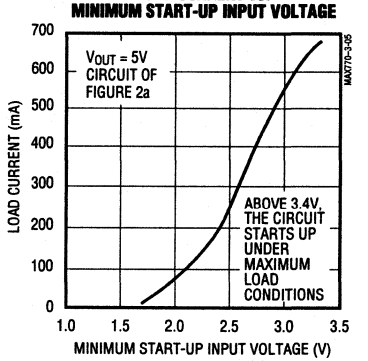
MAX772
EFFICIENCY vs. OUTPUT CURRENT
(BOOTSTRAPPED)



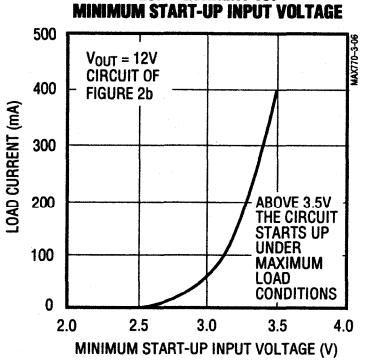
MAX771
EFFICIENCY vs. OUTPUT CURRENT
(NON-BOOTSTRAPPED)



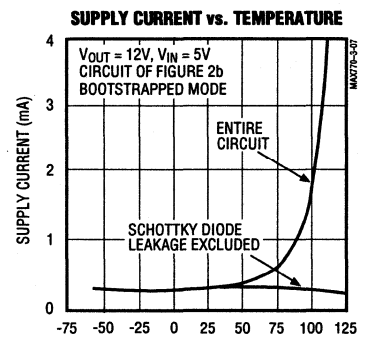
MAX770
LOAD CURRENT vs.
MINIMUM START-UP INPUT VOLTAGE



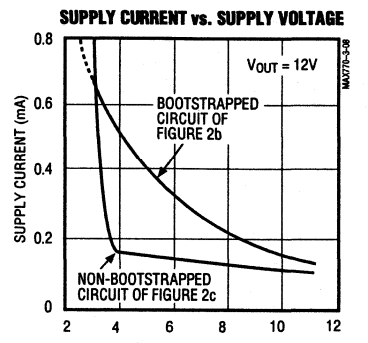
MAX771
LOAD CURRENT vs.
MINIMUM START-UP INPUT VOLTAGE



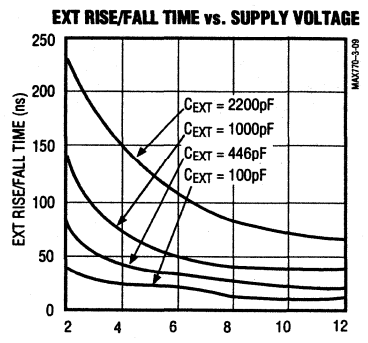
SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



EXT RISE/FALL TIME vs. SUPPLY VOLTAGE

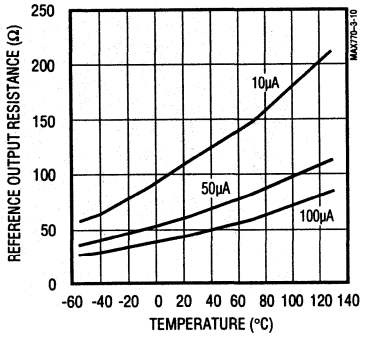


5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

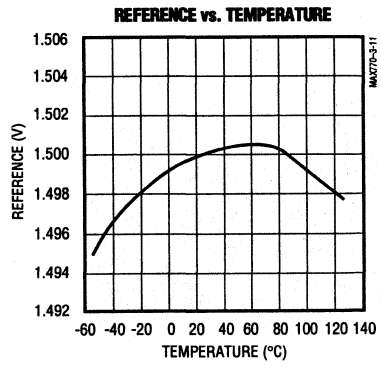
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

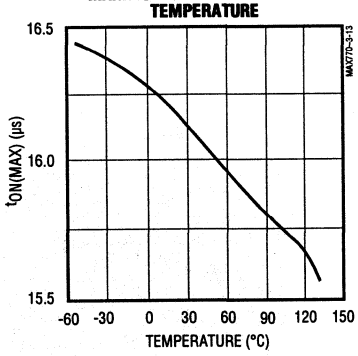
REFERENCE OUTPUT RESISTANCE vs. TEMPERATURE



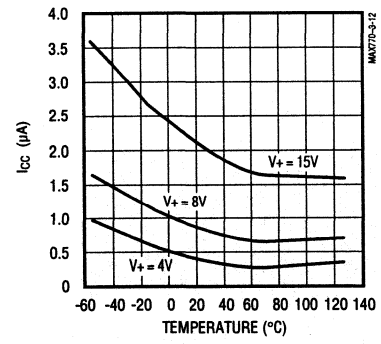
REFERENCE vs. TEMPERATURE



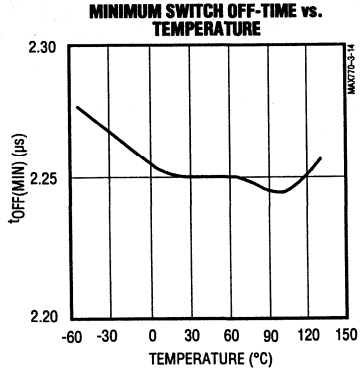
MAXIMUM SWITCH ON-TIME vs. TEMPERATURE



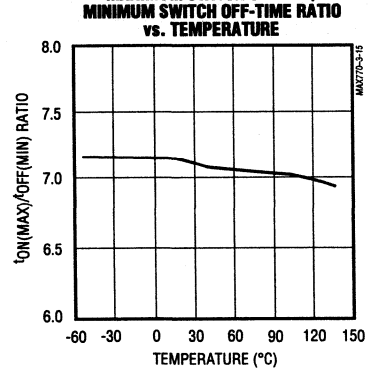
SHUTDOWN CURRENT vs. TEMPERATURE



MINIMUM SWITCH OFF-TIME vs. TEMPERATURE



MAXIMUM SWITCH ON-TIME/ MINIMUM SWITCH OFF-TIME RATIO vs. TEMPERATURE

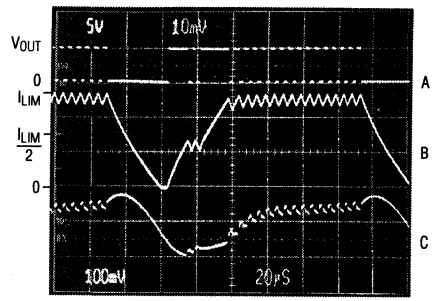


5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, T_A = +25°C, unless otherwise noted.)

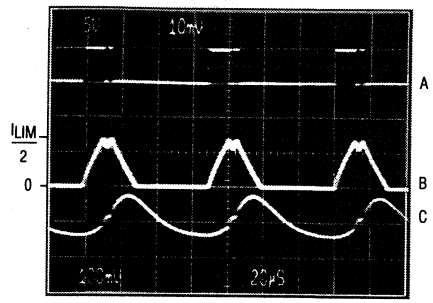
MAX770
HEAVY-LOAD SWITCHNG WAVEFORMS



20µs/div

V_{IN} = 2.9V, I_{OUT} = 0.9A
A: EXT VOLTAGE, 5V/div
B: INDUCTOR CURRENT 1A/div
C: V_{OUT} RIPPLE 100mV/div, AC-COUPLED

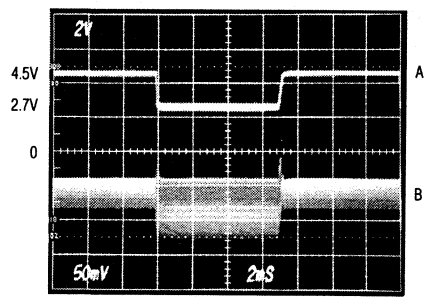
MAX770
LIGHT-LOAD SWITCHING WAVEFORMS



20µs/div

V+ = 3V, I_{OUT} = 165mA
A: EXT VOLTAGE, 5V/div
B: INDUCTOR CURRENT, 1A/div
C: V_{OUT} RIPPLE 100mV/div, AC-COUPLED

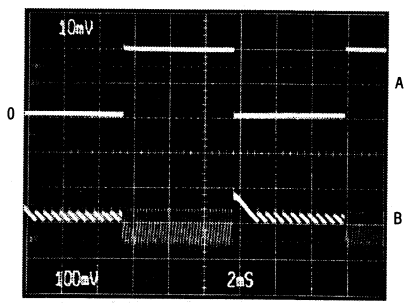
MAX770
LINE-TRANSIENT RESPONSE



2ms/div

I_{OUT} = 0.7A
A: V_{IN}, 2.7V TO 4.5V, 2V/div
B: V_{OUT} RIPPLE, 100mV/div, AC-COUPLED

MAX770
LOAD-TRANSIENT RESPONSE



2ms/div

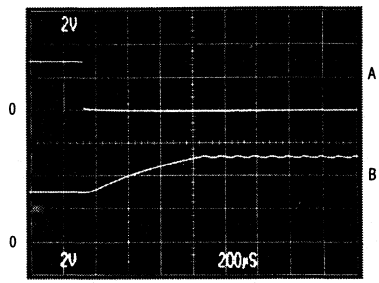
V_{IN} = 3V
A: LOAD CURRENT 0.5A/div (0A to 1A)
B: V_{OUT} RIPPLE, 100mV/div, AC-COUPLED

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, T_A = +25°C, unless otherwise noted.)

MAX770
EXITING SHUTDOWN



200µs/div

V_{IN} = 3V, I_{OUT} = 0.5A
A: SHDN, 2V/div
B: V_{OUT}, 2V/div

Pin Description

PIN		NAME	FUNCTION
MAX770 MAX771 MAX772	MAX773		
1	—	EXT	Gate drive for external N-channel power transistor
2	3	V+	Power-supply input. Also acts as a voltage-sense point when in bootstrapped mode for the MAX770/MAX771/MAX772, or as a shunt regulator when SGND is connected to ground for the MAX773. Bypass to SGND with 0.1µF when using the shunt regulator.
3	6	FB	Feedback input for adjustable-output operation. Connect to ground for fixed-output operation. Use a resistor divider network to adjust the output voltage. See *Setting the Output Voltage* section.
4	7	SHDN	Active-high TTL/CMOS logic-level shutdown input. In shutdown mode, V_{OUT} is a diode drop below V+ (due to the DC path from V+ to the output) and the supply current drops to 5µA maximum. Connect to ground for normal operation.
5	8	REF	1.5V reference output that can source 100µA for external loads. Bypass to GND with 0.1µF. The reference is disabled in shutdown.
6	—	AGND	Analog ground
7	9	GND	High-current ground return for the output driver
8	11	CS	Positive input to the current-sense amplifier. Connect the current-sense resistor between CS and GND.
—	1	V12	Input sense point for 12V-output operation. Connect V_{OUT} to V12 for 12V-output operation. Leave unconnected for adjustable-output operation.
—	2	V5	Input sense point for 5V-output operation. Connect V_{OUT} to V5 for 5V-output operation. Leave unconnected for adjustable-output operation.
—	4	LBO	Low-battery output is an open-drain output that goes low when LBI is less than 1.5V. Connect to V+ through a pull-up resistor. Leave floating if not used. LBO is high impedance in shutdown mode.
—	5	LBI	Input to the internal low-battery comparator. Tie to GND or V+ if not used.
—	10	SGND	Shunt regulator ground. Leave unconnected if the shunt regulator is **not** used.

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

Pin Description (continued)

PIN		NAME	FUNCTION
MAX770 MAX771 MAX772	MAX773		
—	12	EXTL	Low-level gate/base drive for external power transistor. Connect to the gate of an external N-channel MOSFET or to the base of an external NPN transistor.
—	13	EXTH	High-level gate/base drive for external power transistor. Connect to EXTL when using an external N-channel MOSFET. When using an external NPN transistor, connect a resistor R_{BASE} from EXTH to the base of the NPN to set the maximum base-drive current.
—	14	V15	Input sense point for 15V-output operation. Connect V_{OUT} to V15 for 15V-output operation. Leave unconnected for adjustable-output operation

Detailed Description

The MAX770–MAX773 are BiCMOS, step-up, switch-mode power-supply controllers that provide preset 5V, 12V, and 15V output voltages, in addition to adjustable-output operation. Their unique control scheme combines the advantages of pulse-frequency modulation (low supply current) and pulse-width modulation (high efficiency with heavy loads), providing high efficiency over a wide output current range, as well as increased output current capability over previous PFM devices. In addition, the external sense resistor and power transistor allow the user to tailor the output current capability for each application. Figure 1 shows the MAX770–MAX773 block diagram.

The MAX770–MAX773 offer three main improvements over prior pulse-skipping control solutions: 1) the converters operate with tiny (5mm height and less than 9mm diameter) surface-mount inductors due to their 300kHz switching frequency; 2) the current-limited PFM control scheme allows 87% efficiencies over a wide range of load currents; and 3) the maximum supply current is only 110µA.

The MAX773 can be configured to operate from an internal 6V shunt regulator, allowing very high input/output voltages. Its output can be configured for an adjustable voltage or for one of three fixed voltages (5V, 12V, or 15V), and it has a power-fail comparator for low-battery detection.

All devices have shutdown capability, reducing the supply current to 5µA max.

Bootstrapped/Non-Bootstrapped Modes

Figures 2 and 3 show standard application circuits for bootstrapped and non-bootstrapped modes. In bootstrapped mode, the IC is powered from the output (V_{OUT}, which is connected to V+) and the input voltage range is 2V to V_{OUT}. The voltage applied to the gate of the external power transistor is switched from V_{OUT} to ground, providing more switch gate drive and thus reducing the transistor's on resistance.

In non-bootstrapped mode, the IC is powered from the input voltage (V+) and operates with minimum supply current. In this mode, FB is the output voltage sense point. Since the voltage swing applied to the gate of the external power transistor is reduced (the gate swings from V+ to ground), the power transistor's on resistance increases at low input voltages. However, the supply current is also reduced because V+ is at a lower voltage, and because less energy is consumed while charging and discharging the external MOSFET's gate capacitance. The minimum input voltage for the MAX770–MAX773 is 3V when using external feedback resistors. With supply voltages below 5V, bootstrapped mode is recommended.

Note: When using the MAX770/MAX771/MAX772 in non-bootstrapped mode, there is no preset output operation because V+ is also the output voltage sense point for fixed-output operation. External resistors must be used to set the output voltage. Use 1% external feedback resistors when operating in adjustable-output mode (Figures 2c, 2d, 3b, 3d, 3e) to achieve an overall output voltage accuracy of ±5%. The MAX773 can be operated in non-bootstrapped mode without using external feedback resistors because V+ does not act as the output voltage sense point with preset-output operation. To achieve highest efficiency, operate in bootstrapped mode whenever possible.

MAX773 Shunt-Regulator Operation

The MAX773 has an internal 6V shunt regulator that allows the device to step up from very high input voltages (Figure 4).

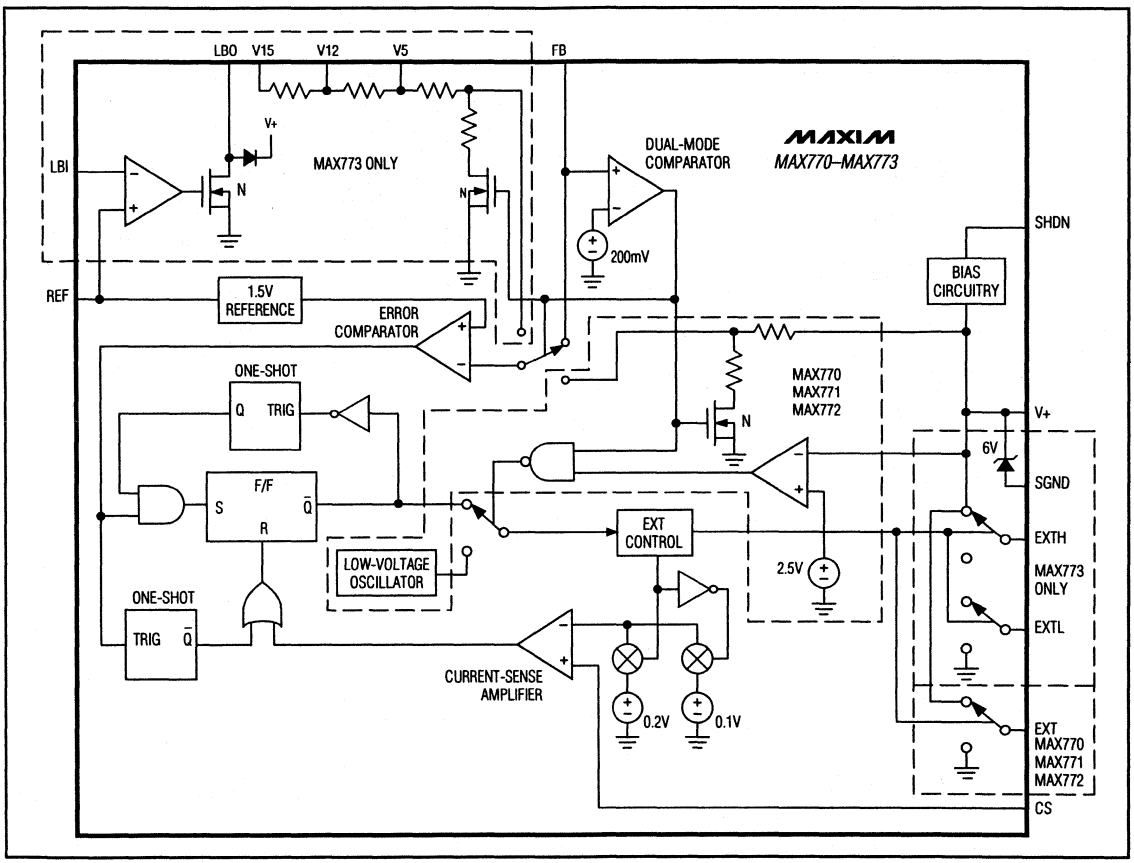


Figure 1. Block Diagram

Floating the shunt-regulator ground (SGND) disables the shunt regulator. To enable it, connect SGND to GND. The shunt regulator requires 1mA minimum current for proper operation; the maximum current must not exceed 20mA. The MAX773 operates in non-bootstrapped mode when the shunt regulator is used, and EXT swings between the 6V shunt-regulator voltage and GND.

When using the shunt regulator, use an N-channel power FET instead of an NPN power transistor as the power switch. Otherwise, excessive base drive will collapse the shunt regulator.

External Power-Transistor Control Circuitry

PFM Control Scheme

The MAX770–MAX773 use a proprietary current-limited PFM control scheme to provide high efficiency over a wide range of load currents. This control scheme combines the ultra-low supply current of PFM converters (or pulse skippers) with the high full-load efficiency of PWM converters.

Unlike traditional PFM converters, the MAX770–MAX773 use a sense resistor to control the peak inductor current. They also operate with high switching

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

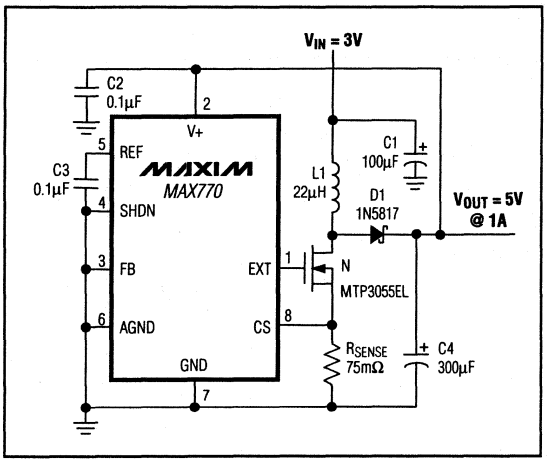


Figure 2a. 5V Preset Output, Bootstrapped

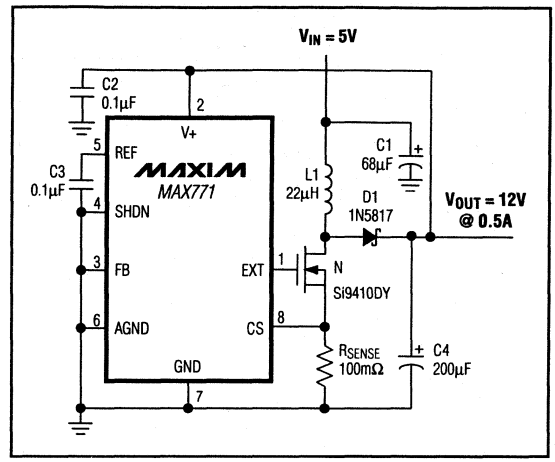


Figure 2b. 12V Preset Output, Bootstrapped

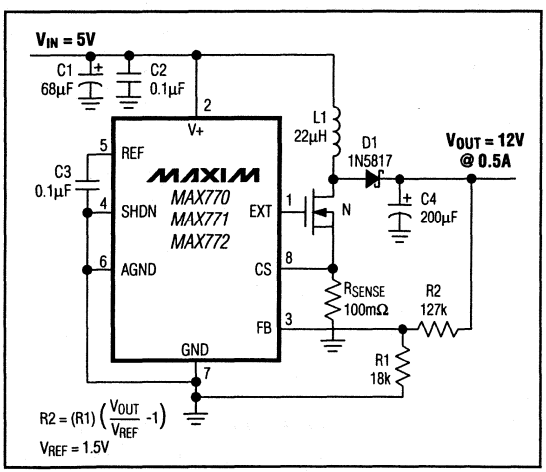


Figure 2c. 12V Output, Non-Bootstrapped

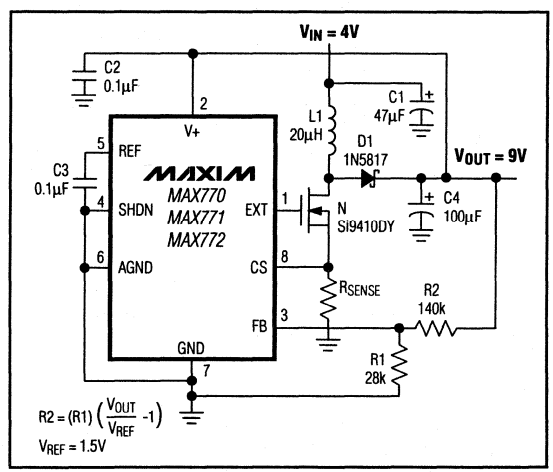


Figure 2d. 9V Output, Bootstrapped

frequencies (up to 300kHz), allowing the use of tiny external components.

As with traditional PFM converters, the power transistor is not turned on until the voltage comparator senses that the output is out of regulation. However, unlike traditional PFM converters, the MAX770–MAX773 switch using the combination of a peak current limit and a pair of one-shots that set the maximum on-time (16µs) and minimum off-time (2.3µs); there is no oscillator. Once off, the minimum off-time one-shot holds the switch off for 2.3µs. After this minimum time, the switch either 1) stays off if the output is in regulation, or 2) turns on again if the output is out of regulation.

The control circuitry allows the ICs to operate in continuous-conduction mode (CCM) while maintaining high efficiency with heavy loads. When the power switch is

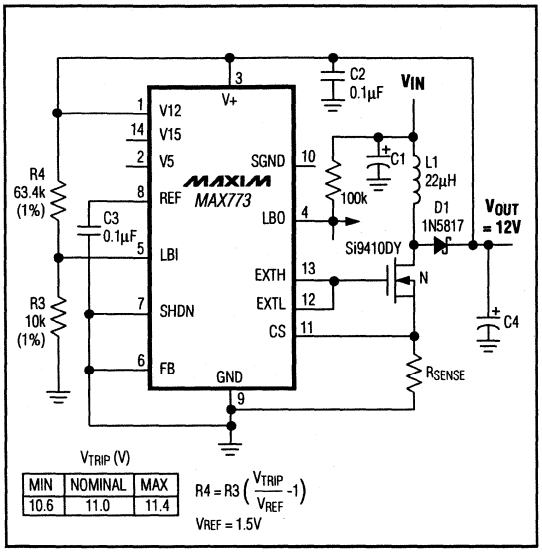


Figure 3a. 12V Preset Output, Bootstrapped, N-Channel Power MOSFET

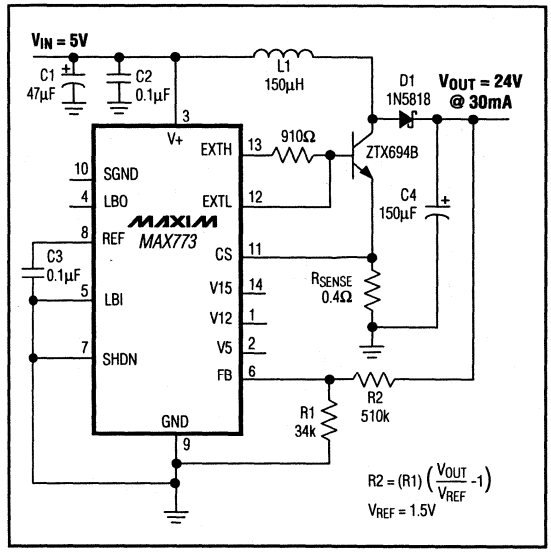


Figure 3b. 24V Output, Non-Bootstrapped, NPN Power Transistor

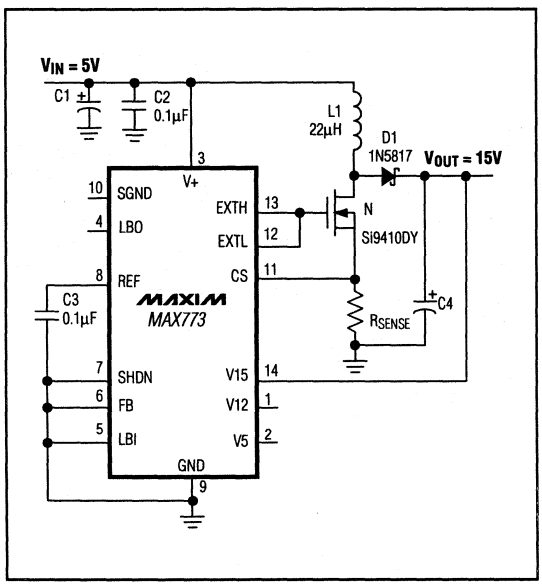


Figure 3c. 15V Preset Output, Non-Bootstrapped N-Channel Power MOSFET

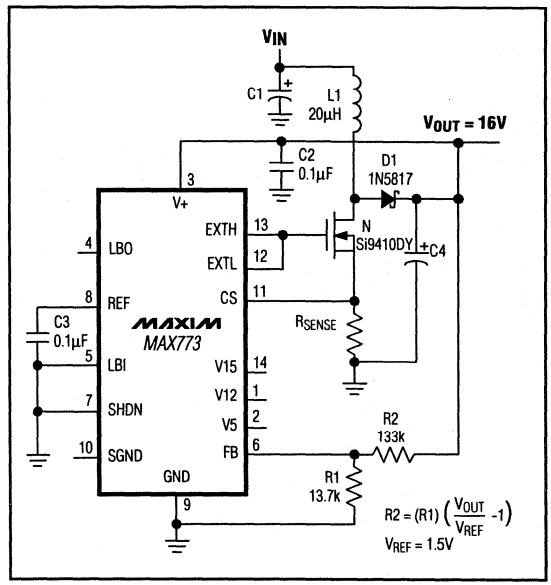


Figure 3d. 16V Output, Bootstrapped, N-Channel Power MOSFET

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

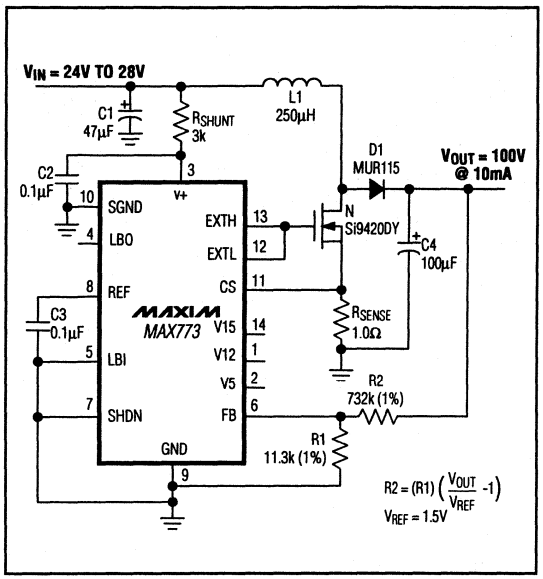


Figure 3e. 100V Output, Shunt Regulator, N-Channel Power MOSFET

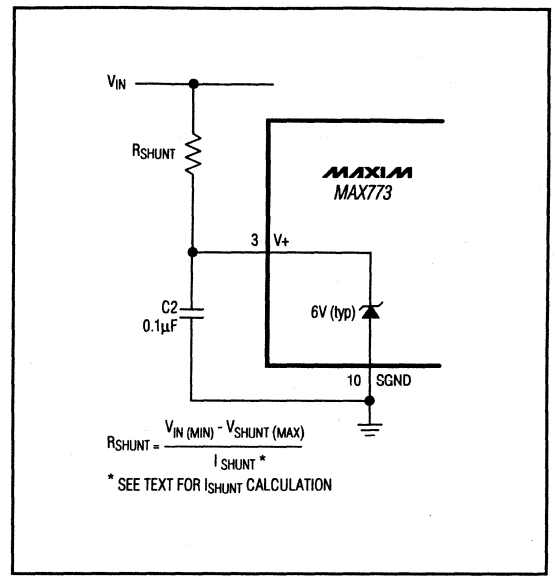


Figure 4. MAX773 Shunt Regulator

turned on, it stays on until either 1) the maximum on-time one-shot turns it off (typically 16µs later), or 2) the switch current reaches the peak current limit set by the current-sense resistor.

To increase light-load efficiency, the current limit for the first two pulses is set to one-half the peak current limit. If those pulses bring the output voltage into regulation, the error comparator holds the MOSFET off and the current limit remains at one-half the peak current limit. If the output voltage is still out of regulation after two pulses, the current limit for the next pulse is raised to the peak current limit set by the external sense resistor (see inductor current waveforms in the *Typical Operating Characteristics*).

The MAX770–MAX773 switching frequency is variable (depending on load current and input voltage), causing variable switching noise. However, the subharmonic noise generated does not exceed the peak current limit times the filter capacitor equivalent series resistance (ESR). For example, when generating a 12V output at 500mA from a 5V input, only 180mV of output ripple occurs using the circuit of Figure 2b.

Low-Voltage Start-Up Oscillator

The MAX770/MAX771/MAX772 feature a low input voltage start-up oscillator that guarantees start-up with no load down to 2V when operating in bootstrapped mode and using internal feedback resistors. At these low voltages, the supply voltage is not large enough for proper error-comparator operation and internal biasing. The start-up oscillator has a fixed 50% duty cycle and the MAX770/MAX771/MAX772 disregard the error-comparator output when the supply voltage is less than 2.5V. Above 2.5V, the error-comparator and normal one-shot timing circuitry are used. The low voltage start-up circuitry is disabled if non-bootstrapped mode is selected (FB is not tied to ground).

The MAX773 does not provide the low-voltage 50% duty-cycle oscillator. Its minimum start-up voltage is 3V for all modes.

External Transistor

An N-FET power switch is recommended for the MAX770/MAX771/MAX772.

The MAX773 can drive either an N-channel MOSFET (N-FET) or an NPN because it provides two separate

drive outputs (EXTH and EXTL) that operate 180° out of phase (Figures 3a and 3b). In Figure 3b, the resistor in series with EXTH limits the base current, and EXTL (which is connected directly to the base) turns the transistor off.

Shutdown Mode

When SHDN is high, the MAX770–MAX773 enter shutdown mode. In this mode, the internal biasing circuitry is turned off (including the reference) and V_{OUT} falls to a diode drop below V_{IN} (due to the DC path from the input to the output). In shutdown mode, the supply current drops to less than 5µA. SHDN is a TTL/CMOS logic-level input. Connect SHDN to GND for normal operation.

The MAX773's shunt regulator is **not** disabled in shutdown mode.

Low-Battery Detector

The MAX773 provides a low-battery comparator that compares the voltage on LBI to the reference voltage. When the LBI voltage is below V_{REF}, LBO (an open-drain output) goes low. The low-battery comparator's 20mV of hysteresis adds noise immunity, preventing repeated triggering of LBO. Use a resistor-divider network between V+, LBI, and GND to set the desired trip voltage V_{TRIP}. LBO is high impedance in shutdown mode.

Design Procedure

Setting the Output Voltage

To set the output voltage, first determine the mode of operation, either bootstrapped or non-bootstrapped. Bootstrapped mode provides more output current capability, while non-bootstrapped mode reduces the supply current (see *Typical Operating Characteristics*). If a decaying voltage source (such as a battery) is used, see the additional notes in the *Low Input Voltage Operation* section.

Use the MAX770/MAX771/MAX772 unless one or more of the following conditions applies. If one or more of the following is true, use the MAX773:

1) An NPN power transistor will be used as the power switch
2) The LBI/LBO function is required
3) The shunt regulator must accommodate a high input voltage
4) Preset-output non-bootstrapped operation is desired—for example, to reduce the no-load supply current in a 5V to 12V application.

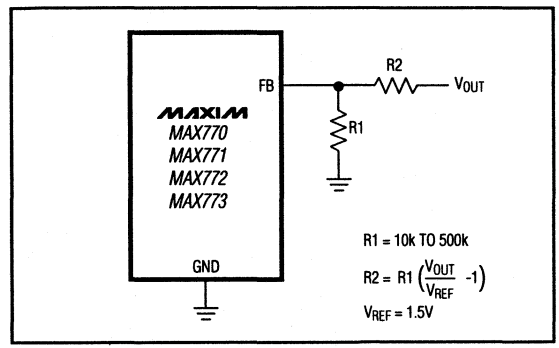


Figure 5. Adjustable Output Circuit

See Table 1 for a summary of operating characteristics and requirements for the ICs in bootstrapped and non-bootstrapped modes.

The MAX770–MAX773's output voltage can be adjusted from very high voltages down to 3V, using external resistors R1 and R2 configured as shown in Figure 5. For adjustable-output operation, select feedback resistor R1 in the range of 10kΩ to 500kΩ. R2 is given by:

$$R2 = (R1)\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} equals 1.5V.

For preset-output operation, tie FB to GND (this forces bootstrapped-mode operation for the MAX770/MAX771/MAX772).

Configure the MAX773 for a preset voltage of 5V, 12V, or 15V by connecting the output to the corresponding sense input pin (i.e., V5, V12, or V15). FB must be tied to ground for preset-output operation. Leave all unused sense input pins unconnected. Failure to do so will cause an incorrect output voltage. The MAX773 can provide a preset output voltage in both bootstrapped and non-bootstrapped modes.

Figures 2 and 3 show various circuit configurations for bootstrapped/non-bootstrapped, preset/adjustable operation.

Shunt-Regulator Operation

When using the shunt regulator, connect SGND to ground and place a 0.1µF capacitor between V+ and SGND, as close to the IC as possible. Increase C2 to 1.0µF to improve shunt regulators performance with heavy loads. Select R_{SHUNT} such that $1mA \le I_{SHUNT} \le 20mA$.

5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

Table 1. Bootstrapped vs. Non-Bootstrapped Operation

PARAMETER	BOOTSTRAPPED*	NON-BOOTSTRAPPED
Gate Drive	GND to V_{OUT}	GND to V+
FET On Resistance	Lower	Higher
Gate-Drive Capacitive Losses	Higher	Lower
No-Load Supply Current	Higher	Lower
Possible Input Voltage Range	2V to 16.5V (MAX770/MAX771/MAX772), (internal feedback resistors) 3V to 16.5V (MAX770/MAX771/MAX772), (external feedback resistors) 3V to 16.5V (MAX773)	3V to 16.5V (MAX770/MAX771/MAX772), 3V and up (MAX773)
Normally Recommended Input Voltage Range	2V to 5V (MAX770/MAX771/MAX772), 3V to 5V (MAX773)	5V to 16.5V (MAX770/MAX771/MAX772), 5V and up (MAX773)
Fixed Output Available	MAX770–MAX773(N)	MAX773(N)/MAX773(S)
Adjustable Output Available	MAX770–MAX773(N)	MAX770/MAX771/MAX772/ MAX773(N)/MAX773(S)

*MAX773(S) indicates shunt mode; MAX773(N) indicates NOT in shunt mode.

Use an N-channel FET as the power switch when using the shunt regulator (see *MAX773 Shunt-Regulator Operation* in the *Detailed Description*). The shunt-regulator current powers the MAX773 and also provides the FET gate-drive current, which depends largely on the FET's total gate charge at V_{GS} = 5V. To determine the shunt-resistor value, first determine the maximum shunt current required.

$$I_{SHUNT} = I_{SUPP} + I_{GATE}$$

See *N-Channel MOSFETs* in the *Power-Transistor Selection* section to determine I_{GATE}.

Determine the shunt-resistor value using the following equation:

$$R_{SHUNT(max)} = \frac{V_{IN(min)} - V_{SHUNT(max)}}{I_{SHUNT}}$$

where $V_{SHUNT(max)}$ is 6.3V.

The shunt regulator is not disabled in shutdown mode, and continues to draw the calculated shunt current.

If the calculated shunt regulator current exceeds 20mA, or if the shunt current exceeds 5mA and less shunt regulator current is desired, use the circuit of Figure 6 to provide increased drive and reduced shunt current when driving N-FETs with large gate capacitances. Select I_{SHUNT} = 3mA. This provides adequate biasing current for this circuit, although higher shunt currents can be used.

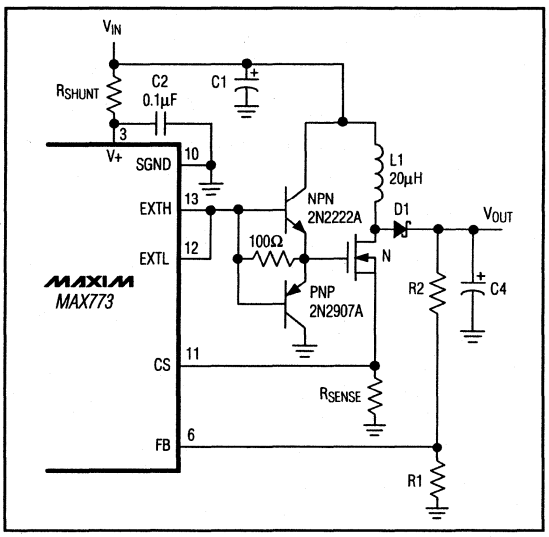


Figure 6. Increased N-FET Gate Drive when Using the Shunt Regulator

To prevent the shunt regulator from drawing current in shutdown mode, place a switch in series with the shunt resistor.

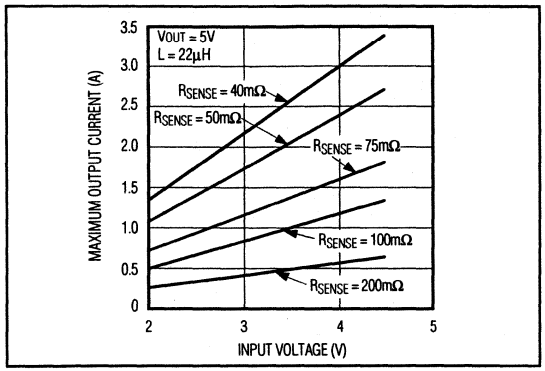


Figure 7a. Maximum Output Current vs. Input Voltage (VOUT = 5V)

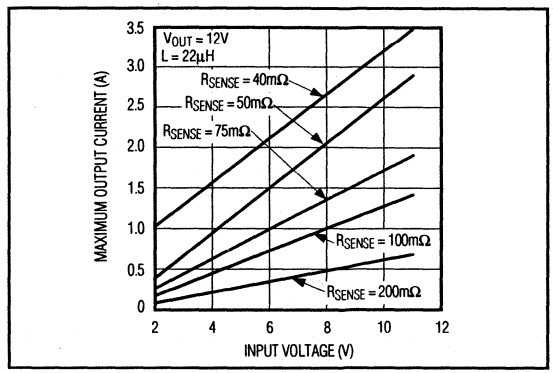


Figure 7b. Maximum Output Current vs. Input Voltage (VOUT = 12V)

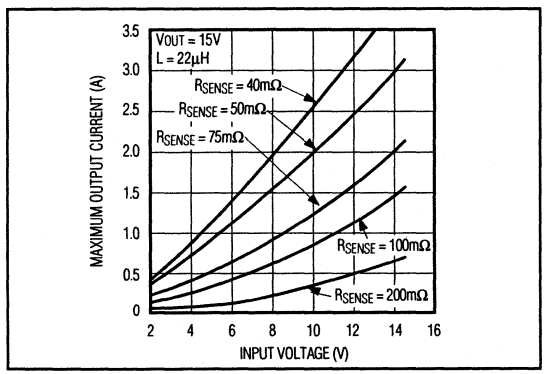


Figure 7c. Maximum Output Current vs. Input Voltage (VOUT = 15V)

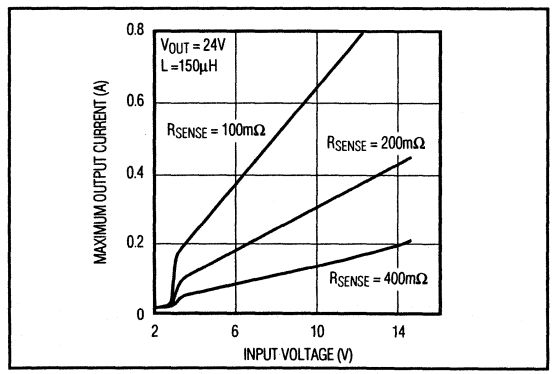


Figure 7d. Maximum Output Current vs. Input Voltage (VOUT = 24V)

Determining RSENSE

The *Typical Operating Characteristics* graphs show the output current capability for various modes, sense resistors, and input/output voltages. Use these graphs, along with the theoretical output current curves shown in Figures 7a-7d, to select RSENSE. These theoretical curves assume that an external N-FET power switch is used. They were derived using the minimum (worst-case) current-limit comparator threshold value, and the inductance value. No tolerance was included for RSENSE. The voltage drop across the diode was assumed to be 0.5V, and the drop across the power switch rDS(ON) and coil resistance was assumed to be 0.3V. To use the graphs, locate the graph with the appropriate output voltage or the graph having the nearest output voltage higher than the desired output voltage. On this graph, find the curve for the largest sense-resistor value with an output current that is adequate at the lowest input voltage.

Determining the Inductor (L)

Practical inductor values range from 10µH to 300µH. 20µH is a good choice for most applications. In applications with large input/output differentials, the IC's output current capability will be much less when the inductance value is too low, because the IC will always operate in discontinuous mode. If the inductor value is too low, the current will ramp up to a high level before the current-limit comparator can turn off the switch. The minimum on-time for the switch (tON(min)) is approximately 2µs; select an inductor that allows the current to ramp up to ILIM/2 in no less than 2µs. Choosing a value of ILIM/2 allows the half-size current pulses to occur, increasing light-load efficiency and minimizing output ripple.

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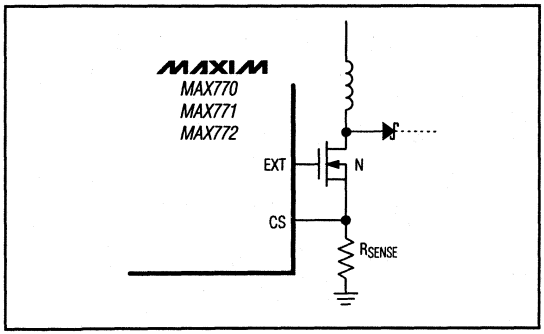

Figure 8a. Use an N-Channel MOSFET with the MAX770/MAX771/MAX772

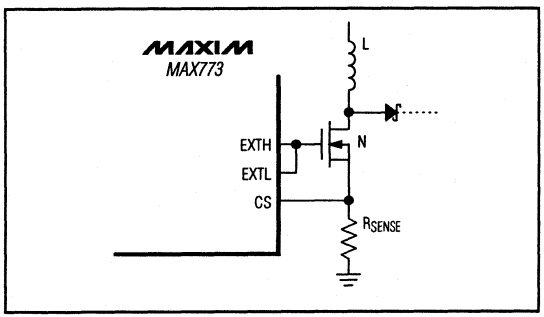

Figure 8b. Using an N-Channel MOSFET with the MAX773

The standard operating circuits use a 22µH inductor. If a different inductance value is desired, select L such that:

$$L \geq \frac{V_{IN}(max) \times t_{ON}(min)}{I_{LIM}/2}$$

Larger inductance values tend to increase the start-up time slightly, while smaller inductance values allow the coil current to ramp up to higher levels before the switch turns off, increasing the ripple at light loads.

Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current rating set by RSENSE. However, it is generally acceptable to bias the inductor into saturation by approximately 20% (the point where the inductance is 20% below the nominal value). For highest efficiency, use a coil with low DC resistance, preferably under 20mΩ. To minimize radiated noise, use a toroid, a pot core, or a shielded coil.

Table 2 lists inductor suppliers and specific recommended inductors.

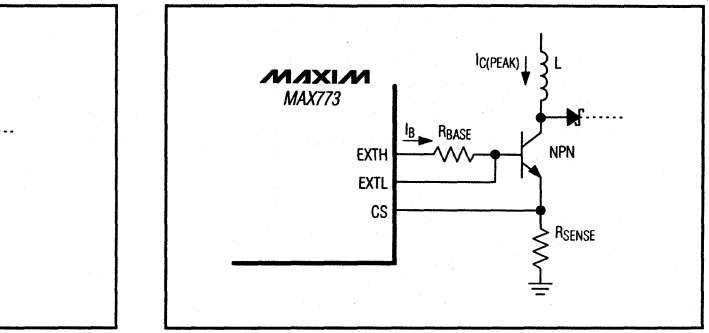

Figure 8c. Using an NPN Transistor with the MAX773

Power Transistor Selection

Use an N-channel MOSFET power transistor with the MAX770/MAX771/MAX772 (Figure 8a).

Use an N-FET whenever possible with the MAX773. An NPN transistor can be used, but be extremely careful when determining the base current (see *NPN Transistors* section). An NPN transistor is not recommended when using the shunt regulator.

N-Channel MOSFETs

To ensure the external N-channel MOSFET (N-FET) is turned on hard, use logic-level or low-threshold N-FETs when the input drive voltage is less than 8V. This applies even in bootstrapped mode, to ensure start-up.

N-FETs provide the highest efficiency because they do not draw any DC gate-drive current, but they are typically more expensive than NPN transistors. When using an N-FET with the MAX773, connect EXTH and EXTL to the N-FET's gate (Figure 8b).

When selecting an N-FET, three important parameters are the total gate charge (Q_g), on resistance ($r_{DS(ON)}$), and reverse transfer capacitance (C_{RSS}).

Q_g takes into account all capacitances associated with charging the gate. Use the typical Q_g value for best results; the maximum value is usually grossly overspecified since it is a guaranteed limit and not the measured value. The typical total gate charge should be 50nC or less. With larger numbers, the EXT pins may not be able to adequately drive the gate. The EXT rise/fall time with various capacitive loads as shown in the *Typical Operating Characteristics*.

The two most significant losses contributing to the N-FET's power dissipation are I^2R losses and switching losses. Select a transistor with low $r_{DS(ON)}$ and low C_{RSS} to minimize these losses.

Determine the maximum required gate-drive current from the Q_G specification in the N-FET data sheet.

The MAX773's maximum allowed switching frequency during normal operation is 300kHz; but at start-up the maximum frequency can be 500kHz, so the maximum current required to charge the N-FET's gate is f(max) x Q_G(typ). Use the typical Q_G number from the transistor data sheet. For example, the Si9410DY has a Q_G(typ) of 17nC (at V_{GS} = 5V), therefore the current required to charge the gate is:

$$I_{GATE}(max) = (500kHz)(17nC) = 8.5mA.$$

The bypass capacitor on V+ (C2) must instantaneously furnish the gate charge without excessive droop (e.g., less than 200mV):

$$\Delta V+ = \frac{Q_G}{C2}$$

Continuing with the example, $\Delta V+ = 17nC/0.1\mu F = 170mV$.

Use I_{GATE} when calculating the appropriate shunt resistor. See the *Shunt Regulator Operation* section.

Figure 2a's application circuit uses an MTD3055EL logic-level N-FET with a guaranteed threshold voltage (V_{TH}) of 2V. Figure 2b's application circuit uses an 8-pin Si9410DYsurface-mount N-FET that has 50mΩ on resistance with 4.5V V_{GS}, and a guaranteed V_{TH} of less than 3V.

NPN Transistors

The MAX773 can drive NPN transistors, but be extremely careful when determining the base-current requirements. Too little base current can cause excessive power dissipation in the transistor; too much base current can cause the base to oversaturate, so the transistor remains on continually. Both conditions can damage the transistor.

When using the MAX773 with an NPN transistor, connect EXTL to the transistor's base, and connect R_{BASE} between EXTH and the base (Figure 8c).

To determine the required peak inductor current, $I_{C(PEAK)}$, observe the *Typical Operating Characteristics* efficiency graphs and the theoretical output current capability vs. input voltage graphs to determine a sense resistor that will allow the desired output current. Divide the 170mV worst-case (smallest) voltage across the current-sense amplifier V_{CS}(max) by the sense-resistor value. To determine I_B, set the peak inductor current (I_{LIM}) equal to the peak transistor collector current $I_{C(PEAK)}$. Calculate I_B as follows:

$$I_B = I_{LIM}/\beta$$

Use the worst-case (lowest) value for ß given in the transistor's electrical specification, where the collector current used for the test is approximately equal to I_{LIM}. It may be necessary to use even higher base currents (e.g., $I_B = I_{LIM}/10$), although excessive I_B may impair operation by extending the transistor's turn-off time.

R_{BASE} is determined by:

$$R_{BASE} = \frac{(V_{EXTH} - V_{BE} - V_{CS(min)})}{I_B}$$

Where V_{EXTH} is the voltage at V+ (in bootstrapped mode V_{EXTH} is the output voltage), V_{BE} is the 0.7V transistor base-emitter voltage, V_{CS}(min) is the voltage drop across the current-sense resistor, and I_B is the minimum base current that forces the transistor into saturation. This equation reduces to (V+ - 700mV - 170mV) / I_B.

For maximum efficiency, make R_{BASE} as large as possible, but small enough to ensure the transistor is always driven near saturation. Highest efficiency is obtained with a fast-switching NPN transistor ($f_T \geq 150MHz$) with a low collector-emitter saturation voltage and a high current gain. A good transistor to use is the Zetex ZTX694B.

Diode Selection

The MAX770–MAX773's high switching frequency demands a high-speed rectifier. Schottky diodes such as the 1N5817–1N5822 are recommended. Make sure that the Schottky diode's average current rating exceeds the peak current limit set by R_{SENSE}, and that its breakdown voltage exceeds V_{OUT}. For high-temperature applications, Schottky diodes may be inadequate due to their high leakage currents; high-speed silicon diodes may be used instead. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantages of its high leakage current.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor (C2) is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the ripple seen on the output voltage. An OS-CON 300µF, 6.3V output filter capacitor has approximately 50mΩ of ESR and typically provides 180mV ripple when stepping up from 3V to 5V at 1A (Figure 2a).

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Smaller capacitors are acceptable for light loads or in applications that can tolerate higher output ripple.

Since the output filter capacitor's ESR affects efficiency, use low-ESR capacitors for best performance. The smallest low-ESR surface-mount tantalum capacitors currently available are the Sprague 595D series. Sanyo OS-CON organic semiconductor through-hole capacitors and the Nichicon PL series also exhibit low ESR. See Table 2.

Input Bypass Capacitors

The input bypass capacitor (C1) reduces peak currents drawn from the voltage source and also reduces noise at the voltage source caused by the switching action of the MAX770–MAX773. The input voltage source impedance determines the size of the capacitor required at the V+ input. As with the output filter capacitor, a low-ESR capacitor is recommended. For output currents up to 1A, 150µF (C1) is adequate, although smaller bypass capacitors may also be acceptable.

Bypass the IC with a 0.1µF ceramic capacitor (C2) placed close to the V+ and GND pins.

Reference Capacitor

Bypass REF with a 0.1µF capacitor (C3). REF can source up to 100µA of current.

Setting the Low-Battery-Detector Voltage

To set the low-battery detector's falling trip voltage (V_{TRIP}(falling)), select R3 between 10kΩ and 500kΩ (Figure 9), and calculate R4 as follows:

$$R4 = (R3)\left(\frac{VTRIP - VREF}{V_{REF}}\right)$$

where V_{REF} = 1.5V.

The rising trip voltage is higher because of the comparator's approximately 20mV of hysteresis, and is determined by:

$$V_{TRIP}\,(rising) = (V_{REF} + 20mV)\left(1 + \frac{R4}{R3}\right)$$

Connect a high value resistor (larger than R3 + R4) between LBI and LBO if additional hysteresis is required.

Connect a pull-up resistor (e.g., 100kΩ) between LBO and V+. Tie LBI to GND and leave LBO floating if the low-battery detector is not used.

Applications Information

MAX773 Operation with High Input/Output Voltages

The MAX773's shunt regulator input allows high voltages to be converted to very high voltages. Since the MAX773 runs off the 6V shunt (bootstrapped operation is not allowed), the IC will not see the high input voltage. Use an external logic-level N-FET as the power switch, since only 6V of V_{GS} are available. Also, make sure all external components are rated for very high output voltage. Figure 3e shows a circuit that converts 28V to 100V.

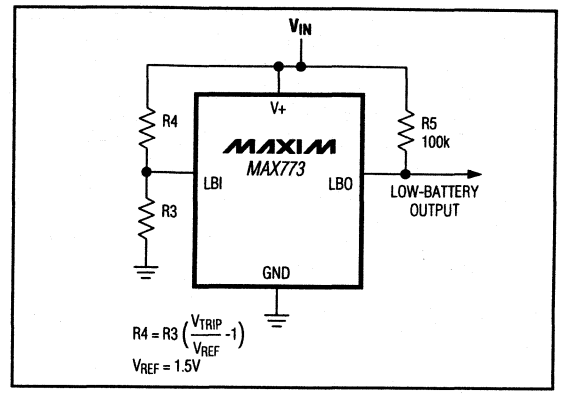


Figure 9. Input Voltage Monitor Circuit

Low Input Voltage Operation

When using a power supply that decays with time (such as a battery), the N-FET transistor will operate in its linear region when the voltage at EXT approaches the threshold voltage of the FET, dissipating excessive power. Prolonged operation in this mode may damage the FET. This effect is much more significant in non-bootstrapped mode than in bootstrapped mode, since bootstrapped mode typically provides much higher V_{GS} voltages. To avoid this condition, make sure V_{EXT} is above the V_{TH} of the FET, or use a voltage detector (such as the MAX8211) to put the IC in shutdown mode once the input supply voltage falls below a predetermined minimum value. Excessive loads with low input voltages can also cause this condition.

Starting Up under Load

The *Typical Operating Characteristics* show the Start-Up Voltage vs. Load Current graph for bootstrapped-mode operation. This graph depends on the type of power switch used. The MAX770–MAX773 are not designed to start up under full load in bootstrapped mode with low input voltages.

Layout Considerations

Due to high current levels and fast switching waveforms, which radiate noise, proper PC board layout is

essential. Protect sensitive analog grounds by using a star ground configuration. Minimize ground noise by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise. Place input bypass capacitor C2 as close as possible to V+ and GND.

Excessive noise at the V+ input may falsely trigger the timing circuitry, resulting in short pulses at EXT. If this occurs it will have a negligible effect on circuit efficiency. If desired, place a 4.7µF directly across the V+ and GND pins (in parallel with the 0.1µF C2 bypass capacitor) to reduce the noise at V+.

Table 2. Component Suppliers

PRODUCTION	INDUCTORS	CAPACITORS	TRANSISTORS	DIODES
Surface Mount	Sumida CD54 series CDR125 series Coiltronics CTX20 series	Matsuo 267 series Sprague 595D series	N-FET Siliconix Si9410DY Si9420DY (high voltage) Motorola MTP3055EL MTD20N03HDL	Nihon EC10 series
Through Hole	Sumida RCH855 series RCH110 series Renco RL1284-18	Sanyo OS-CON series Nichicon PL series United Chemi-Con LXF series	NPN Zetex ZTX694B	Motorola 1N5817–1N5822 MUR115 (high voltage)

SUPPLIER	PHONE	FAX
Coiltronics	USA: (407) 241-7876	(407) 241-9339
Matsuo	USA: (714) 969-2491 Japan: 81-6-337-6450	(714) 960-6492 81-6-337-6456
Nichicon	USA: (708) 843-7500	(708) 843-2798
Nihon	USA: (805) 867-2555	(805) 867-2556
Renco	USA: (516) 586-5566	(516) 586-5562
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	81-3-3607-5144
United Chemi-Con	USA: (714) 255-9500	(714) 255-9400
Zetex	USA: (516) 543-7100 UK: 44-61-627-4963	(516) 864-7630 44-61-627-5467

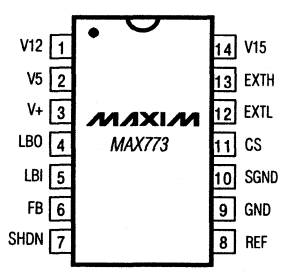
5V/12V/15V or Adjustable, High-Efficiency, Low IQ, Step-Up DC-DC Controllers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX771CPA	0°C to +70°C	8 Plastic DIP
MAX771CSA	0°C to +70°C	8 SO
MAX771C/D	0°C to +70°C	Dice*
MAX771EPA	-40°C to +85°C	8 Plastic DIP
MAX771ESA	-40°C to +85°C	8 SO
MAX771MJA	-55°C to +125°C	8 CERDIP
MAX772CPA	0°C to +70°C	8 Plastic DIP
MAX772CSA	0°C to +70°C	8 SO
MAX772C/D	0°C to +70°C	Dice*
MAX772EPA	-40°C to +85°C	8 Plastic DIP
MAX772ESA	-40°C to +85°C	8 SO
MAX772MJA	-55°C to +125°C	8 CERDIP
MAX773CPD	0°C to +70°C	14 Plastic DIP
MAX773CSD	0°C to +70°C	14 SO
MAX773C/D	0°C to +70°C	Dice*
MAX773EPD	-40°C to +85°C	14 Plastic DIP
MAX773ESD	-40°C to +85°C	14 Narrow SO
MAX773MJD	-55°C to +125°C	14 CERDIP

Pin Configurations (continued)

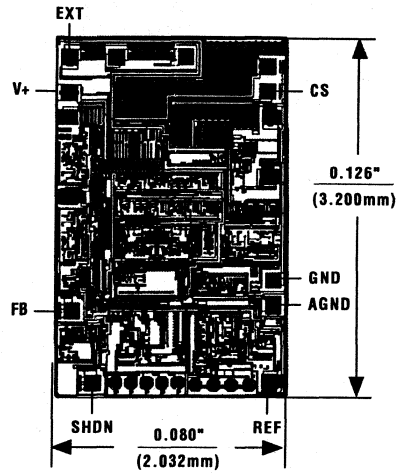
TOP VIEW



DIP/SO

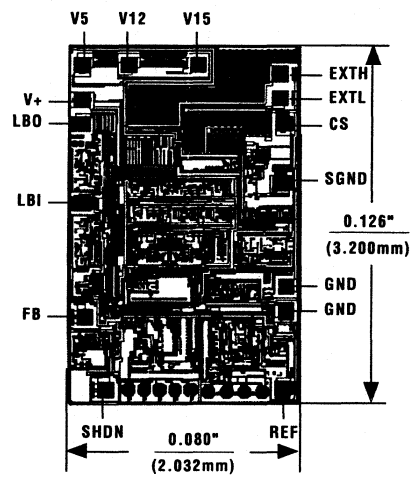
Chip Topographies

MAX770/MAX771/MAX772



TRANSISTOR COUNT: 501;
SUBSTRATE CONNECTED TO V+.

MAX773



TRANSISTOR COUNT: 501;
SUBSTRATE CONNECTED TO V+.

19-0191; Rev 1; 3/94

EVALUATION KIT AVAILABLE

MAXIM

-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

General Description

The MAX774/MAX775/MAX776 inverting switching regulators deliver high efficiency over three decades of load current. A unique current-limited, pulse-frequency-modulated (PFM) control scheme provides the benefits of pulse-width modulation (high efficiency with heavy loads), while using less than 100µA of supply current (vs. 2mA to 10mA for PWM converters). The result is high efficiency over a wide range of loads.

These ICs also use tiny external components; their high switching frequency (up to 300kHz) allows for less than 5mm diameter surface-mount magnetics.

The MAX774/MAX775/MAX776 accept input voltages from 3V to 16.5V, and have preset output voltages of -5V, -12V, and -15V, respectively. Or, the output voltage can be user-adjusted with two resistors. Maximum V_{IN} - V_{OUT} differential voltage is limited only by the breakdown voltage of the chosen external switch transistor.

These inverters use external P-channel MOSFET switches, allowing them to power loads up to 5W. If less power is required, use the MAX764/MAX765/MAX766 inverting switching regulators with on-board MOSFETs.

Applications

LCD-Bias Generators

High-Efficiency DC-DC Converters

Battery-Powered Applications

Data Communicators

Features

- ♦ **85% Efficiency for 5mA to 1A Load Currents**
- ♦ **Up to 5W Output Power**
- ♦ **100µA Max Supply Current**
- ♦ **5µA Max Shutdown Current**
- ♦ **3V to 16.5V Input Range**
- ♦ **-5V (MAX774), -12V (MAX775), -15V (MAX776), or Adjustable Output Voltage**
- ♦ **Current-Limited PFM Control Scheme**
- ♦ **300kHz Switching Frequency**

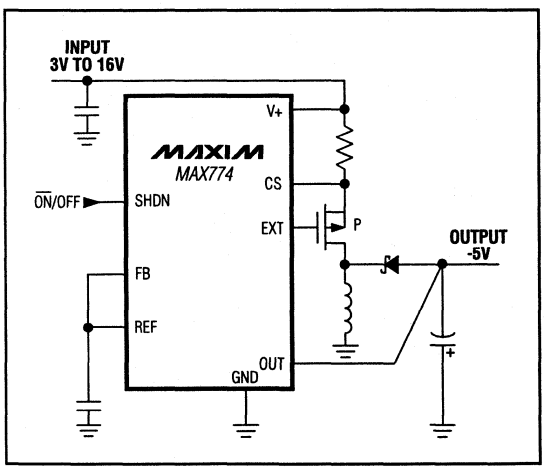
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX774CPA	0°C to +70°C	8 Plastic DIP
MAX774CSA	0°C to +70°C	8 SO
MAX774C/D	0°C to +70°C	Dice*
MAX774EPA	-40°C to +85°C	8 Plastic DIP
MAX774ESA	-40°C to +85°C	8 SO
MAX774MJA	-55°C to +125°C	8 CERDIP

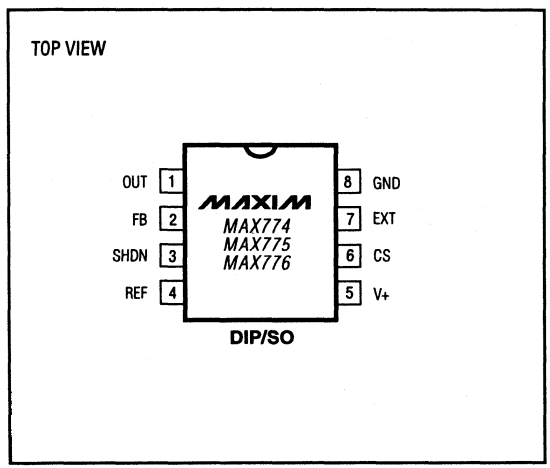
Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V+ to OUT 21V
- V+ to GND ..... -0.3V, +17V
- OUT to GND ..... -0.3V, to -17V
- REF, SHDN, FB, CS ..... -0.3V to (V+ + 0.3V)
- EXT ..... (V_{OUT} - 0.3V) to (V+ + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX77_C__ ..... 0°C to +70°C
- MAX77_E__ ..... -40°C to +85°C
- MAX77_MJA ..... -55°C to +125°C

Maximum Junction Temperatures:
- MAX77_C__/E__ ..... +150°C
- MAX77_MJA ..... +175°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, I_{LOAD} = 0mA, C_{REF} = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V+ Input Voltage Range	V+			3.0		16.5	V
Supply Current		V+ = 16.5V, SHDN ≤ 0.4V (operating)				100	µA
		V+ = 10V, SHDN ≥ 1.6V (shutdown)			2	5	
		V+ = 16.5V, SHDN ≥ 1.6V (shutdown)			4		
FB Trip Point		3V ≤ V+ ≤ 16.5V		-10		10	mV
FB Input Current	I_{FB}	MAX77_C				±50	nA
		MAX77_E				±70	
		MAX77_M				±90	
Output Voltage	V_{OUT}	MAX774		-4.80	-5	-5.20	V
		MAX775		-11.52	-12	-12.48	
		MAX776		-14.40	-15	-15.60	
Reference Voltage	V_{REF}	I_{REF} = 0µA	MAX77_C	1.4700	1.5	1.5300	V
			MAX77_E	1.4625	1.5	1.5375	
			MAX77_M	1.4550	1.5	1.5450	
REF Load Regulation		0µA ≤ I_{REF} ≤ 100µA	MAX77_C/E		4	10	mV
			MAX77_M		4	15	
REF Line Regulation		3V ≤ V+ ≤ 16.5V			40	100	µV/V
Output Voltage Line Regulation (Circuit of Figure 2—Bootstrapped)		MAX774, 4V ≤ V+ ≤ 15V, I_{LOAD} = 0.5A			0.035		mV/V
		MAX775, 4V ≤ V+ ≤ 8V, I_{LOAD} = 0.2A			0.088		
		MAX776, 4V ≤ V+ ≤ 6V, I_{LOAD} = 0.1A			0.137		
Output Voltage Load Regulation (Circuit of Figure 2—Bootstrapped)		MAX774, 0A ≤ I_{LOAD} ≤ 1A, V+ = 5V			1.5		mV/A
		MAX775, 0mA ≤ I_{LOAD} ≤ 500mA, V+ = 5V			1.5		
		MAX776, 0mA ≤ I_{LOAD} ≤ 400mA, V+ = 5V			1.0		

ELECTRICAL CHARACTERISTICS (continued)

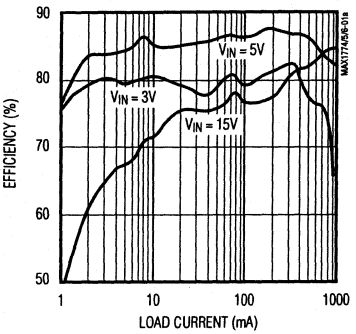
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Efficiency (Circuit of Figure 2—Bootstrapped)		MAX774, V+ = 5V, I_{LOAD} = 1A			82		%
		MAX775, V+ = 5V, I_{LOAD} = 500mA			88		
		MAX776, V+ = 5V, I_{LOAD} = 400mA			87		
SHDN Input Current		V+ = 16.5V, SHDN = 0V or V+				±1	µA
SHDN Input Voltage High	V_{IH}	3V ≤ V+ ≤ 16.5V		1.6			V
SHDN Input Voltage Low	V_{IL}	3V ≤ V+ ≤ 16.5V				0.4	V
Current-Limit Trip Level (V+ – CS)	V_{CS}	3V ≤ V+ ≤ 16.5V	MAX77_C/E	180	210	240	mV
			MAX77_M	160	210	260	
CS Input Current						±1	µA
Switch Maximum On-Time	t_{ON} (max)	V+ = 12V		12	16	20	µs
Switch Minimum Off-Time	t_{OFF} (max)	V+ = 12V		1.8	2.3	2.8	µs
EXT Rise Time		C_{EXT} = 1nF, V+ = 12V			50		ns
EXT Fall Time		C_{EXT} = 1nF, V+ = 12V			50		ns

-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

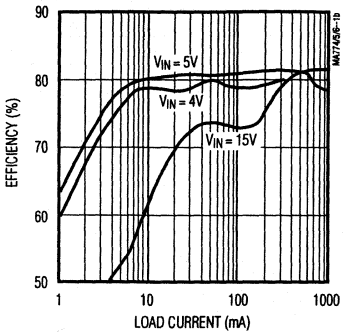
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

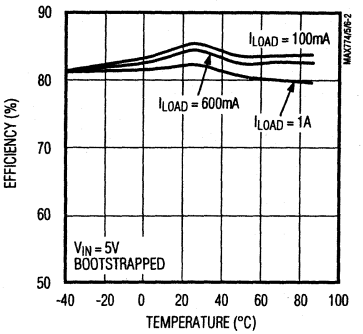
MAX774
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = -5V (BOOTSTRAPPED)



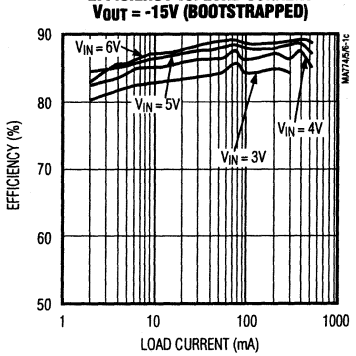
MAX774
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = -5V (NON-BOOTSTRAPPED)



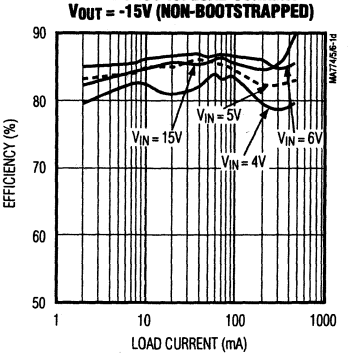
MAX774
EFFICIENCY vs. TEMPERATURE



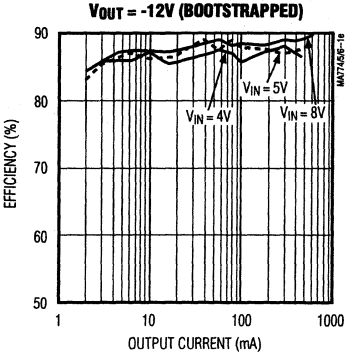
MAX776
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = -15V (BOOTSTRAPPED)



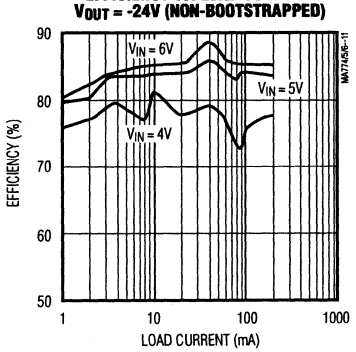
MAX776
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = -15V (NON-BOOTSTRAPPED)



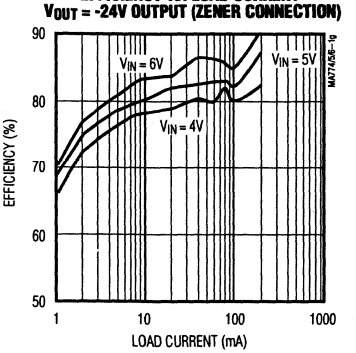
MAX775
EFFICIENCY vs. OUTPUT CURRENT
V_{OUT} = -12V (BOOTSTRAPPED)



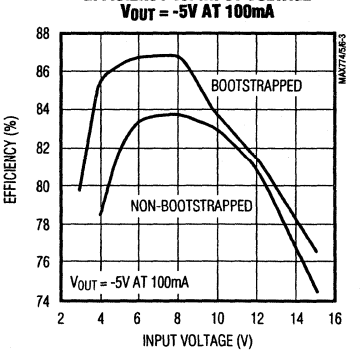
MAX774/MAX775/MAX776
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = -24V (NON-BOOTSTRAPPED)



MAX774/MAX775/MAX776
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = -24V OUTPUT (ZENER CONNECTION)



MAX774
EFFICIENCY vs. INPUT VOLTAGE
V_{OUT} = -5V AT 100mA

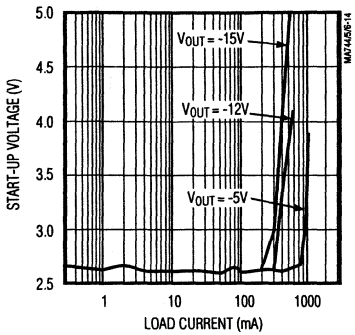


-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

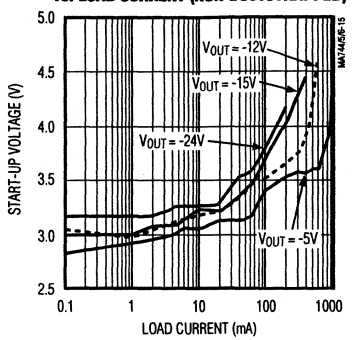
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

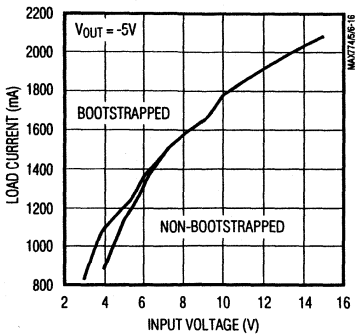
START-UP VOLTAGE vs. LOAD CURRENT (BOOTSTRAPPED)



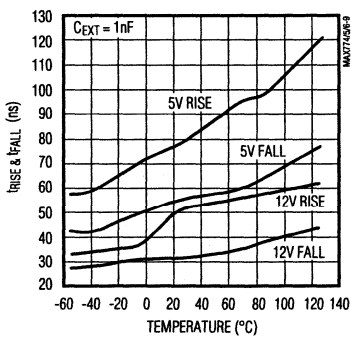
START-UP VOLTAGE vs. LOAD CURRENT (NON-BOOTSTRAPPED)



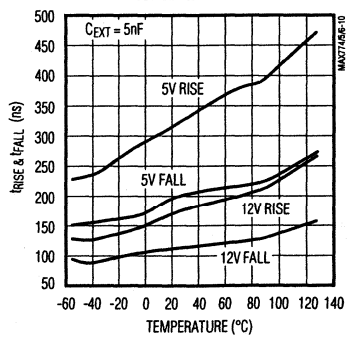
MAX774 MAXIMUM LOAD vs. INPUT VOLTAGE



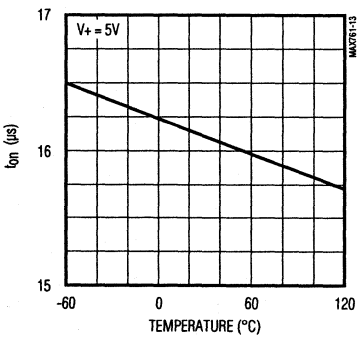
EXT RISE AND FALL TIMES vs. TEMPERATURE



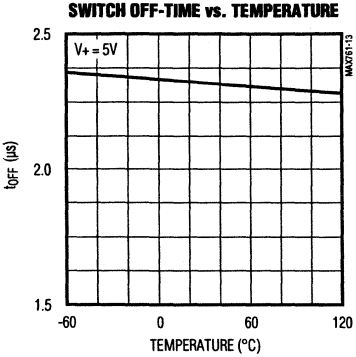
EXT RISE AND FALL TIMES vs. TEMPERATURE



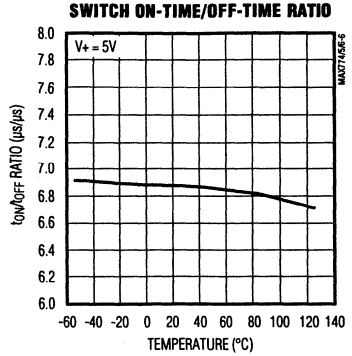
SWITCH ON-TIME vs. TEMPERATURE



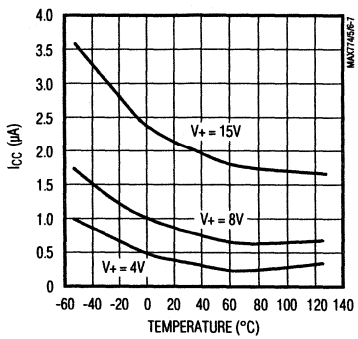
SWITCH OFF-TIME vs. TEMPERATURE



SWITCH ON-TIME/OFF-TIME RATIO



SHUTDOWN CURRENT vs. TEMPERATURE

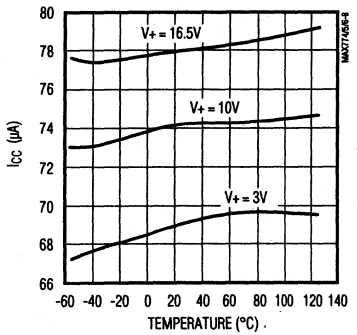


-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

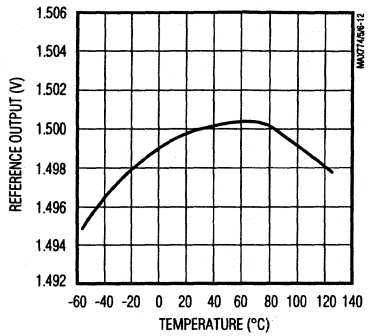
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

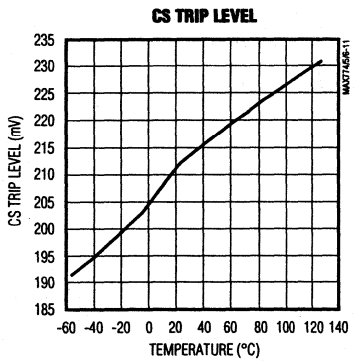
OPERATING SUPPLY CURRENT vs. TEMPERATURE



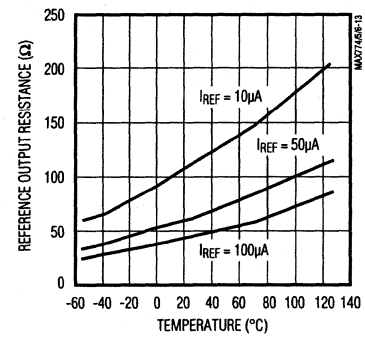
REFERENCE TEMPERATURE COEFFICIENT



CS TRIP LEVEL



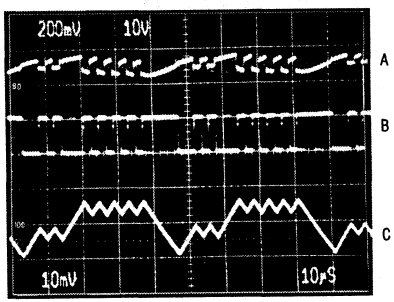
REFERENCE OUTPUT RESISTANCE



Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

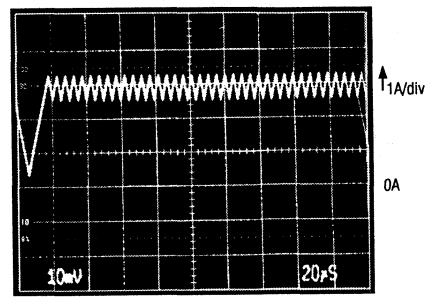
OPERATING WAVEFORMS



10µs/div

CIRCUIT OF FIGURE 2
V+ = 6.5V, I_{LOAD} = 1A, V_{OUT} = -5V
A: OUTPUT RIPPLE, 200mV/div
B: EXT WAVEFORM, 10V/div
C: INDUCTOR CURRENT, 2A/div

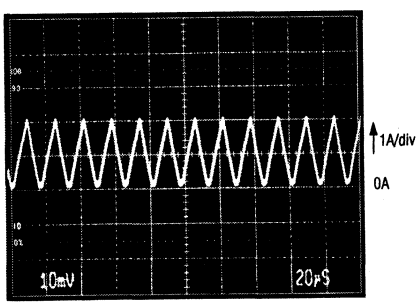
INDUCTOR CURRENT NEAR FULL LOAD



20µs/div

CIRCUIT OF FIGURE 2
V_{OUT} = -5V, V+ = 4.7V
I_{LOAD} = 1.05A (1A/div)

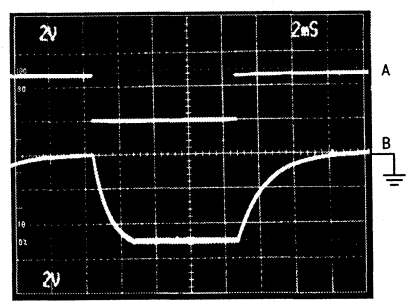
CONTINUOUS CONDUCTION AT ONE-HALF CURRENT LIMIT



20µs/div

CIRCUIT OF FIGURE 2
I_{LOAD} = 300mA, V_{OUT} = -5V
V+ = 8V, L = 22µH

ENTRY/EXIT FROM SHUTDOWN



2ms/div

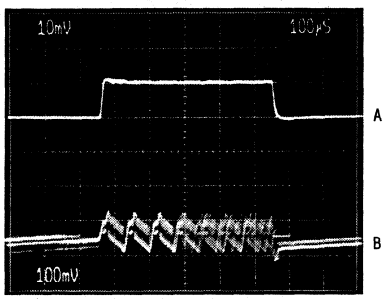
CIRCUIT OF FIGURE 2
V+ = 6V, I_{LOAD} = 1A, V_{OUT} = -5V
A: SHUTDOWN PULSE, 0V TO V+, 5V/div
B: V_{OUT}, 2V/div

-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

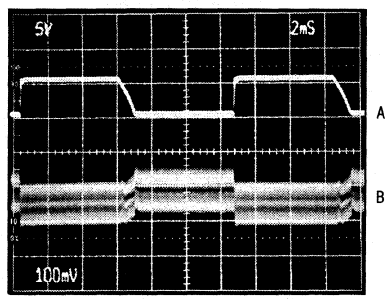
LOAD-TRANSIENT RESPONSE



100µs/div

CIRCUIT OF FIGURE 2
V_+ = 6V, V_{OUT} = -5V
A: I_{LOAD}, 30mA TO 1A, 1A/div
B: V_{OUT}, 100mV/div, AC-COUPLED

LINE-TRANSIENT RESPONSE



2ms/div

CIRCUIT OF FIGURE 2
V_{OUT} = -5V, I_{LOAD} = 1A
A: V_+, 3V TO 8V, 5V/div
B: V_{OUT}, 100mV/div, AC-COUPLED

Pin Description

PIN	NAME	FUNCTION
1	OUT	The sense input for fixed-output operation (V_{FB} = V_{REF}). OUT is connected to the internal voltage divider, and it is the negative supply input for the EXT driver.
2	FB	Feedback input. When V_{FB} = V_{REF}, the output will be the factory preset value. For adjustable operation, use an external voltage divider, as described in the *Adjustable Output* section.
3	SHDN	Active-high shutdown input. With SHDN high, the part is in shutdown mode and the supply current is less than 5µA. Connect to GND for normal operation.
4	REF	1.5V reference output that can source 100µA. Bypass to ground with 0.1µF.
5	V+	Positive power-supply input
6	CS	Noninverting input to the current-sense comparator. Typical trip level is 210mV (relative to V+).
7	EXT	The gate-drive output for an external P-channel power MOSFET. EXT swings from OUT to V+.
8	GND	Ground

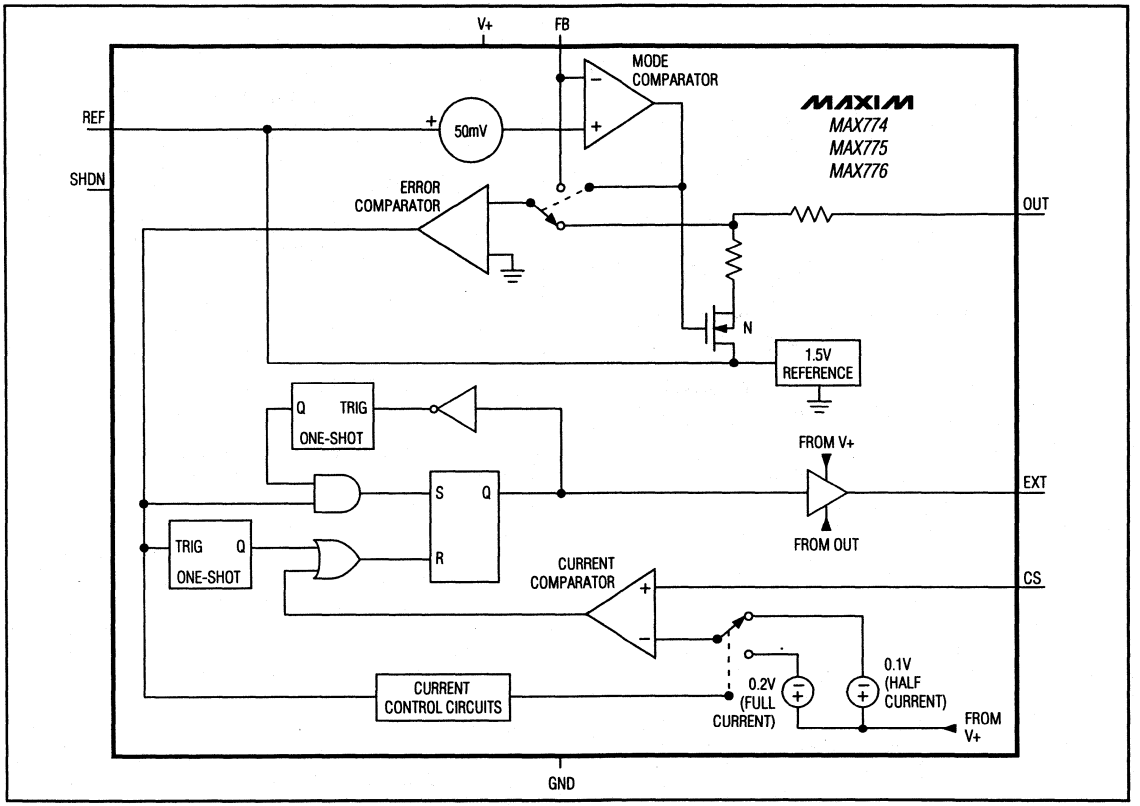


Figure 1. Block Diagram

Detailed Description

The MAX774/MAX775/MAX776 are negative-output, inverting power controllers that can be configured to drive an external P-channel MOSFET. The output voltages are preset to -5V (MAX774), -12V (MAX775), or -15V (MAX776). Additionally, all three parts can be set to any desired output voltage using an external resistor divider.

The MAX774/MAX775/MAX776 have a unique control scheme (Figure 1) that combines the advantage of pulse-skipping, pulse-frequency-modulation (PFM) converters (ultra-low supply current) with the advantage of pulse-width-modulation (PWM) converters (high efficiency with heavy loads). This control scheme allows the devices to achieve 85% efficiency with loads from 5mA to 1A.

As with traditional PFM converters, the external P-channel MOSFET power transistor is turned on when the voltage comparator senses that the output is below the reference voltage. However, unlike traditional PFM converters, switching is controlled by the combination of a switch current limit (210mV/R_{SENSE}) and on-time/off-time limits set by one-shots. Once turned on, the MOSFET stays on until:

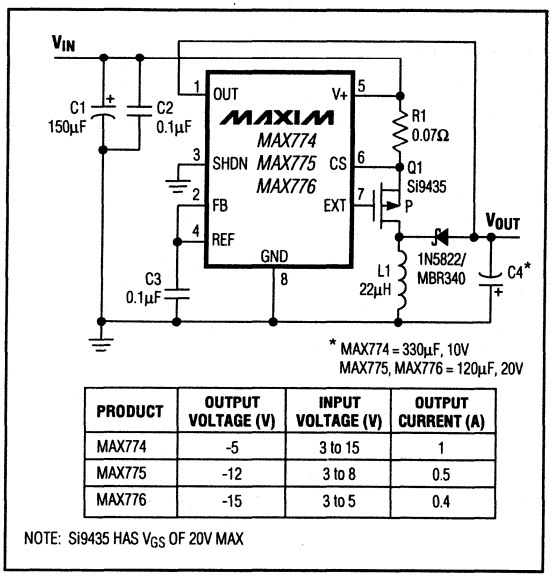
1) the 16µs maximum on-time limit is reached

or

2) the switch current reaches its limit (as set by the current-sense resistor).

Once off, the switch is typically held off for a minimum of 2.3µs. It will stay off until the output drops below the level determined by V_{REF} and the feedback divider network.

-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers



PRODUCT	OUTPUT VOLTAGE (V)	INPUT VOLTAGE (V)	OUTPUT CURRENT (A)
MAX774	-5	3 to 15	1
MAX775	-12	3 to 8	0.5
MAX776	-15	3 to 5	0.4

NOTE: Si9435 HAS V_{GS} OF 20V MAX

Figure 2. Bootstrapped Connection Using Fixed Output Voltages

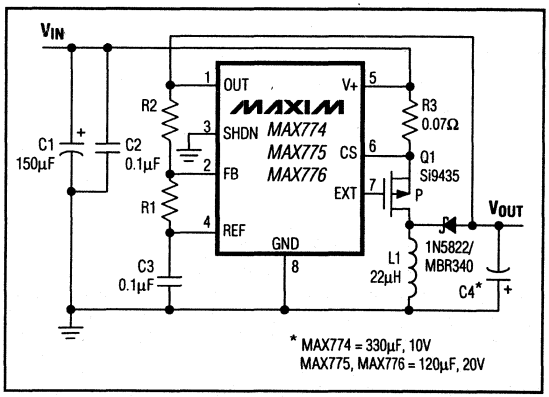


Figure 3. Bootstrapped Connection Using External Feedback Resistors

With light loads, the MOSFET switches on for one or more cycles and then switches off, much like in traditional PFM converters. To increase light-load efficiency, the current limit for the first two pulses is set to one-half the peak current limit. If those pulses bring the output voltage into regulation, the voltage comparator keeps

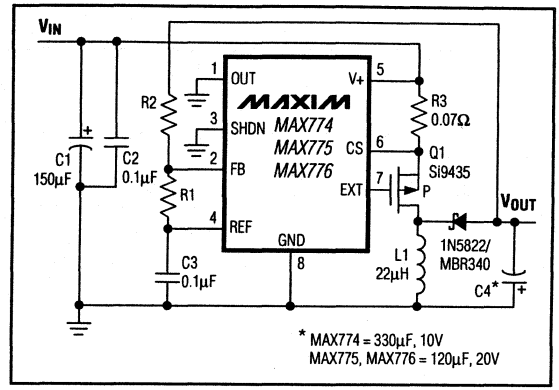


Figure 4. Non-Bootstrapped Operation (V_{IN} > 4.5V)

the MOSFET off, and the current limit remains at one-half the peak current limit. If the output voltage is out of regulation after two consecutive pulses, the current limit for the next pulse will equal the full current limit.

With heavy loads, the MOSFET first switches twice at one-half the peak current value. Subsequently, it stays on until the switch current reaches the full current limit, and then turns off. After it is off for 2.3µs, the MOSFET switches on once more, and remains on until the switch current again reaches its limit. This cycle repeats until the output is in regulation.

A benefit of this control scheme is that it is highly efficient over a wide range of input/output ratios and load currents. Additionally, PFM converters do not operate with constant-frequency switching, and have relaxed stability criterion (unlike PWM converters). As a result, their external components require smaller values.

With PFM converters, the output voltage ripple is not concentrated at the oscillator frequency (as it is with PWM converters). So for applications where the ripple frequency is important, the PWM control scheme must be used. However, for many other applications, the smaller capacitors and lower supply current of the PFM control scheme make it the better choice. The output voltage ripple with the MAX774/MAX775/MAX776 can be held quite low. For example, using the circuit of Figure 2, only 100mV of output ripple is produced when generating a -5V at 1A output from a +5V input.

Bootstrapped vs. Non-Bootstrapped Operation

Figures 2 and 3 are the standard application circuits for bootstrapped mode, and Figure 4 is the circuit for non-bootstrapped mode. Since EXT is powered by OUT,

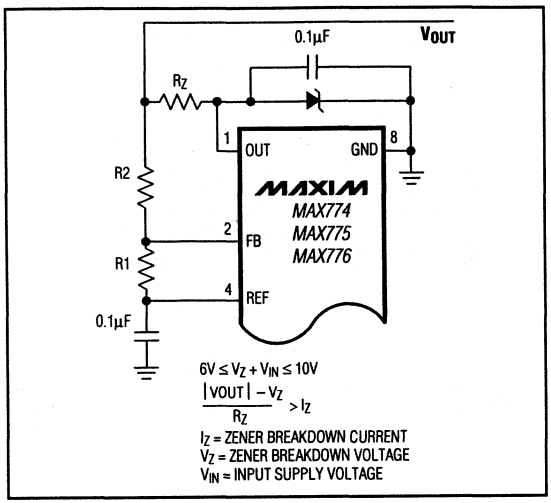


Figure 5. Connection Using Zener Diode to Boost Base Drive

using bootstrapped or non-bootstrapped mode will directly affect the gate drive to the FET. EXT swings from V+ to V_{OUT}. In bootstrapped operation, OUT is connected to the output voltage (-5V, -12V, -15V). In non-bootstrapped operation, OUT is connected to ground, and EXT now swings from V+ to ground.

At high input-to-output differentials, it may be necessary to use non-bootstrapped mode to avoid the 21V V+ to V_{OUT} maximum rating. Also, observe the V_{GS} maximum rating of the external transistor. At intermediate voltages and currents, the advantages of bootstrapped vs. non-bootstrapped operation are slight. When input voltages are less than about 4V, always use the bootstrapped circuit.

Shutdown and Quiescent Current

The MAX774/MAX775/MAX776 are designed to save power in battery-powered applications. A TTL/CMOS logic-level shutdown input (SHDN) has been provided for the lowest-power applications. When shut down (SHDN = V+), most internal bias current sources and the reference are turned off so that less than 5µA of current is drawn.

In normal operation, the quiescent current will be less than 100µA. However, this current is measured by forcing the external switch transistor off. Even with no load, in an actual application, additional current will be drawn to supply the feedback resistors' and the diode's and capacitor's leakage current. Under no-load conditions, you should see a short current pulse at half the peak current approximately every 100ms (the exact period depends on actual circuit leakages).

EXT Drive Voltages

EXT swings from OUT to V+ and provides the drive output for an external power MOSFET. When using the on-chip feedback resistors for the preset output voltages, the voltage at OUT equals the output voltage. When using external feedback resistors, OUT may be tied to GND or some other potential between V_{OUT} and GND.

Always observe the V+ to OUT absolute maximum rating of 21V. For V+ to output differentials greater than 21V, OUT must be tied to a potential more positive than the output and, therefore, the output voltage must be set with an external resistor divider.

In non-bootstrapped operation with low input voltages (<4V), tie OUT to a negative voltage to fully enhance the external MOSFET. Accomplish this by creating an intermediate voltage for V_{OUT} with a zener diode (Figure 5).

Design Procedure

Setting the Output Voltage

The MAX774/MAX775/MAX776 are preset for -5V, -12V, and -15V output voltages, respectively; however, they may also be adjusted to other values with an external voltage divider. For the preset output voltage, connect FB to REF and connect OUT to the output (Figure 3). In this case, the output voltage is sensed by OUT.

For an adjustable output (Figures 3 and 4), connect an external resistor divider from the output voltage to FB, and from FB to REF. In this case, the divided-down output voltage is sensed via the FB pin.

There are three reasons to use the external resistor divider:

1) You desire an output voltage other than a preset value
2) The input-to-output differential exceeds 21V

or

3) The output voltage (V_{OUT} to GND) exceeds -15V.

For adjustable operation, refer to Figures 3 and 4. The impedance of the feedback network should be low enough that the input bias current of FB is not a factor. For best efficiency and precision, allow 10µA to flow through the network. Calculate (V_{REF} - V_{FB}) / R1 = 10µA. Since V_{REF} = 1.5V and V_{FB} = 0V, R1 becomes 150kΩ. Then calculate R2 as follows:

$$\frac{R2}{R1} = \frac{V_{OUT}}{V_{REF}}$$

$$\left(\text{or, } \frac{V_{OUT}}{R2} = 10\mu A\right)$$

-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

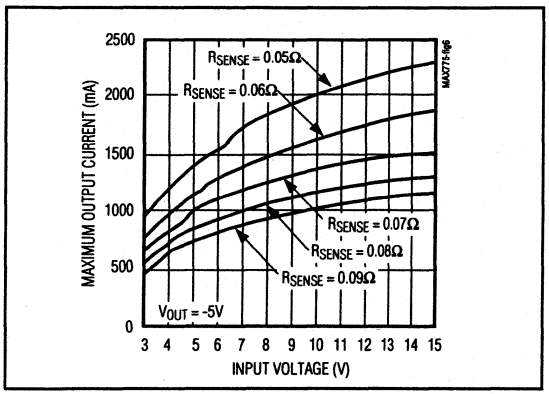


Figure 6. MAX774 Maximum Output Current vs. Input Voltage (V_{OUT} = -5V)

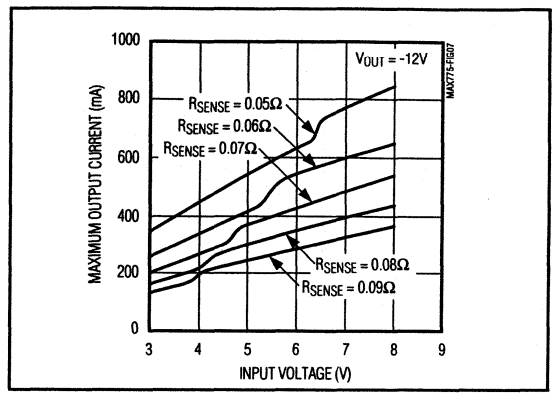


Figure 7. MAX775 Maximum Output Current vs. Input Voltage (V_{OUT} = -12V)

Choosing an Inductor

Practical inductor values range from 10µH to 50µH. The maximum inductor value is not particularly critical. For highest current at high $|V_{OUT}|$ to V+ ratios, the inductor should not be so large that the peak current never reaches the current limit. That is:

$$L(max) \leq \frac{[V+(min) - V_{SW}(max)] \times 12\mu s}{I_{LIM}(max)}$$

This is only important if

$$\left|\frac{V_{IN}}{V_{OUT}}\right| < \frac{1}{6} = \frac{t_{OFF}(min)}{t_{ON}(max)}$$

More important is that the inductor not be so small that the current rises much faster than the current-limit comparator can respond. This would be wasteful and reduce efficiency. Calculate the minimum inductor value as follows:

$$L(min) \geq \frac{[V+(max) - V_{SW}(min)] \times 0.3\mu s}{\delta(I) \times I_{LIM}(min)}$$

Where L is in µH, 0.3µs is an ample time for the comparator response, I_{LIM} is the current limit (see *Current-Sense Resistor* section), and δ(I) is the allowable percentage of overshoot. As an example, Figure 2's circuit uses a 3A peak current. If we allow a 15% overshoot and 15V is the maximum input voltage, then L(min) is 16µH. The actual value of L above this limit has minimal effect on this circuit's operation.

For highest efficiency, use a coil with low DC resistance. Coils with 30mΩ or lower resistance are available. To minimize radiated noise, use a torroid, pot-core, or shielded-bobbin inductor. Inductors with a ferrite core or equivalent are recommended. Make sure that the inductor's saturation current rating is greater than I_{LIM}(max).

Diode Selection

The ICs' high switching frequencies demand a high-speed rectifier. Schottky diodes such as the 1N5817 to 1N5822 families are recommended. Choose a diode with an average current rating approximately equal to or greater than I_{LIM} (max) and a voltage rating higher than V_{IN}(max) + V_{OUT}. For high-temperature applications, Schottky diodes may be inadequate due to their high leakage currents; instead, high-speed silicon diodes may be used. At heavy loads and high temperature, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantages of its high leakage current.

Current-Sense Resistor

The current-sense resistor limits the peak switch current to 210mV/R_{SENSE}, where R_{SENSE} is the value of the current-sense resistor, and 210mV is the current-sense comparator threshold (see Current-Limit Trip Level in the *Electrical Characteristics*).

To maximize efficiency and reduce the size and cost of external components, minimize the peak current. However, since the output current is a function of the peak current, do not set the limit too low. Refer to Figures 6–9 to determine the sense resistor (and, therefore, peak current) for the required load current.

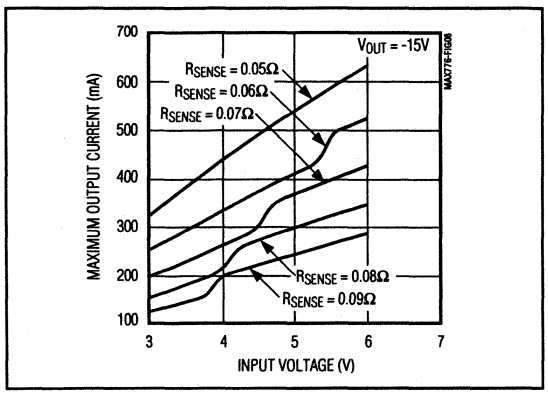


Figure 8. MAX776 Maximum Output Current vs. Input Voltage (V_{OUT} = -15V)

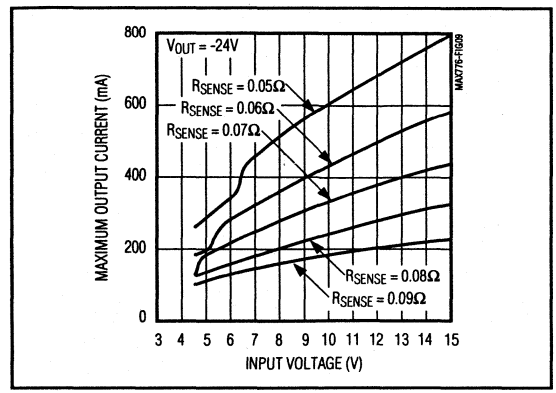


Figure 9. MAX774/MAX775/MAX776 Maximum Output Current vs. Input Voltage (V_{OUT} = -24V)

To choose the proper current-sense resistor, simply follow the two-step procedure outlined below.

1) Determine:
   - Input voltage range, V+
   - Maximum (absolute) output voltage, V_{OUT}
   - Maximum output current, I_{LOAD}

For example, let V+ range from 4V to 6V, and choose V_{OUT} = -24V and I_{OUT} = 150mA.

2) Next, referring to Figure 9, find the curve with the lowest current limit whose output current (with the lowest input voltage) meets your requirements.

In our example, we want a curve where I_{OUT} is >150mA with a 4V input and a -24V output.

The R_{SENSE} = 80mΩ (shown in Figure 9) shows only approximately 125mA of output current with a 4V input, so we look next at the R_{SENSE} = 70mΩ line. It shows I_{OUT} >150mA for V+ = 4V and V_{OUT} = -24V. The current limit will be 0.210V / 0.070Ω = 3A. These curves take into account worst-case inductor (±10%) and current-sense trip levels, but not sense-resistor tolerance. The switch on resistance is 70mΩ.

Standard wire-wound and metal-film resistors have an inductance high enough to degrade performance. Metal-film resistors are usually deposited on a ceramic rod in a spiral, making their inductances relatively high. Surface-mount (or chip) resistors have very little inductance and are well suited for use as current-sense resistors. If you want to use through-hole resistors, IRC has a wire resistor that is simply a band of metal shaped as a "U" so that inductance is less than 10nH (an order of magnitude less than metal-film resistors). These are available in resistance values between 5mΩ and 0.1Ω.

External Switching Transistor

The MAX774/MAX775/MAX776 are capable of driving P-channel enhancement-mode MOSFET transistors only. The choice of power transistor is dictated by input and output voltage, peak current rating, on resistance, gate-source threshold, and gate capacitance. The drain-to-source rating must be greater than the V+ - V_{OUT} input-to-output voltage differential. The gate-to-source rating must be greater than V+ (the source voltage) plus the absolute value of the most negative swing of EXT. For bootstrapped operation, the most negative swing of EXT is V_{OUT}. In non-bootstrapped operation, this may be ground or some other negative voltage. Gate capacitance is not normally a limiting factor, but values should be less than 1nF for best efficiency. For maximum efficiency, the MOSFET should have a very low on resistance at the peak current and be capable of handling that current. The transistor chosen for the typical operating circuit has a 30V drain-source voltage limit and a 0.07Ω drain-source on resistance at V_{GS} = -10V.

Table 1 lists suppliers of switching transistors suitable for use with the MAX774/MAX775/MAX776.

-5V/-12V/-15V or Adjustable, High-Efficiency, Low I_Q Inverting DC-DC Controllers

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coiltronics	(407) 241-7876	(407) 241-9339
Gowanda	(716) 532-2234	(716) 532-2702
Sumida USA	(708) 956-0666	(708) 956-0702
Sumida Japan	81-3-3607-5111	81-3-3607-5144
CAPACITORS		
Kemet	(803) 963-6300	(803) 963-6322
Matsuo	(714) 969-2491	(714) 960-6492
Nichicon	(708) 843-7500	(708) 843-2798
Sanyo USA	(619) 661-6835	(619) 661-1055
Sanyo Japan	81-7-2070-6306	81-7-2070-1174
Sprague	(603) 224-1961	(603) 224-1430
United Chemi-Con	(714) 255-9500	(714) 255-9400
DIODES		
Motorola	(800) 521-6274	(602) 952-4190
Nihon USA	(805) 867-2555	(805) 867-2556
Nihon Japan	81-3-3494-7411	81-3-3494-7414
POWER MOSFETS		
Harris	(407) 724-3729	(407) 724-3937
International Rectifier	(310) 322-3331	(310) 322-3332
Siliconix	(408) 988-8000	(408) 970-3950
CURRENT-SENSE RESISTORS		
IRC	(704) 264-8861	(704) 264-8866

Capacitors

Choose the output capacitor (C4 of Figures 2, 3, and 4) to be consistent with your size, ripple, and output voltage requirements. Place capacitors in parallel if the size you want is unobtainable. You will not only increase the capacitance, but also decrease the capacitor's ESR (a major contributor of ripple). A 330µF tantalum output filter capacitor with 0.07Ω ESR typically maintains $120mV_{p-p}$ output ripple when generating -5V at 1A from a 5V input. Smaller capacitors are acceptable for lighter loads or in applications that can tolerate higher output ripple.

The value of C4 is chosen such that it acquires as small a charge as possible during the switch on-time. The amount of ripple as a function of capacitance is give by:

$$\Delta V_{p-p} = \frac{V_{OUT} \times I_{OUT} \times ESR}{V_{IN}} + \frac{I_{OUT} \times t_{OFF(min)}}{C}$$

When evaluating this equation, be sure to use the capacitance value at the switching frequency. At 200kHz, the 330µF tantalum capacitor of Figures 2, 3, or 4 may degrade by a factor of ten, which will significantly alter the ripple voltage calculation.

The ESR of both the bypass and filter capacitors also affects efficiency. Best performance is obtained by doubling up on the filter capacitors or using low-ESR capacitors. Capacitors must have a ripple current rating equal to the peak current.

The smallest low-ESR SMT capacitors currently available are the Sprague 595D series. Sanyo OS-CON organic semiconductor through-hole capacitors also exhibit low ESR and are especially effective at low temperatures. Table 1 lists the phone numbers of these and other manufacturers.

PC Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. Use a star ground configuration; connect the ground lead of the input bypass capacitor, the output capacitor, the inductor, and the GND pin of the MAX774/MAX775/MAX776 at a common point very close to the device. Additionally, input capacitor C2 (Figures 3 and 4) should be placed extremely close to the device.

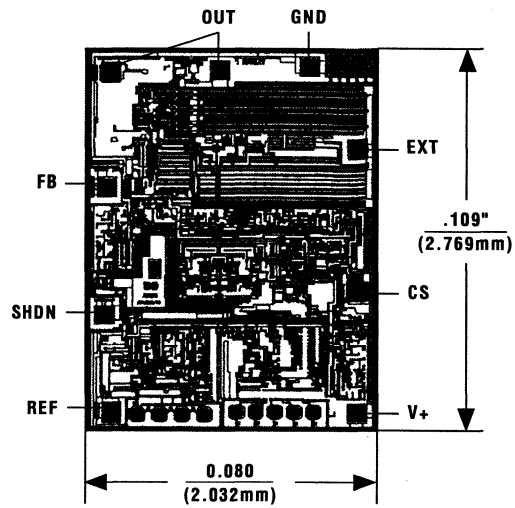
If an external resistor divider is used (Figures 3 and 4), the trace from FB to the resistors must be extremely short.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX775CPA	0°C to +70°C	8 Plastic DIP
MAX775CSA	0°C to +70°C	8 SO
MAX775C/D	0°C to +70°C	Dice*
MAX775EPA	-40°C to +85°C	8 Plastic DIP
MAX775ESA	-40°C to +85°C	8 SO
MAX775MJA	-55°C to +125°C	8 CERDIP
MAX776CPA	0°C to +70°C	8 Plastic DIP
MAX776CSA	0°C to +70°C	8 SO
MAX776C/D	0°C to +70°C	Dice*
MAX776EPA	-40°C to +85°C	8 Plastic DIP
MAX776ESA	-40°C to +85°C	8 SO
MAX776MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Chip Topography



TRANSISTOR COUNT: 442;
SUBSTRATE CONNECTED TO V+.

19-0186; Rev 0; 10/93

MAXIM

Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

General Description

The MAX777/MAX778/MAX779 are pulse-skipping DC-DC converters that step up from low-voltage inputs (1V guaranteed). They require only three external components—an inductor (typically 22µH) and two capacitors. The MAX777 delivers a 5V output, the MAX778 generates pin-selectable voltages of 3.0V or 3.3V, and the MAX779 output can be adjusted from 2.5V to 6V through an external resistive divider.

The devices include an Active Rectifier™ that eliminates the need for an external catch diode, and permits regulation even when the input is greater than the output. Also, unlike those in other step-up converters, the MAX777/MAX778/MAX779's Active Rectifier™ turns off in the shutdown mode, disconnecting the output from the source. This eliminates the current drain associated with conventional step-up converters when off or in shutdown.

High-frequency operation (up to 150kHz) allows the use of small, surface-mount inductors with values of 10µH or less. Supply current is 190µA under no load and only 20µA in standby mode; supply voltage can range from 1V to 6.2V (1 to 4 cells). With a 2V input, the devices typically deliver 200mA at 5V, or 300mA at 3V.

For fully specified devices designed for step-up/step-down applications (where the input can be above or below the output), refer to the MAX877/MAX878/MAX879 data sheet.

Applications

Single Battery-Cell (1V), Step-Up Voltage Conversion

Efficient, High-Power Step-Up Regulation from Low Input Voltages

Pagers

Portable Instruments & Hand-Held Terminals

Notebook and Palmtop Computers

Features

- ♦ **1V to 6.2V Input Guarantees Start-Up Under Load**
- ♦ **Up to 240mA Output**
- ♦ **Load Fully Disconnected in Shutdown**
- ♦ **82% Efficiency**
- ♦ **Output in Regulation with Input Voltage above Output Voltage**
- ♦ **Internal 1A Power Switch and Active Rectifier**
- ♦ **Adjustable Current Limit Allows Low-Cost Inductors**
- ♦ **190µA No Load Supply Current**
- ♦ **20µA Shutdown Supply Current**
- ♦ **3V/3.3V (MAX778), 5V (MAX777), and Adjustable (MAX779) Output Voltage**

Ordering Information

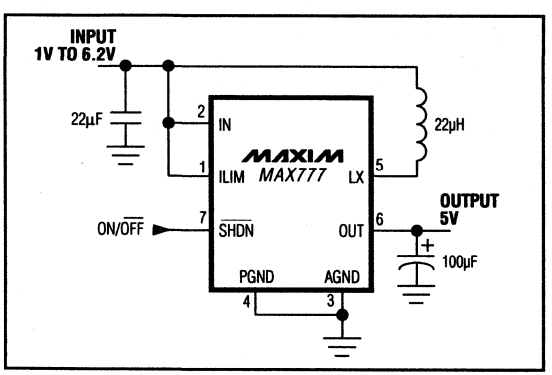
PART	TEMP. RANGE	PIN-PACKAGE
MAX777CPA	0°C to +70°C	8 Plastic DIP
MAX777CSA	0°C to +70°C	8 SO
MAX777C/D	0°C to +70°C	Dice*
MAX777EPA	-40°C to +85°C	8 Plastic DIP
MAX777ESA	-40°C to +85°C	8 SO
MAX777MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C, DC parameters only.*

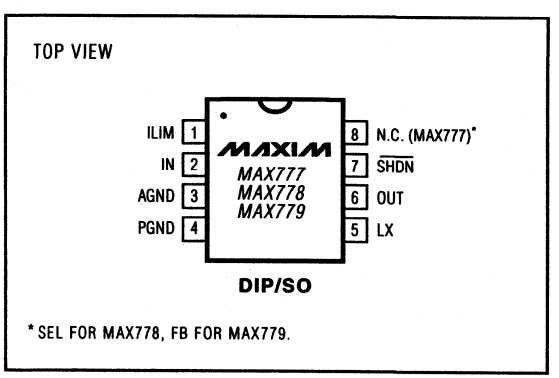
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



™Active Rectifier is a trademark of Maxim Integrated Products.

Pin Configuration



Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IN to PGND) ..... 0V to +7V
Output Short-Circuit Duration to PGND, AGND (Note 1) 30sec
Voltage Applied to:
LX (switch off) ..... -0.3V to +7V
(switch on) ..... 30sec short to IN or OUT
OUT, $\overline{SHDN}$ ..... -0.3V to +7V
FB ..... -0.3V to (OUT + 0.3V)
AGND to PGND ..... -0.3V, +0.3V
Reverse Battery Current 900mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges:
MAX77_C_A ..... 0°C to +70°C
MAX77_E_A ..... -40°C to +85°C
MAX77_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The output may be shorted to ground if the package power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +2.5V, I_{LOAD} = 0mA, L = 22µH, C_{OUT} = 100µF, $\overline{SHDN}$ and ILIM connected to IN, AGND connected to PGND, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Minimum Operating Voltage	I_{LOAD} < 10mA, T_A = +25°C (Note 2)					1	V
Maximum Operating	(Notes 2, 3)			6.2			V
Output Voltage MAX777/MAX779 (set to 5V)		MAX777C/ MAX779C	$I_{LOAD} \le 30mA$, $1.1V \le V_{IN} \le 5V$ or $I_{LOAD} \le 140mA$, $1.8V \le V_{IN} \le 5V$	4.80	5.00	5.20	V
		MAX777E/ MAX779E	$I_{LOAD} \le 30mA$, $1.2V \le V_{IN} \le 5V$ or $I_{LOAD} \le 130mA$, $1.8V \le V_{IN} \le 5V$				
		MAX777M/ MAX779M	$I_{LOAD} \le 25mA$, $1.25V \le V_{IN} \le 5V$ or $I_{LOAD} \le 120mA$, $1.8V \le V_{IN} \le 5V$				
Output Voltage MAX778	SEL = 0V	MAX778C	$I_{LOAD} \le 60mA$, $1.1V \le V_{IN} \le 3.3V$ or $I_{LOAD} \le 240mA$, $1.8V \le V_{IN} \le 3.3V$	3.17	3.30	3.43	V
		MAX778E	$I_{LOAD} \le 60mA$, $1.2V \le V_{IN} \le 3.3V$ or $I_{LOAD} \le 240mA$, $1.8V \le V_{IN} \le 3.3V$				
		MAX778M	$I_{LOAD} \le 50mA$, $1.25V \le V_{IN} \le 3.3V$ or $I_{LOAD} \le 200mA$, $1.8V \le V_{IN} \le 3.3V$				
	SEL = OPEN	MAX778C	$I_{LOAD} \le 60mA$, $1.1V \le V_{IN} \le 3V$ or $I_{LOAD} \le 240mA$, $1.8V \le V_{IN} \le 3V$	2.88	3.00	3.12	
		MAX778E	$I_{LOAD} \le 60mA$, $1.2V \le V_{IN} \le 3V$ or $I_{LOAD} \le 240mA$, $1.8V \le V_{IN} \le 3V$				
		MAX778M	$I_{LOAD} \le 50mA$, $1.25V \le V_{IN} \le 3V$ or $I_{LOAD} \le 200mA$, $1.8V \le V_{IN} \le 3V$				
Output Voltage Range (MAX779)	(Note 4)			2.5		6.0	V
Efficiency	I_{LOAD} = 100mA				82		%
No-Load Supply Current	I_{LOAD} = 0mA (switch off)				190	310	µA
Shutdown Supply Current	$\overline{SHDN}$ = 0V	MAX77_C, MAX77_E			20	30	µA
		MAX77_M			20	35	
$\overline{SHDN}$ Input Current	0V < $\overline{SHDN}$ < V_{IN}				15	100	nA
	V_{IN} < $\overline{SHDN}$ < 5V				12	40	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +2.5V, I_{LOAD} = 0mA, L = 22µH, C_{OUT} = 100µF, $\overline{SHDN}$ and ILIM connected to IN, AGND connected to PGND, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Threshold	V_{IN} = 1V to 6.2V		$V_{IN}/2 + 0.25$		V
	V_{IN} = 2.5V	1.20		1.6	
$\overline{SHDN}$ Enable Delay			150		µs
Current Limit			1.0		A
Current Limit Temperature Coefficient			-0.3		%/°C
Switch Saturation Voltage	I_{SW} = 400mA		0.275		V
	I_{SW} = 600mA		0.33		
	I_{SW} = 1000mA		0.50		
Maximum Switch On Time	V_{IN} = 2.5V		4.0		µs
	V_{IN} = 1.8V		5.9		
	V_{IN} = 1V		12.6		
Minimum Switch Off Time	MAX777, MAX779		1.2		µs
	MAX778		2.2		
Rectifier Forward Voltage Drop	I_{SW} = 400mA		0.21		V
	I_{SW} = 600mA		0.31		
	I_{SW} = 1000mA		0.50		
Error-Comparator Trip Point	MAX779, over operating input voltage (Note 5)	197.5	202.5	207.5	mV
FB Pin Bias Current	MAX779, V_{FB} = 0.3V		10	40	nA
Switch Off Leakage Current			0.1		µA
Rectifier Off Leakage Current			0.1		µA

Note 2: Output in regulation, V_{OUT} = V_{OUT} (nominal) ±4%.

Note 3: At high V_{IN} to V_{OUT} differentials, the maximum load current is limited by the maximum allowable power dissipation in the package (see *Absolute Maximum Ratings*).

Note 4: Minimum value is production tested. Maximum value is guaranteed by design and is not production tested.

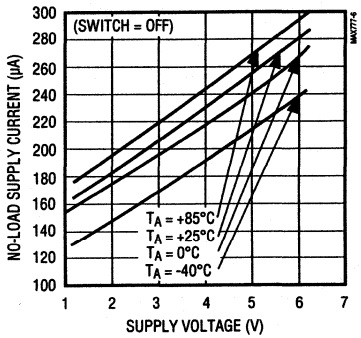
Note 5: V_{OUT} is set to a target value of +5V by 0.1% external feedback resistors. V_{OUT} is measured to be 5V ±2.5% to guarantee the error comparator trip point.

Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

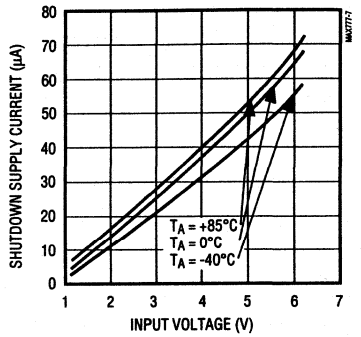
Typical Operating Characteristics

(Typical Operating Circuit, T_A = +25°C, unless otherwise noted).

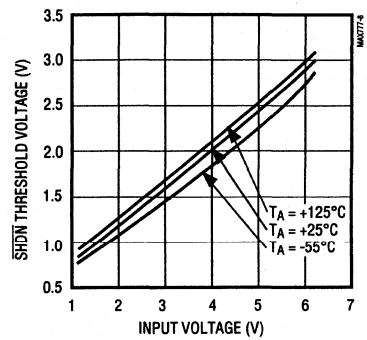
NO-LOAD SUPPLY CURRENT vs. VOLTAGE AND TEMPERATURE



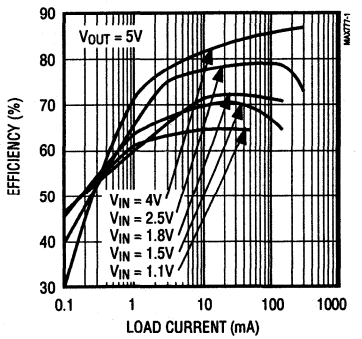
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE AND TEMPERATURE



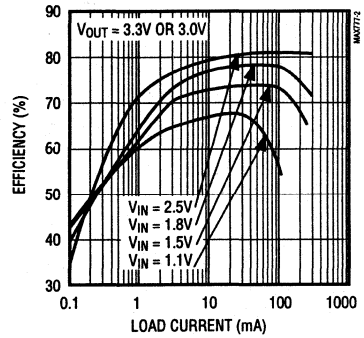
MAX778 SHDN THRESHOLD VOLTAGE vs. INPUT VOLTAGE AND TEMPERATURE



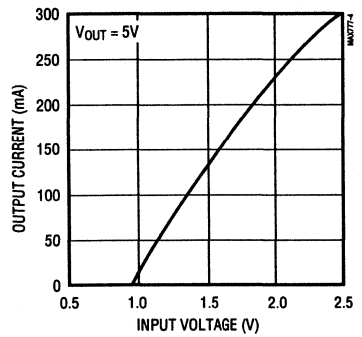
MAX777/MAX779 EFFICIENCY vs. LOAD CURRENT



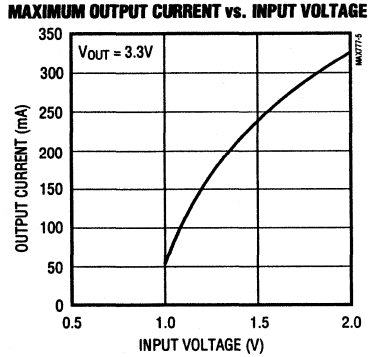
MAX778 EFFICIENCY vs. LOAD CURRENT



MAX777/MAX779 MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



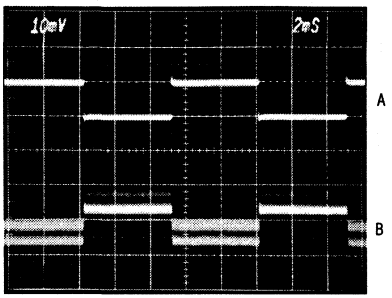
MAX778 MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE

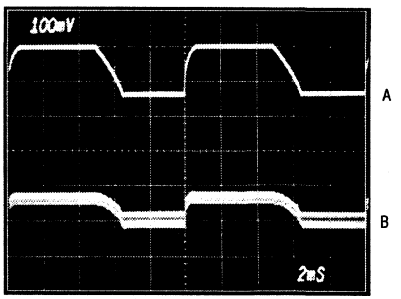


2ms/div

A: I_{OUT}, 200mA/div, 0mA to 200mA
B: V_{OUT}, 50mV/div, AC COUPLED

MAX778, V_{OUT} = 3.3V, V_{IN} = 2.5V

LINE-TRANSIENT RESPONSE

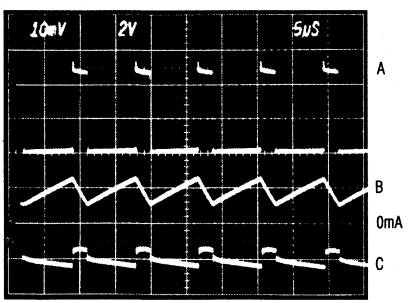


2ms/div

A: V_{IN}, 1V/div, 1.8V to 3.3V
B: V_{OUT}, 100mV/div, AC-COUPLED, I_{OUT} = 240mA

MAX778, V_{OUT} = 3.3V

SWITCHING WAVEFORMS, CONTINUOUS CONDUCTION

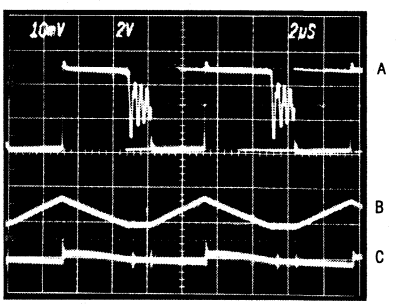


5µs/div

A: SWITCH VOTLAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 0.5A/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div, AC COUPLED

MAX777, V_{IN} = 1.5V, I_{OUT} = 100mA

SWITCHING WAVEFORMS, DISCONTINUOUS CONDUCTION



2µs/div

A: SWITCH VOTLAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 0.5A/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div, AC COUPLED

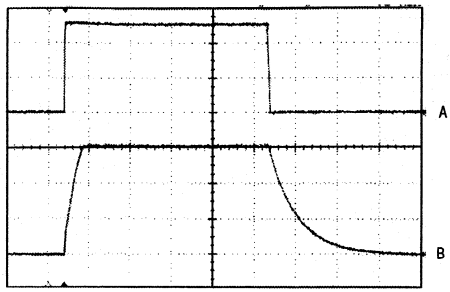
MAX777, V_{IN} = 3V, I_{OUT} = 70mA

Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

MAX778
START-UP TIME



10ms/div

A: $\overline{SHDN}$, 2V/div
B: V_{OUT}, 1V/div

V_{OUT} = 3V

Pin Description

PIN	NAME	FUNCTION
1	ILIM	Sets switch current-limit input. Connect to IN for 1A current limit. A resistor from ILIM to IN sets lower peak inductor currents.
2	IN	Input from battery
3	AGND	Analog ground. Not internally connected to PGND.
4	PGND	Power ground. Must be low impedance; solder directly to ground plane or star ground. Connect to AGND, close to the device.
5	LX	Collector of 1A NPN power switch and emitter of Active Rectifier PNP.
6	OUT	Voltage output. Connect filter capacitor close to pin.
7	$\overline{SHDN}$	Shutdown input disables power supply when low. Also disconnects load from input. Threshold is set at $V_{IN}/2$.
8	N.C. (MAX777)	No connect—not internally connected.
	SEL (MAX778)	Selects the main output voltage. 3.3V when hard-wired to AGND, 3.0V when left open.
	FB (MAX779)	Feedback input for adjustable-output operation. Connect to an external voltage divider between V_{OUT} and AGND.

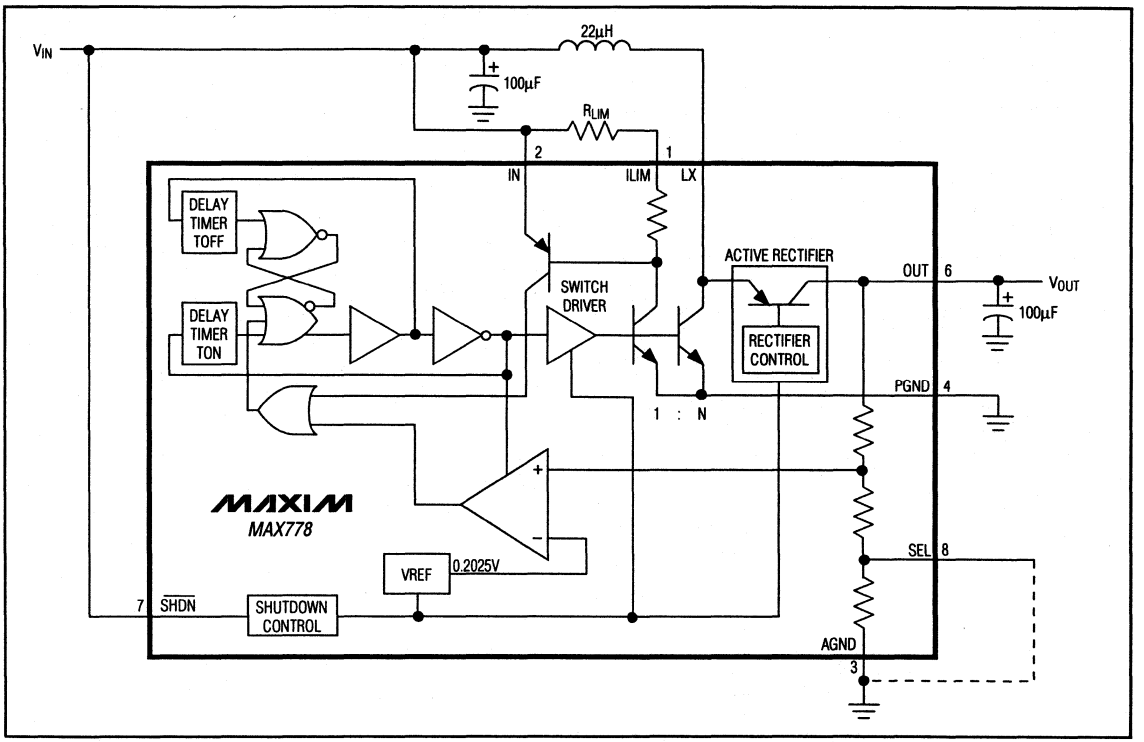


Figure 1. MAX778 Block Diagram

Detailed Description

Operating Principle

The MAX777/MAX778/MAX779 combine a switch-mode regulator with an NPN bipolar switch, current limit, precision voltage reference, and active rectifier—all in a single monolithic device. In shutdown mode, the internal rectifier is completely turned off and disconnects the load from the source. Only two external components are required in addition to the input bypass capacitor: a 22µH inductor and a 100µF filter capacitor.

A minimum off-time, current-limited, pulse-frequency-modulation (PFM) control scheme combines the advantages of pulse width modulation (PWM) (high output power and efficiency) with those of a traditional PFM pulse skipper (low quiescent currents).

External conditions (inductor value, load, and input voltage) determine the way the converter operates, as follows:

At light loads, the current through the inductor starts at zero, rises to a peak value, and drops down to zero in each cycle (discontinuous-conduction mode). In this case, the switching frequency is governed by a pair of one-shots that set a maximum on-time inversely proportional to V_{IN} [t_{ON} = 8.8/(V_{IN} - 0.25)] and a minimum off-time (1.3µs for MAX777/MAX779 and 2.3µs for MAX778). With a 22µH inductor, LX's peak current is about 350mA and is independent of input voltage. Efficiency at light loads is improved because of lower peak currents.

At very light loads, more energy is stored in the coil than is required by the load in each cycle. The converter regulates by skipping entire cycles. Efficiency is typically 65% to 75% in the pulse-skipping mode. Pulse-skipping waveforms can be irregular, and the output waveform contains a low-frequency component. Larger, low equivalent series resistance (ESR) filter capacitors can help reduce the ripple voltage if needed.

Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

At heavy loads above approximately 100mA, the converter enters continuous-conduction mode, where current always flows in the inductor. The switch-on state is controlled cycle-by-cycle by either the maximum t_{ON} time or the switch's preset current limit. As a result, the switch's current rating is not exceeded and the inductor is not saturated. At very heavy loads, the inductor current self-oscillates between this peak current limit and some lower value governed by the minimum off-time, the inductance value, and the input/output differential.

With ILIM shorted to IN, the peak switch current of the internal NPN power switch is set to 1A. The peak switch current can be set to a lower value by connecting a resistor between ILIM and IN (see *Current Limit* section). This enables the use of physically smaller inductors with lower saturation-current ratings. At 1A, the switch voltage drop (V_{SW}) is about 500mV. V_{SW} decreases to about 250mV at 0.1A.

Conventional PWM converters generate constant-frequency switching noise, while this architecture produces variable-frequency switching noise. However, the noise does not exceed the current limit times the filter-capacitor ESR, unlike conventional pulse-skippers.

Step-Down Mode

If the input voltage exceeds the output voltage, the MAX777/MAX778/MAX779 behave as "switched" linear regulators. If the output voltage starts to drop, the switch turns on and energy is stored in the coil, as in normal step-up mode. After the switch turns off, the voltage at LX flies high. The active rectifier turns on when LX rises above V_{IN}. As in a linear regulator, the voltage difference between V_{IN} and V_{OUT} appears across the rectifier (actually a PNP transistor) until the current goes to zero and the rectifier turns off. At high V_{IN} to V_{OUT} differentials, the maximum load current is limited by the maximum allowable power dissipation in the package. For fully specified buck/boost converters, refer to the data sheet for the pin-compatible MAX877/MAX878/MAX879.

Active Rectifier

The internal active rectifier of the MAX777/MAX778/MAX779 replaces the external Schottky catch diode in normal boost operation. The rectifier consists of a PNP pass transistor and a unique control circuit which, in shutdown mode, entirely disconnects the load from the source. This is a distinct advantage over standard boost topologies, since it prevents battery drain in shutdown.

The active rectifier also acts as a zero-dropout regulator if the input exceeds the regulated output. This allows the MAX777/MAX778/MAX779 to act as buck/boost converters. Useful in battery-powered applications, where the battery voltage may initially exceed the output voltage, the converters will regulate down to the output voltage and seamlessly switch into boost mode as the input drops below the output voltage. The pin-compatible MAX877/MAX878/MAX879 are fully specified buck/boost converters with higher specified output currents than the MAX777/MAX778/MAX779.

Shutdown

Shutdown ($\overline{SHDN}$) is a high-impedance, active-low input. Connect $\overline{SHDN}$ to V_{IN} for normal operation. Keeping $\overline{SHDN}$ at ground holds the converters in shutdown mode. Since the active rectifier is turned off in shutdown mode, the path from input to load is cut, and the output effectively drops to 0V. The supply current in the shutdown state ranges from 4µA at V_{IN} = 1V to 50µA at V_{IN} = 5V. The shutdown circuit threshold is set nominally to $V_{IN}/2$ + 250mV. When $\overline{SHDN}$ is below this threshold, the device is shut down and is enabled with $\overline{SHDN}$ above the threshold. When driven from external logic, $\overline{SHDN}$ can be driven to a higher voltage than V_{IN}.

Current Limit

Connecting ILIM to IN sets an LX current limit of 1A. For smaller output power levels that do not require the maximum peak current, the peak inductor current can be reduced to optimize overall efficiency and to allow very small, low-cost coils with lower current ratings. See also the *Inductor Selection* section.

Reduce the MAX777/MAX778/MAX779 peak inductor current by connecting a resistor between ILIM and IN. See Figure 2 to select the resistor.

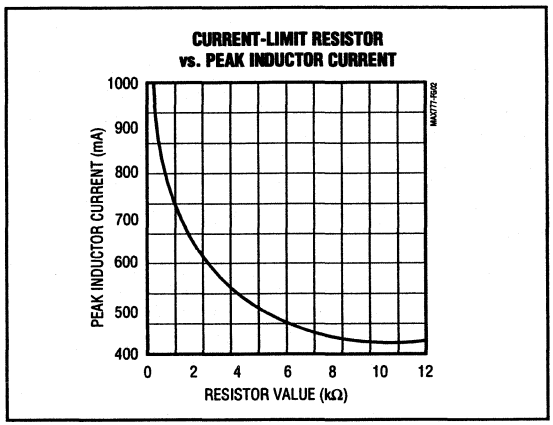


Figure 2. Current-Limit Resistor vs. Current Limit

Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

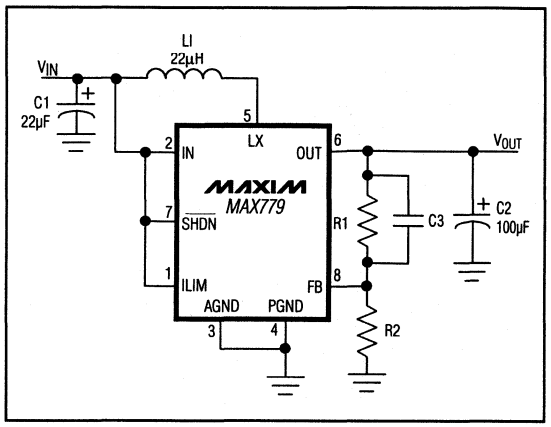


Figure 3. MAX779 Adjustable Voltage

Output Voltage Selection

The output voltage of the MAX777 is fixed at 5V. The MAX778 output voltage can be set to 3V by leaving the SEL pin open. Connect SEL to AGND for 3.3V operation.

The MAX779's output voltage is set by two resistors, R1 and R2 (Figure 3), which form a voltage divider between the output and the FB pin. The output voltage can be set from 2.5V to 6.0V by the equation:

$$V_{OUT} = (0.2025)\ [(R1 + R2)/R2]$$

To simplify the resistor selection:

$$R1 = (R2)[(V_{OUT}/0.2025) - 1]$$

Since the input current at FB is 40nA maximum, large values (10kΩ to 50kΩ for R2) can be used with no significant loss of acccuracy. For 1% error, the current through R2 should be at least 100 times FB's bias current.

When large values are used for the feedback resistors (R1 > 50kΩ), stray output impedance at FB can add "lag" to the feedback response, destabilizing the regulator and creating a larger ripple at the output. Lead lengths and circuit board traces at the FB node should be kept short. Reduce ripple by adding a "lead" compensation capacitor (C3, 100pF to 50nF) in parallel with R1.

Applications Information

The *Typical Operating Circuit* shows a MAX777 step-up application circuit. This circuit starts up and operates with inputs ranging from 1.0V to 6.2V. Start-up time is a function of the load, typically less than 5ms. Output current capability is a function of the input voltage. See *Typical Operating Characteristics.*

Inductor Selection

The 22µH inductor shown in the *Typical Operating Circuit* is sufficient for most MAX777/MAX778/MAX779 designs. Other inductor values ranging from 10µH to 47µH are also suitable. The inductor should have a **saturation rating** equal to or greater than the peak switch-current limit, which is 1A without an external current limit (ILIM connected to IN). It is acceptable to operate the inductor at 120% of its saturation rating; however, this will reduce efficiency. For highest efficiency, use an inductor with a low **DC resistance**, preferably under 0.2Ω. Table 1 lists suggested inductor suppliers.

Capacitor Selection

The 100µF, 10V surface-mount tantalum (SMT) output capacitor shown in the *Typical Operating Circuit* will provide a 20mV output ripple or less, stepping up from 2V to 3.3V at 200mA. Smaller capacitors, down to 10µF, are acceptable for light loads or in applications that tolerate higher output ripple. The input capacitor may be omitted if the input lead length is less than 2 inches (5cm) or if the loads are small.

The primary factor in selecting both the output and input filter capacitor is low ESR. The ESR of both bypass and filter capacitors affects efficiency. Optimize performance by increasing filter capacitors or using specialized low-ESR capacitors. The smallest low-ESR SMT tantalum capacitors currently available are Sprague 595D or 695D series. Sanyo OS-CON organic semiconductor through-hole capacitors also exhibit very low ESR, are rated for the wide temperature range, and are particularly useful for operation at cold temperatures. Table 1 lists suggested capacitor suppliers.

Layout

The MAX777/MAX778/MAX779's high peak currents and high-frequency operation make PC layout important for minimum ground bounce and noise. Locate input bypass and output filter capacitors close to the device pins. All connections to the FB pin (MAX779) should also be kept as short as possible. A ground plane is recommended. Solder AGND (pin 3) and PGND (pin 4), directly to the ground plane. Refer to the MAX777/MAX778/MAX779 evaluation kit (EV kit) manual for a suggested surface-mount layout.

Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida CD54-220 (22µH) Murata-Erie LQHYN1501K04M00-D5 (15µH) Coiltronics CTX20-1	Sprague 595D Sprague 695D Matsuo 267 series AVX TPS series
Miniature Through-Hole	Sumida RCH654-220	Sanyo OS-CON low-ESR organic semiconductor
Low-Cost Through-Hole	Renco RL 1284-22 Coilcraft PCH-27-223	Nichicon PL series low-ESR electrolyic United Chemi-Con, LXF series

AVX	USA:	(803) 448-9411, FAX (803) 626-3123
Coiltronics	USA:	(305) 781-8900, FAX (305) 782-4163
Matsuo	USA:	(714) 969-2491, FAX (714) 960-6492
	Japan:	(06) 332-0871
Murata-Erie	USA:	(404) 736-1300, FAX (404) 736-3030
Nichicon	USA:	(708) 843-7500, FAX (708) 843-2798
Renco	USA:	(516) 586-5566, FAX (516) 586-5562
Sanyo	USA:	(619) 661-6835
	Japan:	(0720) 70-1005, FAX (0720) 70-1174
Sprague	USA:	(508) 339-8900, FAX (508) 339-5063
Sumida	USA:	(708) 956-0666, FAX (708) 956-0702
	Japan:	(03) 3607-5111, FAX (03) 3607-5428
United Chemi-Con	USA:	(708) 696-2000, FAX (708) 640-6311

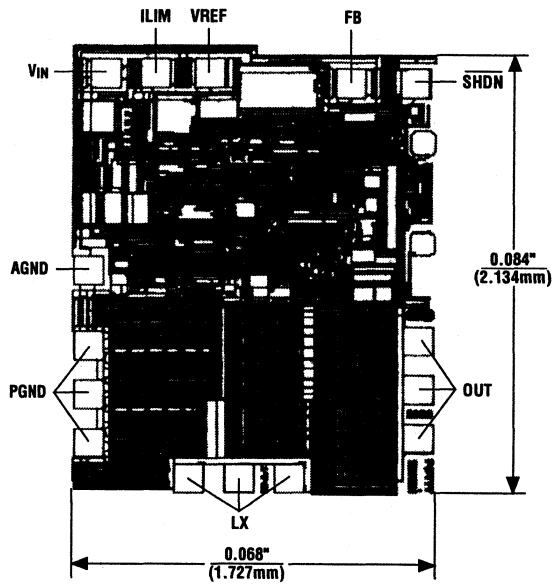
Low-Voltage Input, 3V/3.3V/5V/ Adjustable Output, Step-Up DC-DC Converters

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX778CPA	0°C to +70°C	8 Plastic DIP
MAX778CSA	0°C to +70°C	8 SO
MAX778C/D	0°C to +70°C	Dice*
MAX778EPA	-40°C to +85°C	8 Plastic DIP
MAX778ESA	-40°C to +85°C	8 SO
MAX778MJA	-55°C to +125°C	8 CERDIP**
MAX779CPA	0°C to +70°C	8 Plastic DIP
MAX779CSA	0°C to +70°C	8 SO
MAX779C/D	0°C to +70°C	Dice*
MAX779EPA	-40°C to +85°C	8 Plastic DIP
MAX779ESA	-40°C to +85°C	8 SO
MAX779MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

_Chip Topography



TRANSISTOR COUNT: 170;
SUBSTRATE CONNECTED TO AGND.

19-0160; Rev 1; 5/94

EVALUATION KIT AVAILABLE

MAXIM

Dual-Output Power-Supply Controller for Notebook Computers

General Description

The MAX786 is a system-engineered power-supply controller for notebook computers or similar battery-powered equipment. It provides two high-performance step-down (buck) pulse-width modulators (PWMs) for +3.3V and +5V. Other features include dual, low-dropout, micropower linear regulators for CMOS/RTC back-up, and two precision low-battery-detection comparators.

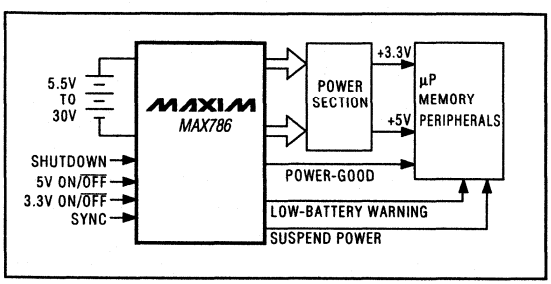
High efficiency (95% at 2A; greater than 80% at loads from 5mA to 3A) is achieved through synchronous rectification and PWM operation at heavy loads, and Idle-Mode™ operation at light loads. The MAX786 uses physically small components, thanks to high operating frequencies (300kHz/200kHz) and a new current-mode PWM architecture that allows for output filter capacitors as small as 30µF per ampere of load. Line- and load-transient responses are terrific, with a high 60kHz unity-gain crossover frequency allowing output transients to be corrected within four or five clock cycles. Low system cost is achieved through a high level of integration and the use of low-cost, external N-channel MOSFETs.

Other features include low-noise, fixed-frequency PWM operation at moderate to heavy loads, and a synchronizable oscillator for noise-sensitive applications such as electromagnetic pen-based systems and communicating computers. The MAX786 is a monolithic, BiCMOS IC available in fine-pitch, surface-mount SSOP packages.

Applications

Notebook Computers
Portable Data Terminals
Communicating Computers
Pen-Entry Systems

Typical Application Diagram



Features

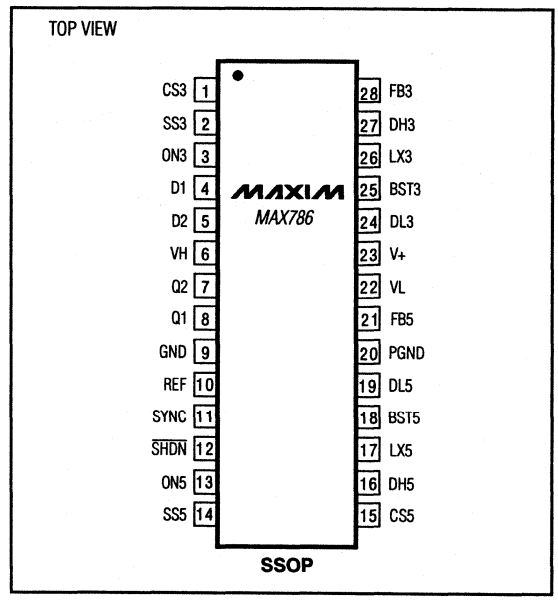
- ♦ **Dual PWM Buck Controllers (+3.3V and +5V)**
- ♦ **Two Precision Comparators or Level Translators**
- ♦ **95% Efficiency**
- ♦ **420µA Quiescent Current, 70µA in Standby (linear regulators alive)**
- ♦ **25µA Shutdown Current (+5V linear alive)**
- ♦ **5.5V to 30V Input Range**
- ♦ **Small SSOP Package**
- ♦ **Fixed Output Voltages:**
  3.3V (standard)
  3.45V (High-Speed Pentium™)
  3.6V (PowerPC™)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	V_{OUT}
MAX786CAI	0°C to +70°C	28 SSOP	3.3V
MAX786RCAI	0°C to +70°C	28 SSOP	3.45V

Ordering Information continued at end of data sheet.

Pin Configuration



™ Idle-Mode is a trademark of Maxim Integrated Products. Pentium is a trademark of Intel. PowerPC is a trademark of IBM.

Dual-Output Power-Supply Controller for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V, +36V
PGND to GND .....±2V
VL to GND .....-0.3V, +7V
BST3, BST5 to GND .....-0.3V, +36V
LX3 to BST3 .....-7V, +0.3V
LX5 to BST5 .....-7V, +0.3V
Inputs/Outputs to GND
(D1, D2, $\overline{SHDN}$, ON5, REF, SS5, CS5,
FB5, SYNC, CS3,FB3, SS3, ON3) .....-0.3V, (VL + 0.3V)
VH to GND .....-0.3V, 20V
Q1, Q2 to GND .....-0.3V, (VH + 0.3V)
DL3, DL5 to PGND .....-0.3V, (VL + 0.3V)
DH3 to LX3 .....-0.3V, (BST3 + 0.3V)
DH5 to LX5 .....-0.3V, (BST5 + 0.3V)
REF, VL Short to GND .....Momentary
REF Current 20mA
VL Current 50mA
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
MAX786CAI/MAX786_CAI .....0°C to +70°C
MAX786EAI/MAX786_EAI .....-40°C to +85°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0mA, $\overline{SHDN}$ = ON3 = ON5 = 5V, other digital input levels are 0V or +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V AND 5V STEP-DOWN CONTROLLERS						
Input Supply Range			5.5		30	V
FB5 Output Voltage	0mV < (CS5-FB5) < 70mV, 6V < V + < 30V (includes load and line regulation)		4.80	5.08	5.20	V
FB3 Output Voltage	0mV < (CS3-FB3) < 70mV, 6V < V + < 30V (includes load and line regulation)	MAX786	3.17	3.35	3.46	V
		MAX786R	3.32	3.50	3.60	
		MAX786S	3.46	3.65	3.75	
Load Regulation	Either controller (CS_ -FB_ = 0mV to 70mV)			2.5		%
Line Regulation	Either controller (V+ = 6V to 30V)			0.03		%/V
Current-Limit Voltage	CS3-FB3 or CS5-FB5		80	100	120	mV
SS3/SS5 Source Current			2.5	4.0	6.5	µA
SS3/SS5 Fault Sink Current			2			mA
INTERNAL REGULATOR AND REFERENCE						
VL Output Voltage	ON5 = ON3 = 0V, 5.5V < V+ < 30V, 0mA < I_L < 25mA		4.5		5.5	V
VL Fault Lockout Voltage	Falling edge, hysteresis = 1%		3.6		4.2	V
VL/FB5 Switchover Voltage	Rising edge of FB5, hysteresis = 1%		4.2		4.7	V
REF Output Voltage	No external load (Note 1)		3.24		3.36	V
REF Fault Lockout Voltage	Falling edge		2.4		3.2	V
REF Load Regulation	0mA < I_L < 5mA (Note 2)			30	75	mV
V+ Shutdown Current	$\overline{SHDN}$ = D1 = D2 = ON3 = ON5 = 0V, V+ = 30V			25	40	µA
V+ Standby Current	D1 = D2 = ON3 = ON5 = 0V, V+ = 30V			70	110	µA
Quiescent Power Consumption (both PWM controllers on)	D1 = D2 = 0V, FB5 = CS5 = 5.25V, FB3 = CS3 = 3.5V			5.5	8.6	mW
V+ Off Current	FB5 = CS5 = 5.25V, VL switched over to FB5			30	60	µA
COMPARATORS						
D1, D2 Trip Voltage	Falling edge, hysteresis = 1%		1.61		1.69	V
D1, D2 Input Current	D1 = D2 = 0V, 5V				±100	nA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0mA, $\overline{SHDN}$ = ON3 = ON5 = 5V, other digital input levels are 0V or +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Q1, Q2 Source Current	VH = 15V, V_{OUT} = 2.5V	12	20	30	µA
Q1, Q2 Sink Current	VH = 15V, V_{OUT} = 2.5V	200	500	1000	µA
Q1, Q2 Output High Voltage	I_{SOURCE} = 5µA, VH = 3V	VH - 0.5			V
Q1, Q2 Output Low Voltage	I_{SINK} = 20µA, VH = 3V			0.4	V
Quiescent VH Current	VH = 18V, D1 = D2 = 5V, no external load		4	10	µA
OSCILLATOR AND INPUTS/OUTPUTS					
Oscillator Frequency	SYNC = 3.3V	270	300	330	kHz
	SYNC = 0V, 5V	170	200	230	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Rise/Fall Time	Not tested			200	ns
Oscillator SYNC Range		240		350	kHz
Maximum Duty Cycle	SYNC = 3.3V	89	92		%
	SYNC = 0V or 5V	92	95		
Input Low Voltage	$\overline{SHDN}$, ON3, ON5, SYNC			0.8	V
Input High Voltage	$\overline{SHDN}$, ON3, ON5	2.4			V
	SYNC	VL - 0.5			
Input Current	$\overline{SHDN}$, ON3, ON5 V_{IN} = 0V, 5V			±1	µA
DL3/DL5 Sink/Source Current	V_{OUT} = 2V		1		A
DH3/DH5 Sink/Source Current	BST3-LX3 = BST5-LX5 = 4.5V, V_{OUT} = 2V		1		A
DL3/DL5 On-Resistance	High or low			7	Ω
DH3/DH5 On-Resistance	High or low, BST3-LX3 = BST5-LX5 = 4.5V			7	Ω

Note 1: Since the reference uses VL as its supply, its V+ line regulation error is insignificant.

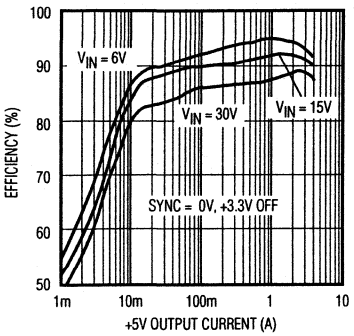
Note 2: The main switching outputs track the reference voltage. Loading the reference reduces the main outputs slightly according to the closed-loop gain (AV_{CL}) and the reference voltage load-regulation error. AV_{CL} for the +3.3V supply is unity gain. AV_{CL} for the +5V supply is 1.54.

Dual-Output Power-Supply Controller for Notebook Computers

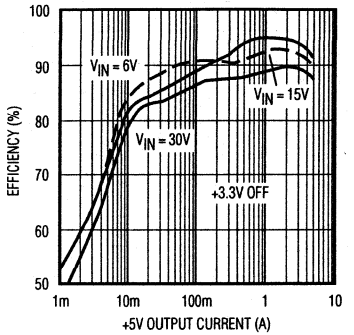
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

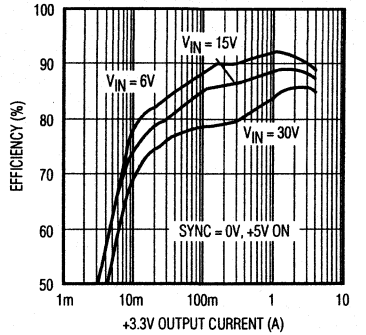
EFFICIENCY vs. +5V OUTPUT CURRENT, 200kHz



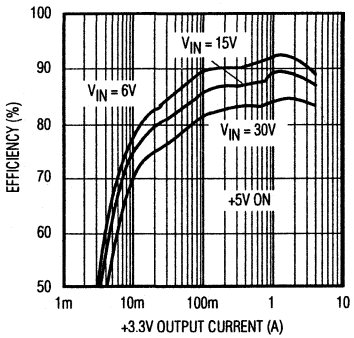
EFFICIENCY vs. +5V OUTPUT CURRENT, 300kHz



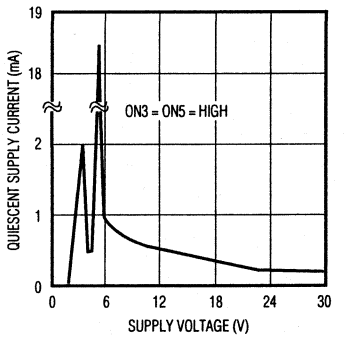
EFFICIENCY vs. +3.3V OUTPUT CURRENT, 200kHz



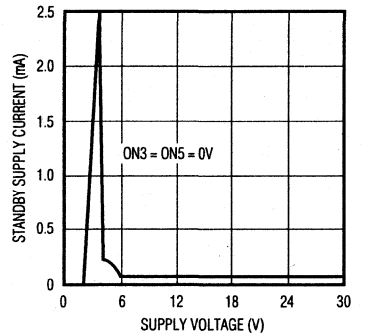
EFFICIENCY vs. +3.3V OUTPUT CURRENT, 300kHz



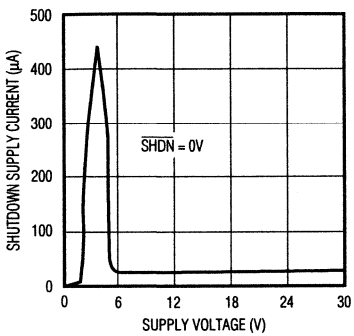
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



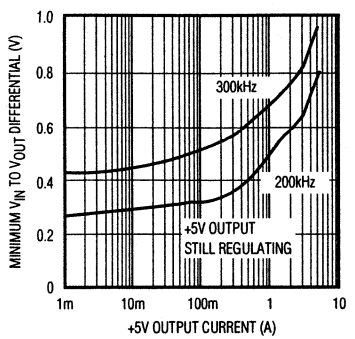
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



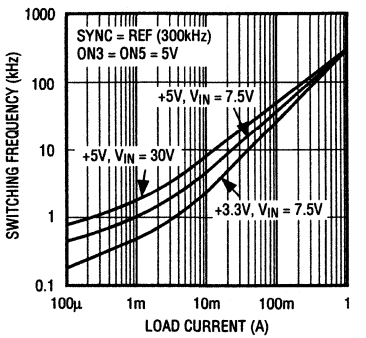
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



MINIMUM V_{IN} TO V_{OUT} DIFFERENTIAL vs. +5V OUTPUT CURRENT



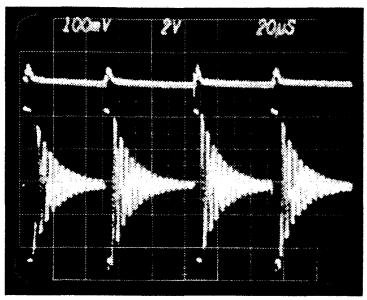
SWITCHING FREQUENCY vs. LOAD CURRENT



Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

IDLE-MODE WAVEFORMS

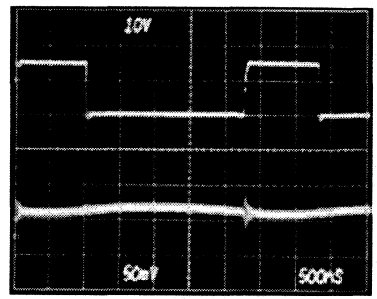


+5V OUTPUT
50mV/div

2V/div

200µs/div
I_{LOAD} = 100mA
V_{IN} = 10V

PULSE-WIDTH MODULATION MODE WAVEFORMS

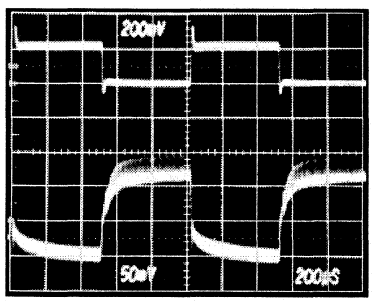


LX 10V/div

+5V OUTPUT
50mV/div

500ns/div
+5V OUTPUT CURRENT = 1A
V_{IN}= 16V

+5V LOAD-TRANSIENT RESPONSE

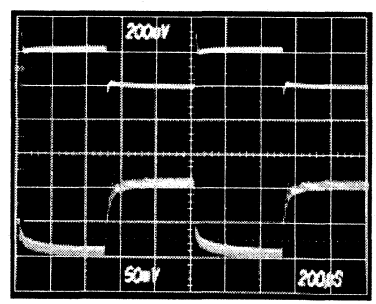


3A
LOAD CURRENT
0A

+5V OUTPUT
50mV/div

200µs/div
V_{IN} = 15V

+3.3V LOAD-TRANSIENT RESPONSE



3A
LOAD CURRENT
0A

+3.3V OUTPUT
50mV/div

200µs/div
V_{IN} = 15V

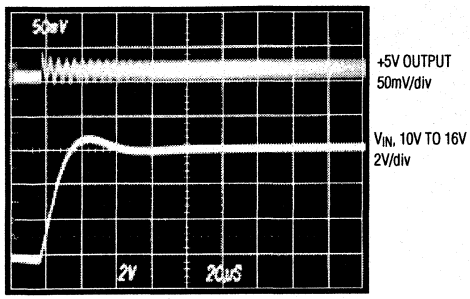
4

Dual-Output Power-Supply Controller for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

+5V LINE-TRANSIENT RESPONSE, RISING

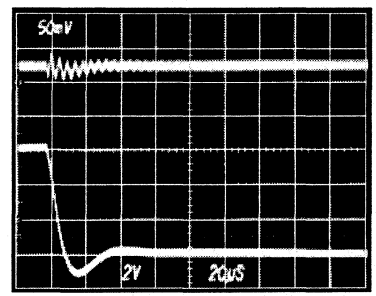


+5V OUTPUT
50mV/div

V_{IN}, 10V TO 16V
2V/div

20µs/div
I_{LOAD} = 2A

+5V LINE-TRANSIENT RESPONSE, FALLING

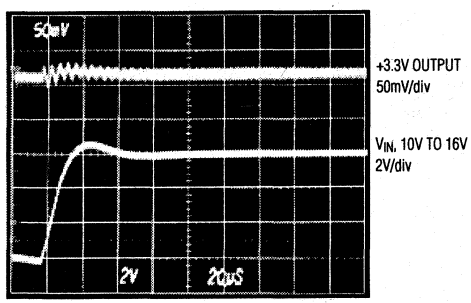


+5V OUTPUT
50mV/div

V_{IN}, 16V TO 10V
2V/div

20µs/div
I_{LOAD} = 2A

+3.3V LINE-TRANSIENT RESPONSE, RISING

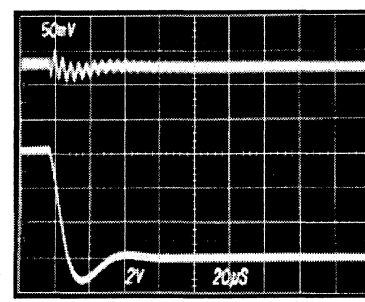


+3.3V OUTPUT
50mV/div

V_{IN}, 10V TO 16V
2V/div

20µs/div
I_{LOAD} = 2A

+3.3V LINE-TRANSIENT RESPONSE, FALLING



+3.3V OUTPUT
50mV/div

V_{IN}, 16V TO 10V
2V/div

20µs/div
I_{LOAD} = 2A

Dual-Output Power-Supply Controller for Notebook Computers

Pin Description

PIN	NAME	FUNCTION
1	CS3	Current-sense input for +3.3V; +100mV = current limit level referenced to FB3.
2	SS3	Soft-start input for +3.3V. Ramp time to full current limit is 1ms/nF of capacitance to GND.
3	ON3	ON/$\overline{OFF}$ control input disables the +3.3V PWM. Tie directly to VL for automatic start-up.
4	D1	#1 level-translator/comparator noninverting input, threshold = +1.650V. Controls Q1. Tie to GND if unused.
5	D2	#2 level-translator/comparator noninverting input (see D1)
6	VH	External positive supply-voltage input for the level translators/comparators
7	Q2	#2 level-translator/comparator output. Sources 20µA from VH when D2 is high. Sinks 500µA to GND when D2 is low, even with VH = 0V.
8	Q1	#1 level translator/comparator output (see Q2)
9	GND	Low-current analog ground
10	REF	3.3V reference output. Sources up to 5mA for external loads. Bypass to GND with 1µF/mA of load or 0.22µF minimum.
11	SYNC	Oscillator control/synchronization input. Connect to VL or GND for 200kHz; connect to REF for 300kHz. For external clock synchronization in the 240kHz to 350kHz range, a high-to-low transition causes a new cycle to start.
12	$\overline{SHDN}$	Shutdown control input, active low. Tie to VL for automatic start-up. The 5V VL supply stays active in shutdown, but all other circuitry is disabled. Do not force $\overline{SHDN}$ higher than VL + 0.3V.
13	ON5	ON/$\overline{OFF}$ control input disables the +5V PWM supply. Tie to VL for automatic start-up.
14	SS5	Soft-start control input for +5V. Ramp time to full current limit is 1ms/nF of capacitance to GND.
15	CS5	Current-sense input for +5V; +100mV = current-limit level referenced to FB5.
16	DH5	Gate-drive output for the +5V high-side MOSFET
17	LX5	Inductor connection for the +5V supply
18	BST5	Boost capacitor connection for the +5V supply (0.1µF)
19	DL5	Gate-drive output for the +5V low-side MOSFET
20	PGND	Power ground
21	FB5	Feedback and current-sense input for the +5V PWM
22	VL	5V logic supply voltage for internal circuitry. VL is always on and can source 5mA for external loads.
23	V+	Supply voltage input from battery, 5.5V to 30V
24	DL3	Gate-drive output for the +3.3V low-side MOSFET
25	BST3	Boost capacitor connection for the +3.3V supply (0.1µF)
26	LX3	Inductor connection for the +3.3V supply
27	DH3	Gate-drive output for the +3.3V high-side MOSFET
28	FB3	Feedback and current-sense input for the +5V PWM

Dual-Output Power-Supply Controller for Notebook Computers

Detailed Description

The MAX786 converts a 5.5V to 30V input to four outputs (Figure 1). It produces two high-power, PWM, switch-mode supplies, one at +5V and the other at +3.3V. The two supplies operate at either 300kHz or 200kHz, allowing for small external components. Output current capability depends on external components, and can exceed 6A on each supply. An internal 5V, 5mA supply (VL) and a 3.3V, 5mA reference voltage are also generated via linear regulators, as shown in Figure 2. Fault protection circuitry shuts off the PWMs when the internal supplies lose regulation.

Two precision voltage comparators are also included. Their output stages permit them to be used as level translators for driving external N-channel MOSFETs in load-switching applications, or for more conventional logic signals.

The MAX786 has two close relatives: the MAX782 and the MAX783. The MAX782 and MAX783 each include an extra flyback winding regulator and linear regulators for dual, +12V/programmable PCMCIA VPP outputs. The MAX782/MAX783 data sheet contains extra applications information on the MAX786 not found in this data sheet.

+3.3V Switch-Mode Supply

The +3.3V supply is generated by a current-mode, PWM step-down regulator using two N-channel MOSFETs, a rectifier, and an LC output filter (Figure 1). The gate-drive signal to the high-side MOSFET, which must exceed the battery voltage, is provided by a boost circuit that uses a 100nF capacitor connected to BST3.

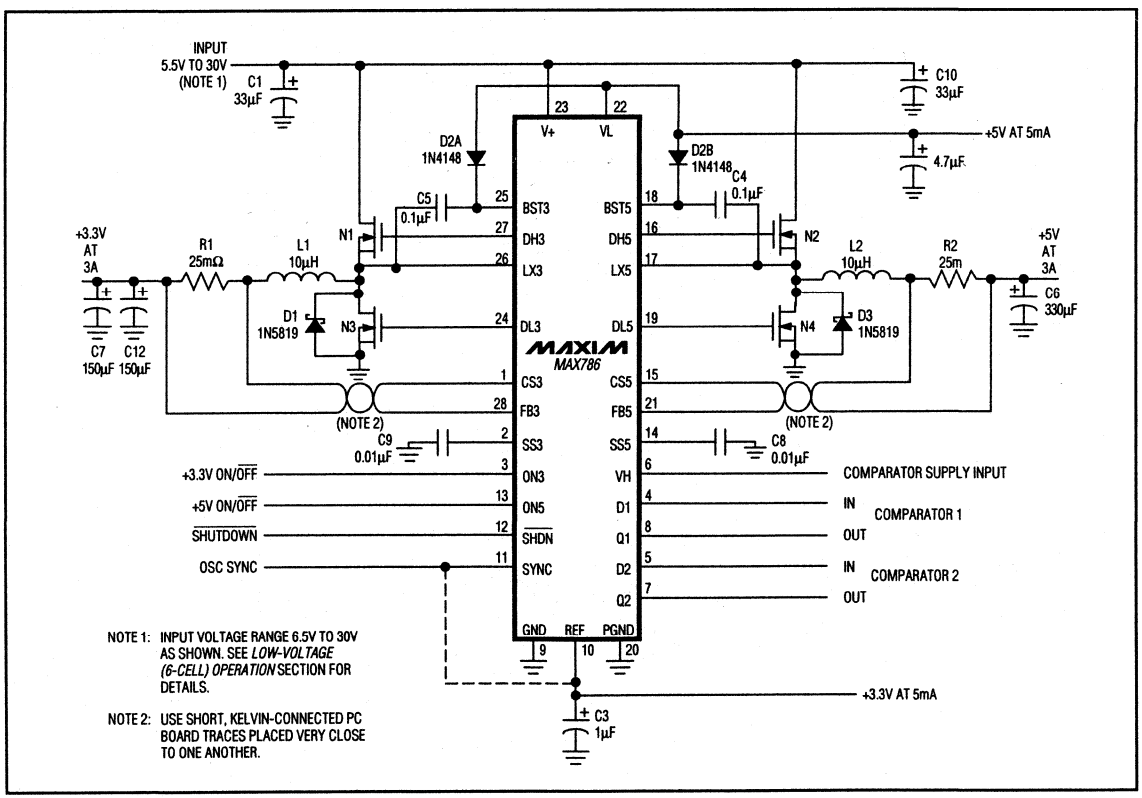


Figure 1. MAX786 Application Circuit

Dual-Output Power-Supply Controller for Notebook Computers

A synchronous rectifier at LX3 keeps efficiency high by clamping the voltage across the rectifier diode. Maximum current limit is set by an external low-value sense resistor, which prevents excessive inductor current during start-up or under short-circuit conditions.

Programmable soft-start is set by an optional external capacitor; this reduces in-rush surge currents upon start-up and provides adjustable power-up times for power-supply sequencing purposes.

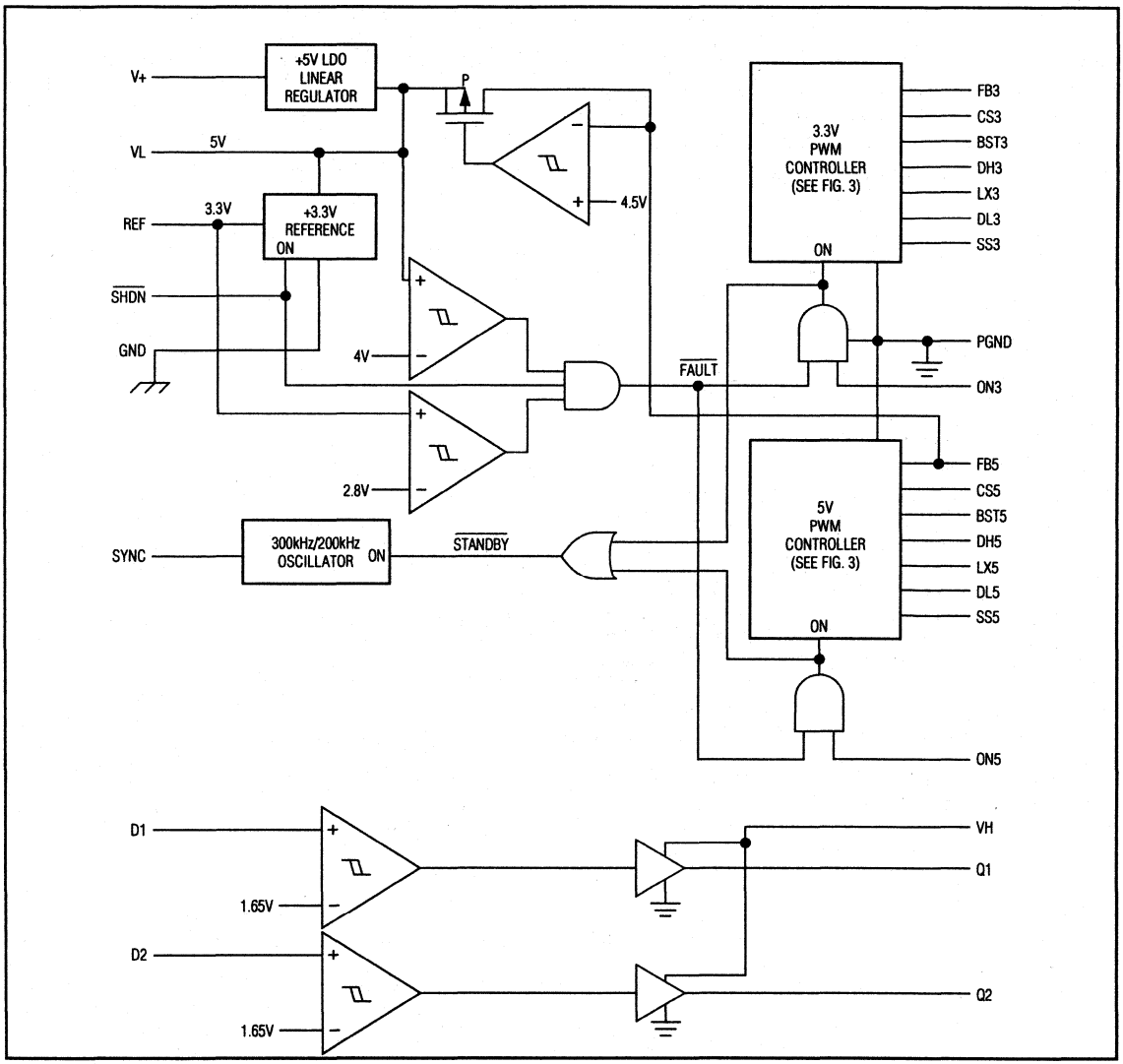


Figure 2. MAX786 Block Diagram

Dual-Output Power-Supply Controller for Notebook Computers

+5V Switch-Mode Supply

The +5V output is produced by a current-mode, PWM step-down regulator, which is nearly identical to the +3.3V supply. The +5V supply's dropout voltage, as configured in Figure 1, is typically 400mV at 2A. As V+ approaches 5V, the +5V output gracefully falls with V+ until the VL regulator output hits its undervoltage-lockout threshold at 4V. At this point, the +5V supply turns off.

The default frequency for both PWM controllers is 300kHz (with SYNC connected to REF), but 200kHz may be used by connecting SYNC to GND or VL.

+3.3V and +5V PWM Buck Controllers

The two current-mode PWM controllers are identical except for different preset output voltages (Figure 3). Each PWM is independent except for being synchronized to a master oscillator and sharing a common reference (REF) and logic supply (VL). Each PWM can be turned on and off separately via ON3 and ON5. The PWMs are a direct-summing type, lacking a traditional integrator error amplifier and the phase shift associated with it. They therefore do not require any external feedback compensation components if the filter capacitor ESR guidelines given in the *Design Procedure* are followed.

The main gain block is an open-loop comparator that sums four input signals: an output voltage error signal, current-sense signal, slope-compensation ramp, and precision voltage reference. This direct-summing method approaches the ideal of cycle-by-cycle control of the output voltage. Under heavy loads, the controller operates in full PWM mode. Every pulse from the oscillator sets the output latch and turns on the high-side switch for a period determined by the duty cycle (approximately V_{OUT}/V_{IN}). As the high-side switch turns off, the synchronous rectifier latch is set and, 60ns later, the low-side switch turns on (and stays on until the beginning of the next clock cycle, in continuous mode, or until the inductor current crosses through zero, in discontinuous mode). Under fault conditions where the inductor current exceeds the 100mV current-limit threshold, the high-side latch is reset and the high-side switch is turned off.

At light loads, the inductor current fails to exceed the 25mV threshold set by the minimum current comparator. When this occurs, the PWM goes into idle-mode, skipping most of the oscillator pulses in order to reduce the switching frequency and cut back switching losses. The oscillator is effectively gated off at light loads because the minimum current comparator immediately resets the high-side latch at the beginning of each cycle, unless the FB_ signal falls below the reference voltage level.

Soft-Start/SS_ Inputs

Connecting capacitors to SS3 and SS5 allows gradual build-up of the +3.3V and +5V supplies after ON3 and ON5 are driven high. When ON3 or ON5 is low, the appropriate SS capacitors are discharged to GND. When ON3 or ON5 is driven high, a 4µA constant current source charges these capacitors up to 4V. The resulting ramp voltage on the SS_ pins linearly increases the current-limit comparator setpoint so as to increase the duty cycle to the external power MOSFETs up to the maximum output. With no SS capacitors, the circuit will reach maximum current limit within 10µs.

Soft-start greatly reduces initial in-rush current peaks and allows start-up time to be programmed externally.

Synchronous Rectifiers

Synchronous rectification allows for high efficiency by reducing the losses associated with the Schottky rectifiers.

When the external power MOSFET N1 (or N2) turns off, energy stored in the inductor causes its terminal voltage to reverse instantly. Current flows in the loop formed by the inductor, Schottky diode, and load—an action that charges up the filter capacitor. The Schottky diode has a forward voltage of about 0.5V which, although small, represents a significant power loss, degrading efficiency. A synchronous rectifier, N3 (or N4), parallels the diode and is turned on by DL3 (or DL5) shortly after the diode conducts. Since the on resistance ($r_{DS(ON)}$) of the synchronous rectifier is very low, the losses are reduced.

The synchronous rectifier MOSFET is turned off when the inductor current falls to zero.

Cross conduction (or "shoot-through") occurs if the high-side switch turns on at the same time as the synchronous rectifier. The MAX786's internal break-before-make timing ensures that shoot-through does not occur. The Schottky rectifier conducts during the time that neither MOSFET is on, which improves efficiency by preventing the synchronous-rectifier MOSFET's lossy body diode from conducting.

The synchronous rectifier works under all operating conditions, including discontinuous-conduction and idle-mode.

Boost Gate-Driver Supply

Gate-drive voltage for the high-side N-channel switch is generated with a flying-capacitor boost circuit as shown in Figure 4. The capacitor is alternately charged from the VL supply via the diode and placed in parallel with the high-side MOSFET's gate-source terminals. On start-up, the synchronous rectifier (low-side) MOSFET forces LX_ to 0V and charges the BST_ capacitor to 5V. On the

second half-cycle, the PWM turns on the high-side MOSFET by connecting the capacitor to the MOSFET gate by closing an internal switch between BST_ and DH_. This provides the necessary enhancement voltage to turn on the high-side switch, an action that "boosts" the 5V gate-drive signal above the battery voltage.

Ringing seen at the high-side MOSFET gates (DH3 and DH5) in discontinuous-conduction mode (light loads) is a natural operating condition caused by the residual energy in the tank circuit formed by the inductor and stray capacitance at the LX_ nodes. The gate driver negative rail is referred to LX_, so any ringing there is directly coupled to the gate-drive supply.

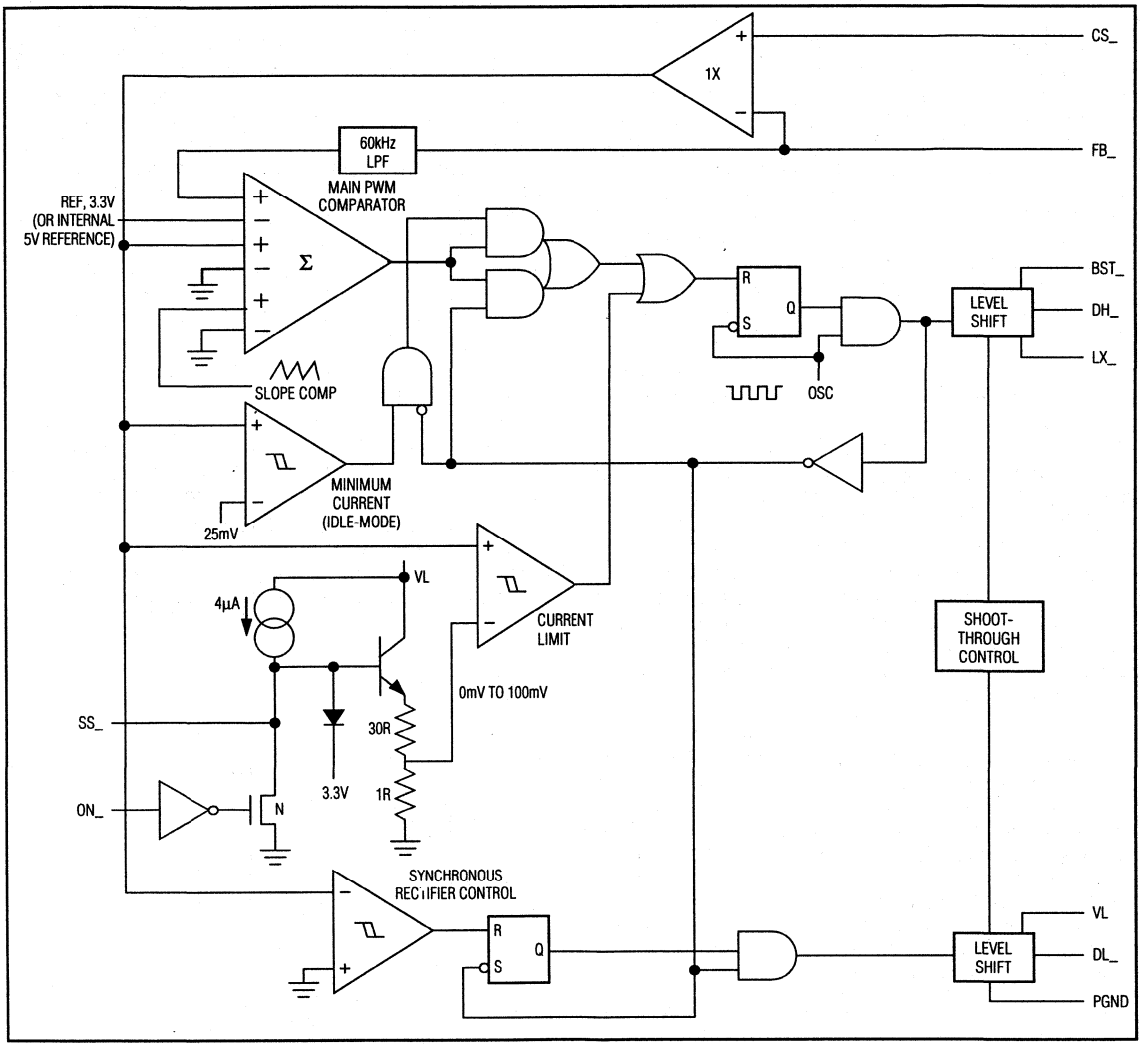


Figure 3. PWM Controller Block Diagram

Dual-Output Power-Supply Controller for Notebook Computers

Modes of Operation

PWM Mode

Under heavy loads—over approximately 25% of full load—the +3.3V and +5V supplies operate as continuous-current PWM supplies (see *Typical Operating Characteristics*). The duty cycle (%ON) is approximately:

$$\%ON = V_{OUT}/V_{IN}$$

Current flows continuously in the inductor: First, it ramps up when the power MOSFET conducts; then, it ramps down during the flyback portion of each cycle as energy is put into the inductor and then discharged into the load. Note that the current flowing into the inductor when it is being charged is also flowing into the load, so the load is continuously receiving current from the inductor. This minimizes output ripple and maximizes inductor use, allowing very small physical and electrical sizes. Output ripple is primarily a function of the filter capacitor (C7 or C6) effective series resistance (ESR) and is typically under 50mV (see the *Design Procedure* section). Output ripple is worst at light load and maximum input voltage.

Idle Mode

Under light loads (<25% of full load), efficiency is further enhanced by turning the drive voltage on and off for only a single clock period, skipping most of the clock pulses entirely. Asynchronous switching, seen as "ghosting" on an oscilloscope, is thus a normal operating condition whenever the load current is less than approximately 25% of full load.

At certain input voltage and load conditions, a transition region exists where the controller can pass back and forth from idle-mode to PWM mode. In this situation, short bursts of pulses occur that make the current waveform look erratic, but do not materially affect the output ripple. Efficiency remains high.

Current Limiting

The voltage between CS3 (CS5) and FB3 (FB5) is continuously monitored. An external, low-value shunt resistor is connected between these pins, in series with the inductor, allowing the inductor current to be continuously measured throughout the switching cycle. Whenever this voltage exceeds 100mV, the drive voltage to the external high-side MOSFET is cut off. This protects the MOSFET, the load, and the battery in case of short circuits or temporary load surges. The current-limiting resistors R1 and R2 are typically 25mΩ for 3A load current.

Oscillator Frequency; SYNC Input

The SYNC input controls the oscillator frequency. Connecting SYNC to GND or to VL selects 200kHz operation; connecting to REF selects 300kHz operation. SYNC can also be driven with an external 240kHz to 350kHz CMOS/TTL source to synchronize the internal oscillator.

Normally, 300kHz is used to minimize the inductor and filter capacitor sizes, but 200kHz may be necessary for low input voltages (see *Low-Voltage (6-Cell) Operation*).

Comparators

Two noninverting comparators can be used as precision voltage comparators or high-side drivers. The supply for these comparators (VH) is brought out and may be connected to any voltage between +3V and +19V irrespective of V+. The noninverting inputs (D1-D2) are high impedance, and the inverting input is internally connected to a 1.650V reference. Each output (Q1-Q2) sources 20µA from VH when its input is above 1.650V, and sinks 500µA to GND when its input is below 1.650V. The Q1-Q2 outputs can be fixed together in wired-OR configuration since the pull-up current is only 20µA.

Connecting VH to a logic supply (5V or 3V) allows the comparators to be used as low-battery detectors. For driving N-channel power MOSFETs to turn external loads on and off, VH should be 6V to 12V higher than the load voltage. This enables the MOSFETs to be fully turned on and results in low $r_{DS(ON)}$.

The comparators are always active when V+ is above +4V, even when VH is 0V. Thus, Q1-Q2 will sink current to GND even when VH is 0V, but they will only source current from VH when VH is above approximately 1.5V.

If Q1 or Q2 is externally pulled above VH, an internal diode conducts, pulling VH a diode drop below the output and powering anything connected to VH. This voltage will also power the other comparator outputs.

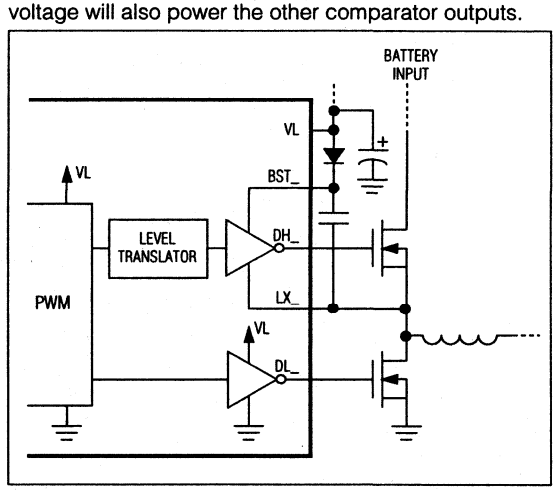


Figure 4. Boost Supply for Gate Drivers

Table 1. Surface-Mount Components

(See Figure 1 for Standard Application Circuit.)

COMPONENT	SPECIFICATION	MANUFACTURER	PART NO.
C1, C10	33µF, 35V tantalum capacitors	AVX Sprague	TPSE226M035R0100 595D336X0035R
C2	4.7µF, 6V tantalum capacitor	AVX Sprague	TAJB475M016 595D475X0016A
C3	1µF, 20V tantalum capacitor	AVX Sprague	TAJA105M025 595D105X0020A2B
C4, C5	0.1µF, 16V ceramic capacitors	Murata-Erie	GRM42-6X7R104K50V
C6	330µF, 10V tantalum capacitor	Sprague	595D337X0010R
C7, C12	150µF, 10V tantalum capacitors	Sprague	595D157X0010D
C8, C9	0.01µF, 16V ceramic capacitors	Murata-Erie	GRM42-6X7R103K50V
D2A, D2B	1N4148-type dual diode	Central Semiconductor	CMPD2836
D1, D3	1N5819 SMT diodes	Nihon	EC10QS04
L1, L2	10µH, 2.65A inductor	Sumida	CDR125-100
N1–N4	N-channel MOSFETs (SO-8)	Siliconix	Si9410DY
R1, R2	0.025Ω, 1% (SMT) resistor	IRC	LR2010-01-R025-F

Table 2. Component Suppliers

COMPANY	FACTORY FAX [COUNTRY CODE]	USA PHONE
AVX	[1] (207) 283-1941	(207) 282-5111 (800) 282-4975
Central Semiconductor	[1] (516) 435-1824	(516) 435-1110
IRC	[1] (213) 992-3377	(512) 992-7900
Murata-Erie	[1] (404) 736-3030	(404) 736-1300
Nihon	[81] 3-3494-7414	(805) 867-2555
Siliconix	[1] (408) 727-5414	(408) 988-8000
Sprague	[1] (508) 339-5063	(508) 339-8900
Sumida	[81] 3-3607-5428	(708) 956-0666

Internal VL and REF Supplies

An internal linear regulator produces the 5V used by the internal control circuits. This regulator's output is available on pin VL and can source 5mA for external loads. Bypass VL to GND with 4.7µF. To save power, when the +5V switch-mode supply is above 4.5V, the internal linear regulator is turned off and the high-efficiency +5V switch-mode supply output is connected to VL.

The internal 3.3V bandgap reference (REF) is powered by the internal 5V VL supply. It can furnish up to 5mA. Bypass REF to GND with 0.22µF, plus 1µF/mA of load current. The main switching outputs track the reference voltage. Loading the reference will reduce the main outputs slightly, according to the reference load-regulation error.

Both the VL and REF outputs remain active, even when the switching regulators are turned off, to supply memory keep-alive power (see *Shutdown Mode* section).

These linear-regulator outputs can be directly connected to the corresponding step-down regulator outputs (i.e., REF to +3.3V, VL to +5V) to keep the main supplies alive in standby mode. However, to ensure start-up, standby load currents must not exceed 5mA on each supply.

Fault Protection

The +3.3V and +5V PWM supplies and the comparators are disabled when either of two faults is present: VL < +4.0V or REF < +2.8V (85% of its nominal value).

Design Procedure

Figure 1's schematic and Table 2's component list show values suitable for a 3A, +5V supply and a 3A, +3.3V supply. This circuit operates with input voltages from 6.5V to 30V, and maintains high efficiency with output currents between 5mA and 3A (see the *Typical Operating Characteristics*). This circuit's components may be changed if the design guidelines described in this section are used—but before beginning the design, the following information should be firmly established:

Dual-Output Power-Supply Controller for Notebook Computers

$V_{IN(MAX)}$, the maximum input (battery) voltage. This value should include the worst-case conditions under which the power supply is expected to function, such as no-load (standby) operation when a battery charger is connected but no battery is installed. $V_{IN(MAX)}$ cannot exceed 30V.

$V_{IN(MIN)}$, the minimum input (battery) voltage. This value should be taken at the full-load operating current under the lowest battery conditions. If $V_{IN(MIN)}$ is below about 6.5V, the filter capacitance required to maintain good AC load regulation increases, and the current limit for the +5V supply has to be increased for the same load level.

Inductor (L1, L2)

Three inductor parameters are required: the inductance value (L), the peak inductor current (I_{LPEAK}), and the coil resistance (R_L). The inductance is:

$$L = \frac{(V_{OUT})(V_{IN(MAX)} - V_{OUT})}{(V_{IN(MAX)})(f)(I_{OUT})(LIR)}$$

where: V_{OUT} = output voltage (3.3V or 5V);
$V_{IN(MAX)}$ = maximum input voltage (V);
f = switching frequency, normally 300kHz;
I_{OUT} = maximum DC load current (A);
LIR = ratio of inductor peak-to-peak AC current to average DC load current, typically 0.3.

A higher value of LIR allows smaller inductance, but results in higher losses and higher ripple.

The highest peak inductor current (I_{LPEAK}) equals the DC load current (I_{OUT}) plus half the peak-to-peak AC inductor current (I_{LPP}). The peak-to-peak AC inductor current is typically chosen as 30% of the maximum DC load current, so the peak inductor current is 1.15 times I_{OUT}.

The peak inductor current at full load is given by:

$$I_{LPEAK} = I_{OUT} + \frac{(V_{OUT})(V_{IN(MAX)} - V_{OUT})}{(2)(f)(L)(V_{IN(MAX)})}.$$

The coil resistance should be as low as possible, preferably in the low milliohms. The coil is effectively in series with the load at all times, so the wire losses alone are approximately:

$$\text{Power loss} = (I_{OUT}^2)(R_L).$$

In general, select a standard inductor that meets the L, I_{LPEAK}, and R_L requirements (see Tables 1 and 2). If a standard inductor is unavailable, choose a core with an LI^2 parameter greater than (L) (I_{LPEAK}^2), and use the largest wire that will fit the core.

Current-Sense Resistors (R1, R2)

The sense resistors must carry the peak current in the inductor, which exceeds the full DC load current. The internal current limiting starts when the voltage across the sense resistors exceeds 100mV nominally, 80mV minimum. Use the minimum value to ensure adequate output current capability: For the +3.3V supply, R1 = 80mV / (1.15 x I_{OUT}); for the +5V supply, R2 = 80mV/(1.15 x I_{OUT}), assuming that LIR = 0.3.

Since the sense resistance values (e.g., R1 = 25mΩ for I_{OUT} = 3A) are similar to a few centimeters of narrow traces on a printed circuit board, trace resistance can contribute significant errors. To prevent this, Kelvin connect the CS_ and FB_ pins to the sense resistors; i.e., use separate traces not carrying any of the inductor or load current, as shown in Figure 5.

Run these traces parallel at minimum spacing from one another. The wiring layout for these traces is critical for stable, low-ripple outputs (see the *Layout and Grounding* section).

MOSFET Switches (N1-N4)

The four N-channel power MOSFETs are usually identical and must be "logic-level" FETs; that is, they must be fully on (have low $r_{DS(ON)}$) with only 4V gate-source drive voltage. The MOSFET $r_{DS(ON)}$ should ideally be about twice the value of the sense resistor. MOSFETs with even lower $r_{DS(ON)}$ have higher gate capacitance, which increases switching time and transition losses.

MOSFETs with low gate-threshold voltage specifications (i.e., maximum $V_{GS(TH)}$ = 2V rather than 3V) are preferred, especially for high-current (5A) applications.

Output Filter Capacitors (C6, C7, C12)

The output filter capacitors determine the loop stability and output ripple voltage. To ensure stability, the minimum capacitance and maximum ESR values are:

$$C_F > \frac{V_{REF}}{(V_{OUT})(R_{CS})(2)(\pi)(GBWP)}$$

and,

$$ESR_{CF} < \frac{(V_{OUT})(R_{CS})}{V_{REF}}$$

where: C_F = output filter capacitance (F);
V_{REF} = reference voltage, 3.3V;
V_{OUT} = output voltage, 3.3V or 5V;
R_{CS} = sense resistor (Ω);
GBWP = gain-bandwidth product, 60kHz;
ESR_{CF} = output filter capacitor ESR (Ω).

Be sure to select output capacitors that satisfy **both** the minimum capacitance and maximum ESR requirements. To achieve the low ESR required, it may be appropriate to use a capacitance value 2 or 3 times larger than the calculated minimum.

The output ripple in continuous-current mode is:

$V_{OUT(RPL)} = I_{LPP(MAX)} \times (ESR_{CF} + 1/(2 \times \pi \times f \times C_F))$.

In idle-mode, the ripple has a capacitive and resistive component:

$$V_{OUT(RPL)}(C) = \frac{(4)(10^{-4})(L)}{(R_{CS}^2)(C_F)} \times \left(\frac{1}{V_{OUT}} + \frac{1}{V_{IN} - V_{OUT}} \right) \text{ Volts}$$

$$V_{OUT(RPL)}(R) = \frac{(0.02)(ESR_{CF})}{R_{CS}} \text{ Volts}$$

The total ripple, $V_{OUT(RPL)}$, can be approximated as follows:

if $V_{OUT(RPL)}(R) < 0.5\ V_{OUT(RPL)}(C)$,
then $V_{OUT(RPL)} = V_{OUT(RPL)}(C)$,
otherwise, $V_{OUT(RPL)} = 0.5\ V_{OUT(RPL)}(C) + V_{OUT(RPL)}(R)$.

Diodes D1 and D3

Use 1N5819s or similar Schottky diodes. D1 and D3 conduct only about 3% of the time, so the 1N5819's 1A current rating is conservative. The voltage rating of D1 and D3 must exceed the maximum input supply voltage from the battery. These diodes must be Schottky diodes to prevent the lossy MOSFET body diodes from turning on, and they must be placed physically close to their associated synchronous rectifier MOSFETs.

Soft-Start Capacitors (C8, C9)

A capacitor connected from GND to either SS pin causes that supply to ramp up slowly. The ramp time to full current limit, t_{SS}, is approximately 1ms for every nF of capacitance on SS_, with a minimum value of 10µs. Typical capacitor values are in the 10nF to 100nF range; a 5V rating is sufficient.

Because this ramp is applied to the current-limit circuit, the actual time for the output voltage to ramp up depends on the load current and output capacitor value. Using Figure 1's circuit with a 2A load and no SS capacitor, full output voltage is reached about 600µs after ON_ is driven high.

Boost Capacitors (C4, C5)

Capacitors C4 and C5 store the boost voltage and provide the supply for the DH3 and DH5 drivers. Use 0.1µF and place each within 10mm of the BST_ and LX_ pins.

Boost Diodes (D1A, D1B)

Use high-speed signal diodes; e.g., 1N4148 or equivalent.

Bypass Capacitors

Input Filter Capacitors (C1, C10)

Use at least 3µF/W of output power for the input filter capacitors, C1 and C10. They should have less than 150mΩ ESR, and should be located no further than 10mm from N1 and N2 to prevent ringing. Connect the negative terminals directly to PGND. Do not exceed the surge current ratings of input bypass capacitors.

Shutdown Mode

Shutdown ($\overline{SHDN}$ = low) forces both PWMs off and disables the REF output and both comparators (Q1 = Q2 = 0V). Supply current in shutdown mode is typically 25µA. The VL supply remains active and can source 25mA for external loads. Note that the VL load capability is higher in shutdown and standby modes than when the PWMs are operating (25mA vs. 5mA). Standby mode is achieved by holding ON3 and ON5 low while $\overline{SHDN}$ is high. This disables both PWMs, but keeps VL, REF, and the precision comparators alive. Supply current in standby mode is typically 70µA.

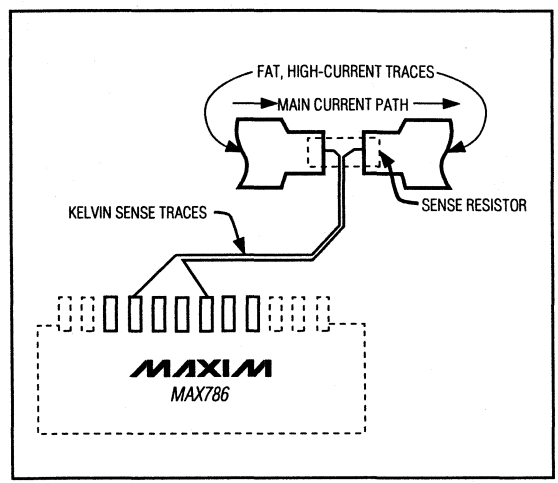


Figure 5. Kelvin Connections for the Current-Sense Resistors

Dual-Output Power-Supply Controller for Notebook Computers

Table 3. EV Kit Power-Supply Controls (SW1)

SWITCH	NAME	FUNCTION	ON SETTING	OFF SETTING
1	$\overline{SHDN}$	Enable shutdown mode	Operate	Shutdown
2	ON3	Enable 3.3V power supply	3.3V ON	3.3V OFF
3	ON5	Enable 5.0V power supply	5V ON	5V OFF
4	SYNC	Oscillator	200kHz	300kHz

Other ways to shut down the MAX786 are suggested in the applications section of the MAX782/MAX783 data sheet.

Applications Information

Low-Voltage (6-Cell) Operation

The standard application circuit can be configured to accept input voltages from 5.5V to 12V by changing the oscillator frequency to 200kHz and increasing the +5V filter capacitor to 660µF. This allows stable operation at 5V loads up to 2A (the 3.3V side requires no changes and still delivers 3A).

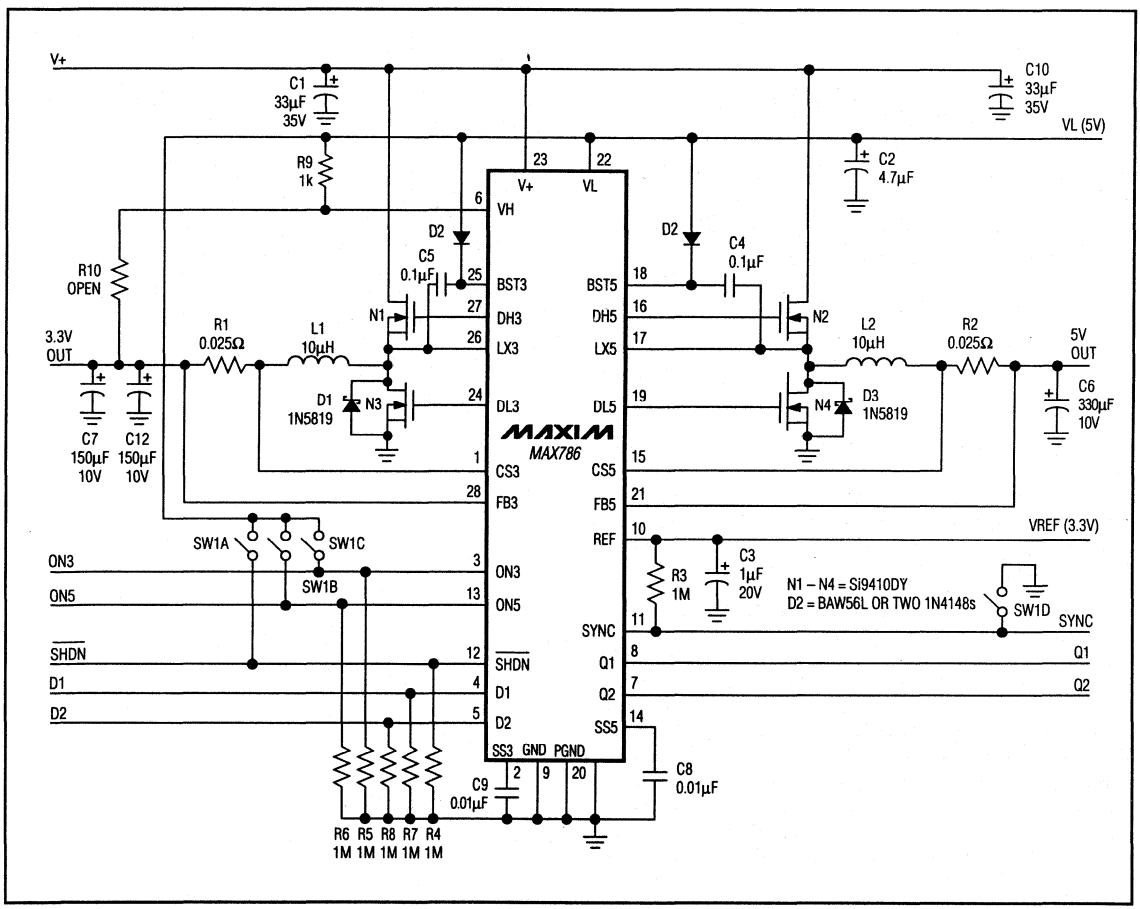


Figure 6. MAX786 EV Kit Schematic

19-0182; Rev 0; 9/93

MAXIM

5V/3.3V/3V 5A Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

The MAX787/MAX788/MAX789 are monolithic, bipolar, pulse-width modulation (PWM), switch-mode, step-down DC-DC regulators. Each is rated at 5A. Very few external components are needed for standard operation because the power switch, oscillator, feedback, and control circuitry are all on-chip. Employing a classic buck topology, these regulators perform high-current step-down functions.

The MAX787/MAX788/MAX789 have excellent dynamic and transient response characteristics, while featuring cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. They also have a wide 8V to 40V input range (up to 60V for the high-voltage "H" version).

Each regulator is available in 5-pin TO-220, 7-pin TO-220, and 4-pin TO-3. These devices have a preset 100kHz oscillator frequency and a preset current limit of 6.5A. The 7-pin package allows for adjustable current limit and micropower shutdown. See the MAX724/MAX726 data sheet for more applications information.

Applications

Distributed Power from High-Voltage Buses
High-Current, High-Voltage Step-Down
Multiple-Output Buck Converter

Features

- **Input Range: Up to 40V**
  Up to 60V (H Version)
- **5A On-Chip Power Switch**
- **Fixed Outputs: 5V (MAX787)**
  3.3V (MAX788)
  3V (MAX789)
- **100kHz Switching Frequency**
- **Excellent Dynamic Characteristics**
- **Few External Components**
- **8.5mA Quiescent Current**
- **TO-220 and TO-3 Packages**

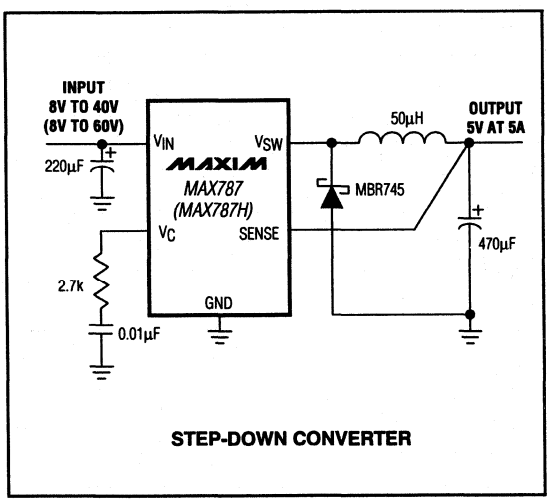
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX787CCK	0°C to +70°C	5 TO-220
MAX787CCM	0°C to +70°C	7 TO-220†
MAX787CKS	0°C to +70°C	4 TO-3†
MAX787C/D	0°C to +70°C	Dice*
MAX787ECK	-40°C to +85°C	5 TO-220
MAX787ECM	-40°C to +85°C	7 TO-220†
MAX787EKS	-40°C to +85°C	4 TO-3†
MAX787MKS	-55°C to +125°C	4 TO-3†

Ordering Information continued on last page.

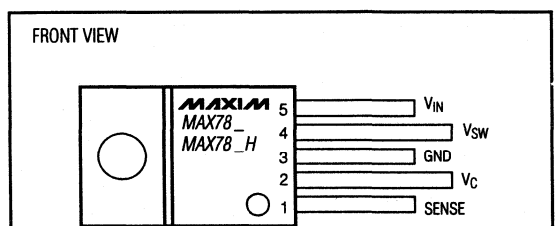
* *Contact factory for dice specifications.*
† *Contact factory for package availability.*

Typical Operating Circuit



STEP-DOWN CONVERTER

Pin Configurations



5-PIN TO-220

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STRAIGHT PINS.
Pin Configurations continued on last page.

5V/3.3V/3V 5A Step-Down, PWM, Switch-Mode DC-DC Regulators

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- MAX78_ 45V
- MAX78_H 64V

Switch Voltage with Respect to Input Voltage
- MAX78_ 64V
- MAX78_H 75V

Switch Voltage with Respect to GND Pin (V_{SW} negative)
- MAX78_ (Note 8) 35V
- MAX78_H (Note 8) 45V

SENSE Pin Voltage ..... -0.3V, +10V
SHUT Pin Voltage (not to exceed V_{IN}) 40V
I_{LIM} Pin Voltage (forced) 5.5V

Operating Temperature Ranges:
- MAX78_C_ _/HC_ _ ..... 0°C to +70°C
- MAX78_E_ _/HE_ _ ..... -40°C to +85°C
- MAX78_MKS/HMKS ..... -55°C to +125°C

Junction Temperature Ranges:
- MAX78_C_ _/HC_ _ ..... 0°C to +125°C
- MAX78_E_ _/HE_ _ ..... -40°C to +125°C
- MAX78_MKS/HMKS ..... -55°C to +150°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 25V, T_j = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch-On Voltage (Note 1)	I_{SW} = 1A	$T_j \geq 0°C$			1.85	V
		$T_j < 0°C$			2.10	
	I_{SW} = 5A	$T_j \geq 0°C$			2.30	
		$T_j < 0°C$			2.50	
Switch-Off Leakage	$V_{IN} = \leq 25V$, V_{SW} = 0V	T_j = +25°C		5	300	µA
	$V_{IN} = V_{MAX}$, V_{SW} = 0V (Note 2)	T_j = +25°C		10	500	
Supply Current (Note 3)	$V_{IN} \leq 40V$, V_{SENSE} = 5.5V			8.5	11	mA
	"H" version only, 40V < V_{IN} < 60V			9	12	
	V_{SHUT} = 0.1V (Note 4)			140	300	µA
Minimum Operating Supply Voltage				7.3	8.0	V
Minimum Start-Up Supply Voltage (Note 5)	$T_A \geq +25°C$			3.5	4.8	V
	$T_A < +25°C$			3.5	5.0	
Switch-Current Limit (Note 6)	I_{LIM} open	$T_j = T_{MIN}$ to T_{MAX}	5.5	6.5	8.5	A
	R_{LIM} = 10kΩ (Note 7)	T_j = +25°C		4.5		
	R_{LIM} = 7kΩ (Note 7)	T_j = +25°C		3		
Maximum Duty Cycle			85	90		%
Switching Frequency		T_j = +25°C	90	100	110	kHz
		$T_j \leq +125°C$	85		120	
	V_{OUT} = V_{SENSE} = 0V (Note 6)	T_j = +25°C		20		
Switching Frequency Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)			0.03	0.10	%/V
Error-Amplifier Voltage Gain	1V ≤ V_C ≤ 4V	T_j = +25°C		2000		V/V
Error-Amplifier Transconductance		T_j = +25°C	3700	5000	8000	µmho
Error-Amplifier Source Current	V_{SENSE} = V_{OUT} + 10%	T_j = +25°C	100	140	225	µA
Error-Amplifier Sink Current	V_{SENSE} = V_{OUT} - 10%	T_j = +25°C	0.7	1.0	1.6	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 25V, T_j = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SENSE Voltage	V_C = 2V	MAX787	4.85	5.00	5.15	V
		MAX788	3.20	3.30	3.40	
		MAX789	2.90	3.00	3.10	
SENSE Pin Divider Resistance	T_j = +25°C	MAX787	3.0	5.0	8.0	kΩ
		MAX788	2.5	4.2	7.0	
		MAX789	2.2	3.8	6.5	
Output Voltage Tolerance	V_{OUT} (nominal) = 5V (MAX787), 3.3V (MAX788), or 3V (MAX789); all conditions of input voltage, output voltage, and load current	T_j = +25°C		±0.5	±2.0	%
		T_j = T_{MIN} to T_{MAX}		±1.0	±3.0	
Output Voltage Line Regulation	8V ≤ V_{IN} ≤ V_{MAX} (Note 2)			0.005	0.020	%/V
V_C Voltage	0% duty cycle	T_j = +25°C		1.5		V
V_C Voltage Temperature Coefficient	0% duty cycle	T_j = T_{MIN} to T_{MAX}		-4		mV/°C
SHUT Pin Current	V_{SHUT} = 5V		5	10	20	µA
	V_{SHUT} ≤ $V_{THRESHOLD}$ (≈ 2.5V)				50	
SHUT Thresholds	Switch duty cycle = 0%		2.20	2.45	2.70	V
	Fully shut down		0.10	0.30	0.50	
Thermal Resistance Junction to Case (Note 9)					2.5	°C/W

Note 1: For switch currents between 1A and 5A, maximum switch-on voltage can be calculated via linear interpolation.

Note 2: V_{MAX} = 40V for MAX787/MAX788/MAX789 and 60V for MAX787H/MAX788H/MAX789H.

Note 3: By setting the SENSE pin to 5.5V, the V_C pin is forced to its low clamp level and the switch duty cycle is forced to zero, approximating the zero load condition.

Note 4: Device shut down. Switch leakage current not included.

Note 5: For proper regulation, total voltage from V_{IN} to GND must be ≥ 8V after start-up.

Note 6: To avoid extremely short switch-on times, the switch frequency is internally scaled down when V_{SENSE} is less than 2.6V (MAX787), 2.0V (MAX788), or 1.8V (MAX789). Switch current limit is tested with V_{SENSE} adjusted to give a 1µs minimum switch-on time.

Note 7: $R_{LIM} = \left[\frac{I_{LIM}}{1A} \times 2k\Omega\right] + 1k\Omega$.

Note 8: Do not exceed switch-to-input voltage limitation.

Note 9: Guaranteed, not production tested.

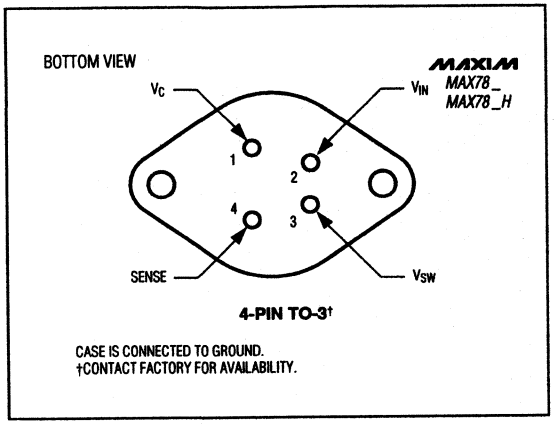
5V/3.3V/3V 5A Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Description

PIN			NAME	FUNCTION
5-PIN TO-220	4-PIN TO-3	7-PIN TO-220		
1	4	5	SENSE	SENSE Input is the internal error amplifier's input, and should be directly connected to V_{OUT}. SENSE also aids current limiting by reducing oscillator frequency when V_{OUT} is low.
2	1	6	V_C	Error-Amplifier Output. A series RC network connected to this pin compensates the MAX787/MAX788/MAX789. Output swing is limited to about 5.8V in the positive direction and -0.7V in the negative direction. V_C can also synchronize the MAX787/MAX788/MAX789 to an external TTL clock in the 115kHz to 170kHz range.
3	CASE	4	GND	Ground requires a short, low-noise connection to ensure good load regulation. The internal reference is referred to GND, so errors at this pin are multiplied by the error amplifier.
4	3	2	V_{SW}	Internal Power Switch Output. The switch output can swing 40V below ground and is rated for 5A.
5	2	1	V_{IN}	V_{IN} supplies power to the internal circuitry and also connects to the collector of the internal power switch. V_{IN} must be bypassed with a low-ESR capacitor, typically 200µF or 220µF.
–	–	3	I_{LIM}	Switch current limit can be reduced by connecting an external resistor (R_{LIM}) from I_{LIM} to GND (7-pin version only).
–	–	7	SHUT	Shutdown is achieved by pulling SHUT low (7-pin version only). Below 2.45V turns off the switch. Below 0.3V forces total device shutdown. Leave open, or drive above 2.7V to turn the device fully on.

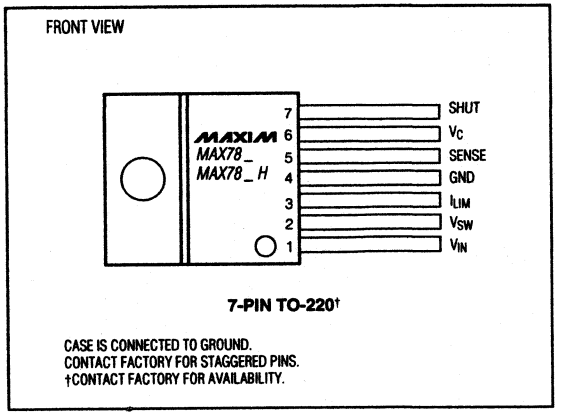
5V/3.3V/3V 5A Step-Down, PWM, Switch-Mode DC-DC Regulators

Pin Configurations (continued)



4-PIN TO-3†

CASE IS CONNECTED TO GROUND.
†CONTACT FACTORY FOR AVAILABILITY.



7-PIN TO-220†

CASE IS CONNECTED TO GROUND.
CONTACT FACTORY FOR STAGGERED PINS.
†CONTACT FACTORY FOR AVAILABILITY.

4

5V/3.3V/3V 5A Step-Down, PWM, Switch-Mode DC-DC Regulators

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX787HCCK	0°C to +70°C	5 TO-220
MAX787HCCM	0°C to +70°C	7 TO-220†
MAX787HCKS	0°C to +70°C	4 TO-3†
MAX787HC/D	0°C to +70°C	Dice*
MAX787HECK	-40°C to +85°C	5 TO-220
MAX787HECM	-40°C to +85°C	7 TO-220†
MAX787HEKS	-40°C to +85°C	4 TO-3†
MAX787HMKS	-55°C to +125°C	4 TO-3†
MAX788CCK	0°C to +70°C	5 TO-220
MAX788CCM	0°C to +70°C	7 TO-220†
MAX788CKS	0°C to +70°C	4 TO-3†
MAX788C/D	0°C to +70°C	Dice*
MAX788ECK	-40°C to +85°C	5 TO-220
MAX788ECM	-40°C to +85°C	7 TO-220†
MAX788EKS	-40°C to +85°C	4 TO-3†
MAX788MKS	-55°C to +125°C	4 TO-3†
MAX788HCCK	0°C to +70°C	5 TO-220
MAX788HCCM	0°C to +70°C	7 TO-220†
MAX788HCKS	0°C to +70°C	4 TO-3†
MAX788HC/D	0°C to +70°C	Dice*
MAX788HECK	-40°C to +85°C	5 TO-220
MAX788HECM	-40°C to +85°C	7 TO-220†
MAX788HEKS	-40°C to +85°C	4 TO-3†
MAX788HMKS	-55°C to +125°C	4 TO-3†

PART	TEMP. RANGE	PIN-PACKAGE
MAX789CCK	0°C to +70°C	5 TO-220
MAX789CCM	0°C to +70°C	7 TO-220†
MAX789CKS	0°C to +70°C	4 TO-3†
MAX789C/D	0°C to +70°C	Dice*
MAX789ECK	-40°C to +85°C	5 TO-220
MAX789ECM	-40°C to +85°C	7 TO-220†
MAX789EKS	-40°C to +85°C	4 TO-3†
MAX789MKS	-55°C to +125°C	4 TO-3†
MAX789HCCK	0°C to +70°C	5 TO-220
MAX789HCCM	0°C to +70°C	7 TO-220†
MAX789HCKS	0°C to +70°C	4 TO-3†
MAX789HC/D	0°C to +70°C	Dice*
MAX789HECK	-40°C to +85°C	5 TO-220
MAX789HECM	-40°C to +85°C	7 TO-220†
MAX789HEKS	-40°C to +85°C	4 TO-3†
MAX789HMKS	-55°C to +125°C	4 TO-3†

** Contact factory for dice specifications.*
† Contact factory for package availability.

Product Selection Guide

PART	V_{OUT} (V)	I_{OUT} MAX (A)
MAX724	Adjustable	5
MAX726	Adjustable	2
MAX727	5	2
MAX728	3.3	2
MAX729	3	2
MAX787	5	5
MAX788	3.3	5
MAX789	3	5

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

Step-Down Controllers with Synchronous Rectifier for CPU Power

General Description

The MAX796–MAX799 high-performance, step-down DC-DC converters with single or dual outputs provide main CPU power in battery-powered systems. These buck controllers achieve up to 95% efficiency by using synchronous rectification and Maxim's proprietary Idle Mode™ control scheme to extend battery life at full-load (up to 10A) and no-load outputs. Excellent dynamic response corrects output transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Unique bootstrap circuitry drives inexpensive N-channel MOSFETs, reducing system cost and eliminating the crowbar switching currents found in some PMOS/NMOS switch designs.

The MAX796/MAX799 are specially equipped with a secondary feedback input (SECFB) for transformer-based dual-output applications. This secondary feedback path improves cross-regulation of positive (MAX796) or negative (MAX799) auxiliary outputs.

The MAX797/MAX798 have a logic-controlled and synchronizable fixed-frequency pulse-width-modulating (PWM) operating mode, which reduces noise and RF interference in sensitive mobile-communications and pen-entry applications. The $\overline{SKIP}$ override input allows automatic switchover to idle-mode operation (for high-efficiency pulse skipping) at light loads, or forces fixed-frequency mode for lowest noise at all loads.

The MAX796–MAX799 are all available in 16-pin DIP and narrow SO packages. See the table below to compare these four converters.

PART	MAIN OUTPUT	SPECIAL FEATURE
MAX796	3.3V/5V or adj.	Regulates positive secondary voltage (such as +12V)
MAX797	3.3V/5V or adj.	Logic-controlled low-noise mode
MAX798	2.9V/5V or adj.	Logic-controlled low-noise mode
MAX799	3.3V/5V or adj.	Regulates negative secondary voltage (such as -5V)

Applications

Notebook and Subnotebook Computers

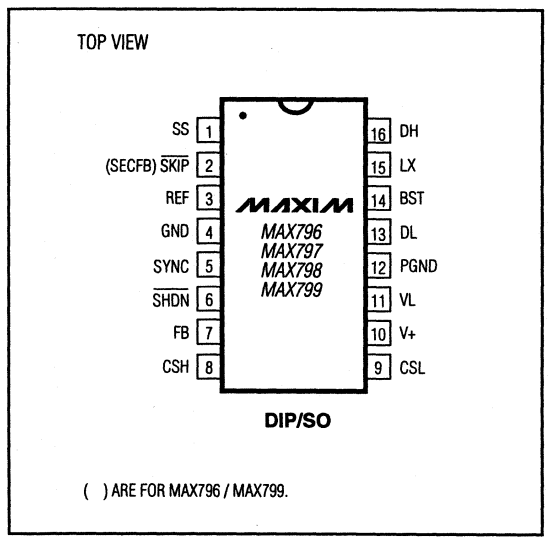
PDAs and Mobile Communicators

Cellular Phones

Features

- ♦ **>95% Efficiency**
- ♦ **4.5V to 30V Input Range**
- ♦ **2.5V to 6V Adjustable Output**
- ♦ **Preset 2.9V, 3.3V, and 5V Outputs (at up to 10A)**
- ♦ **Multiple Regulated Outputs**
- ♦ **+5V Linear-Regulator Output**
- ♦ **Precision 2.505V Reference Output**
- ♦ **Automatic Bootstrap Circuit**
- ♦ **150kHz/300kHz Fixed-Frequency PWM Operation**
- ♦ **Programmable Soft-Start**
- ♦ **375µA Typ Quiescent Current (V_{IN} = 12V, V_{OUT} = 5V)**
- ♦ **1µA Typ Shutdown Current**

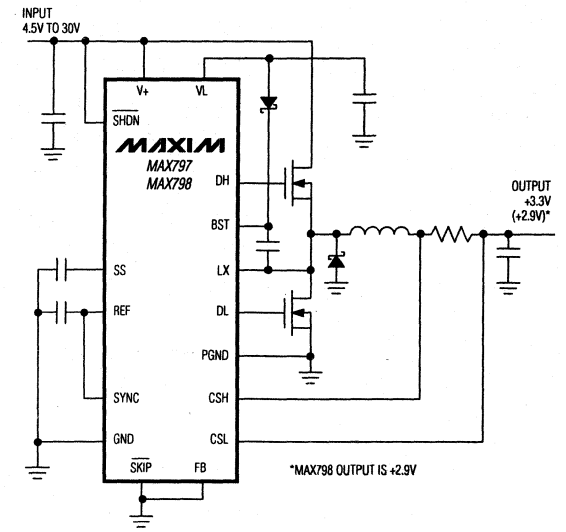
Pin Configuration

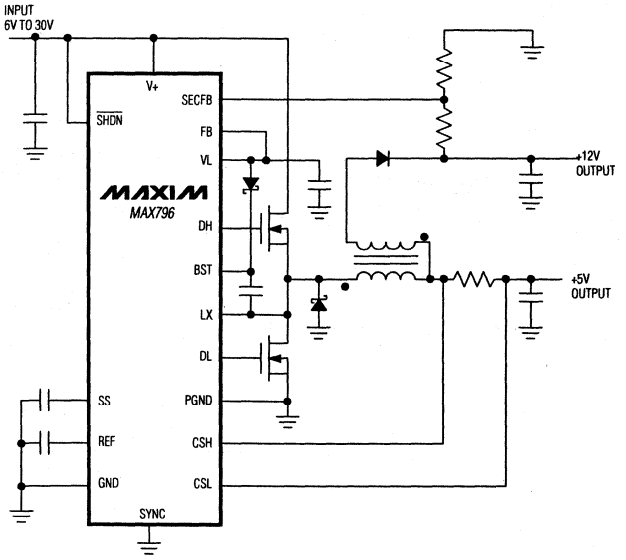


™ *Idle Mode is a trademark of Maxim Integrated Products.*

Step-Down Controllers with Synchronous Rectifier for CPU Power

Typical Operating Circuits





ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/94
EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V/Adjustable-Output, 1A, Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

The MAX830/MAX831/MAX832/MAX833 are monolithic, bipolar, pulse-width-modulation (PWM), switch-mode, step-down DC-DC regulators. Each is rated at 1A. Very few external components are needed for standard operation because the power switch, oscillator, feedback, and control circuitry are all on-chip. Employing a classic buck topology, these regulators perform high-current step-down functions.

These regulators have excellent dynamic and transient response characteristics, while featuring cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. They have a wide 8V to 40V input range. Outputs for the MAX831/MAX832/MAX833 are fixed at 5V/3.3V/3V, respectively. The MAX830 output is adjustable.

Available in 16-pin SO packages, the MAX830–MAX833 have a preset 100kHz oscillator frequency. In addition, the preset current limit and micropower shutdown can be externally controlled. See the MAX724/MAX726 data sheet for more applications information.

Applications

Distributed Power from High-Voltage Buses

High-Current, High-Voltage Step-Down Applications

Multiple-Output Buck Converter

Features

- ♦ **Input Range: Up to 40V**
- ♦ **1A On-Chip Power Switch**
- ♦ **Adjustable Output (MAX830)**
  Fixed Outputs: 5V (MAX831)
  3.3V (MAX832)
  3V (MAX833)
- ♦ **100kHz Switching Frequency**
- ♦ **Excellent Dynamic Characteristics**
- ♦ **Few External Components**
- ♦ **8mA Quiescent Current**
- ♦ **16-Pin SO Package**
- ♦ **Evaluation Kit Available**

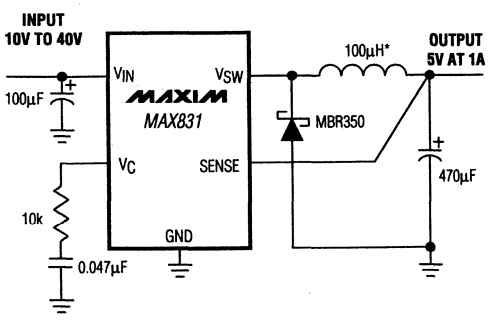
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX830CWE	0°C to +70°C	16 Wide SO
MAX831CWE	0°C to +70°C	16 Wide SO
MAX832CWE	0°C to +70°C	16 Wide SO
MAX833CWE	0°C to +70°C	16 Wide SO

PART	TEMP. RANGE	BOARD TYPE
MAX831EVKIT-SO	0° to +70°C	Surface Mount

4

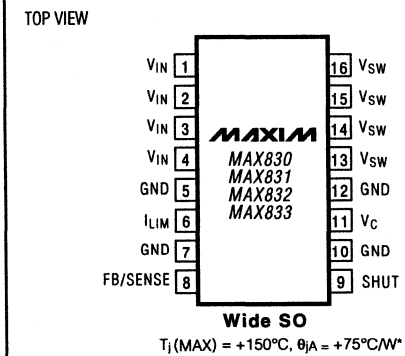
Typical Operating Circuit



STEP-DOWN CONVERTER

* Coilcraft DO3316-104

Pin Configuration



Wide SO

$T_j(MAX) = +150°C$, $\theta_{JA} = +75°C/W$*

* THIS THERMAL RESISTANCE NUMBER IS FOR A TYPICAL MOUNTING TECHNIQUE. LOWER THERMAL RESISTANCE CAN BE OBTAINED WITH LARGE COPPER GROUND, THERMAL PASTE, OR HEATSINKS.

19-0238; Rev 0; 3/94

EVALUATION KIT AVAILABLE

MAXIM

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

General Description

The MAX850–MAX853 low-noise, inverting, charge-pump power supplies are ideal for biasing GaAs FETs in cellular telephone transmitter amplifiers.

The MAX850–MAX852 offer both preset (-4.1V) and adjustable (-0.5V to -9.0V) output voltages. The MAX853 uses an external positive control voltage to set the negative output voltage. Input voltage range for all four devices is 4.5V to 10V. Output current is 5mA.

An internal linear regulator reduces the output voltage ripple to 2mVp-p. With a well-filtered control voltage (V_{CTRL}), the MAX853 achieves typical output ripple of less than 1mVp-p. Supply current is 3mA max and shutdown current is less than 1µA max over temperature (5µA max for MAX851).

Applications

Cellular Phones

Negative Regulated Power Supplies

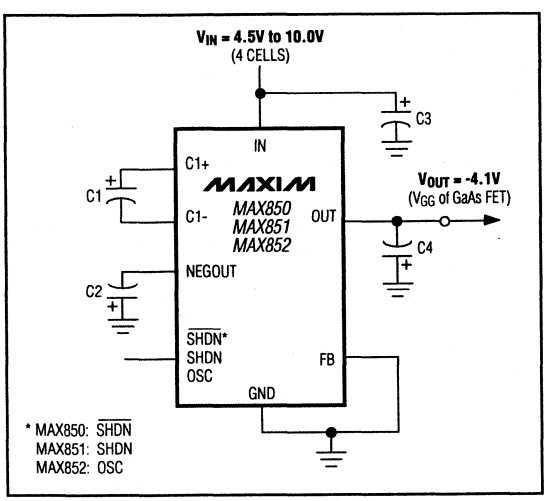
Personal Communicators, PDAs

Wireless Data Loggers

Continuously Adjustable GaAs FET Bias

LCD-Bias Contrast Control

Typical Operating Circuit



Features

- ♦ **Fixed -4.1V or Adjustable -0.5V to -9V Output at 5mA**
- ♦ **4.5V to 10V Input Voltage Range**
- ♦ **2mVp-p Output Voltage Ripple (MAX850–MAX852)**
  1mVp-p Output Voltage Ripple (MAX853)
- ♦ **100kHz Charge-Pump Switching Frequency (MAX850/MAX851/MAX853)**
- ♦ **External Synchronizing Clock Input (MAX852)**
- ♦ **Logic-Level Shutdown Mode: 1µA Max Over Temperature (MAX850/MAX852/MAX853)**
- ♦ **Low Cost, 8-Pin SO Package**

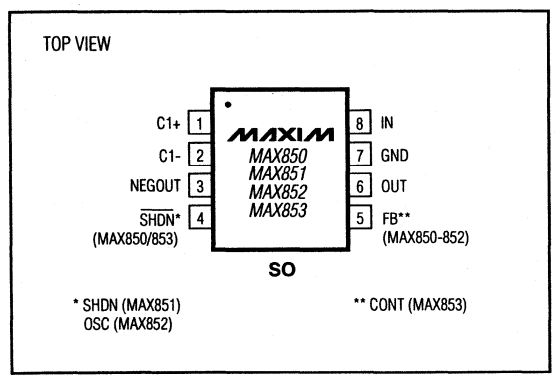
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX850CSA	0°C to +70°C	8 SO
MAX850C/D	0°C to +70°C	Dice*
MAX850ESA	-40°C to +85°C	8 SO
MAX851CSA	0°C to +70°C	8 SO
MAX851C/D	0°C to +70°C	Dice*
MAX851ESA	-40°C to +85°C	8 SO
MAX852CSA	0°C to +70°C	8 SO
MAX852C/D	0°C to +70°C	Dice*
MAX852ESA	-40°C to +85°C	8 SO
MAX853CSA	0°C to +70°C	8 SO
MAX853C/D	0°C to +70°C	Dice*
MAX853ESA	-40°C to +85°C	8 SO

*Dice are specified at T_A = +25°C only.

PART	TEMP. RANGE	BOARD TYPE
MAX850EVKIT-SO	0°C to +70°C	Surface Mount

Pin Configuration



Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} to GND .....-0.3V to 10.5V
V_{NEGOUT} to GND .....-10.5V to 0.3V
V_{IN} to V_{NEGOUT} .....-0.3V to 21V
$\overline{V_{OUT}}$ to GND (Note 1) .....V_{NEGOUT} to 0.3V
$\overline{SHDN}$ or OSC (pin 4) Voltage to GND .....-0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges
MAX85_C_ _ .....0°C to +70°C
MAX85_ESA .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The output may be shorted to NEGOUT or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(+5V ≤ V_{IN} ≤ +10V, GND = 0V, V_{OUT} = -4.1V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. A 100kHz, 50% duty cycle square wave between GND and V_{IN} is applied to the OSC pin of the MAX852.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range (Note 2)	V_{IN}		5		10	V
Output Voltage	V_{OUT}	MAX850–MAX852, V_{FB} = 0V, R_L = ∞ or 820Ω, Figure 2a	-4.3	-4.1	-3.9	V
		MAX853, V_{CTRL} = 4.1V, R_L = ∞ or 820Ω, Figure 2c	-4.2		-4.0	
Output Voltage Range			-0.5 to - (V_{IN} - 1)			V
Set Voltage	V_{FBset}	MAX850–MAX852, no load, Figure 2b	-1.32	-1.28	-1.24	V
Supply Current	I_Q			2.0	3.0	mA
Shutdown Supply Current	I_{SHUT}	MAX850/MAX853, V_{IN} = 10V, $\overline{SHDN}$ = 0V		0.002	1	µA
		MAX851, SHDN = 2V		2	5	
		MAX852, OSC low			1	
V_{OUT} Load Regulation		MAX850–MAX852, V_{FB} = 0V, R_L = ∞ or 820Ω, Figure 2a		4	8	mV/mA
		MAX853, V_{CTRL} = 4.1V, R_L = ∞ or 820Ω, Figure 2c		3	8	
V_{OUT} Ripple		MAX850–MAX852		2		mVp-p
		MAX853		1		
Oscillator Frequency (Note 3)	f_{OSC}	MAX850/MAX851/MAX853, T_A = +25°C	80	100	120	kHz
Input High Voltage	V_{IH}	Pin 4	2.0			V
Input Low Voltage	V_{IL}	Pin 4			0.5	V
Input Current	I_{IN}	Pin 4			±1	µA
Input Capacitance	C_{IN}	Pin 4		10		pF

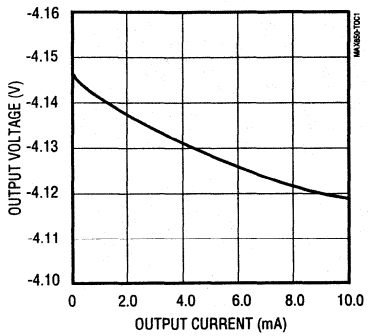
Note 2: The supply voltage can drop to 4.5V, but the output may no longer sink 5mA at -4.1V.
Note 3: The MAX852 will operate with a 50kHz to 250kHz square wave of 40% to 60% duty cycle. For best performance, use an 80kHz to 120kHz square wave with 50% duty cycle.

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

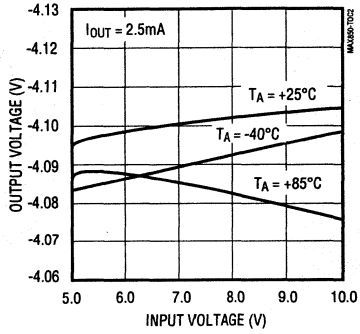
Typical Operating Characteristics

(Circuit of Figure 2a, V_{IN} = 6V, T_A = +25°C, unless otherwise noted.)

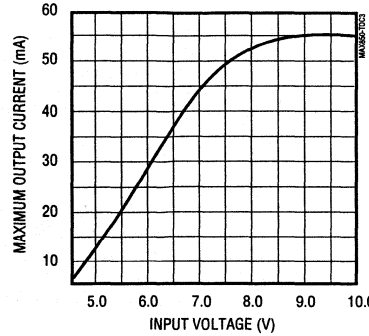
OUTPUT VOLTAGE vs. OUTPUT CURRENT



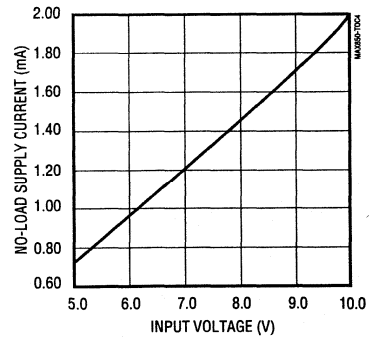
OUTPUT VOLTAGE vs. INPUT VOLTAGE OVER TEMPERATURE



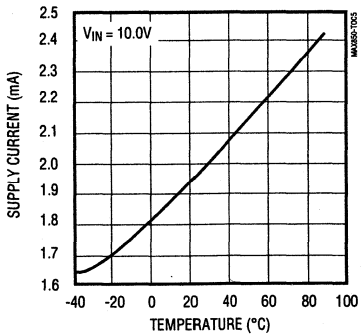
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



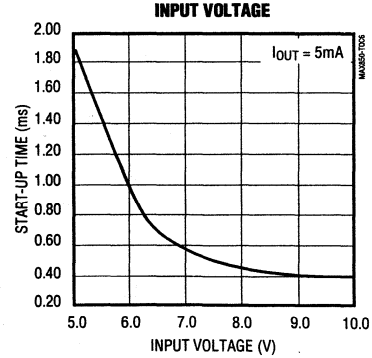
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



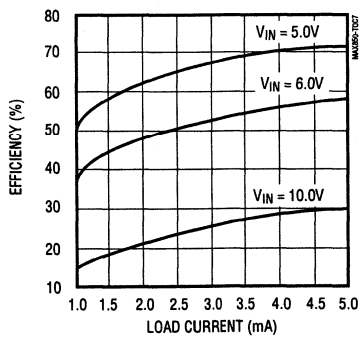
SUPPLY CURRENT vs. TEMPERATURE



START-UP TIME vs. INPUT VOLTAGE



EFFICIENCY vs. LOAD CURRENT



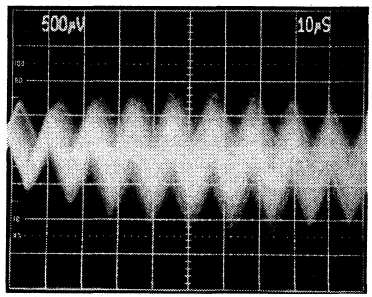
4

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, V_{IN} = 6V, T_A = +25°C, unless otherwise noted.)

MAX850–MAX852
OUTPUT NOISE AND RIPPLE

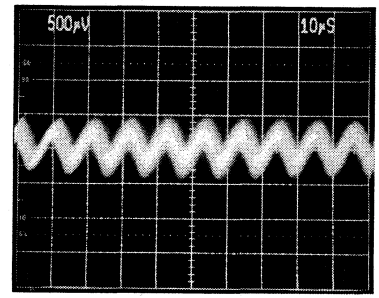


V_{OUT}
500µV/div

10µs/div

V_{IN} = 6.0V, V_{OUT} = -4.1V, I_{OUT} = 5mA, AC COUPLED

MAX853
OUTPUT NOISE AND RIPPLE

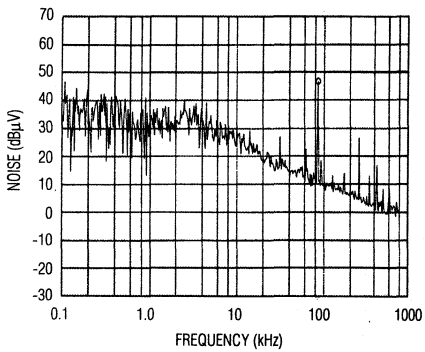


V_{OUT}
500µV/div

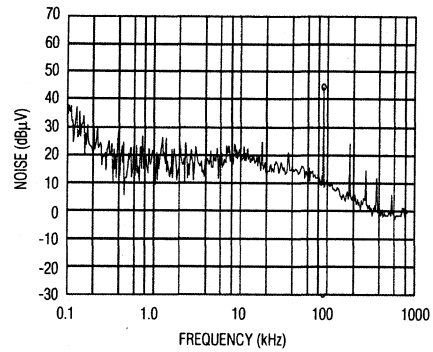
10µs/div

V_{IN} = 6.0V, V_{OUT} = -4.1V, I_{OUT} = 5mA, AC COUPLED

MAX850–MAX852
NOISE SPECTRUM



MAX853
NOISE SPECTRUM



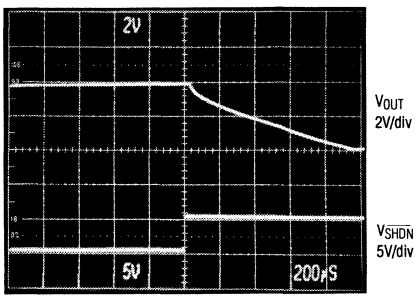
NOTE: $dB\mu V = 20 \log \frac{V_{OUT}}{1\mu V}$

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

Typical Operating Characteristics (continued)

(Circuit of Figure 2a, V_{IN} = 6V, T_A = +25°C, unless otherwise noted.)

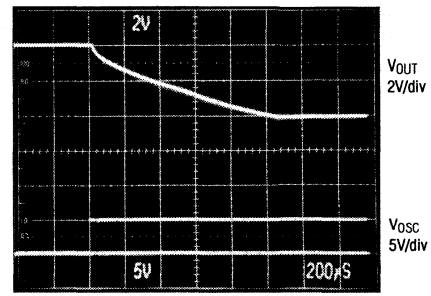
MAX850/MAX851/MAX853
START-UP FROM SHUTDOWN



200µs/div

CIRCUIT OF FIGURE 2a, V_{IN} = 6.0V, V_{OUT} = -4.1V, I_{OUT} = 5mA

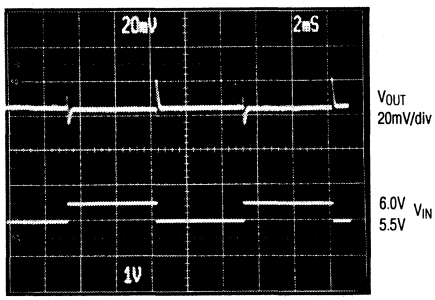
MAX852
START-UP FROM SHUTDOWN



200µs/div

CIRCUIT OF FIGURE 2a, V_{IN} = 6.0V, V_{OUT} = -4.1V, I_{OUT} = 5mA
SHUTDOWN OCCURS WHEN 100kHz EXTERNAL CLOCK IS GATED OFF

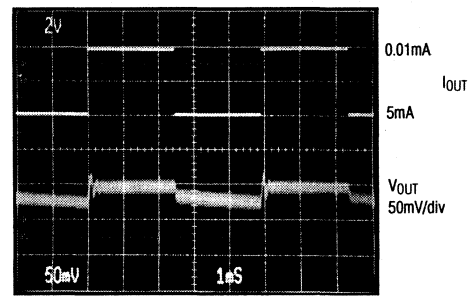
LINE-TRANSIENT RESPONSE



2ms/div

V_{OUT} = -4.08V, I_{OUT} = 5mA, AC COUPLED

LOAD-TRANSIENT RESPONSE



1ms/div

V_{OUT} = -4.0V, AC COUPLED

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

Pin Description

PIN				NAME	FUNCTION
MAX850	MAX851	MAX852	MAX853		
1	1	1	1	C1+	Positive terminal for C1
2	2	2	2	C1-	Negative terminal for C1
3	3	3	3	NEGOUT	Negative Output Voltage (unregulated), $V_{NEGOUT} = -V_{IN} + 0.2V$
4	–	–	4	$\overline{SHDN}$	Active-low TTL logic level Shutdown Input
–	4	–	–	SHDN	Active-high TTL logic level Shutdown Input
–	–	4	–	OSC	External Clock Input
5	5	5	–	FB	Dual-Mode Feedback Input. When FB is grounded, the output is preset to -4.1V. To select other output voltages, connect FB to an external resistor divider. See Figure 2b.
–	–	–	5	CONT	Control Voltage Input. To set V_{OUT}, connect a resistor divider between OUT and a positive control voltage between 0V and 10V. See Figure 2c.
6	6	6	6	OUT	Output Voltage
7	7	7	7	GND	Ground
8	8	8	8	IN	Positive Power-Supply Input (4.5V to 10V)

Detailed Description

The MAX850–MAX853 are low-noise, inverting, regulated charge-pump power supplies designed for biasing GaAs FET devices, such as power-amplifier modules in cellular handsets.

The applied input voltage (V_{IN}) is first inverted to a negative voltage at NEGOUT by a capacitive charge pump. This voltage is then regulated by an internal linear regulator, and appears at OUT (Figure 1). The minimum (most negative) output voltage (V_{OUT}) achievable is the inverted positive voltage, plus the 1.0V required by the post-regulator. The ripple noise induced by the charge-pump inverter is reduced by the linear regulator to 2mVp-p at V_{OUT} for the MAX850–MAX852. In addition, the excellent AC rejection of the linear regulator attenuates noise on the incoming supply. Up to 5mA is available at OUT.

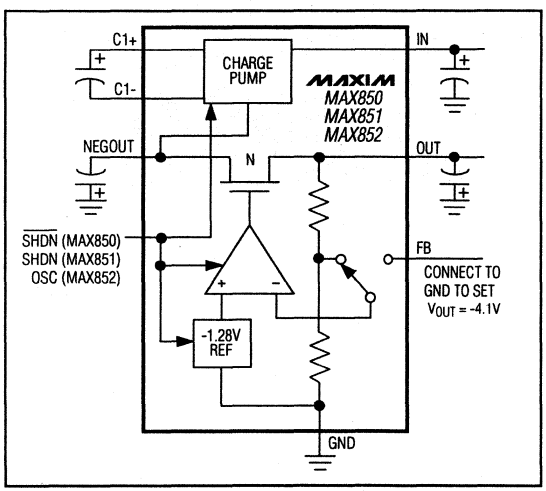


Figure 1a. MAX850–MAX852 Block Diagram

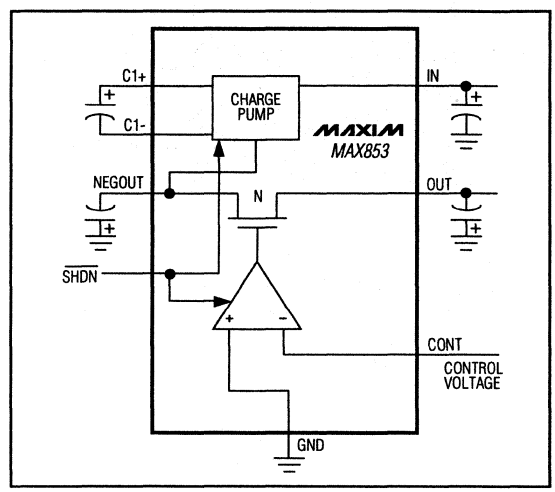


Figure 1b. MAX853 Block Diagram

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

Applications Information

Setting the Output Voltage

For the MAX850–MAX852, select either a fixed or an adjustable output voltage. Connect FB directly to GND to select the fixed -4.1V output (Figure 2a). To select an alternate output voltage, connect FB to the midpoint of a resistor voltage divider from OUT to GND (Figure 2b). V_{IN} must be 1.0V above the absolute value of V_{OUT} to allow proper regulation. The output voltage is calculated from the formula below. Choose R2 to be between 100kΩ to 400kΩ.

$$V_{OUT} = (-1.28)\left(1 + \frac{R2}{R1}\right)$$

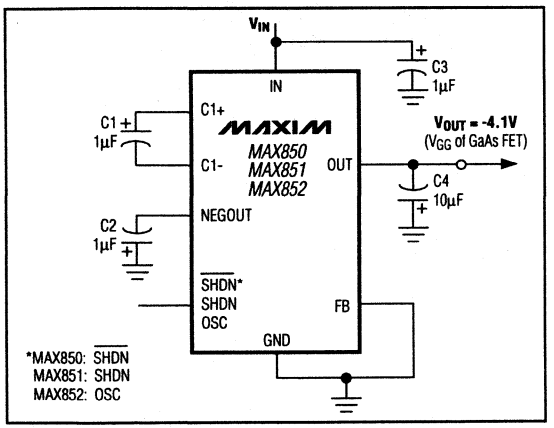


Figure 2a. MAX850/MAX851/MAX852 Standard Application Circuit

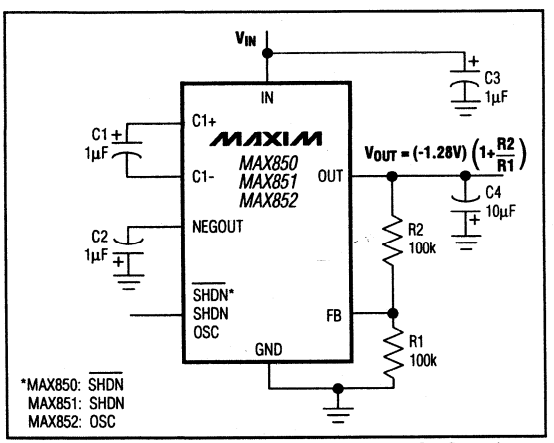


Figure 2b. MAX850/MAX851/MAX852 Adjustable Configuration

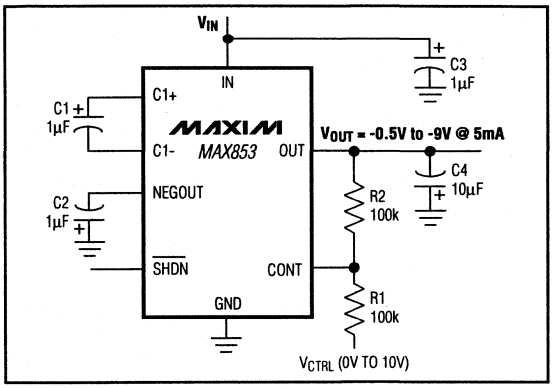


Figure 2c. MAX853 Standard Application Circuit

For the MAX853, set the output voltage, V_{OUT}, by connecting a resistor voltage divider between OUT and a positive control voltage, V_{CTRL} (Figure 2c).

$$V_{OUT} = -V_{CTRL}\left(\frac{R2}{R1}\right)$$

Shutdown

The MAX850–MAX853 feature a shutdown mode that reduces the supply current to 1µA max over temperature (5µA max for the MAX851). The MAX850 and MAX853 have an active-low TTL logic level $\overline{SHDN}$ input, whereas the MAX851 has an active-high SHDN input. To shut down the MAX852, set the OSC input to a logic-low level. The device is powered up by the resumption of the clock signal.

Capacitors

Use capacitors with low effective series resistance (ESR) to maintain a low dropout voltage (V_{IN} - $|V_{OUT}|$). The overall dropout voltage is a function of the charge pump's output resistance and the voltage drop across the linear regulator (N-channel pass transistor). At the 100kHz switching frequency, the charge-pump output resistance is a function of C1 and C2's ESR. Therefore, minimizing the ESR of the charg-pump capacitors minimizes the dropout voltage.

1µF, 0.8Ω ESR capacitors are recommended for C1, C2, and C3. C4 should be 10µF, 0.2Ω ESR. All capacitors should be either surface-mount chip tantalum or chip ceramic types. External capacitor values may be adjusted to optimize size and cost.

Switching-Frequency Control

Use the MAX852 to minimize system interference caused by conflicting clock frequencies. An external oscillator can set the charge-pump frequency and reduce clock frequency sensitivity and interference. The clock must be

Low-Noise, Regulated, Negative Charge-Pump Power Supplies for GaAs FET Bias

a square wave between 40% and 60% duty cycle. The maximum clock frequency is 250kHz and the minimum frequency is 50kHz.

Layout and Grounding

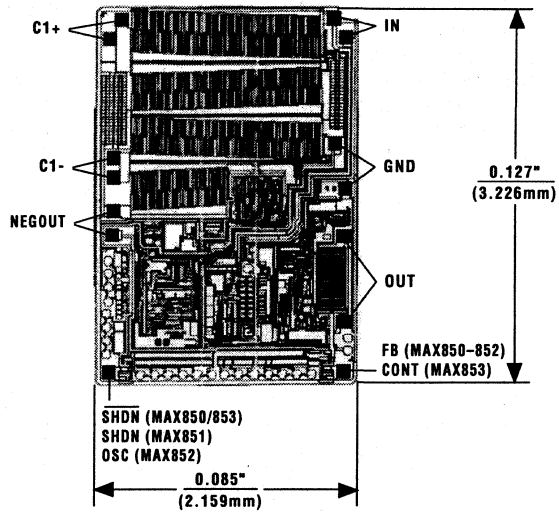
Good layout is important, primarily for good noise performance.

1) Mount all components as close together as possible.
2) Keep traces short to minimize parasitic inductance and capacitance. This includes connections to FB.
3) Use a ground plane.

Noise and Ripple Measurement

Accurately measuring the output noise and ripple is a challenge. Brief differences in ground potential between the MAX850–MAX853 circuit and the oscilloscope (which result from the charge pump's switching action) cause ground currents in the probe's wires, inducing sharp voltage spikes. For best results, measure directly across the output capacitor (C4). Do not use the ground lead of the oscilloscope probe; instead, remove the probe's tip cover and touch the ground ring on the probe directly to C4's ground terminal. You can also use a Tektronix chassis mount test jack (part no. 131-0258) to connect your scope probe directly. This direct connection gives the most accurate noise and ripple measurement.

Chip Topography



TRANSISTOR COUNT: 164
SUBSTRATE CONNECTED TO IN

19-0211; Rev 1; 8/94

EVALUATION KIT AVAILABLE

3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

General Description

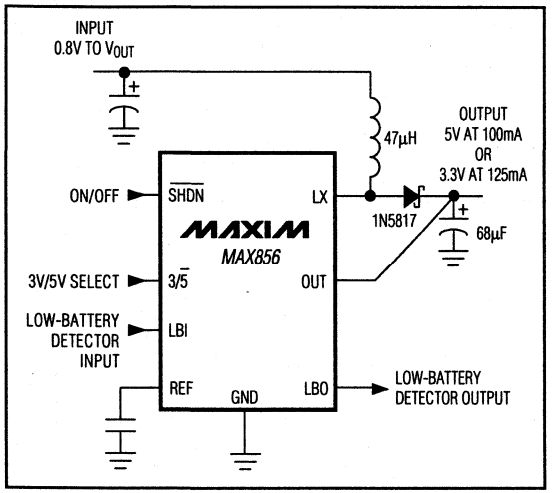
The MAX856–MAX859 are high-efficiency, CMOS, step-up, DC-DC switching regulators for small, low input voltage or battery-powered systems. The MAX856/MAX858 accept a positive input voltage between 0.8V and V_{OUT} and convert it to a higher, pin-selectable output voltage of 3.3V or 5V. The MAX857/MAX859 adjustable versions accept 0.8V to 6.0V input voltages and generate higher adjustable output voltages in the 2.7V to 6.0V range. Typical efficiencies are greater than 85%. Typical quiescent supply current is 25µA (1µA in shutdown).

The MAX856–MAX859 combine ultra-low quiescent supply current and high efficiency to give maximum battery life. An internal MOSFET power transistor permits high switching frequencies. This benefit, combined with internally set peak inductor current limits, permits the use of small, low-cost inductors. The MAX856/MAX857 have a 500mA peak inductor current limit. The MAX858/MAX859 have a 125mA peak inductor current limit.

Applications

3.3V to 5V Step-Up Conversion
Palmtop Computers
Portable Data-Collection Equipment
Personal Data Communicators/Computers
Medical Instrumentation
2-Cell & 3-Cell Battery-Operated Equipment
Glucose Meters

Typical Operating Circuit



Features

- ♦ **0.8V to 6.0V Input Supply Voltage**
- ♦ **0.8V Typ Start-Up Supply Voltage**
- ♦ **85% Efficiency at 100mA**
- ♦ **25µA Quiescent Current**
- ♦ **1µA Shutdown Mode**
- ♦ **125mA and 500mA Switch-Current Limits Permit Use of Low-Cost Inductors**
- ♦ **Up to 500kHz Switching Frequency**
- ♦ **±1.5% Reference Tolerance Over Temperature**
- ♦ **Low-Battery Detector (LBI/LBO)**
- ♦ **8-Pin SO and µMAX Packages**

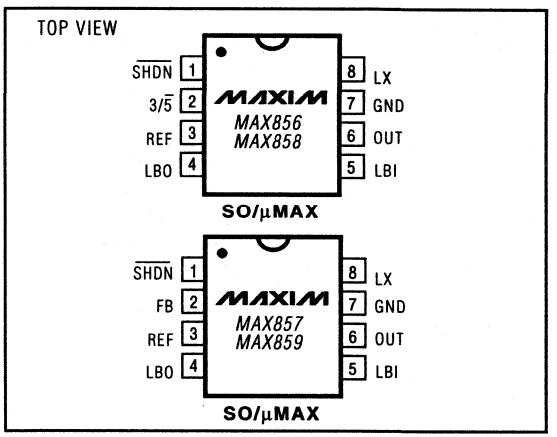
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX856CSA	0°C to +70°C	8 SO
MAX856CUA	0°C to +70°C	8 µMAX
MAX856C/D	0°C to +70°C	Dice*
MAX856ESA	-40°C to +85°C	8 SO
MAX856MJA	-55°C to +125°C	8 CERDIP†
MAX857CSA	0°C to +70°C	8 SO
MAX857CUA	0°C to +70°C	8 µMAX
MAX857C/D	0°C to +70°C	Dice*
MAX857ESA	-40°C to +85°C	8 SO
MAX857MJA	-55°C to +125°C	8 CERDIP†

Ordering Information continued at end of data sheet.

* *Dice are tested at TA = +25°C only.*
† *Contact factory for availability.*

Pin Configuration



3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (OUT to GND) .....-0.3V, +7V
Switch Voltage (LX to GND) .....-0.3V, +7V
$\overline{SHDN}$, LBO to GND .....-0.3V, +7V
LBI, REF, 3/$\overline{5}$, FB to GND .....-0.3V, (V_{OUT} + 0.3V)
Reference Current (I_{REF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.1mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Reverse Battery Current ($T_A \le$ +45°C, Note 1) 750mA
Operating Temperature Ranges
MAX85_C_ _ .....0°C to +70°C
MAX85_E_ _ .....-40°C to +85°C
MAX85_MJA .....-55°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Reverse battery current is measured from the *Typical Operating Circuit's* battery input terminal to GND when the battery is connected backwards. A reverse current of 750mA will not exceed the SO or CERDIP package dissipation limits but, if left for an extended time (more than ten minutes), may degrade performance.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuits of Figure 2, V_{IN} = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	2V ≤ V_{IN} ≤ 3V	MAX856, 3/$\overline{5}$ = 0V, 0mA ≤ I_{LOAD} ≤ 100mA	4.80	5.0	5.20	V
		MAX856, 3/$\overline{5}$ = 3V, 0mA ≤ I_{LOAD} ≤ 150mA	3.17	3.3	3.43	
		MAX857, V_{OUT} = 5V, 0mA ≤ I_{LOAD} ≤100mA	4.80	5.0	5.20	
		MAX858, 3/$\overline{5}$ = 0V, 0mA ≤ I_{LOAD} ≤ 25mA	4.80	5.0	5.20	
		MAX858, 3/$\overline{5}$ = 3V, 0mA ≤ I_{LOAD} ≤ 35mA	3.17	3.3	3.43	
		MAX859, V_{OUT} = 5V, 0mA ≤ I_{LOAD} ≤ 25mA	4.80	5.0	5.20	
Minimum Start-Up Supply Voltage	I_{LOAD} = 0mA			0.8	1.8	V
Minimum Operating Voltage				0.8		V
Quiescent Supply Current in 3.3V Mode (Note 2)	I_{LOAD} = 0mA, 3/$\overline{5}$ = 3V, LBI = 1.5V, V_{OUT} = 3.47V, (FB = 1.5V, MAX857/MAX859 only)			25	60	µA
No Load Battery Current	Output set for 3.3V, measured at V_{IN} in Figure 2, R3 omitted.			60		µA
Shutdown Quiescent Current (Note 2)	$\overline{SHDN}$ = 0V, 3/$\overline{5}$ = 3V, LBI = 1.5V, V_{OUT} = 3.47V, (FB = 1.5V, MAX857/MAX859 only)	MAX85_C			1	µA
		MAX85_E/M		1	5	
Peak Inductor Current Limit	MAX856/MAX857			500		mA
	MAX858/MAX859			125		
Reference Voltage	No REF load		1.23	1.25	1.27	V
Reference-Voltage Regulation	3/$\overline{5}$ = 3V, -20µA ≤ REF load ≤ 250µA, C_{REF} = 0.22µF			0.8	2.0	%
LBI Input Threshold	With falling edge		1.22	1.25	1.28	V
LBI Input Hysteresis				25		mV
LBO Output Voltage Low	I_{SINK} = 2mA				0.4	V
LBO Output Leakage Current	LBO = 5V				1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figure 2, V_{IN} = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

$\overline{SHDN}$, 3/$\overline{5}$ Input Voltage Low				0.4	V
$\overline{SHDN}$, 3/$\overline{5}$ Input Voltage High		1.6			V
$\overline{SHDN}$, 3/$\overline{5}$, FB, LBI Input Current	LBI = 1.5V, FB = 1.5V, $\overline{SHDN}$ = 0V or 3V, 3/$\overline{5}$ = 0V or 3V			±100	nA
FB Voltage	MAX857/MAX859	1.22	1.25	1.28	V
Output Voltage Range	MAX857/MAX859, I_{LOAD} = 0mA (Note 3)	2.7		6.0	V

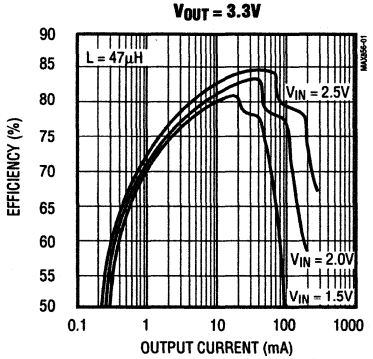
Note 2: Supply current from the 3.3V output is measured with an ammeter between the 3.3V output and OUT pin. This current correlates directly with actual battery supply current, but is reduced in value according to the step-up ratio and efficiency. V_{OUT} = 3.47V to keep the internal switch open when measuring the current into the device.

Note 3: Minimum value is production tested. Maximum value is guaranteed by design and is not production tested.

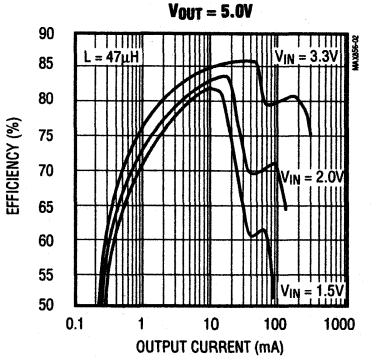
Typical Operating Characteristics

(Circuits of Figure 2, T_A = +25°C, unless otherwise noted.)

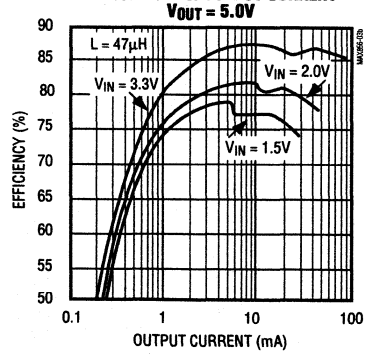
MAX856/MAX857 EFFICIENCY vs. OUTPUT CURRENT V_{OUT} = 3.3V



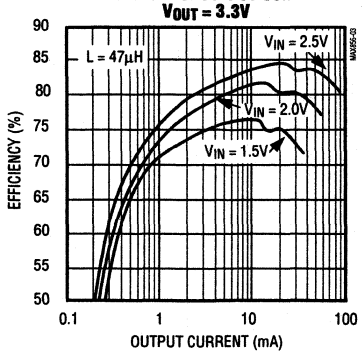
MAX856/MAX857 EFFICIENCY vs. OUTPUT CURRENT V_{OUT} = 5.0V



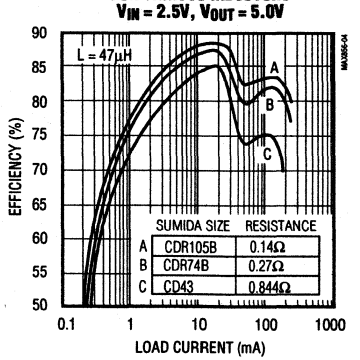
MAX858/MAX859 EFFICIENCY vs. OUTPUT CURRENT V_{OUT} = 5.0V



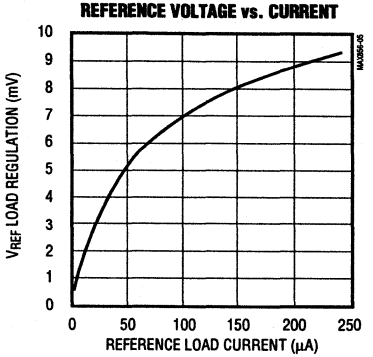
MAX858/MAX859 EFFICIENCY vs. OUTPUT CURRENT V_{OUT} = 3.3V



MAX856 EFFICIENCY vs. LOAD CURRENT FOR VARIOUS INDUCTORS V_{IN} = 2.5V, V_{OUT} = 5.0V



REFERENCE VOLTAGE vs. CURRENT

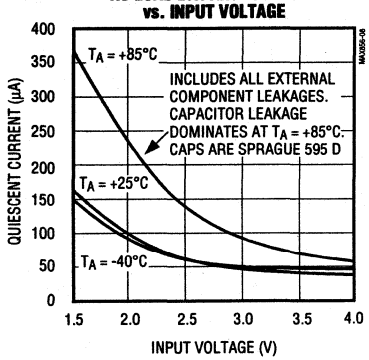


3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

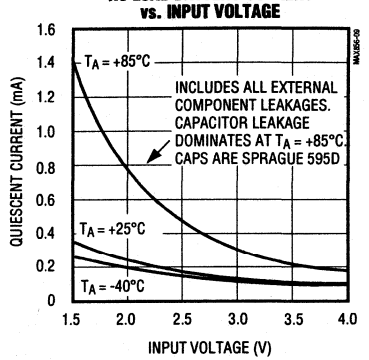
Typical Operating Characteristics (continued)

(Circuits of Figure 2, T_A = +25°C, unless otherwise noted.)

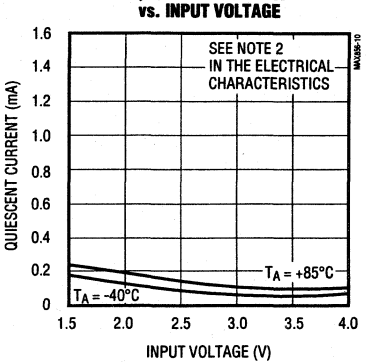
MAX856/MAX857
NO LOAD BATTERY CURRENT
vs. INPUT VOLTAGE



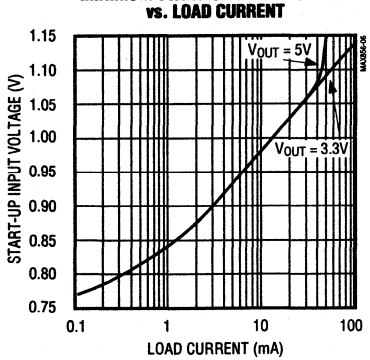
MAX858/MAX859
NO LOAD BATTERY CURRENT
vs. INPUT VOLTAGE



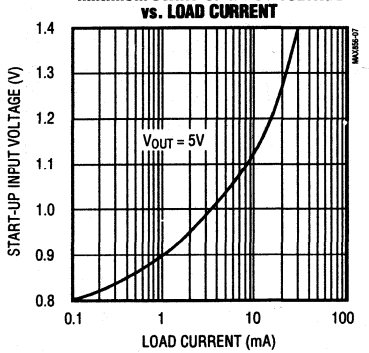
QUIESCENT CURRENT
vs. INPUT VOLTAGE



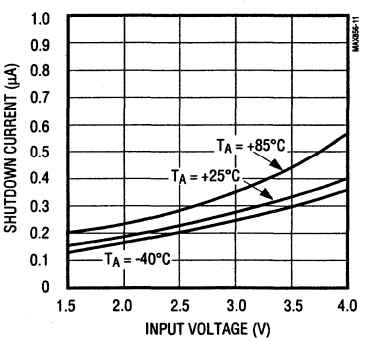
MAX856/MAX857
MINIMUM START-UP INPUT VOLTAGE
vs. LOAD CURRENT



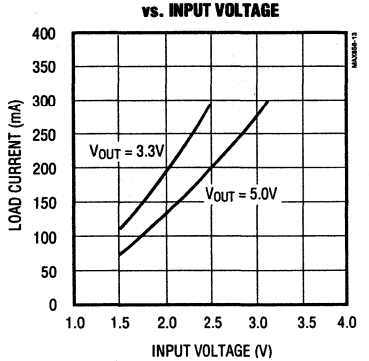
MAX858/MAX859
MINIMUM START-UP INPUT VOLTAGE
vs. LOAD CURRENT



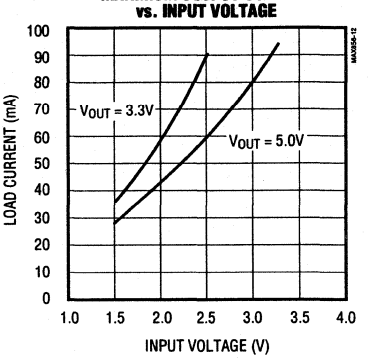
SHUTDOWN CURRENT
vs. INPUT VOLTAGE



MAX856/MAX857
MAXIMUM OUTPUT CURRENT
vs. INPUT VOLTAGE



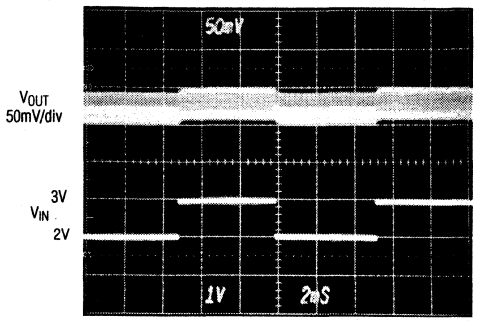
MAX858/MAX859
MAXIMUM OUTPUT CURRENT
vs. INPUT VOLTAGE



Typical Operating Characteristics (continued)

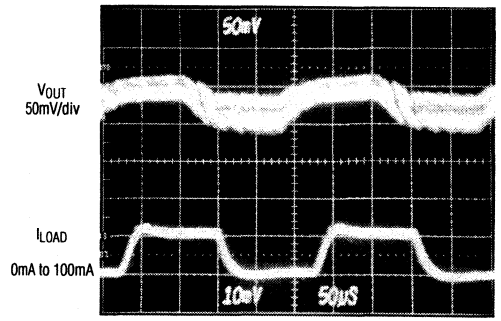
(Circuits of Figure 2, T_A = +25°C, unless otherwise noted.)

MAX856/MAX857 LINE-TRANSIENT RESPONSE (5V MODE)



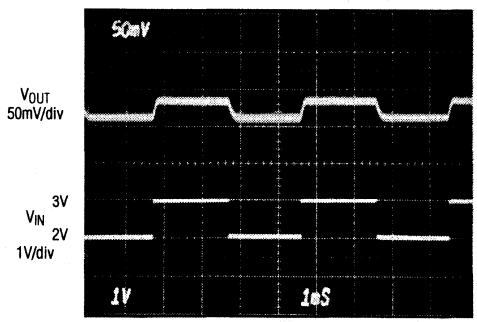
2ms/div

MAX856/MAX857 LOAD-TRANSIENT RESPONSE (5V MODE)



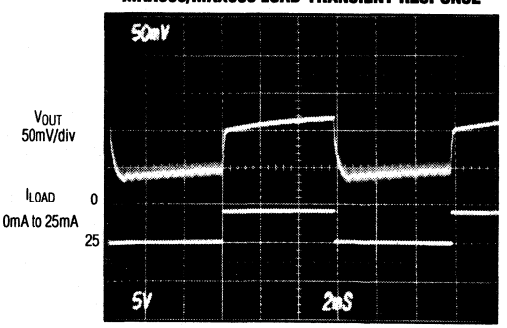
V_{IN} = 2.5V 50µs/div

MAX859 LINE-TRANSIENT RESPONSE



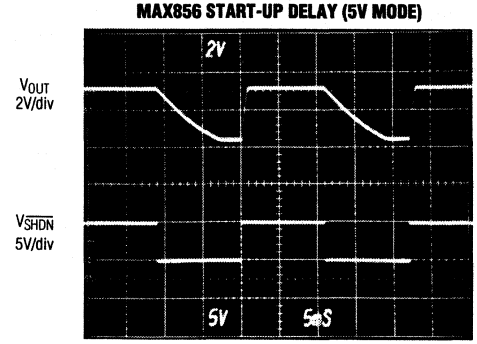
1ms/div

MAX858/MAX859 LOAD-TRANSIENT RESPONSE



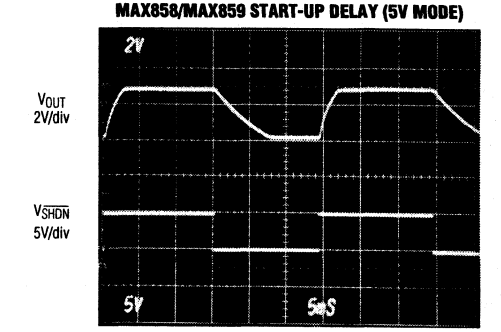
V_{IN} = 2.5V 2ms/div

MAX856 START-UP DELAY (5V MODE)



V_{IN} = 2.5V, I_{LOAD} = 100mA 5ms/div

MAX858/MAX859 START-UP DELAY (5V MODE)



V_{IN} = 2.5V, I_{LOAD} = 25mA 5ms/div

3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

Pin Description

PIN		NAME	FUNCTION
MAX856 MAX858	MAX857 MAX859		
1	1	$\overline{SHDN}$	Shutdown Input. When low, the entire circuit is off and $V_{OUT} = V_{IN} - V_D$, where V_D is the forward voltage drop of the external Schottky rectifier.
2	—	$3/\overline{5}$	Selects the output voltage; connect to GND for 5V output, and to OUT for 3.3V output.
—	2	FB	Feedback Input for adjustable-output operation. Connect to an external resistor voltage divider between OUT and GND.
3	3	REF	1.25V Reference Voltage Output. Bypass with 0.22µF to GND (0.1µF if there is no external reference load). Maximum load capability is 250µA source, 20µA sink.
4	4	LBO	Low-Battery Output. An open-drain N-channel MOSFET sinks current when the voltage at LBI drops below 1.25V.
5	5	LBI	Low-Battery Input. When the voltage on LBI drops below 1.25V, LBO sinks current. If not used, connect to V_{IN}.
6	6	OUT	Connect OUT to the regulator output. OUT provides bootstrap power to the IC.
7	7	GND	Power Ground. Must be low impedance; solder directly to ground plane.
8	8	LX	N-Channel Power-MOSFET Drain

Detailed Description

Operating Principle

The MAX856–MAX859 combine a switch-mode regulator, N-channel power MOSFET, precision voltage reference, and power-fail detector in a single monolithic device. The MOSFET is a "sense-FET" type for best efficiency, and has a very low gate threshold voltage to ensure start-up with low battery voltages (0.8V typ).

PFM Control Scheme

A unique minimum-off-time, current-limited pulse-frequency modulation (PFM) control scheme is a key feature of the MAX856 series (Figure 1). This scheme combines the high output power and efficiency of a pulse-width modulation (PWM) device with the ultra-low quiescent current of a traditional PFM pulse-skipper. There is no oscillator; at heavy loads, switching is accomplished through a constant-peak-current limit in the switch, which allows the inductor current to vary between this peak limit and some lesser value. At light loads, switching frequency is governed by a pair of one-shots, which set a minimum off-time (1µs) and a maximum on-time (4µs). The switching frequency depends upon the load and the input voltage, and can range up to 500kHz.

The peak switch current of the internal MOSFET power switch is fixed at 500mA ±100mA (MAX856/MAX857) or 125mA ±25mA (MAX858/MAX859). The switch's on-resistance is typically 1Ω (MAX856/MAX857) or 4Ω (MAX858/MAX859), resulting in a switch voltage drop (V_{SW}) of about 500mV under high output loads. The value of V_{SW} will decrease with light current loads.

Conventional PWM converters generate constant-frequency switching noise, whereas the unique architecture of the MAX856–MAX859 produces variable-frequency switching noise. However, unlike conventional pulse-skippers (where noise amplitude varies with input voltage), noise in the MAX856 series does not exceed the switch current limit times the filter-capacitor equivalent series resistance (ESR).

Voltage Reference

The precision voltage reference is suitable for driving external loads, such as an analog-to-digital converter. The voltage-reference output changes less than ±2% when sourcing up to 250µA and sinking up to 20µA. If the reference drives an external load, bypass it with 0.22µF to GND. If the reference is unloaded, bypass it with at least 0.1µF.

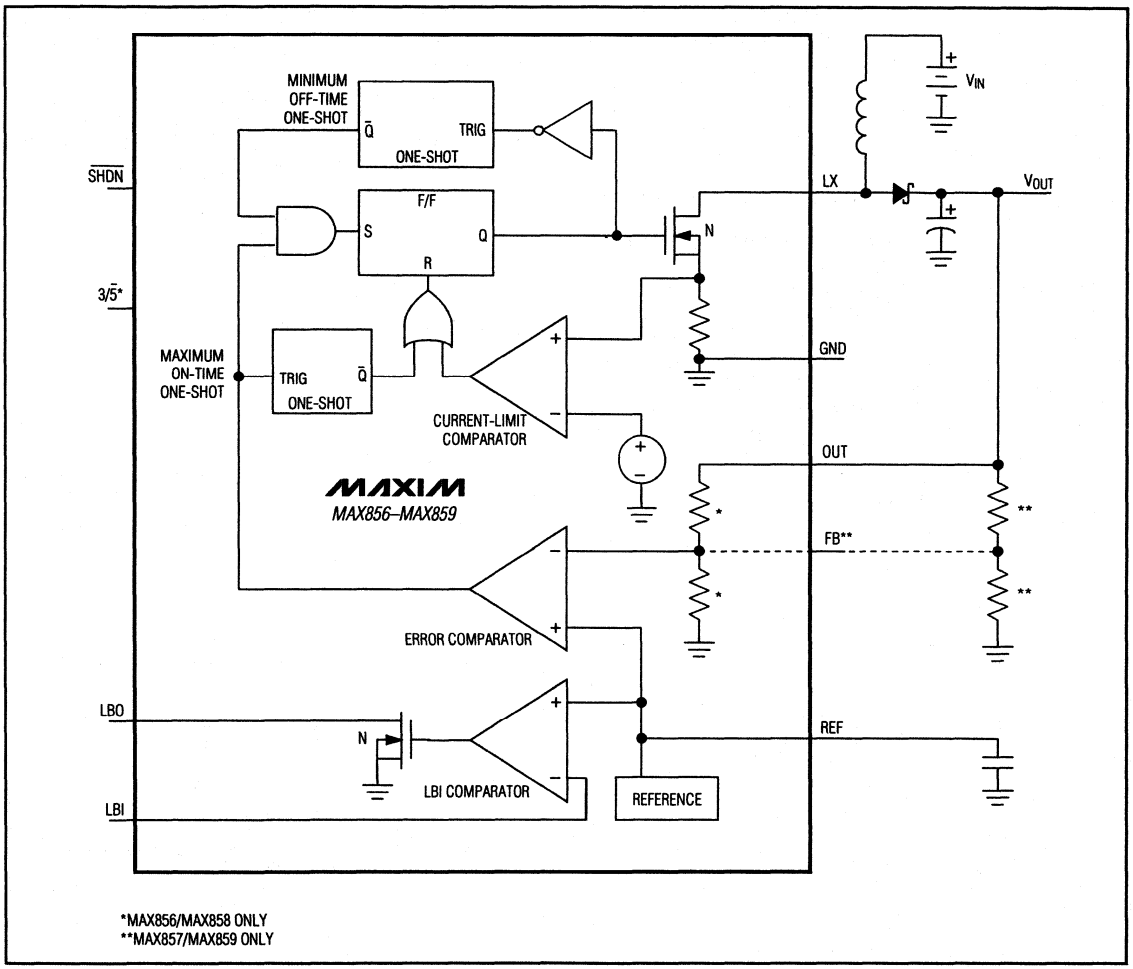


Figure 1. Block Diagram

3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

Logic Inputs and Outputs

The 3/$\overline{5}$ input is internally diode clamped to GND and OUT, and should not be connected to signals outside this range. The $\overline{SHDN}$ input and LBO output (open-drain) are not clamped to V+ and can be pulled as high as 7V regardless of the voltage at OUT. **Do not leave control inputs (3/$\overline{5}$, LBI, or $\overline{SHDN}$) floating.**

Design Procedure

Output Voltage Selection

For the MAX856/MAX858,you can select a 3.3V or 5V output voltage under logic control, or by tying 3/$\overline{5}$ to GND or OUT. Efficiency is typically better than 80% over a 2mA to 100mA (MAX856/MAX857) load range. The device is internally bootstrapped, with power derived from the output voltage (via OUT). When the output is in 5V mode, the higher internal supply voltage results in lower switch-transistor on-resistance, slightly greater output power, and higher efficiency. Bootstrapping allows the battery voltage to sag to 0.8V once the system is started. Therefore, the battery voltage ranges from (V_{OUT} + V_D) to 0.8V (where V_D is the forward drop of the Schottky rectifier). If the battery voltage exceeds the programmed output voltage, the output will follow the battery voltage. This is acceptable in many systems; however, the input or output voltage must not be forced above 7V.

The MAX857/MAX859's output voltage is set by two resistors, R1 and R2 (Figure 2b), which form a voltage divider between the output and FB. Use the following equation to determine the output voltage:

$$V_{OUT} = V_{REF} \left(\frac{R1 + R2}{R2} \right)$$

where V_{REF} = 1.25V.

To simplify resistor selection:

$$R1 = R2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

Since the input bias current at FB has a maximum value of 100nA, large values (10kΩ to 300kΩ) can be used for R1 and R2 with no significant accuracy loss. For 1% error, the current through R1 should be at least 100 times FB's bias current.

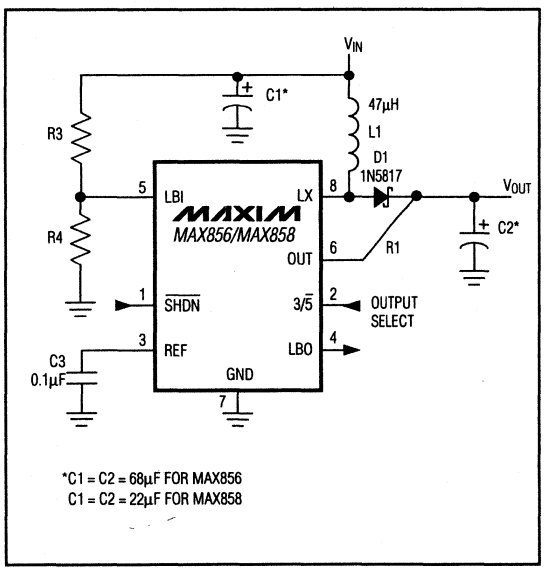


Figure 2a. Standard Application Circuit—Preset Output Voltage

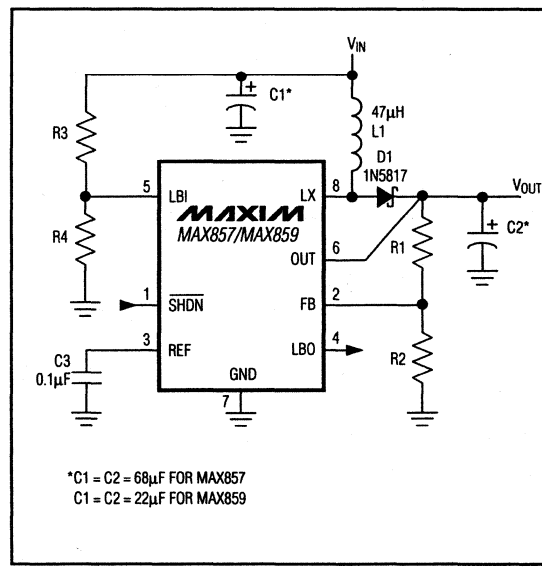


Figure 2b. Standard Application Circuit—Adjustable Output Voltage

3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

Low-Battery Detection

The MAX856 series contains an on-chip comparator for low-battery detection. If the voltage at LBI falls below the regulator's internal reference voltage (1.25V), LBO (an open-drain output) sinks current to GND. The low-battery monitor's threshold is set by two resistors, R3 and R4 (Figure 2). Set the threshold voltage using the following equation:

$$R3 = R4 \left(\frac{V_{LBI}}{V_{REF}} - 1 \right)$$

where V_{LBI} is the desired threshold of the low-battery detector and V_{REF} is the internal 1.25V reference.

Since the LBI current is less than 100nA, large resistor values (typically 10kΩ to 300kΩ) can be used for R3 and R4 to minimize loading of the input supply.

When the voltage at LBI is below the internal threshold, LBO sinks current to GND. Connect a pull-up resistor of 10kΩ or more from LBO to OUT when driving CMOS circuits. When LBI is above the threshold, the LBO output is off. If the low-battery comparator is not used, connect LBI to V_{IN} and leave LBO open.

Inductor Selection

An inductor value of 47µH performs well in most MAX856–MAX859 applications. However, the inductance value is not critical, and the MAX856–MAX859 will work with inductors in the 10µH to 100µH range. Smaller inductance values typically offer a smaller physical size for a given series resistance, allowing the smallest overall circuit dimensions. However, due to higher peak inductor currents, the output voltage ripple (I_{PEAK} x output filter capacitor ESR) also tends to be higher. Circuits using larger inductance values exhibit higher output current capability and larger physical dimensions for a given series resistance.

The inductor's incremental saturation current rating should be greater than the peak switch-current limit, which is 500mA for the MAX856/MAX857, and 125mA for the MAX858/MAX859. However, it is generally acceptable to bias the inductor into saturation by as much as 20%, although this will slightly reduce efficiency.

The inductor's DC resistance significantly affects efficiency. See the Efficiency vs. Load Current for Various Inductors graph in the *Typical Operating Characteristics*. See Tables 1 and 2 for a list of suggested inductor suppliers.

Capacitor Selection

A 68µF, 10V, 0.85Ω, surface-mount tantalum (SMT) output filter capacitor typically provides 50mV output ripple when stepping up from 2V to 5V at 100mA (MAX856/ MAX857). Smaller capacitors (down to 10µF with higher ESRs) are acceptable for light loads or in applications that can tolerate higher output ripple. Values in the 10µF to 47µF range are recommended for the MAX858/MAX859.

The equivalent series resistance (ESR) of both bypass and filter capacitors affects efficiency and output ripple. The output voltage ripple is the product of the peak inductor current and the output capacitor's ESR. Use low-ESR capacitors for best performance, or connect two or more filter capacitors in parallel. Low-ESR, SMT tantalum capacitors are currently available from Sprague (595D series) and AVX (TPS series). Sanyo OS-CON organic-semiconductor through-hole capacitors also exhibit very low ESR, and are especially useful for operation at cold temperatures. See Table 1 for a list of suggested capacitor suppliers.

Rectifier Diode

For optimum performance, a switching Schottky diode (such as the 1N5817) is recommended. Refer to Table 1 for a list of component suppliers. For low output power applications, a PN-junction switching diode (such as the 1N4148) will also work well, although its greater forward voltage drop will reduce efficiency.

PC Layout and Grounding

The MAX856 series' high-frequency operation makes PC layout important for minimizing ground bounce and noise. Keep the IC's GND pin and the ground leads of C1 and C2 (Figure 1) less than 0.2in (5mm) apart. Also keep all connections to the FB and LX pins as short as possible. To maximize output power and efficiency and minimize output ripple voltage, use a ground plane and solder the IC's GND (pin 7) directly to the ground plane.

3.3V/5V or Adjustable-Output, Step-Up DC-DC Converters

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS	RECTIFIERS
Surface Mount	See Table 2	Matsuo 267 series Sprague 595D series AVX TPS series	Motorola MBR 0530 Nihon EC15QS02L
Miniature Through Hole	Sumida RCH654-220	Sanyo OS-CON series low-ESR organic semiconductor	
Low-Cost Through Hole	Renco RL 1284-22 CoilCraft PCH-27-223	Maxim MAXC001 150µF, low-ESR electrolytic Nichicon PL series low-ESR electrolytic United Chemi-Con LXF series	Motorola 1N5817

COMPANY	PHONE	FAX
AVX	USA: (207) 282-5111	(207) 283-1941
CoilCraft	USA: (708) 639-6400	(708) 639-1469
Coiltronics	USA: (407) 241-7876	(407) 241-9339
Matsuo	USA: (714) 969-2491	(714) 960-6492
Motorola	USA: (408) 749-0510 (800) 521-6274	
Murata-Erie	USA: (800) 831-9172	(404) 684-1541
Nichicon	USA: (708) 843-7500	(708) 843-2798
Nihon	USA: (805) 867-2555 Japan: 81-3-3494-7411	(805) 867-2556 81-3-3494-7414
Renco	USA: (516) 586-5566	(516) 586-5562
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (708) 956-0666 Japan: 81-3-3607-5111	(708) 956-0702 81-3-3607-5144
TDK	USA: (708) 803-6100 Japan: 03-3278-5111	(708) 803-6294 03-3278-5358
United Chemi-Con	USA: (714) 255-9500	(714) 255-9400

Table 2. Surface-Mount Inductor Information

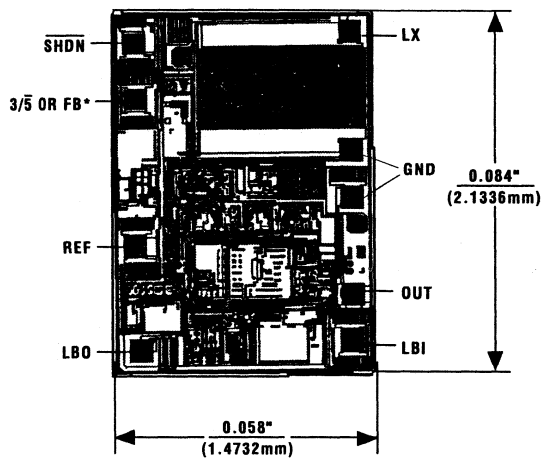
MANUFACTURER PART	INDUCTANCE (µH)	RESISTANCE (Ω)	RATED CURRENT (A)	HEIGHT (mm)
Sumida CDR105B-470	47	0.14	1.0	5.0
Sumida CDR74B-470	47	0.27	0.8	4.5
Sumida CD43-470	47	0.85	0.540	3.2
Sumida CD43-220	22	0.38	0.760	3.2
Murata-Erie LQH4N220	22	0.94	0.320	2.6
Murata-Erie LQH4N470	47	1.5	0.220	2.6
Murata-Erie LQH1N220	22	3.1	0.85	1.8
TDK NLC322522T-220K	22	1.15	0.210	2.2
TDK NLC322522T-470K	47	2.25	0.150	2.2
Coiltronics CTX20-1	20	0.175	1.15	4.2
Coilcraft DT1608-223	22	0.16	0.500	3.2

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX858CSA	0°C to +70°C	8 SO
MAX858CUA	0°C to +70°C	8 µMAX
MAX858C/D	0°C to +70°C	Dice*
MAX858ESA	-40°C to +85°C	8 SO
MAX858MJA	-55°C to +125°C	8 CERDIP†
MAX859CSA	0°C to +70°C	8 SO
MAX859CUA	0°C to +70°C	8 µMAX
MAX859C/D	0°C to +70°C	Dice*
MAX859ESA	-40°C to +85°C	8 SO
MAX859MJA	-55°C to +125°C	8 CERDIP†

** Dice are tested at TA = +25°C only.*
† Contact factory for availability.

Chip Topography



***3/5 FOR MAX856/MAX858; FB FOR MAX857/MAX859.**

TRANSISTOR COUNT: 357;
SUBSTRATE CONNECTED TO OUT.

19-0239; Rev 0; 7/94

MAXIM

50mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

General Description

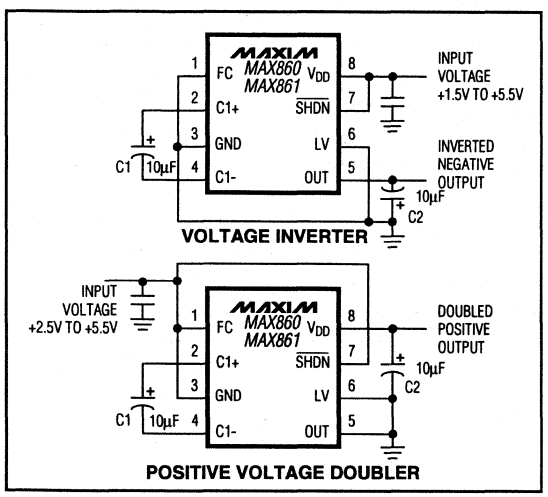
The MAX860/MAX861 charge-pump voltage converters invert input voltages ranging from 1.5V to 5.5V, or double input voltages ranging from 2.5V to 5.5V. Because of their high switching frequencies, these devices use only two small, low-cost capacitors. Their 50mA output makes switching regulators unnecessary, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of the load-current range, combined with a typical operating current of only 200µA (MAX860), provides ideal performance for both battery-powered and board-level voltage-conversion applications.

A frequency-control (FC) pin provides three switching-frequencies to optimize capacitor size and quiescent current and to prevent interference with sensitive circuitry. Each device has a unique set of three available frequencies. A shutdown ($\overline{SHDN}$) pin reduces current consumption to less than 1µA. The MAX860/MAX861 are suitable for use in applications where the ICL7660 and MAX660's switching frequencies are too low. The MAX860/MAX861 are available in 8-pin µMAX and SO packages.

Applications

Portable Computers
Medical Instruments
Interface Power Supplies
Hand-Held Instruments
Operational-Amplifier Power Supplies

Typical Operating Circuit



Features

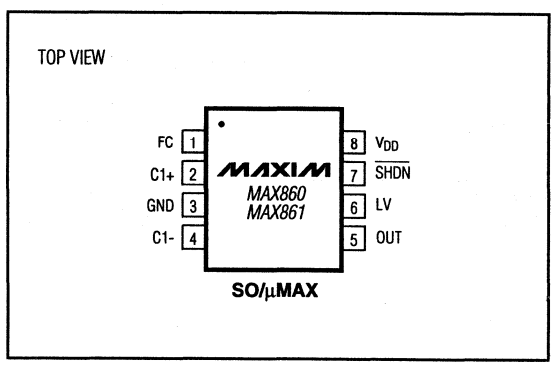
- ♦ **8-Pin, 1.11mm High µMAX Package**
- ♦ **Invert or Double the Input Supply Voltage**
- ♦ **Three Selectable Switching Frequencies**
- ♦ **High Frequency Reduces Capacitor Size**
- ♦ **87% Efficiency at 50mA**
- ♦ **200µA Quiescent Current (MAX860)**
- ♦ **1µA Shutdown Supply Current**
- ♦ **600mV Voltage Drop at 50mA Load**
- ♦ **12Ω Output Resistance**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX860CSA	0°C to +70°C	8 SO
MAX860CUA	0°C to +70°C	8 µMAX
MAX860C/D	0°C to +70°C	Dice*
MAX860ESA	-40°C to +85°C	8 SO
MAX860MJA	-55°C to +125°C	8 CERDIP†
MAX861CSA	0°C to +70°C	8 SO
MAX861CUA	0°C to +70°C	8 µMAX
MAX861C/D	0°C to +70°C	Dice*
MAX861ESA	-40°C to +85°C	8 SO
MAX861MJA	-55°C to +125°C	8 CERDIP†

** Dice are tested at T_A = +25°C, DC parameters only.*
† Contact factory for availability.

Pin Configuration



50mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to GND or GND to OUT) 6.0V
Input Voltage Range (LV, FC, $\overline{SHDN}$) .....(OUT - 0.3V) to (V_{DD} + 0.3V)
Continuous Output Current (OUT, V_{DD}) 60mA
Output Short-Circuit to GND (Note 1).....1sec
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C).....471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX86_C_A.....0°C to +70°C
MAX86_ESA.....-40°C to +85°C
MAX86_MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: OUT may be shorted to GND for 1sec without damage, but shorting OUT to V_{DD} may damage the device and should be avoided. Also, for temperatures above +85°C, OUT must not be shorted to GND or V_{DD}, even instantaneously, or device damage may result.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit (Inverter), V_{DD} = +5V, $\overline{SHDN}$ = V_{DD}, FC = LV = GND, C1 = C2 = 10µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	R_L = 1kΩ	Inverter, LV = open	3.0		5.5	V
			Inverter, LV = GND	1.5		5.5	
			Doubler, LV = OUT	2.5		5.5	
No-Load Supply Current	I_{DD}	MAX860C/E	FC = V_{DD} = 5V		0.2	0.3	mA
			FC = V_{DD} = 3V		0.07		
			FC = GND		0.6	1.0	
			FC = OUT		1.4	2.5	
		MAX860M	FC = V_{DD}			0.4	
			FC = GND			1.3	
			FC = OUT			3.3	
		MAX861C/E	FC = V_{DD}		0.3	0.4	
			FC = GND		1.1	2.0	
			FC = OUT		2.5	5.0	
		MAX861M	FC = V_{DD}			0.5	
			FC = GND			2.6	
			FC = OUT			6.5	
Output Current	I_{OUT}	V_{DD} = 5V, V_{OUT} more negative than -3.75V		50	100		mA
		V_{DD} = 3V, V_{OUT} more negative than -2.5V		10	30		
Output Resistance (Note 3)	R_{OUT}	I_L = 50mA			12	25	Ω
		I_L = 10mA, V_{DD} = 2V			20	35	

ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit (Inverter), V_{DD} = +5V, $\overline{SHDN}$ = V_{DD}, FC = LV = GND, C1 = C2 = 10µF (Note 2), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Frequency (Note 4)	f_S	MAX860	FC = V_{DD}	3	6		kHz
			FC = GND	30	50		
			FC = OUT	80	130		
		MAX861	FC = V_{DD}	8	13		
			FC = GND	60	100		
			FC = OUT	160	250		
FC Current (from V_{DD})	I_{FC}	FC < 4V			-2	-4	µA
Power Efficiency (Note 5)		MAX860, FC = V_{DD}	R_L = 2kΩ from V_{DD} to OUT	93	96		%
			R_L = 1kΩ from OUT to GND	90	93		
		MAX861, FC = V_{DD}	R_L = 2kΩ from V_{DD} to OUT	93	96		
			R_L = 1kΩ from OUT to GND	88	92		
		MAX860/MAX861, FC = V_{DD}, I_L = 50mA to GND, C1 = C2 = 68µF			87		
Voltage-Conversion Efficiency		No load		99	99.9		%
$\overline{SHDN}$ Threshold	V_{IH}	LV = open		2.5			V
		LV = GND		1.2			
	V_{IL}					0.3	
Shutdown Supply Current		$\overline{SHDN}$ < 0.3V	MAX86_C/E			1	µA
			MAX86_M			10	
Time to Exit Shutdown		No load, V_{OUT} = -4V			500		µs

Note 2: C1 and C2 are low-ESR (<0.2Ω) aluminum electrolytics. Capacitor ESR adds to the circuit's output resistance. Using capacitors with higher ESR may reduce output voltage and efficiency.

Note 3: Specified output resistance includes the effect of the 0.2Ω ESR of the test circuit's capacitors.

Note 4: The switches are driven directly at the oscillator frequency, without any division.

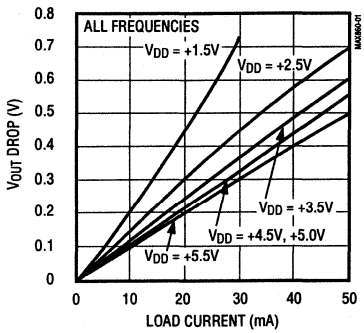
Note 5: At lowest frequencies, using 10µF capacitors gives worse efficiency figures than using the recommended capacitor values in Table 3, due to larger $1/(f_S \times C1)$ term in R_{OUT}.

50mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

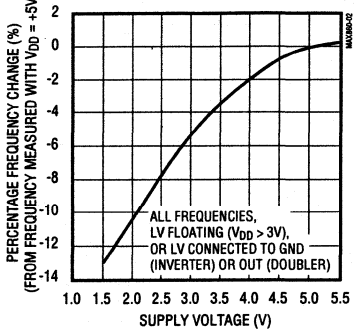
Typical Operating Characteristics

(All curves generated using the inverter circuit shown in the *Typical Operating Circuits* with LV = GND and T_A = +25°C, unless otherwise noted. Test results also valid for doubler mode with LV = OUT and T_A = +25°C, unless otherwise noted. All capacitor values used are those recommended in Table 3. All capacitors are low-ESR Sanyo OS-CONs. The output resistance curves represent the resistance of the device itself, which is R_O in the equation for R_{OUT} shown in the *Capacitor Selection* section.)

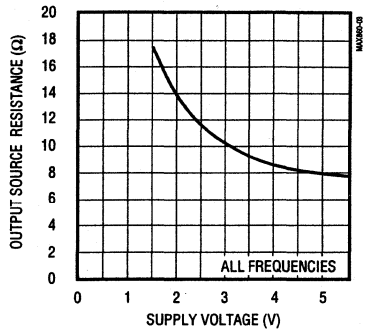
OUTPUT VOLTAGE DROP FROM SUPPLY VOLTAGE vs. LOAD CURRENT



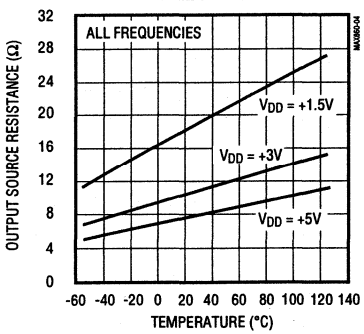
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



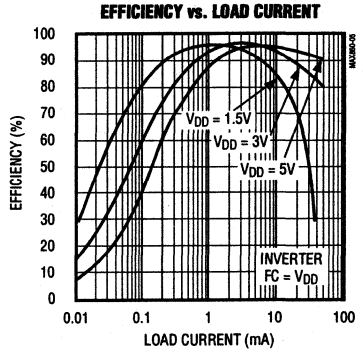
OUTPUT SOURCE RESISTANCE (R_O) vs. SUPPLY VOLTAGE



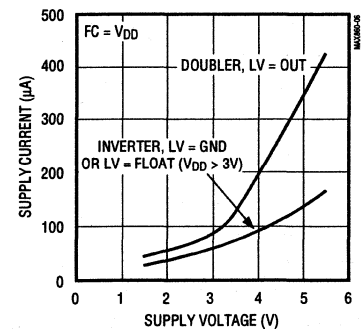
OUTPUT SOURCE RESISTANCE (R_O) vs. TEMPERATURE



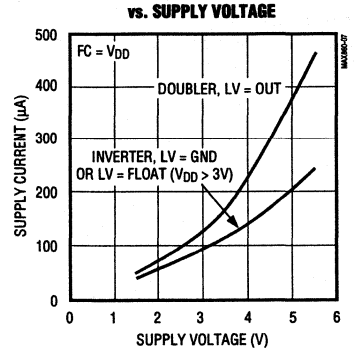
MAX860 EFFICIENCY vs. LOAD CURRENT



MAX860 SUPPLY CURRENT vs. SUPPLY VOLTAGE



MAX861 SUPPLY CURRENT vs. SUPPLY VOLTAGE



50mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

Pin Description

PIN	NAME	FUNCTION	
		INVERTER	DOUBLER
1	FC	Frequency Control, see Table 1	Frequency Control, see Table 1
2	C1+	Flying-Capacitor Positive Terminal	Flying-Capacitor Positive Terminal
3	GND	Ground	Positive Input Supply
4	C1-	Flying-Capacitor Negative Terminal	Flying-Capacitor Negative Terminal
5	OUT	Negative Output	Ground
6	LV	Low-Voltage-Operation Input. Connect to GND for V_{DD} < 3V. Connect to GND or leave floating for V_{DD} > 3V.	Low-Voltage-Operation Input. Connect to OUT.
7	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to V_{DD} if not used. Connect to GND to disable the charge pump.	Active-Low Shutdown Input. Connect to GND pin if not used. Connect to OUT to disable the charge pump.
8	V_{DD}	Positive Input Supply	Doubled Positive Output

Detailed Description

The MAX860/MAX861 capacitive charge pumps either invert or double the voltage applied to their inputs. For highest performance, use low equivalent series resistance (ESR) capacitors. See the *Capacitor Selection* section for more details. The frequency-control (FC) pin allows you to choose one of three switching frequencies; these three selectable frequencies are different for each device. When shut down, MAX860/MAX861 current consumption reduces to less than 1µA.

Common Applications

Voltage Inverter

The most common application for these devices is a charge-pump voltage inverter (see *Typical Operating Circuits*). This application requires only two external components—capacitors C1 and C2—plus a bypass capacitor if necessary (see *Bypass Capacitor* section). Refer to the *Capacitor Selection* section for suggested capacitor types and values.

Even though the MAX860/MAX861's output is not actively regulated, it is fairly insensitive to load-current changes. A circuit output source resistance of 12Ω (calculated using the formula given in the *Capacitor Selection* section) means that, with a +5V input, the output voltage is -5V under no load and decreases to -4.4V with a 50mA load. The MAX860/MAX861 output source resistance (used to calculate the circuit output source resistance) vs. temperature and supply voltage are shown in the *Typical Operating Characteristics* graphs.

Calculate the output ripple voltage using the formula given in the *Capacitor Selection* section.

Positive Voltage Doubler

The MAX860/MAX861 can also operate as positive voltage doublers (see *Typical Operating Circuits*). This application requires only two external components, capacitors C1 and C2. The no-load output is twice the input voltage. The electrical specifications in the doubler mode are very similar to those of the inverter mode except for the Supply Voltage Range (see *Electrical Characteristics* table) and No-Load Supply Current (see graph in *Typical Operating Characteristics*). The circuit output source resistance and output ripple voltage are calculated using the formulas in the *Capacitor Selection* section.

Active-Low Shutdown Input

When driven low, the $\overline{SHDN}$ input shuts down the device. In inverter mode, connect $\overline{SHDN}$ to V_{DD} if it is not used. In doubler mode, connect $\overline{SHDN}$ to GND if it is not used. When the device is shut down, all active circuitry is turned off.

In the inverting configuration, loads connected from OUT to GND are not powered in shutdown mode. However, a reverse-current path exists through two diodes between OUT and GND; therefore, loads connected from V_{DD} to OUT draw current from the input supply.

50mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

In the doubling configuration, loads connected from the V_{DD} pin to the GND pin are not powered in shutdown mode. Loads connected from the V_{DD} pin to the OUT pin draw current from the input supply through a path similar to that of the inverting configuration (described above).

Frequency Control

Charge-pump frequency for both devices can be set to one of three values. Each device has a unique set of three available frequencies, as indicated in Table 1. The oscillator and charge-pump frequencies are the same (i.e., the charge-pump frequency is not half the oscillator frequency, as it is on the MAX660, MAX665, and ICL7660).

Table 1. Nominal Switching Frequencies*

FC CONNECTION	FREQUENCY (kHz)	
	MAX860	MAX861
FC = V_{DD} or open	6	13
FC = GND	50	100
FC = OUT	130	250

**See the Electrical Characteristics for detailed switching-frequency specifications.*

A higher switching frequency minimizes capacitor size for the same performance and increases the supply current (Table 2). The lowest fundamental frequency of the switching noise is equal to the minimum specified switching frequency (e.g., 3kHz for the MAX860 with FC open). The spectrum of noise frequencies extends above this value because of harmonics in the switching waveform. To get best noise performance, choose the device and FC connection to select a minimum switching frequency that lies above your sensitive bandwidth.

Low-Voltage-Operation Input

LV should normally be connected to GND for inverting operation. To enhance compatibility with the MAX660, MAX665, and ICL7660, you may float LV if the input voltage exceeds 3V. In doubling mode, LV must be connected to OUT for all input voltages.

Table 2. Switching-Frequency Trade-Offs

ATTRIBUTE	LOWER FREQUENCY	HIGHER FREQUENCY
Output Ripple	Larger	Smaller
C1, C2 Values	Larger	Smaller
Supply Current	Smaller	Larger

Applications Information

Capacitor Selection

The MAX860/MAX861 are tested using 10µF capacitors for both C1 and C2, although smaller or larger values can be used (Table 3). Smaller C1 values increase the output resistance; larger values reduce the output resistance. Above a certain point, increasing the capacitance of C1 has a negligible effect (because the output resistance becomes dominated by the internal switch resistance and the capacitor ESR). Low-ESR capacitors provide the lowest output resistance and ripple voltage. The output resistance of the entire circuit (inverter or doubler) is approximately:

$$R_{OUT} = R_O + 4 \times ESR_{C1} + ESR_{C2} + 1 / (f_S \times C1)$$

where R_O (the effective resistance of the MAX860/MAX861's internal switches) is approximately 8Ω and f_S is the switching frequency. R_{OUT} is typically 12Ω when using capacitors with 0.2Ω ESR and f_S, C1, and C2 values suggested in Table 3. When C1 and C2 are so large (or the switching frequency is so high) that the internal switch resistance dominates the output resistance, estimate the output resistance as follows:

$$R_{OUT} = R_O + 4 \times ESR_{C1} + ESR_{C2}$$

A typical design procedure is as follows:

1) Choose C1 and C2 to be the same, for convenience.
2) Select f_S:
   a) If you want to avoid a specific noise frequency, choose f_S appropriately.
   b) If you want to minimize capacitor cost and size, choose a high f_S.
   c) If you want to minimize current consumption, choose a low f_S.
3) Choose a capacitor based on Table 3, although higher or lower values can be used to optimize performance. Table 4 lists manufacturers who provide low-ESR capacitors.

Table 3. Suggested Capacitor Values

NOMINAL FREQUENCY (kHz)	C1, C2 (µF)
6	68
13	47
50	10
100	4.7
130	4.7
250	2.2

Table 4. Low-ESR Capacitor Manufacturers

MANUFACTURER	PHONE	FAX	DEVICE TYPE
AVX	(207) 282-5111 (800) 282-4975	(207) 283-1941	Surface mount, TPS series
Matsuo	(714) 969-2491	(714) 960-6492	Surface mount, 267 series
Nichicon	USA: (708) 843-7500 Japan: 81-7-5231-8461	USA: (708) 843-2798 Japan: 81-7-5256-4158	Through-hole, PL series
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	USA: (619) 661-1055 Japan: 81-7-2070-1174	Through-hole, OS-CON series
Sprague	(603) 224-1961	(603) 224-1430	Surface mount, 595D series
United Chemi-Con	(714) 255-9500	(714) 255-9400	Through-hole, LXF series

0*Flying Capacitor, C1*

Increasing the size of the flying capacitor reduces the output resistance.

Output Capacitor, C2

Increasing the size of the output capacitor reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Smaller capacitance values can be used if one of the higher switching frequencies is selected, if less than the maximum rated output current (50mA) is required, or if higher ripple can be tolerated. The following equation for peak-to-peak ripple applies to both the inverter and doubler circuits.

$$V_{RIPPLE} = \frac{I_{OUT}}{2 \times f_S \times C2} + 2 \times I_{OUT} \times ESR_{C2}$$

Bypass Capacitor

Bypass the incoming supply to reduce its AC impedance and the impact of the MAX860/MAX861's switching noise. The recommended bypassing depends on the circuit configuration and where the load is connected.

When the inverter is loaded from OUT to GND or the doubler is loaded from V_{DD} to GND, current from the supply switches between 2 x I_{OUT} and zero. Therefore, use a large bypass capacitor (e.g., equal to the value of C1) if the supply has a high AC impedance.

When the inverter and doubler are loaded from V_{DD} to OUT, the circuit draws 2 x I_{OUT} constantly, except for short switching spikes. A 0.1µF bypass capacitor is sufficient.

Cascading Devices

Two devices can be cascaded to produce an even larger negative voltage, as shown in Figure 1. The unloaded output voltage is nominally -2 x V_{IN}, but this is reduced slightly by the output resistance of the first device multiplied by the quiescent current of the second. The output resistance of the complete circuit is approximately *five times* the output resistance of a single MAX860/MAX861.

Three or more devices can be cascaded in this way, but output resistance rises dramatically, and a better solution is offered by inductive switching regulators (such as the MAX755, MAX759, MAX764, or MAX774). Connect LV as with a standard inverter circuit (see *Pin Description*).

Paralleling Devices

Paralleling multiple MAX860s or MAX861s reduces the output resistance. As illustrated in Figure 2, each device requires its own pump capacitor (C1), but the reservoir capacitor (C2) serves all devices. C2's value should be increased by a factor of n, where n is the number of devices. Figure 2 shows the equation for calculating output resistance. An alternative solution is to use the MAX660 or MAX665, which are capable of supplying up to 100mA of load current. Connect LV as with a standard inverter circuit (see *Pin Description*).

Combined Doubler/Inverter

In the circuit of Figure 3, capacitors C1 and C2 form the inverter, while C3 and C4 form the doubler. C1 and C3 are the pump capacitors; C2 and C4 are the reservoir capacitors. Because both the inverter and doubler use part of the charge-pump circuit, loading either output causes both outputs to decline towards GND. Make sure the sum of the currents drawn from the two outputs does not exceed 60mA. Connect LV as with a standard inverter circuit (see *Pin Description*).

50mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

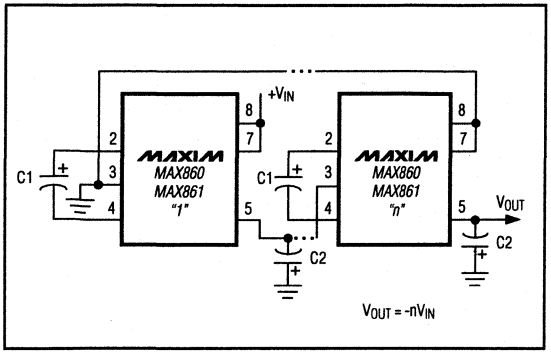


Figure 1. Cascading MAX860s or MAX861s to Increase Output Voltage

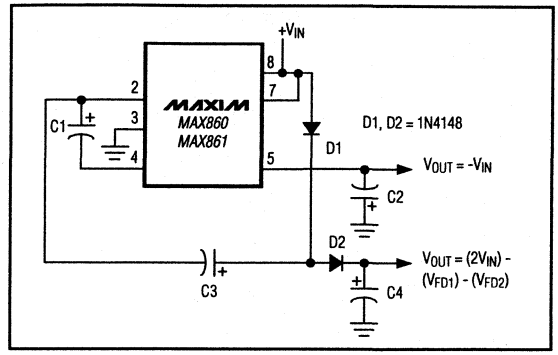


Figure 3. Combined Doubler and Inverter

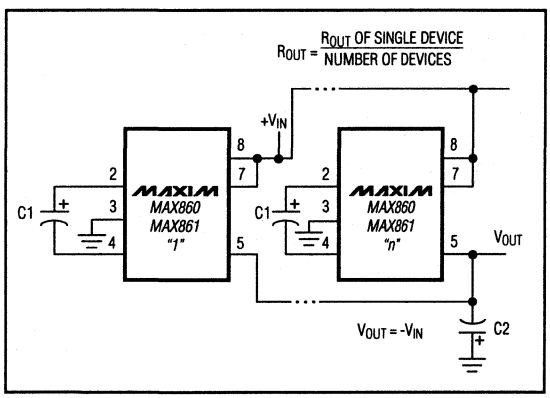


Figure 2. Paralleling MAX860s or MAX861s to Reduce Output Resistance

Table 5. Product Selection Guide

PART NUMBER	OUTPUT CURRENT (mA)	OUTPUT RESISTANCE (Ω)	SWITCHING FREQUENCY (kHz)
MAX660	100	6.5	5/40
MAX665	100	6.5	5/40
MAX860	50	12	6/50/130
MAX861	50	12	13/100/250
ICL7660	10	55	5

Compatibility with MAX660/MAX665/ICL7660

The MAX860/MAX861 can be used in sockets designed for the MAX660, MAX665, and ICL7660 with a minimum of one wiring change. This section gives advice on installing a MAX860/MAX861 into a socket designed for one of the earlier devices.

The MAX660, MAX665, and ICL7660 have an OSC pin instead of $\overline{SHDN}$. MAX660, MAX665, and ICL7660 normal operation is with OSC floating (although OSC can be overdriven). If OSC is floating, pin 7 ($\overline{SHDN}$) should be jumpered to V_{DD} to enable the MAX860/MAX861 permanently. Do not leave $\overline{SHDN}$ on the MAX860/MAX861 floating.

The MAX860/MAX861 operate with FC either floating or connected to V_{DD}, OUT, or GND; each connection defines the oscillator frequency. Thus, any of the normal MAX660, MAX665, or ICL7660 connections to pin 1 will work with the MAX860/MAX861, without modifications. Changes to the FC connection are only required if you want to adjust the operating frequency.

19-0204; Rev 1; 5/94

EVALUATION KIT AVAILABLE

MAXIM

5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

General Description

The MAX877/MAX878/MAX879 are pulse-skipping, step-up/step-down DC-DC converters that provide a regulated output from inputs both above and below the output. They require only three external components—an inductor (typically 22µH) and two filter capacitors.

The MAX877 delivers a regulated 5V output from 2.5V to 6.2V inputs. The MAX878 generates pin-selectable voltages of 3.0V or 3.3V from 1.5V to 6.2V inputs. The MAX879 output can be adjusted from 2.5V to 6V via an external resistor divider from 2.5V to 6.2V inputs.

A unique high-power, internal, synchronous rectifier design (Active Rectifier™) enables the devices to regulate in a switched linear mode if the input voltage is higher than the desired output voltage. When the input voltage falls below the output voltage, the MAX877/MAX878/MAX879 will smoothly switch into a pulse-skipping boost mode and step up from input voltages as low as 1V. In shutdown, the active rectifier disconnects the output from the source. This stops the current drain from input to output associated with conventional step-up converters.

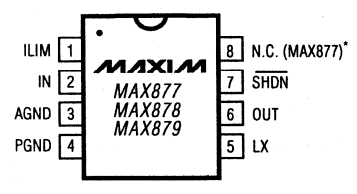
High-frequency operation (up to 300kHz) allows the use of small surface-mount inductors. Supply current is 195µA under no load, and only 20µA in shutdown mode. For 1-cell (1V) step-up converters with similar performance and the same pinout, refer to the MAX777/MAX778/MAX779 data sheet.

Applications

Two or Three NiCd Cells to 3V/3.3V Conversion
Three or Four Alkaline Cells to 5V Conversion
One Lithium Cell to 3V/3.3V Conversion
Pagers
Palmtop and Notebook Computers
Battery-Powered and Hand-Held Instruments

Pin Configuration

TOP VIEW



DIP/SO

* SEL (MAX878), FB (MAX879)

Features

- ♦ **Regulates from Inputs Above & Below the Output**
- ♦ **1V to 6.2V Supply-Voltage Range**
- ♦ **Internal 1A Active Rectifier with Input-to-Output Disconnect in Shutdown**
- ♦ **Up to 210mA Load Currents, Guaranteed**
- ♦ **85% Efficiency**
- ♦ **Only 3 External Components**
- ♦ **Adjustable Current Limit**
- ♦ **195µA Quiescent Supply Current**
- ♦ **20µA Shutdown Supply Current**
- ♦ **3V/3.3V/5V and Adjustable Output Voltage Versions**
- ♦ **Available in 8-Pin DIP and SO Packages**

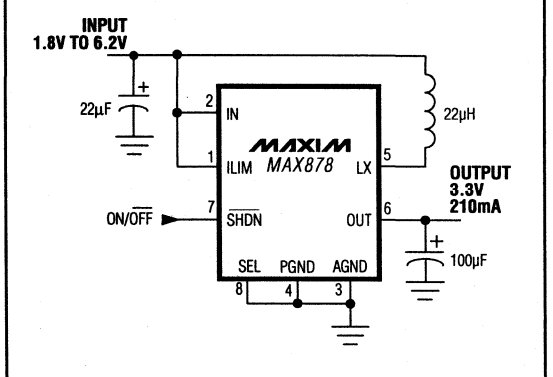
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX877CPA	0°C to +70°C	8 Plastic DIP
MAX877CSA	0°C to +70°C	8 SO
MAX877C/D	0°C to +70°C	Dice*
MAX877EPA	-40°C to +85°C	8 Plastic DIP
MAX877ESA	-40°C to +85°C	8 SO
MAX877MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Typical Operating Circuit



™ Active Rectifier is a trademark of Maxim Integrated Products.

5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IN to PGND) ..... 0V to +7V
Output Short-Circuit Duration to PGND, AGND (Note 1) 30sec
Voltage Applied to:
LX (switch off) ..... -0.3V to +7V
(switch on) ..... 30sec short to IN or OUT
OUT, $\overline{SHDN}$ ..... -0.3V to +7V
FB ..... -0.3V to (OUT + 0.3V)
AGND to PGND ..... -0.3V, +0.3V
Reverse Battery Current 900mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges:
MAX87_C_A ..... 0°C to +70°C
MAX87_E_A ..... -40°C to +85°C
MAX87_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The output may be shorted to ground continuously if the package power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.7V, I_{LOAD} = 0mA, LX = 22µH, C_{OUT} = 100µF, $\overline{SHDN}$ and ILIM connected to IN, AGND connected to PGND, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage (Notes 2, 6)		I_{LOAD} = 0mA, T_A = +25°C			1		V
		MAX877/MAX879 (V_{OUT} = 5V), 0mA < I_{LOAD} < 180mA, T_A = +25°C				2.5	
		MAX878/MAX879 (V_{OUT} = 3.3V), 0mA < I_{LOAD} < 120mA, T_A = +25°C				1.5	
Maximum Operating Voltage		(Notes 2, 3)		6.2			V
Output Voltage (MAX879 set to 5V) (Note 3)		MAX877C/MAX879C: 0mA ≤ I_{LOAD} ≤ 240mA, 2.7V ≤ V_{IN} ≤ 6.2V; MAX877E/MAX879E: 0mA ≤ I_{LOAD} ≤ 220mA, 2.7V ≤ V_{IN} ≤ 6.2V; MAX877M/MAX879M: 0mA ≤ I_{LOAD} ≤ 180mA, 2.7V ≤ V_{IN} ≤ 6.2V		4.80	5.00	5.20	V
Output Voltage (MAX879 set to 3.3V) (Note 3)	SEL = 0V	MAX878C/MAX879C: 0mA ≤ I_{LOAD} ≤ 210mA, 1.8V ≤ V_{IN} ≤ 6.2V; MAX878E/MAX879E: 0mA ≤ I_{LOAD} ≤ 200mA, 1.8V ≤ V_{IN} ≤ 6.2V; MAX878M/MAX879M: 0mA ≤ I_{LOAD} ≤ 180mA, 1.8V ≤ V_{IN} ≤ 6.2V		3.17	3.30	3.43	V
	SEL = Open	MAX878C: 0mA ≤ I_{LOAD} ≤ 210mA, 1.8V ≤ V_{IN} ≤ 6.2V; MAX878E: 0mA ≤ I_{LOAD} ≤ 200mA, 1.8V ≤ V_{IN} ≤ 6.2V; MAX878M: 0mA ≤ I_{LOAD} ≤ 180mA, 1.8V ≤ V_{IN} ≤ 6.2V		2.88	3.00	3.12	
Output Voltage Range		MAX879, I_{LOAD} = 0mA (Note 4)		2.5		6.0	V
Efficiency		MAX877/MAX879 (V_{OUT} = 5V), I_{LOAD} = 100mA, V_{IN} = 4V			85		%
		MAX878/MAX879 (V_{OUT} = 3.3V), I_{LOAD} = 100mA, V_{IN} = 2.5V			82		
No-Load Supply Current		I_{LOAD} = 0mA (switch off)			195	310	µA
Shutdown Supply Current		$\overline{SHDN}$ = 0V	MAX87_C, MAX87_E		20	30	µA
			MAX87_M		20	35	
$\overline{SHDN}$ Bias Current		0V < $\overline{SHDN}$ < V_{IN}			15	100	nA
		V_{IN} < $\overline{SHDN}$ < 5V			12	40	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.7V, I_{LOAD} = 0mA, LX = 22µH, C_{OUT} = 100µF, $\overline{SHDN}$ and ILIM connected to IN, AGND connected to PGND, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Threshold	V_{IN} = 1V to 6.2V		V_{IN}/2 +0.25		V
	V_{IN} = 2.7V	1.3		1.7	
$\overline{SHDN}$ Enable Delay			150		µs
Current Limit			1.0		A
Current-Limit Temperature Coefficient			-0.3		%/°C
Switch Saturation Voltage	I_{SW} = 400mA		0.275		V
	I_{SW} = 600mA		0.33		
	I_{SW} = 1000mA		0.50		
Maximum Switch On Time	V_{IN} = 2.5V		4.0		µs
	V_{IN} = 1.8V		5.9		
	V_{IN} = 1V		12.6		
Minimum Switch Off Time	MAX877/MAX879		1.3		µs
	MAX878		2.3		
Rectifier Forward Voltage Drop	I_{SW} = 400mA		0.21		V
	I_{SW} = 600mA		0.31		
	I_{SW} = 1000mA		0.50		
Error-Comparator Trip Point (V_{REF})	MAX879, V_{IN} = 1.8V to 5V (Note 5)	197.5	202.5	207.5	mV
FB Pin Bias Current	MAX879		10	40	nA
Switch Off Leakage Current			0.1		µA
Rectifier Off Leakage Current			0.1		µA

Note 2: Output in regulation, V_{OUT} = V_{OUT} (nominal) ±4%.

Note 3: At high V_{IN} to V_{OUT} differentials, the maximum load current is limited by the maximum allowable power dissipation in the package (see *Absolute Maximum Ratings* and Maximum Output Current graphs in the *Typical Operating Characteristics*).

Note 4: Minimum value is production tested. Maximum value is guaranteed by design and is not production tested.

Note 5: V_{OUT} is set to a target value of 5V by 0.1% external feedback resistors. V_{OUT} is measured to be within 5V ±2.5% to guarantee error-comparator trip point.

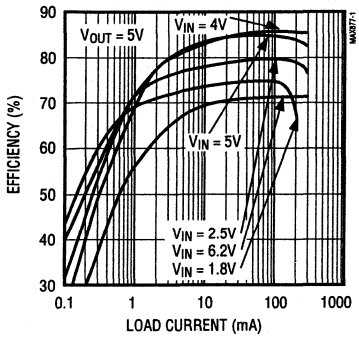
Note 6: Startup guaranteed under these load conditions.

5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

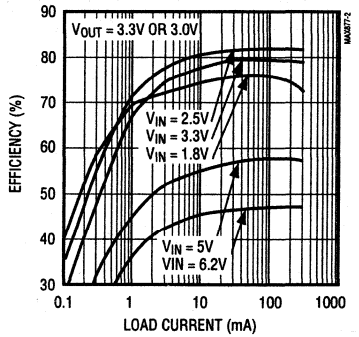
Typical Operating Characteristics

(Circuit of Figure 4, T_A = +25°C, unless otherwise noted.)

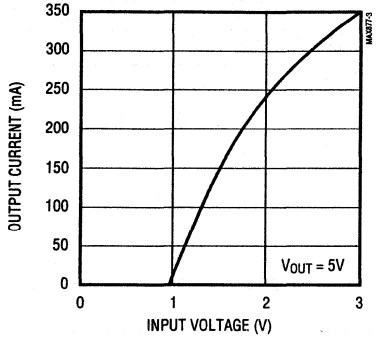
MAX877/MAX879 EFFICIENCY vs. LOAD CURRENT



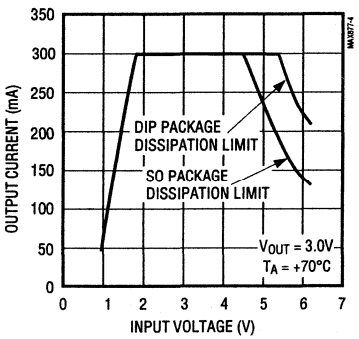
MAX878 EFFICIENCY vs. LOAD CURRENT



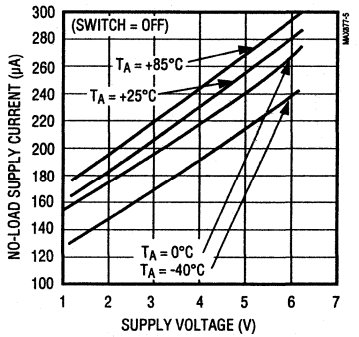
MAX877/MAX879 MAXIMUM OUTPUT CURRENT AT LOW INPUT VOLTAGE



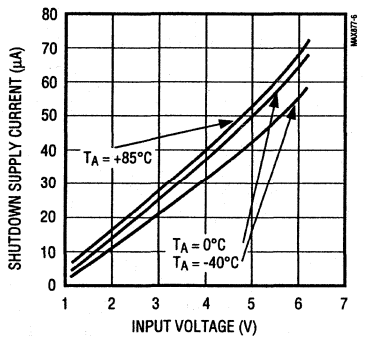
MAX878 MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



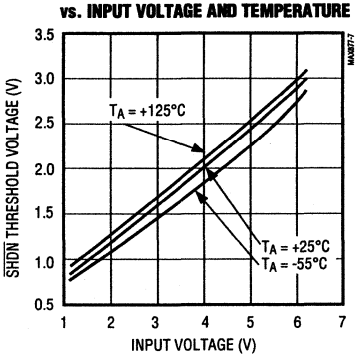
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



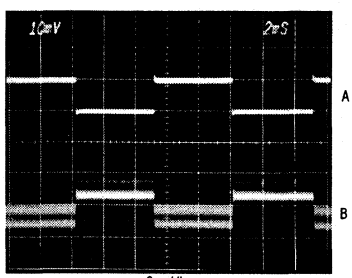
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE AND TEMPERATURE



SHDN THRESHOLD VOLTAGE vs. INPUT VOLTAGE AND TEMPERATURE



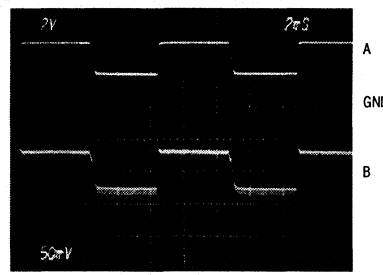
LOAD-TRANSIENT RESPONSE



2ms/div

A: I_{OUT}, 200mA/div, 0mA to 200mA
B: V_{OUT}, 50mV/div, AC COUPLED
MAX878, V_{OUT} = 3.3V, V_{IN} = 2.5V

LINE-TRANSIENT RESPONSE



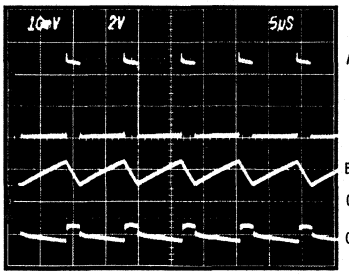
2ms/div

A: V_{IN}, 2V/div, 2V to 4V
B: V_{OUT}, 50mV/div, AC COUPLED
I_{OUT} = 240mA
MAX878, V_{OUT} = 3.3V, $C_{INBYPASS}$ = 47µF

Typical Operating Characteristics (continued)

(Circuit of Figure 4, T_A = +25°C, unless otherwise noted.)

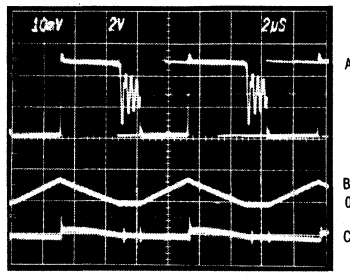
SWITCHING WAVEFORMS— CONTINUOUS CONDUCTION



5µs/div

A: SWITCH VOLTAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 0.5A/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div
MAX877, V_{IN} = 1.5V, I_{OUT} = 100mA

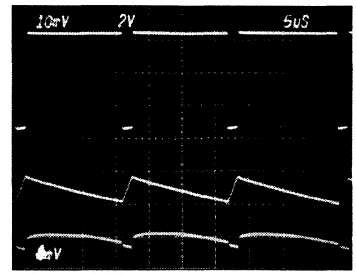
SWITCHING WAVEFORMS— DISCONTINUOUS CONDUCTION



2µs/div

A: SWITCH VOLTAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 0.5A/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div
MAX877, V_{IN} = 3V, I_{OUT} = 70mA

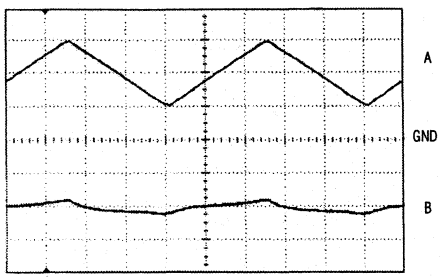
STEP-DOWN CONVERSION



5µs/div

A: SWITCH VOLTAGE (LX PIN), 2V/div
B: INDUCTOR CURRENT, 0.5A/div
C: OUTPUT VOLTAGE RIPPLE, 50mV/div
MAX878, V_{IN} = 6.0V, V_{OUT} = 5.0V, I_{OUT} = 210mA

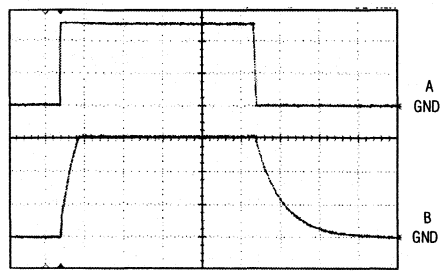
STEP-UP/STEP-DOWN OPERATION



20ms/div

A: INPUT VOLTAGE, 2V/div, 2V to 6V
B: OUTPUT VOLTAGE, 50mV/div
MAX878, I_{OUT} = 100mA, V_{OUT} = 3.3V

MAX878 START-UP TIME



10ms/div

A: $\overline{SHDN}$, 2V/div
B: V_{OUT}, 1V/div
V_{OUT} = 3V

5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

Pin Description

PIN	NAME	FUNCTION
1	ILIM	Sets switch current-limit input. Connect to IN for 1A current limit. A resistor from ILIM to IN sets lower peak inductor currents.
2	IN	Input supply.
3	AGND	Analog ground. Not internally connected to PGND.
4	PGND	Power ground must be low impedance; solder directly to ground plane or star ground. Connect to AGND, close to the device.
5	LX	1A NPN power switch collector and active-rectifier PNP emitter.
6	OUT	Voltage output. Connect filter capacitor close to pin.
7	$\overline{SHDN}$	Shutdown input disables power supply when low. Also disconnects load from input. Threshold is set at $V_{IN}/2$. Connect to IN for normal operation.
8	N.C. (MAX877)	No connect, not internally connected.
	SEL (MAX878)	Selects the main output voltage: 3.3V when connected to AGND, 3.0V when left open.
	FB (MAX879)	Feedback input for adjustable-output operation. Connect to an external voltage divider between V_{OUT} and AGND.

Detailed Description

Operating Principle

The MAX877/MAX878/MAX879 combine a switch-mode regulator with an NPN bipolar power switch and current limit, a precision voltage reference, and a synchronous rectifier—all in a single monolithic device. In shutdown mode, the internal rectifier is completely turned off and disconnects the load from the source. Only two external components are required in addition to the input bypass capacitor—a 22µH inductor, and a 100µF filter capacitor.

A minimum-off-time, current-limited, pulse-frequency-modulation (PFM) control scheme combines the high output power and efficiency of pulse-width modulation (PWM) with the low quiescent currents of traditional PFM pulse skippers.

External conditions (inductor value, load, and input voltage) determine the way the converter operates, as follows:

At light loads, the current through the inductor starts at zero, rises to a peak value, and drops down to zero in each cycle (discontinuous-conduction mode). In this case, the switching frequency is governed by a pair of one-shots, which set a maximum on-time inversely proportional to V_{IN} [$t_{ON} = 8.8/(V_{IN} - 0.25)$] and a minimum off-time (1.3µs for MAX877/MAX879, or 2.3µs for MAX878). With a 22µH inductor, LX's peak current is about 400mA and is independent of input voltage. Efficiency at light loads is improved because of lower peak currents.

At very light loads, more energy is stored in the coil than is required by the load in each cycle. The converter regulates by skipping entire cycles. Efficiency is typically 65% to 75% in the pulse-skipping mode. Pulse-skipping waveforms can be irregular, and the output waveform contains a low-frequency component. Larger, low equivalent-series-resistance (ESR) filter capacitors can help reduce the ripple voltage if needed.

At heavy loads above approximately 100mA, the converter enters continuous-conduction mode, where current always flows in the inductor. The switch ON state is controlled on a cycle-by-cycle basis, either by the t_{ON}(max) time or the preset current limit in the switch. This prevents exceeding the switch current rating or saturating the inductor. At very heavy loads, the inductor current self-oscillates between this peak current limit and some lower value governed by the minimum off-time, the inductance value, and the input/output differential.

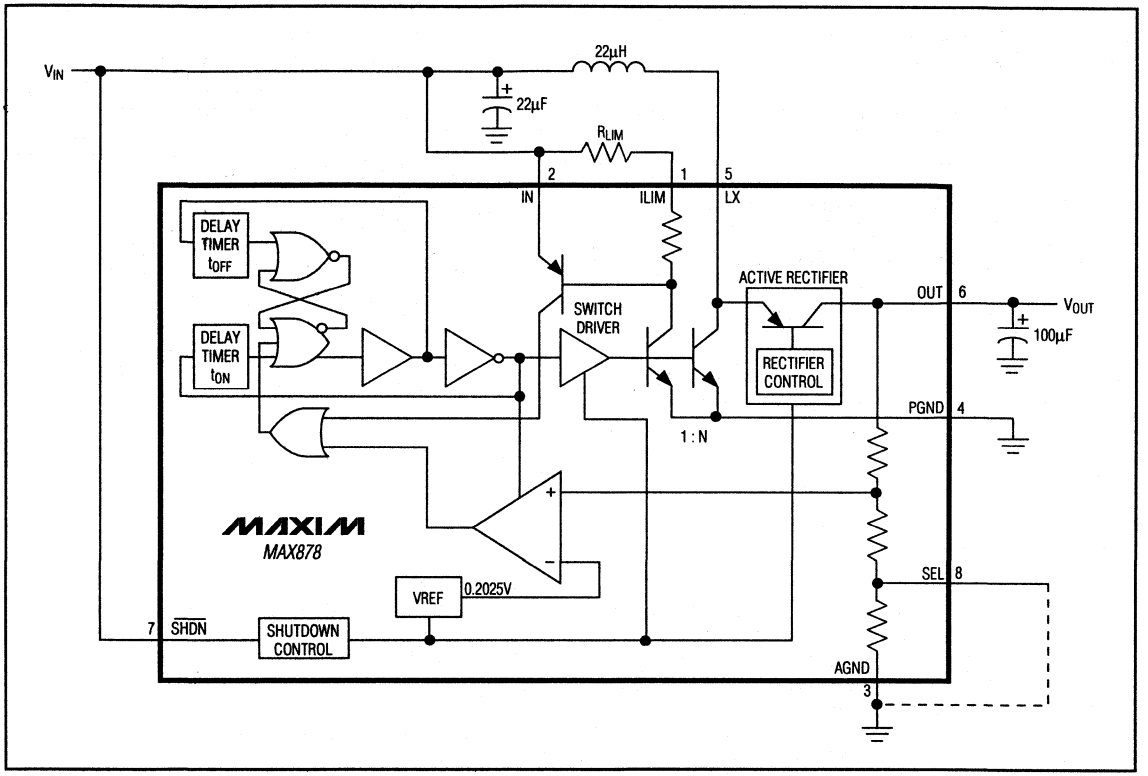


Figure 1. MAX878 Block Diagram

With ILIM shorted to IN, the peak switch current of the internal NPN power switch is set to 1A. It can be set to a lower value by connecting a resistor between ILIM and IN (see *Current Limit* section). This enables the use of physically smaller inductors with lower saturation-current ratings. At 1A, the switch voltage drop (V_{SW}) is about 500mV. V_{SW} decreases to about 250mV at 0.1A.

Conventional PWM converters generate constant-frequency switching noise, while this architecture produces variable-frequency switching noise. The output ripple is the product of the peak inductor current and the output capacitor's ESR. Unlike conventional pulse-skippers, the MAX877/MAX878/MAX879 peak currents are scaled down at light loads, resulting in lower output ripple.

Step-Down Mode and Power Dissipation

In battery-powered applications, for example, where the input voltage exceeds the output voltage, the MAX877/MAX878/MAX879 behave as "switched" linear regulators. If the output voltage starts to drop, the switch turns on and energy is stored in the coil, as in normal step-up mode. After the switch turns off, the voltage at LX flies high. The active rectifier turns on when LX rises above V_{IN}. As in a linear regulator, the voltage difference between V_{IN} and V_{OUT} appears across the rectifier (actually a PNP transistor) until the current goes to zero and the rectifier turns off. At high V_{IN} to V_{OUT} differentials, the maximum load current is limited by the maximum allowable power dissipation in the package (see *Typical Operating Characteristics*).

5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

Active Rectifier

The internal active rectifier of the MAX877/MAX878/MAX879 replaces the external Schottky catch diode in normal boost operation. The rectifier consists of a PNP pass transistor and a unique control circuit which, in shutdown mode, entirely disconnects the load from the source. This is a distinct advantage over standard boost topologies, since it prevents battery drain in shutdown. The MAX877/MAX878/MAX879 can withstand a momentary short at the output in normal operation.

The active rectifier also acts as a zero-dropout regulator if the input exceeds the regulated output.The device still switches to deliver power to the output, and the difference between the input and output voltage appears across the rectifier. Efficiency is similar to that of a linear regulator if the MAX877/MAX878/MAX879 are used as step-down converters. The maximum output current (I_{OUT} (MAX)) with larger input/output differentials is determined by package power dissipation. I_{OUT} (MAX) can be approximated by:

$$I_{OUT}(MAX) \approx \left(\frac{P_{DISS}}{(V_{IN} - V_{OUT})} \right) \times 0.9$$

Shutdown

Shutdown ($\overline{SHDN}$) is a high-impedance, active-low input. Connect it to IN for normal operation. Keeping $\overline{SHDN}$ at ground holds the converters in shutdown mode. Since the active rectifier is turned off in this mode, the path from input to load is cut, and the output effectively drops to 0V. The supply current in shutdown mode ranges from 4µA at V_{IN} = 1V to 50µA at V_{IN} = 5V. The shutdown-circuit threshold is set nominally to $V_{IN}/2$ + 250mV. When $\overline{SHDN}$ is below this threshold, the device is shut down; it is enabled with $\overline{SHDN}$ above the threshold. When driven from external logic, $\overline{SHDN}$ can be driven to a higher voltage than V_{IN}, (6.2V max).

Current Limit

Connecting ILIM to IN sets an LX current limit of 1A. For smaller output power levels that do not require the maximum peak current, reduce the peak inductor current by connecting a resistor between ILIM and IN. This optimizes overall efficiency and allows very small, low-cost coils with lower current ratings. See Figure 2 to select the resistor (see also *Inductor Selection* section).

Output Voltage Selection

The MAX877's output voltage is fixed at 5V. The MAX878's output voltage can be set to 3V by leaving the SEL pin open, or to 3.3V by connecting SEL to AGND.

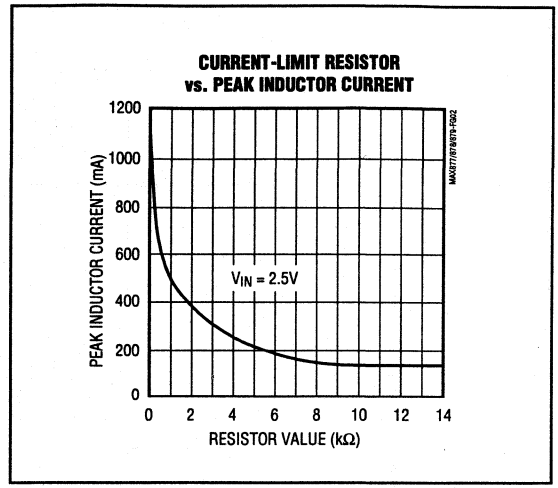


Figure 2. Current-Limit Resistor vs. Peak Inductor Current

The MAX879's output voltage is set by two resistors, R1 and R2 (Figure 3), which form a voltage divider between the output and the FB pin. The output voltage can be set from 2.5V to 6.0V by the equation:

$$V_{OUT} = V_{REF} \frac{(R1 + R2)}{R2}$$

where V_{REF} = 0.2025V.

To simplify the resistor selection:

$$R1 = R2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

Since the input current at FB has a maximum of 40nA, large values (10kΩ to 50kΩ for R2) can be used without significant accuracy loss. For 1% error, the current through R2 should be at least 100 times FB's bias current.

When large values are used for the feedback resistors (R1 > 50kΩ), stray output impedance at FB can add a "lag" to the feedback response, destabilizing the regulator and creating a larger ripple at the output. Lead lengths and circuit board traces at the FB node should be kept short. Reduce ripple by adding a "lead" compensation capacitor (C3, 100pF to 50nF) in parallel with R1.

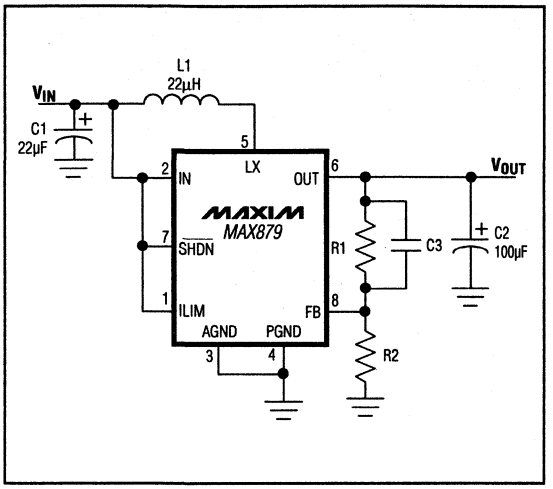


Figure 3. MAX879 Adjustable Voltage

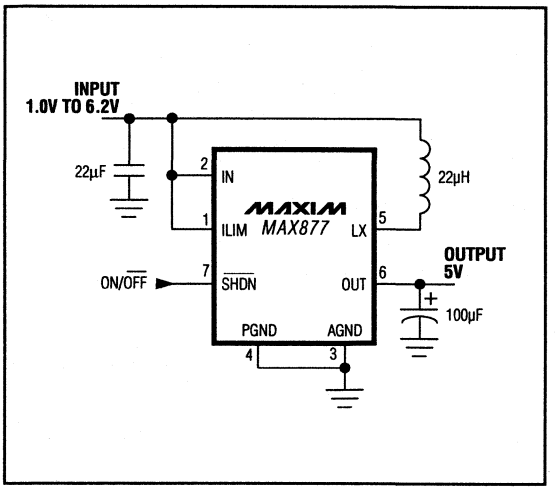


Figure 4. MAX877 Standard Application Circuit

Applications Information

Figure 4 shows a MAX877 step-up application circuit. This circuit starts up and operates with inputs ranging from 1.0V to 6.2V. Start-up time is a function of the load, typically less than 5ms. Output current capability is a function of the input voltage (see *Typical Operating Characteristics*).

The converters will regulate down to the output voltage and seamlessly switch into boost mode as the input drops below the output voltage. This is especially useful in battery-powered applications, where the battery voltage may initially exceed the output voltage. To generate 5V from four alkaline cells in series, the input ranges from 6.2V to 3.6V. When the battery pack is fresh, the MAX877 will step down with the active rectifier acting as the switch. As the batteries approach 5V, or the desired output voltage, the converter's control circuitry will ensure a smooth transition into step-up mode. The converter operates until the batteries are less than 3V; efficiency is typically 80% with fresh batteries, and is close to 85% at V_{IN} = 4V.

Inductor Selection

The 22µH inductor shown in the *Typical Operating Circuit* is sufficient for most MAX877/MAX878/MAX879 designs. Other inductor values ranging from 10µH to 47µH are also suitable. The inductor should have a saturation rating equal to or greater than the peak switch-current limit, which is 1A without an external current limit (ILIM connected to IN). It is acceptable to operate the inductor at 120% of its saturation rating; however, this may slightly reduce efficiency. For highest efficiency, use an inductor with a low **DC resistance**, preferably under 0.2Ω. Table 1 lists suggested inductor suppliers.

Capacitor Selection

The 100µF, 10V surface-mount tantalum (SMT) output capacitor shown in the *Typical Operating Circuit* will provide a 25mV output ripple or less, stepping up from 3V to 5V at 200mA. Smaller capacitors, down to 10µF, are acceptable for light loads or in applications that can tolerate higher output ripple. The input capacitor may be omitted if the supply has low output impedance and the input lead length is less than 2 inches (5cm) or the loads are small.

The primary factor in selecting both the output and input filter capacitor is low ESR. The ESR of both bypass and filter capacitors affects efficiency. Optimize performance by increasing filter capacitors or using specialized low-ESR capacitors. The smallest low-ESR SMT tantalum capacitors currently available are Sprague 595D or 695D series. Sanyo OS-CON organic-semiconductor through-hole capacitors also exhibit very low ESR, are rated for the wide temperature range, and are especially suitable for operation at cold temperatures (below 0°C).

Table 1 lists suggested capacitor suppliers.

5V/3.3V/3V/Adjustable-Output, Step-Up/Step-Down DC-DC Converters

Layout

The MAX877/MAX878/MAX879's high peak currents and high-frequency operation make PC layout important for minimum ground bounce and noise. Locate input bypass and output filter capacitors close to the device pins. All connections to the FB pin (MAX879) should also be kept as short as possible. A ground plane is recommended. Solder AGND (pin 3) and PGND (pin 4) directly to the ground plane. Refer to the MAX877/MAX878/MAX879 evaluation kit (EV kit) manual for a suggested surface-mount layout.

Table 1. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida CD54-220 (22µH) Murata-Erie LQHYN1501K04M00-D5 (15µH) CoilCraft DO3316-223 (22µH) Coiltronics CTX20-1 (22µH)	Sprague 595D Sprague 695D Matsuo 267 series AVX TPS series
Miniature Through-Hole	Sumida RCH654-220 (22µH)	Sanyo OS-CON (low-ESR organic semiconductor)
Low-Cost Through-Hole	Renco RL 1284-22 (22µH) CoilCraft PCH-27-223 (22µH)	Nichicon PL series (low-ESR electrolytic) United Chemi-Con LXF series

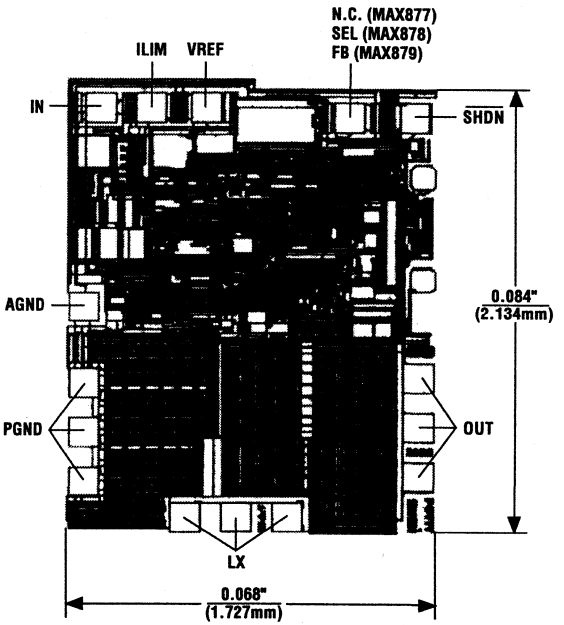
AVX	USA:	(207) 282-5111	FAX (207) 283-1941
CoilCraft	USA:	(708) 639-6400	FAX (708) 639-1469
Coiltronics	USA:	(407) 241-7876	FAX (407) 241-9339
Matsuo	USA:	(714) 969-2491	FAX (714) 960-6492
	Japan:	(06) 332-0871	
Murata-Erie	USA:	(800) 831-9172	FAX (814) 238-0490
Nichicon	USA:	(708) 843-7500	FAX (708) 843-2798
	Japan:	(81) 7-5231-8461	FAX (81) 7-5256-4158
Renco	USA:	(516) 586-5566	FAX (516) 586-5562
Sanyo	USA:	(619) 661-6835	FAX (619) 661-1055
	Japan:	(0720) 70-1005	FAX (0720) 70-1174
Sprague	USA:	(603) 224-1961	FAX (603) 224-1430
Sumida	USA:	(708) 956-0666	FAX (708) 956-0702
	Japan:	(81) 3607-5111	FAX (81) 2070-1174
United Chemi-Con	USA:	(714) 255-9500	FAX (714) 255-9400

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX878CPA	0°C to +70°C	8 Plastic DIP
MAX878CSA	0°C to +70°C	8 SO
MAX878C/D	0°C to +70°C	Dice*
MAX878EPA	-40°C to +85°C	8 Plastic DIP
MAX878ESA	-40°C to +85°C	8 SO
MAX878MJA	-55°C to +125°C	8 CERDIP
MAX879CPA	0°C to +70°C	8 Plastic DIP
MAX879CSA	0°C to +70°C	8 SO
MAX879C/D	0°C to +70°C	Dice*
MAX879EPA	-40°C to +85°C	8 Plastic DIP
MAX879ESA	-40°C to +85°C	8 SO
MAX879MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

Chip Topography



TRANSISTOR COUNT: 170

SUBSTRATE CONNECTED TO AGND

MAXIM

Low-Dropout P-Channel Linear Regulators

General Description

The MAX882/MAX883/MAX884 linear regulators maximize battery life by combining ultra-low supply currents and low dropout voltages. Featuring P-channel MOSFET pass transistors, these regulators draw less than 15µA (max over temperature), independent of output current. Supply current remains low because there are no base currents like those found in conventional PNP bipolar linear regulators. Also, when the input-to-output voltage differential becomes small, the MAX882 family's P-channel transistor will not saturate, thereby avoiding excessive base-current losses. The pass transistor has a 1.2Ω resistance when delivering 5V, so dropout voltage is only 300mV with a 250mA output current.

The MAX882 features a 10µA standby mode that disables the output yet keeps the biasing circuitry (including the low-battery comparator) alive. The MAX883/MAX884 feature a shutdown mode that turns off all circuitry, reducing the supply current to less than 1µA. All three ICs feature a low-battery detector, short-circuit and reverse-voltage protection, and thermal shutdown.

Outputs are preset at 3.3V for the MAX882/MAX884 and 5V for the MAX883. In addition, all devices employ Dual-Mode™ operation, allowing user-adjustable outputs from 1.2V to 10V using external resistors. The input voltage supply range is 2.7V to 11.5V.

These devices are available in a special high-power 8-pin SO package that can dissipate up to 1.4W at +70°C (compared to 0.47W for conventional packages), in addition to an 8-pin DIP package.

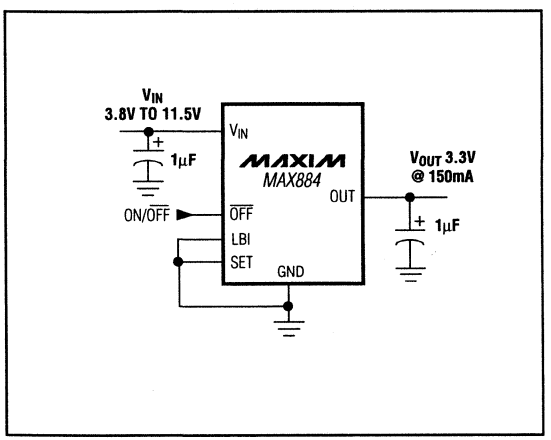
Features

- **Preset or Adjustable Outputs:**
  3.3V (MAX882/MAX884)
  5V (MAX883)
- **250mA Output Current**
- **1.2Ω P-Channel Pass Transistor Draws No Base Current**
- **High-Power 8-Pin SO Package (dissipates 1.4W at +70°C)**
- **15µA Max Supply Current**
- **1µA Max Shutdown Current (MAX883/MAX884)**
- **300mV Dropout Voltage at 250mA Output Current**
- **Low-Battery-Detection Comparator**
- **2.7V to 11.5V Input Voltage Range**
- **Short-Circuit and Reverse-Voltage Protection**
- **Thermal Shutdown**

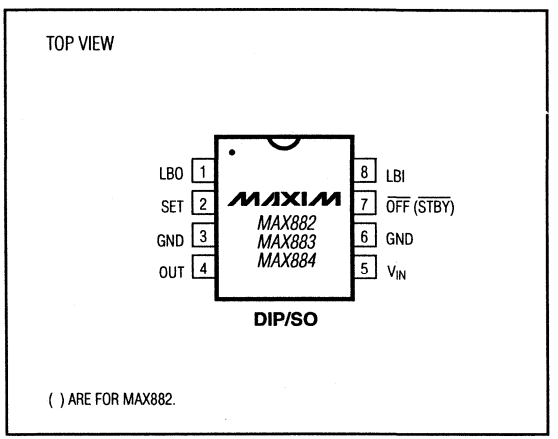
Applications

High-Efficiency Linear Regulators
Battery-Powered Devices
Portable Instruments
Backup Power Supplies

Typical Operating Circuit



Pin Configuration



™ Dual-Mode is a trademark of Maxim Integrated Products.

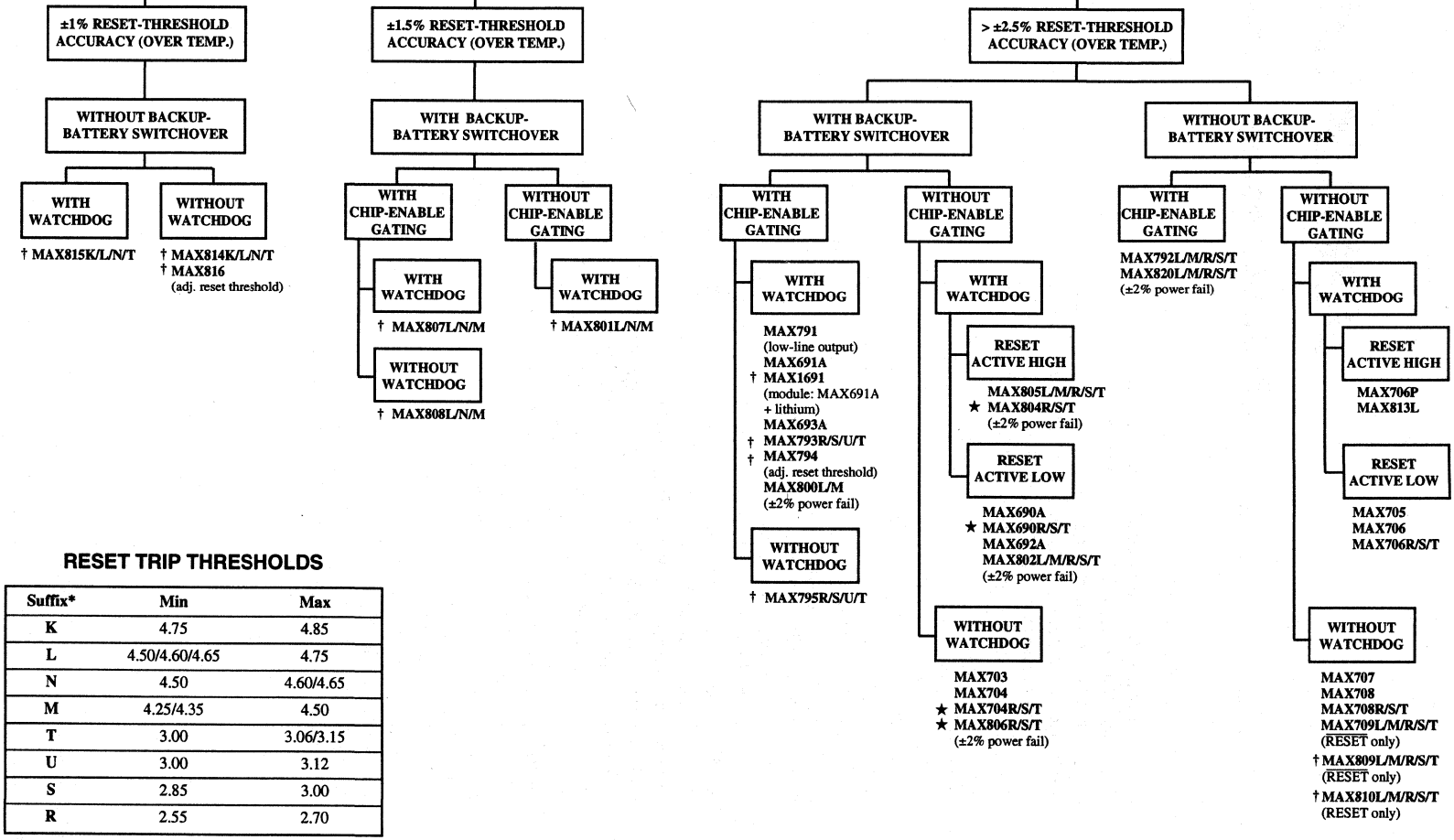
MAXIM

µP Supervisory Circuits

5

*Advance Information–first page of data sheet in preparation.

µP SUPERVISORY CIRCUITS



RESET TRIP THRESHOLDS

Suffix*	Min	Max
K	4.75	4.85
L	4.50/4.60/4.65	4.75
N	4.50	4.60/4.65
M	4.25/4.35	4.50
T	3.00	3.06/3.15
U	3.00	3.12
S	2.85	3.00
R	2.55	2.70

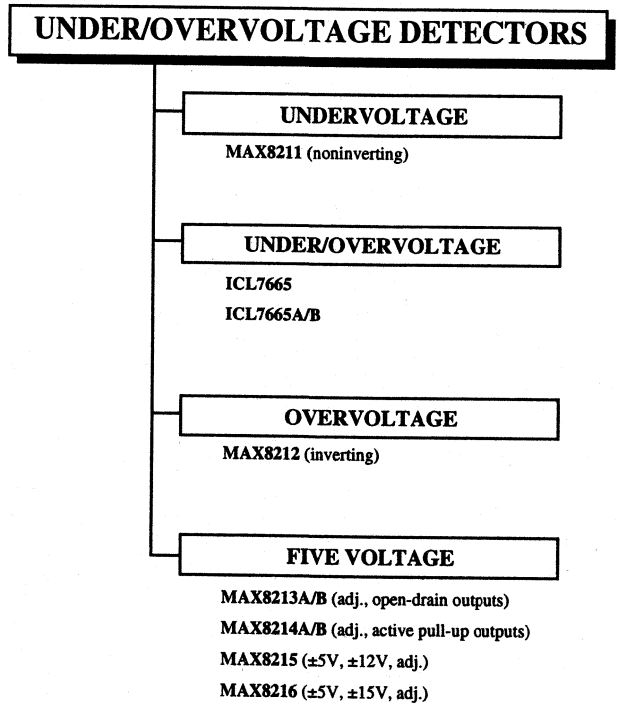
* Not all parts have suffix indicator for trip thresholds.
See *µP Supervisory Circuits* table and data sheets for specific information.

★ **New product**
† **Future product**

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	$\overline{RESET}$ Valid to V_{CC} = 1V	Nominal Watchdog Timeout Period (sec), if Available	Separate Watchdog Output	Backup-Battery Switch	V_{CC}-to-V_{OUT} On Resistance Max (Ω)	V_{BATT}-to-V_{OUT} On Resistance Max (Ω)	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual-Reset Input	Low-Line Output	Battery-On Output	I_{SUPPLY} Operating Mode mA max (typ)	I_{SUPPLY} Backup Mode mA max (typ)	Pins	Price† 1000-up ($)
MAX1232	4.37/4.62	250	✔	✔	✔	0.15/0.6/1.2							✔			0.2(0.05)		8	1.71
MAX690A/692A	4.65/4.40	140	✔		✔	1.6		✔	10	400		✔				0.35(0.2)	5(0.05)	8	3.26
MAX690R/S/T	2.63/2.93/3.08	140	✔		✔	1.6		✔	6	400		✔				0.5(0.4)	1µA(0.4µA)	8	3.23
MAX691A/693A	4.65/4.40	140/adj.	✔	✔	✔	1.6/adj.	✔	✔	1.2	25	✔/10ns	✔			✔	0.1(0.035)	5(0.04)	16	3.61
MAX1691	The MAX1691 is a module with the MAX691A and a 125mAh lithium battery																	16	††
MAX696	Adj.	35/adj.	✔	✔		1.6/adj.	✔	✔				✔			✔			16	3.55
MAX697	Adj.	35/adj.	✔	✔		1.6/adj.	✔				✔	✔						16	3.58
MAX700	4.65/adj.	200	✔	✔									✔			0.2(0.1)		8	2.17
MAX703/704	4.65/4.40	140	✔		✔			✔	10	400		✔	✔			0.35(0.2)	3(0.05)	8	1.38*
MAX704R/S/T	2.63/2.93/3.08	140	✔		✔			✔	6	400		✔	✔			0.5(0.4)	1µA(0.4µA)	8	2.93
MAX705/706	4.65/4.40	140	✔		✔	1.6	✔					✔	✔			0.35(0.2)		8	1.02*
MAX706P	2.63	140		✔	✔	1.6	✔					✔	✔			0.35(0.2)		8	1.71
MAX706R/S/T	2.63/2.93/3.08	140	✔		✔	1.6	✔					✔	✔			0.35(0.2)		8	1.71
MAX707/708	4.65/4.40	140	✔	✔	✔							✔	✔			0.35(0.2)		8	0.88*
MAX708R/S/T	2.63/2.93/3.08	140	✔	✔	✔							✔	✔			0.35(0.2)		8	1.63
MAX709L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔		✔											0.085(0.035)		8	0.70*
MAX791	4.65	140	✔	✔	✔	1	✔	✔	1.2	25	✔/10ns	✔	✔	✔	✔	0.15(0.06)	5(0.04)	16	3.90
MAX792L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔	✔	1	✔				✔/10ns	✔	✔	✔		0.15(0.07)		16	3.48
MAX793R/S/U/T	2.63/2.93/3.07/3.08	140	✔	✔	✔	1.6	✔	✔	TBD	TBD	✔	✔	✔	✔		TBD	TBD	16	††
MAX794	Adj.	140	✔	✔	✔	1.6	✔	✔	TBD	TBD	✔	✔	✔	✔		TBD	TBD	16	††
MAX795R/S/U/T	2.63/2.93/3.07/3.08	140	✔		✔			✔	TBD	TBD	✔			✔		TBD	TBD	8	††
MAX800L/M‡	4.60/4.40	140	✔	✔	✔	1.6/adj.	✔	✔	1.2	25	✔/10ns	✔/±2%			✔	0.1(0.035)	5(0.04)	16	3.88
MAX801L/N/M	4.68/4.58/4.43	140	✔/±1.5%		✔	1.6		✔	TBD	TBD		✔				TBD	TBD	8	††
MAX802L/M/R/S/T	4.60/4.40/ 2.63/2.93/3.08	140	✔		✔	1.6		✔	10	400		✔/±2%				0.35(0.2)	5(0.05)	8	3.59
MAX804R/S/T	2.63/2.93/3.08	140		✔	✔	1.6		✔	6	400		✔/±2%				0.5(0.4)	1µA(0.4µA)	8	3.66
MAX805L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✔	✔	1.6		✔	10	400		✔				0.35(0.2)	5(0.05)	8	3.04
MAX806R/S/T	2.63/2.93/3.08	140	✔	✔	✔			✔	6	400		✔/±2%	✔			0.5(0.4)	1µA(0.4µA)	8	3.90
MAX807L/N/M	4.68/4.58/4.43	140	✔/±1.5%	✔/±1.5%	✔	1.6	✔	✔	TBD	TBD	✔	✔	✔	✔	✔	TBD	TBD	8	††
MAX808L/N/M	4.68/4.58/4.43	140	✔/±1.5%		✔			✔	TBD	TBD	✔			✔		TBD	TBD	16	††
MAX809L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔		✔											TBD		3	††
MAX810L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✔	✔											TBD		3	††
MAX813L	4.65	140		✔	✔	1.6	✔					✔/±2%	✔			0.35(0.2)		8	1.02*
MAX814K/L/N/T	4.80/4.70/4.55/3.03	140	✔/±1%	✔/±1%	✔							✔/±2%	✔	✔		TBD	TBD	8	††
MAX815K/L/N/T	4.80/4.70/4.55/3.03	140	✔/±1%		✔	1.6	✔					✔/±2%	✔			TBD	TBD	8	††
MAX816	Adj./±1%	140	✔	✔	✔							✔/±2%	✔			TBD	TBD	8	††
MAX820L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔	✔	1	✔				✔/10ns	✔/±2%	✔	✔		0.15(0.07)		16	3.82
MXD1210	4.37/4.62							✔	2.5	667	✔					0.5(0.23)	0.1(0.002)	8	2.44

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.
* 25,000 pc. price, factory direct

UNDER/OVERVOLTAGE DETECTORS



Part Number	Supply Voltage (V)	Supply Current (µA), max(typ)	Threshold Accuracy (%)	Package Options*	Temp. Ranges**	Description	Price† 1000-up ($)
MAX8211	+2.0 to +16.5	15(5)	±3.5	DIP,SO,TO-8	C,E,M	Single channel: noninverting	1.33
MAX8212	+2.0 to +16.5	15(5)	±3.5	DIP,SO,TO-8	C,E,M	Single channel: inverting	1.33
MAX8213A	+2.7 to +11	33(16)	±1	DIP,SO	C,E,M	5 voltage monitors, open-drain outputs	2.88
MAX8213B	+2.7 to +11	33(16)	±2	DIP,SO	C,E,M	5 voltage monitors, open-drain outputs	1.98
MAX8214A	+2.7 to +11	33(16)	±1	DIP,SO	C,E,M	5 voltage monitors, active pull-up outputs	2.88
MAX8214B	+2.7 to +11	33(16)	±2	DIP,SO	C,E,M	5 voltage monitors, active pull-up outputs	1.98
MAX8215	+2.7 to +11	250(137)	±1.25	DIP,SO	C,E,M	5 voltage monitors: ±5V, ±12V, adjustable	1.98
MAX8216	+2.7 to +11	250(137)	±1.25	DIP,SO	C,E,M	5 voltage monitors: ±5V, ±15V, adjustable	1.98
ICL7665A	+2.0 to +16	10(2.5)	±1.9	DIP,SO,TO-8	C,E	Dual channel: one inverting, one noninverting	2.03

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-8 = Can
** Temp Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Integrated µP Supervisory Module with Lithium Backup Battery

General Description

The MAX1691 reduces the complexity and number of components required for power-supply monitoring and battery control functions in microprocessor (µP) systems. The MAX1691 features switchover to an internal backup battery, write protection of CMOS RAM or EEPROM, and a watchdog function.

The internal 3V, 125mAh lithium battery connects to the µP supervisory circuit through external pin strapping, minimizing battery drain during shipping.

The MAX1691 is shipped in special nonconductive material. **Note: Storing the MAX1691 in conductive foam will discharge the internal battery.**

Features

- ♦ **Internal 3V, 125mAh Lithium Battery**
- ♦ **200ms Power OK/Reset Time Delay**
- ♦ **1µA Standby Current, 35µA Operating Current**
- ♦ **On-Board Gating of Chip-Enable Signals, 10ns Max Delay**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **16-Pin, 0.6" Plastic DIP Module**

Applications

Computers

Controllers

Intelligent Instruments

Automotive Systems

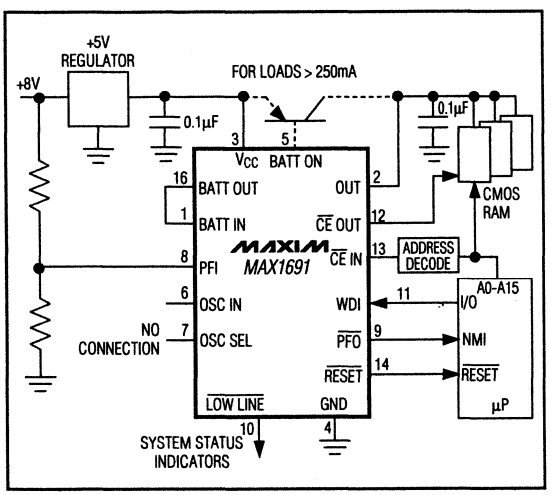
Critical µP Power Monitoring

Ordering Information

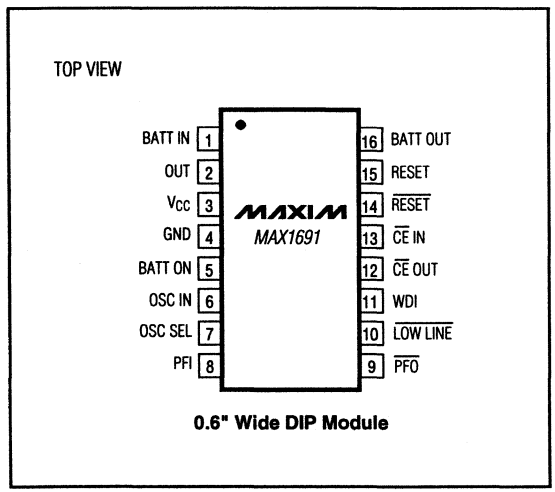
PART	TEMP. RANGE	PIN-PACKAGE
MAX1691CHE	0°C to +70°C	16 Plastic 0.6" Wide DIP Module

5

Typical Operating Circuit



Pin Configuration



0.6" Wide DIP Module

19-4333; Rev 3; 12/93

MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX690A/MAX692A/MAX802L/MAX802M/MAX805L reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

These parts provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µP, or other low-power logic.
3) A reset pulse if the optional watchdog timer has not been toggled within 1.6sec.
4) A 1.25V threshold detector for power-fail warning or low-battery detection, or to monitor a power supply other than +5V.

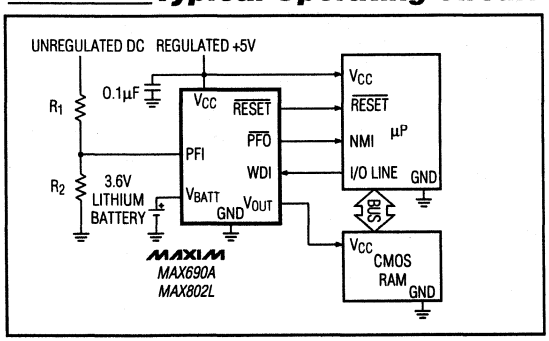
The parts differ in their reset-voltage threshold levels and reset outputs. The MAX690A/MAX802L/MAX805L generate a reset pulse when the supply voltage drops below 4.65V, and the MAX692A/MAX802M generate a reset below 4.40V. The MAX802L/MAX802M guarantee power-fail accuracies to ±2%. The MAX805L is the same as the MAX690A except that RESET is provided instead of $\overline{\text{RESET}}$.

All parts are available in 8-pin DIP and SO packages. The MAX690A/MAX802L are pin compatible with the MAX690 and MAX694. The MAX692A/MAX802M are pin compatible with the MAX692.

Applications

Battery-Powered Computers and Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

- ♦ **Precision Supply-Voltage Monitor: 4.65V for MAX690A/MAX802L/MAX805L 4.40V for MAX692A/MAX802M**
- ♦ **Reset Time Delay – 200ms**
- ♦ **Watchdog Timer – 1.6sec Timeout**
- ♦ **Battery-Backup Power Switching**
- ♦ **200µA Quiescent Supply Current**
- ♦ **50nA Quiescent Supply Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Power-Fail Accuracy Guaranteed to ±2% (MAX802L/M)**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**
- ♦ **8-Pin SO and DIP Packages**

Ordering Information

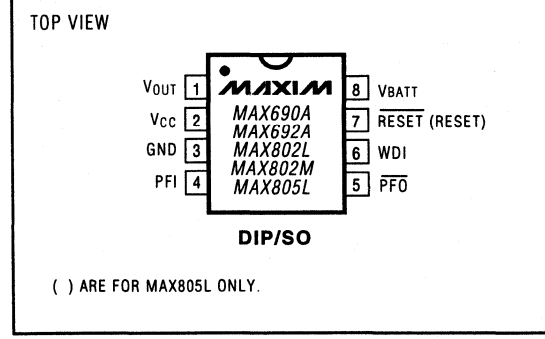
PART	TEMP. RANGE	PIN-PACKAGE
MAX690ACPA	0°C to +70°C	8 Plastic DIP
MAX690ACSA	0°C to +70°C	8 SO
MAX690AC/D	0°C to +70°C	Dice*
MAX690AEPA	-40°C to +85°C	8 Plastic DIP
MAX690AESA	-40°C to +85°C	8 SO
MAX690AMJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

* *Dice are specified at T_A = +25°C*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10sec
- All Other Outputs 20mA

Rate of Rise, V_{CC}, V_{BATT} 100V/µs

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX69_AC_ _, MAX80_ _ C_ _ ..... 0°C to +70°C
- MAX69_AE_ _, MAX80_ _ E_ _ ..... -40°C to +85°C
- MAX69_AMJA, MAX805LMJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI and WDI may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V for MAX690A/MAX802L/MAX805L, V_{CC} = 4.5V to 5.5V for MAX692A/MAX802M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 2)		MAX69_AC, MAX802_C		1.0		5.5	V
		MAX805LC		1.1		5.5	
		MAX69_AE/M, MAX80_ _E		1.2		5.5	
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX69_AC, MAX802_C			200	350	µA
		MAX69_AE/M, MAX802_E, MAX805LE/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
V_{BATT} Standby Current (Note 3)		5.5V > V_{CC} > V_{BATT} +0.2V	T_A = +25°C	-0.1		0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05		V_{CC} - 0.025	V
		I_{OUT} = 50mA		V_{CC} - 0.5		V_{CC} - 0.25	
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1		V_{BATT} - 0.02	V
Battery Switch Threshold, V_{CC} to V_{BATT}		V_{CC} < V_{RT}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV
Reset Threshold	V_{RT}	MAX690A, MAX802L, MAX805L		4.50	4.65	4.75	V
		MAX692A, MAX802M		4.25	4.40	4.50	
		MAX802L, T_A = +25°C, V_{CC} falling		4.55		4.70	
		MAX802M, T_A = +25°C, V_{CC} falling		4.30		4.45	
Reset Threshold Hysteresis					40		mV
Reset Pulse Width	t_{RS}			140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	
		MAX69_AC, MAX802_C, V_{CC} = 1.0V I_{SINK} = 50µA				0.3	
		MAX69_AE/M, MAX802_E, V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V for MAX690A/MAX802L/MAX805L, V_{CC} = 4.5V to 5.5V for MAX692A/MAX802M, V_{BATT} = 2.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET Output Voltage		MAX805LC, I_{SOURCE} = 4µA, V_{CC} = 1.1V		0.8			V
		MAX805LE/M, I_{SOURCE} = 4µA, V_{CC} = 1.2V		0.9			
		MAX805L, I_{SOURCE} = 800µA		V_{CC} - 1.5			
		MAX805L, I_{SINK} = 3.2mA				0.4	
Watchdog Timetout	t_{WD}			1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (0.8) (V_{CC})		50			ns
WDI Input Threshold (Note 4)		V_{CC} = 5V	Logic low			0.8	V
			Logic high	3.5			
WDI Input Current		WDI = V_{CC}			50	150	µA
		WDI = 0V		-150	-50		
PFI Input Threshold		MAX69_A, MAX805L, V_{CC} = 5V		1.20	1.25	1.30	V
		MAX802_C/E, V_{CC} = 5V		1.225	1.250	1.275	
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	

Note 2: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.

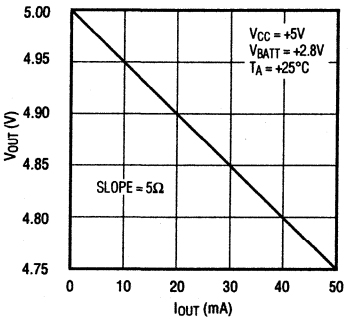
Note 3: "-" = battery-charging current, "+" = battery-discharging current.

Note 4: WDI is guaranteed to be in an intermediate, non-logic level state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 35% of V_{CC} with an input impedance of 50kΩ.

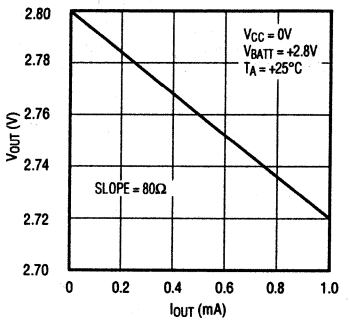
Microprocessor Supervisory Circuits

Typical Operating Characteristics

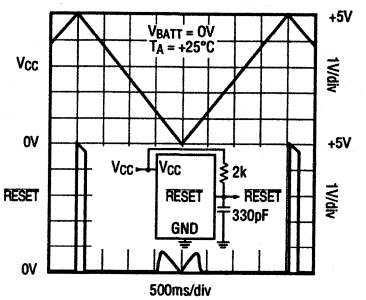
OUTPUT VOLTAGE vs. LOAD CURRENT



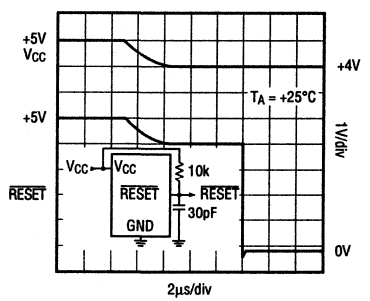
OUTPUT VOLTAGE vs. LOAD CURRENT



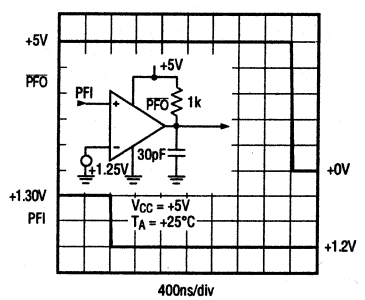
MAX690A RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



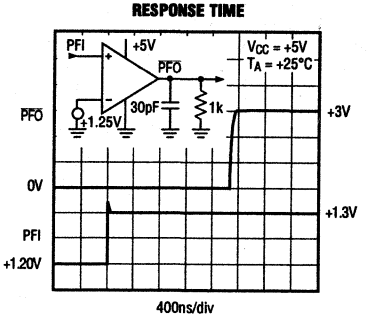
MAX690A RESET RESPONSE TIME



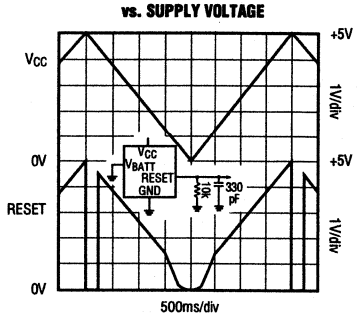
POWER-FAIL COMPARATOR RESPONSE TIME



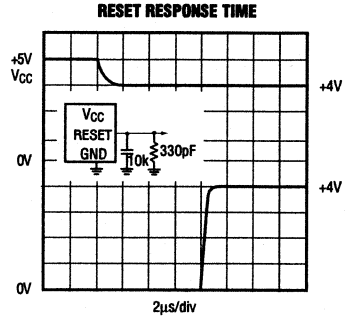
POWER-FAIL COMPARATOR RESPONSE TIME



MAX805L RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



MAX805L RESET RESPONSE TIME



Pin Description

PIN		NAME	FUNCTION
MAX690A/MAX692A MAX802L/MAX802M	MAX805L		
1	1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a P-channel MOSFET switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or V_{BATT} will be connected to V_{OUT}.
2	2	V_{CC}	+5V Supply Input
3	3	GND	Ground
4	4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ stays high.
6	6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset is triggered. If WDI is left floating or connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7		$\overline{RESET}$	Reset Output. Whenever $\overline{RESET}$ is triggered, it pulses low for 200ms. It stays low when V_{CC} is below the reset threshold (4.65V in the MAX690A/MAX802L and 4.4V in the MAX692A/MAX802M) and remains low for 200ms after V_{CC} rises above the reset threshold. A watchdog timeout also triggers $\overline{RESET}$.
–	7	RESET	Active-High Reset Output is the inverse of $\overline{RESET}$. When RESET is asserted, the RESET output voltage = V_{CC} or V_{BATT}, whichever is higher.
8	8	V_{BATT}	Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} will be switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises to 20mV above V_{BATT}, V_{OUT} will be reconnected to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

Microprocessor Supervisory Circuits

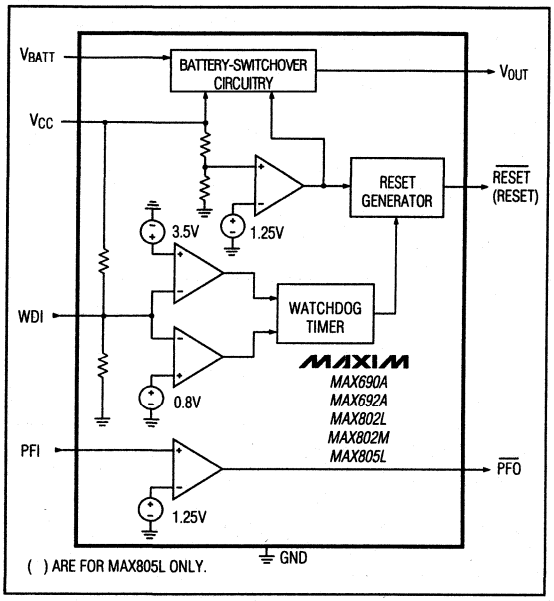


Figure 1. Block Diagram

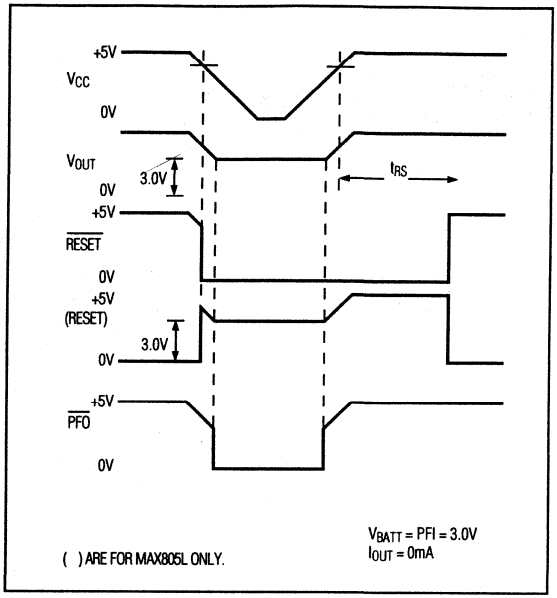


Figure 2. Timing Diagram

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. When the µP is in an unknown state, it should be held in reset. The MAX690A/MAX692A/MAX802L/MAX802M assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for a time equal to the reset pulse width; after this interval, $\overline{RESET}$ goes high (Figure 2). If a brownout condition occurs (if V_{CC} dips below the reset threshold), $\overline{RESET}$ is triggered. Each time $\overline{RESET}$ is triggered, it stays low for the reset pulse width interval. Any time V_{CC} goes below the reset threshold, the internal timer restarts the pulse. If a brownout condition interrupts a previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once V_{CC} goes below the threshold, $\overline{RESET}$ is guaranteed to be logic low until V_{CC} droops below 1V.

$\overline{RESET}$ is also triggered by a watchdog timeout. If a high or low is continuously applied to the WDI pin for 1.6sec, $\overline{RESET}$ pulses low. As long as $\overline{RESET}$ is asserted, the watchdog timer remains clear. When $\overline{RESET}$ comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8sec (t_{WD} plus t_{RS}).

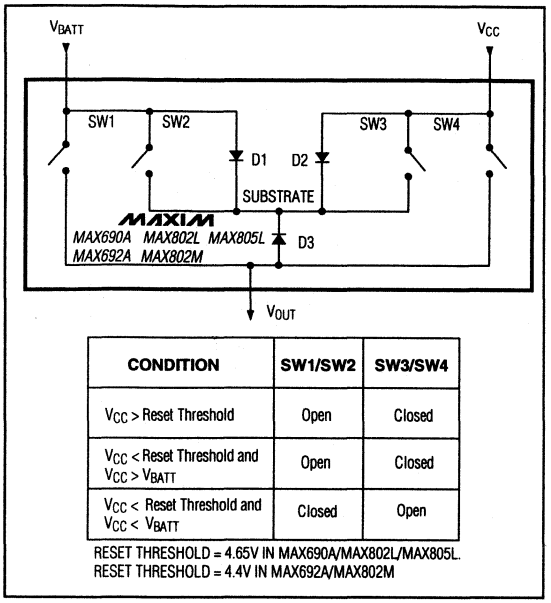
The MAX805L active-high RESET output is the inverse of the MAX690A/MAX692A/MAX802L/MAX802M $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by open circuiting the WDI input. As long as reset is asserted or the WDI input is open circuited, the timer remains cleared and does not count. As soon as reset is released or WDI is driven high or low, the timer starts counting. It can detect pulses as short as 50ns.

Power-Fail Comparator

The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply; it need not be dedicated to this function though, as it is



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and V_{CC} > V_{BATT}	Open	Closed
V_{CC} < Reset Threshold and V_{CC} < V_{BATT}	Closed	Open

RESET THRESHOLD = 4.65V IN MAX690A/MAX802L/MAX805L.
RESET THRESHOLD = 4.4V IN MAX692A/MAX802M

Figure 3. Backup-Battery Switchover Block Diagram

completely separate from the rest of the circuitry. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator (see *Typical Operating Circuit*). The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{PFO}$ then triggers an interrupt which signals the µP to prepare for power-down.

To conserve backup-battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced low when V_{BATT} connects to V_{OUT}.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the devices automatically switch RAM to backup power when V_{CC} fails.

As long as V_{CC} exceeds the reset threshold, V_{OUT} connects to V_{CC} through a 5Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT} (whichever is higher) switches to V_{OUT}. Unlike the MAX690/MAX692, the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L don't always connect V_{BATT} to V_{OUT} when V_{BATT} is greater than V_{CC}. V_{BATT} connects to V_{OUT} (through an 80Ω switch) only when V_{CC} is below the reset threshold **and** V_{BATT} is greater than V_{CC}.

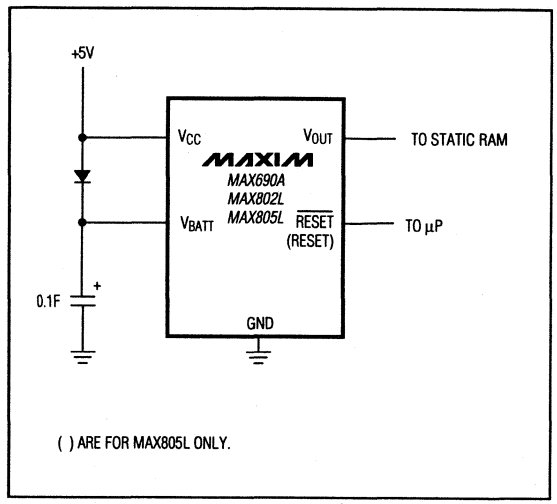


Figure 4. Using a SuperCap as a Backup Power Source with a MAX690A/MAX802L/MAX805L and a +5V±5% Supply

When V_{CC} exceeds the reset threshold, it is connected to the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L substrate, regardless of the voltage applied to V_{BATT} (Figure 3). During this time, the diode (D1) between V_{BATT} and the substrate will conduct current from V_{BATT} to V_{CC} if V_{BATT} is 0.6V or greater than V_{CC}.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}
V_{OUT}	Connected to V_{BATT} through an internal 80Ω PMOS switch
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 1µA, as long as V_{CC} < V_{BATT} - 1V.
PFI	Power-fail comparator is disabled.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
RESET	Logic high (MAX805L only)
WDI	Watchdog timer is disabled

Microprocessor Supervisory Circuits

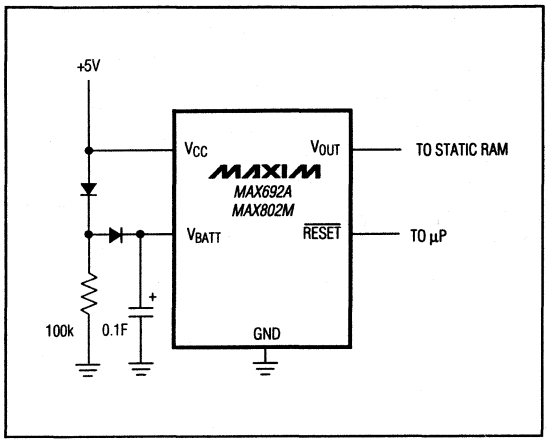


Figure 5. Using a SuperCap™ as a Backup Power Source with the MAX692A/MAX802M and a +5V ± 10% Supply

When V_{BATT} connects to V_{OUT}, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When V_{CC} is just below V_{BATT}, the current drawn from V_{BATT} is typically 30µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Applications Information

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values, on the order of 0.1F. Figure 4 shows a SuperCap used as a backup power source. Do not allow the SuperCap's voltage to exceed the maximum reset threshold by more than 0.6V. In Figure 4's circuit, the SuperCap rapidly charges to within a diode drop of V_{CC}. However, after a long time, the diode leakage current will pull the SuperCap voltage up to V_{CC}. When using a SuperCap with the MAX690A/MAX802L/MAX805L, V_{CC} may not exceed 4.75V + 0.6V = 5.35V.

Use the SuperCap circuit of Figure 5 with a MAX692A or MAX802M and a ±10% supply. This circuit ensures that the SuperCap only charges to V_{CC} - 0.5V. At the maximum V_{CC} of 5.5V, the SuperCap charges up to 5.0V, only 0.5V above the maximum reset threshold—well within the requisite 0.6V.

™SuperCap is a trademark of Baknor Industries.

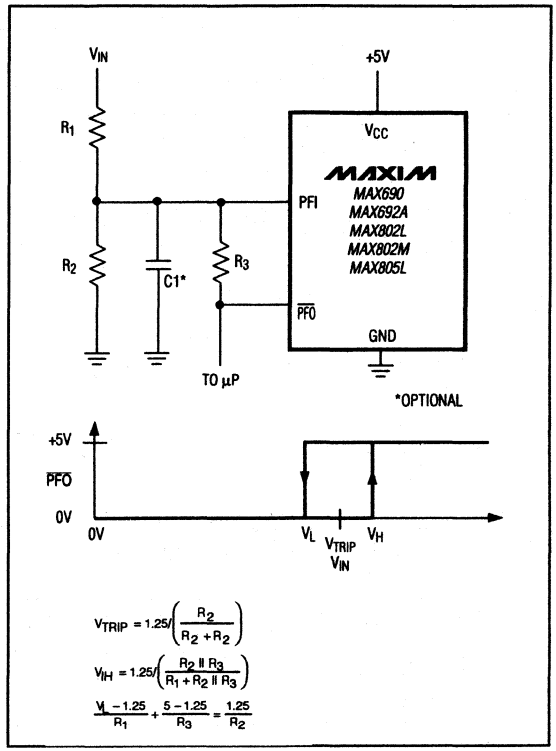


Figure 6. Adding Hysteresis to the Power-Fail Comparator

Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rates and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the V_{BATT} input of the MAX690A/MAX692A/MAX802L/MAX802M/MAX805L with

Table 2. Allowable Backup-Battery Voltages
(see *Using a SuperCap as a Backup Power Source* section for use with a SuperCap)

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX690A/ MAX802L/MAX805L	4.80
MAX692A/ MAX802M	4.55

no additional circuitry (see the *Typical Operating Circuit*). However, batteries with open-circuit voltages that are greater **cannot** be used for backup, as current is sourced into the substrate through the diode (D1 in Figure 3) when V_{CC} is close to the reset threshold.

Operation Without a Backup Power Source

If a backup power source is not used, ground V_{BATT} and connect V_{OUT} to V_{CC}. Since there is no need to switch over to any backup power source, V_{OUT} does not need to be switched. A direct connection to V_{CC} eliminates any voltage drops across the switch which may push V_{OUT} below V_{CC}.

Replacing the Backup Battery

The backup battery can be removed while V_{CC} remains valid, without danger of triggering RESET/$\overline{\text{RESET}}$. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered. In other switchover ICs where battery-backup mode is entered whenever V_{BATT} gets close to V_{CC}, an unconnected V_{BATT} pin accumulates leakage charge and triggers RESET/$\overline{\text{RESET}}$ in error.

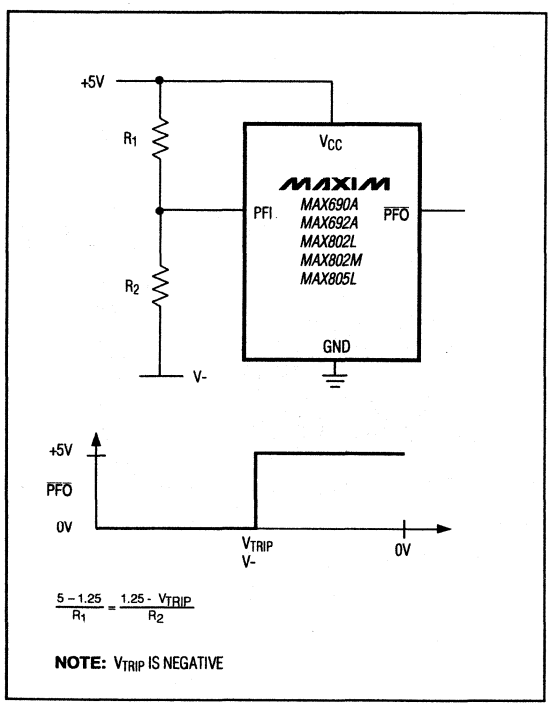


Figure 7. Monitoring a Negative Voltage

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when V_{IN} is close to its trip point. Figure 6 shows how to add hysteresis to the power-fail comparator. Select the ratio of R_1 and R_2 such that PFI sees 1.25V when V_{IN} falls to its trip point (V_{TRIP}). R_3 adds the hysteresis. It will typically be an order of magnitude greater than R_1 or R_2 (about 10 times either R_1 or R_2). The current through R_1 and R_2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R_3 should be larger than 10kΩ so it does not load down the $\overline{\text{PFO}}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply rail using the circuit of Figure 7. When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low. When the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} line, and the resistors.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX690A/MAX692A/MAX802L/MAX802M $\overline{\text{RESET}}$ output. If, for example, the $\overline{\text{RESET}}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{\text{RESET}}$ output and the µP reset I/O, as in Figure 8. Buffer the $\overline{\text{RESET}}$ output to other system components

Microprocessor Supervisory Circuits

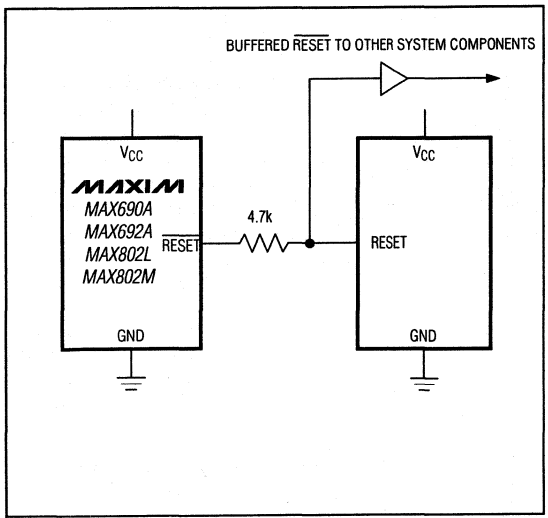


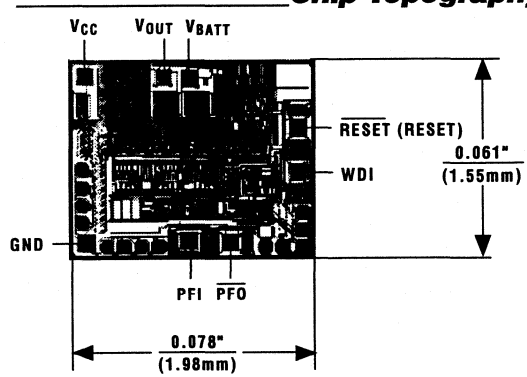
Figure 8. Interfacing to µPs with Bidirectional Reset I/O

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX692ACPA	0°C to +70°C	8 Plastic DIP
MAX692ACSA	0°C to +70°C	8 SO
MAX692AC/D	0°C to +70°C	Dice*
MAX692AEPA	-40°C to +85°C	8 Plastic DIP
MAX692AESA	-40°C to +85°C	8 SO
MAX692AMJA	-55°C to +125°C	8 CERDIP**
MAX802LCPA	0°C to +70°C	8 Plastic DIP
MAX802LCSA	0°C to +70°C	8 SO
MAX802LEPA	-40°C to +85°C	8 Plastic DIP
MAX802LESA	-40°C to +85°C	8 SO
MAX802MCPA	0°C to +70°C	8 Plastic DIP
MAX802MCSA	0°C to +70°C	8 SO
MAX802MEPA	-40°C to +85°C	8 Plastic DIP
MAX802MESA	-40°C to +85°C	8 SO
MAX805LCPA	0°C to +70°C	8 Plastic DIP
MAX805LCSA	0°C to +70°C	8 SO
MAX805LC/D	0°C to +70°C	Dice*
MAX805LEPA	-40°C to +85°C	8 Plastic DIP
MAX805LESA	-40°C to +85°C	8 SO
MAX805LMJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



( ) ARE FOR MAX805L ONLY.
TRANSISTOR COUNT: 573;
SUBSTRATE MUST BE LEFT UNCONNECTED.

19-0243; Rev 0; 3/94

MAXIM

3.0V/3.3V Microprocessor Supervisory Circuits

General Description

These microprocessor (µP) supervisory circuits reduce the complexity and number of components required for power-supply monitoring and battery-control functions in µP systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

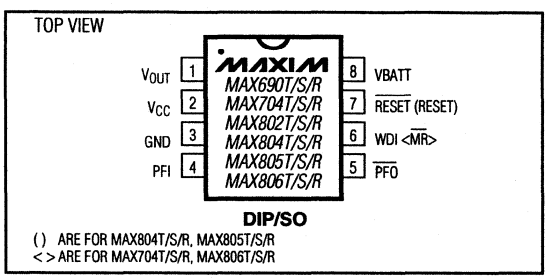
These devices are designed for use in systems powered by 3.0V or 3.3V supplies. See the selector guide in the back of this data sheet for similar devices designed for 5V systems. The suffixes denote different reset threshold voltages: 3.075V (T), 2.925V (S), and 2.625V (R) (see *Reset Threshold* section in the *Detailed Description*). All these parts are available in 8-pin DIP and SO packages. Functions offered in this series are as follows:

Part	Active-Low Reset	Active-High Reset	Watchdog Input	Manual Reset Input	Backup-Battery Switch	Threshold Accuracy	Power-Fail Comparator	Power-Fail Reset Window
MAX690	✓		✓		✓	±4%	✓	±75mV
MAX704	✓			✓	✓	±4%	✓	±75mV
MAX802	✓		✓		✓	±2%	✓	±2%
MAX804		✓	✓		✓	±2%	✓	±2%
MAX805		✓	✓		✓	±4%	✓	±75mV
MAX806	✓			✓	✓	±2%	✓	±2%

Applications

Battery-Powered Computers and Controllers
Embedded Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring
Portable Equipment

Pin Configuration



Features

- ♦ **RESET and RESET Outputs**
- ♦ **Manual Reset Input**
- ♦ **Precision Supply-Voltage Monitor**
- ♦ **200ms Reset Time Delay**
- ♦ **Watchdog Timer (1.6sec timeout)**
- ♦ **Battery-Backup Power Switching—Battery Can Exceed V_{CC} in Normal Operation**
- ♦ **40µA V_{CC} Supply Current**
- ♦ **1µA Battery Supply Current**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Guaranteed RESET Assertion to V_{CC} = 1V**
- ♦ **8-Pin DIP and SO Packages**

Ordering Information

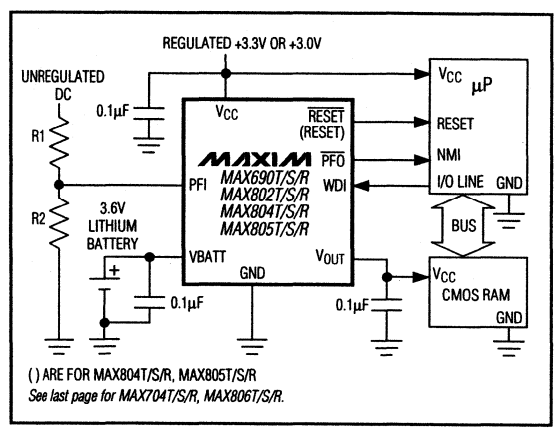
PART**	TEMP. RANGE	PIN-PACKAGE
MAX690_CPA	0°C to +70°C	8 Plastic DIP
MAX690_CSA	0°C to +70°C	8 SO
MAX690_C/D	0°C to +70°C	Dice*
MAX690_EPA	-40°C to +85°C	8 Plastic DIP
MAX690_ESA	-40°C to +85°C	8 SO
MAX690_MJA	-55°C to +125°C	8 CERDIP

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *These parts offer a choice of reset threshold voltage. Select the letter corresponding to the desired nominal reset threshold voltage (T = 3.075V, S = 2.925V, R = 2.625V) and insert it into the blank to complete the part number.*

Typical Operating Circuits



ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- VBATT ..... -0.3V to 6.0V

All Other Inputs ..... -0.3V to the higher of V_{CC} or VBATT

Continuous Input Current
- V_{CC} 100mA
- VBATT 18mA
- GND 18mA

Output Current
- $\overline{RESET}$, PFO 18mA
- V_{OUT} 100mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
- MAX690_C_ _/MAX704_C_ _/MAX80_ _C_ _ ..... 0°C to +70°C
- MAX690_E_ _/MAX704_E_ _/MAX80_ _E_ _ ..... -40°C to +85°C
- MAX690_M_ _/MAX704_M_ _/MAX80_ _M_ _ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80_T, V_{CC} = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80_S, V_{CC} = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80_R; VBATT = 3.6V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, VBATT (Note 1)		MAX690_C, MAX704_C, MAX80_ _C		1.0		5.5	V
		MAX690_E/M, MAX704_E/M, MAX80_ _E/M		1.1		5.5	
V_{CC} Supply Current (excluding I_{OUT})	I_{SUPPLY}	$\overline{MR}$ = V_{CC} (MAX704_/ MAX806_)	MAX690_C/E, MAX704_C/E, MAX80_ _C/E, V_{CC} < 3.6V		40	50	µA
			MAX690_C/E, MAX704_C/E, MAX80_ _C/E, V_{CC} < 5.5V		50	65	
			MAX690_M, MAX704_M, MAX80_ _M, V_{CC} < 3.6V		40	55	
			MAX690_M, MAX704_M, MAX80_ _M, V_{CC} < 5.5V		50	70	
V_{CC} Supply Current in Battery-Backup Mode (excluding I_{OUT})		$\overline{MR}$ = V_{CC} (MAX704_/ MAX806_)	V_{CC} = 2.0V, VBATT = 2.3V		25	50	µA
VBATT Supply Current, Any Mode (excluding I_{OUT}) (Note 2)		MAX690_C/E, MAX704_C/E, MAX80_ _C/E			0.4	1	µA
		MAX690_M, MAX704_M, MAX80_ _M			0.4	10	
Battery Leakage Current (Note 3)		MAX690_C/E, MAX704_C/E, MAX80_ _C/E			0.01	0.5	µA
		MAX690_M, MAX704_M, MAX80_ _M			0.01	5	
V_{OUT} Output Voltage		MAX690_C/E, MAX704_C/E, MAX80_ _C/E, I_{OUT} = 5mA (Note 4)		V_{CC} - 0.03	V_{CC} - 0.015		V
		MAX690_C/E, MAX704_C/E, MAX80_ _C/E I_{OUT} = 50mA		V_{CC} - 0.3	V_{CC} - 0.15		
		MAX690_M, MAX704_M, MAX80_ _M I_{OUT} = 5mA (Note 4)		V_{CC} - 0.035	V_{CC} - 0.015		
		MAX690_M, MAX704_M, MAX80_ _M I_{OUT} = 50mA		V_{CC} - 0.35	V_{CC} - 0.15		
		I_{OUT} = 250µA, V_{CC} > 2.5V (Note 4)		V_{CC} - 0.0015	V_{CC} - 0.0006		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80_T, V_{CC} = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80_S, V_{CC} = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80_R; VBATT = 3.6V; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, VBATT = 2.3V		VBATT - 0.1	VBATT - 0.034		V
		I_{OUT} = 1mA, VBATT = 2.3V			VBATT - 0.14		
Battery Switch Threshold, V_{CC} Falling		VBATT - V_{CC}, V_{SW} > V_{CC} > 1.75V (Note 5)		65	25		mV
	V_{SW}	VBATT > V_{CC} (Note 6)		2.30	2.40	2.50	V
Battery Switch Threshold, V_{CC} Rising (Note 7)		This value is identical to the reset threshold, V_{CC} rising					V
Reset Threshold (Note 8)	V_{RST}	MAX690T/704T/805T	V_{CC} falling	3.00	3.075	3.15	V
			V_{CC} rising	3.00	3.085	3.17	
		MAX802T/804T/806T	V_{CC} falling	3.00	3.075	3.12	
			V_{CC} rising	3.00	3.085	3.14	
		MAX690S/704S/805S	V_{CC} falling	2.85	2.925	3.00	
			V_{CC} rising	2.85	2.935	3.02	
		MAX802S/804S/806S	V_{CC} falling	2.88	2.925	3.00	
			V_{CC} rising	2.88	2.935	3.02	
		MAX690R/704R/805R	V_{CC} falling	2.55	2.625	2.70	
			V_{CC} rising	2.55	2.635	2.72	
		MAX802R/804R/806S	V_{CC} falling	2.59	2.625	2.70	
			V_{CC} rising	2.59	2.635	2.72	
Reset Timeout Period	t_{WP}	V_{CC} < 3.6V		140	200	280	ms
$\overline{PFO}$, $\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 50µA		V_{CC} - 0.3	V_{CC} - 0.05		V
$\overline{PFO}$, $\overline{RESET}$ Output Short to GND Current (Note 4)	I_{OS}	V_{CC} = 3.3V, V_{OH} = 0V			180	500	µV
$\overline{PFO}$, $\overline{RESET}$, RESET Output Voltage	V_{OL}	I_{SINK} = 1.2mA; MAX690_/704_/802_/806_, V_{CC} = V_{RST} min; MAX804_/805_, V_{CC} = V_{RST} max			0.06	0.3	V
$\overline{PFO}$, $\overline{RESET}$ Output Voltage	V_{OL}	VBATT = 0V, V_{CC} = 1.0V, I_{SINK} = 40µA, MAX690_C, MAX704_C, MAX80_ _C			0.13	0.3	V
		VBATT = 0V, V_{CC} = 1.2V, I_{SINK} = 200µA, MAX690_E/M, MAX704_E/M, MAX80_ _E/M			0.17	0.3	
RESET Output Leakage Current (Note 9)		VBATT = 0V, V_{CC} = V_{RST} min; V_{RESET} = 0V, V_{CC}	MAX804_C, MAX805_C	-1		1	µA
			MAX804_E/M, MAX805_E/M	-10		10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80_T, V_{CC} = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80_S, V_{CC} = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80_R; VBATT = 3.6V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PFI Input Threshold	V_{PFT}	V_{CC} < 3.6V V_{PFI} falling	MAX802_C/E, MAX804_C/E, MAX806_C/E	1.212	1.237	1.262	V
			MAX690_/MAX704_/MAX805_	1.187	1.237	1.287	
PFI Input Current		MAX690_C/E, MAX704_C/E, MAX80_ _C/E		-25	2	25	nA
		MAX690_M, MAX704_M, MAX80_ _M		-500	2	500	
PFI Hysteresis, PFI Rising	V_{PFH}	V_{CC} < 3.6V	MAX690_C/E, MAX704_C/E, MAX80_ _C/E		10	20	mV
			MAX690_M, MAX704_M, MAX80_ _M		10	25	
PFI Input Current		MAX690_C/E, MAX704_C/E, MAX80_ _C/E		-25	2	25	nA
		MAX690_M, MAX704_M, MAX80_ _M		-500	2	500	
$\overline{MR}$ Input Threshold	V_{IH}	MAX704_/MAX806_ only				0.7 x V_{CC}	V
	V_{IL}				0.3 x V_{CC}		
$\overline{MR}$ Pulse Width	t_{MR}	MAX704_/MAX806_ only		100	20		ns
$\overline{MR}$ to Reset Delay	t_{MD}	MAX704_/MAX806_ only			60	500	ns
$\overline{MR}$ Pull-Up Current		MAX704_/MAX806_ only, $\overline{MR}$ = 0V, V_{CC} = 3V		20	60	350	µA
WDI Input Threshold	V_{IH}	MAX690_/MAX802_/MAX804_/MAX805_ only				0.7 x V_{CC}	V
	V_{IL}				0.3 x V_{CC}		
WDI Input Current		0V< V_{CC} < 5.5V	MAX690_C/E, MAX802_C/E, MAX804_C/E, MAX805_C/E	-1	0.01	1	µA
			MAX690_M, MAX802_M, MAX804_M, MAX805_M	-10	0.01	10	
Watchdog Timeout Period	t_{WD}	V_{CC} < 3.6V	MAX690/MAX802/MAX804/ MAX805 only	1.12	1.60	2.24	sec
WDI Pulse Width		MAX690_/MAX802_/MAX804_/MAX805_ only		100	20		ns

Note 1: V_{CC} supply current, logic input leakage, watchdog functionality (MAX690_/802_/805_/804_), $\overline{MR}$ functionality (MAX704_/806_), PFI functionality, state of $\overline{RESET}$ (MAX690_/704_/802_/806_), and RESET (MAX804_/805_) tested at VBATT = 3.6V, and V_{CC} = 5.5V. The state of $\overline{RESET}$ or RESET and $\overline{PFO}$ is tested at V_{CC} = V_{CC} min.

Note 2: Tested at VBATT = 3.6V, V_{CC} = 3.5V and 0V. The battery current will rise to 10µA over a narrow transition window around V_{CC} = 1.9V.

Note 3: Leakage current into the battery is tested under the worst-case conditions at V_{CC} = 5.5V, VBATT = 1.8V and at V_{CC} = 1.5V, VBATT= 1.0V.

Note 4: Guaranteed by design.

Note 5: When V_{SW} > V_{CC} > VBATT, V_{OUT} remains connected to V_{CC} until V_{CC} drops below VBATT. The V_{CC}-to-VBATT comparator has a small 25mV typical hysteresis to prevent oscillation. For V_{CC} < 1.75V (typ), V_{OUT} switches to VBATT regardless of the voltage on VBATT.

Note 6: When VBATT > V_{CC} > V_{SW}, V_{OUT} remains connected to V_{CC} until V_{CC} drops below the battery switch threshold (V_{SW}).

Note 7: V_{OUT} switches from VBATT to V_{CC} when V_{CC} rises above the reset threshold, independent of VBATT. Switchover back to V_{CC} occurs at the exact voltage that causes $\overline{RESET}$ to go high (on the MAX804_/805_, RESET goes low); however switchover occurs 200ms prior to reset.

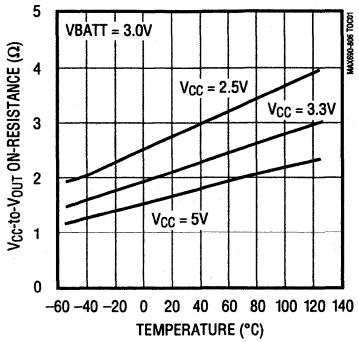
Note 8: The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

Note 9: The leakage current into or out of the RESET pin is tested with RESET asserted (RESET output high impedance).

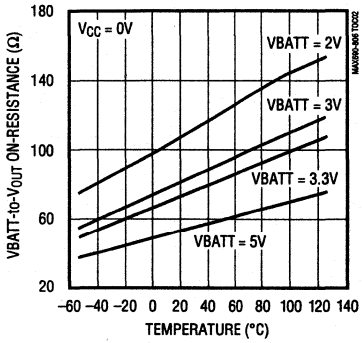
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

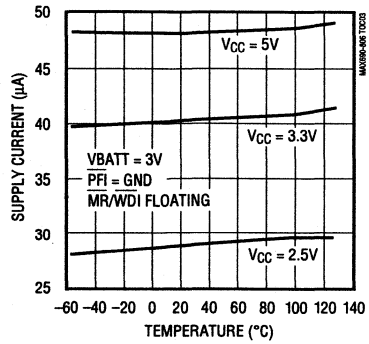
V_{CC}-to-V_{OUT} ON-RESISTANCE vs. TEMPERATURE



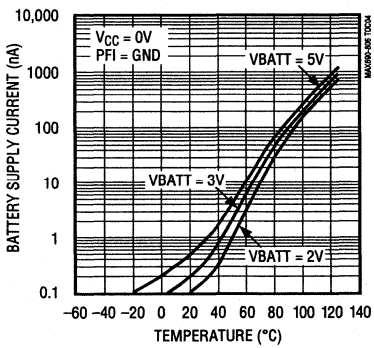
VBATT-to-V_{OUT} ON-RESISTANCE vs. TEMPERATURE



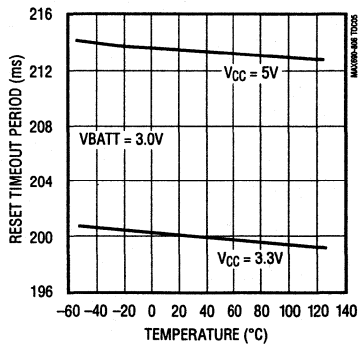
SUPPLY CURRENT vs. TEMPERATURE



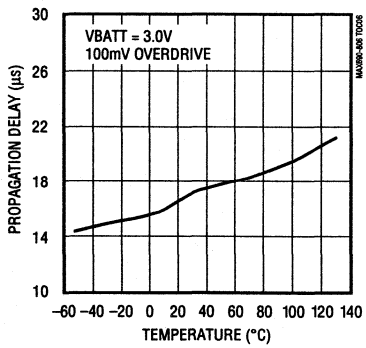
BATTERY SUPPLY CURRENT vs. TEMPERATURE



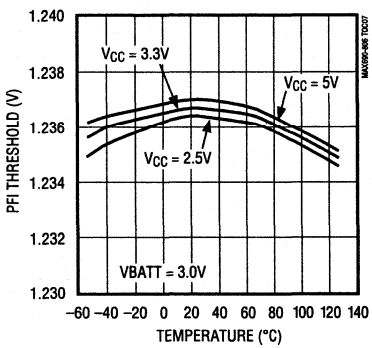
RESET TIMEOUT PERIOD vs. TEMPERATURE



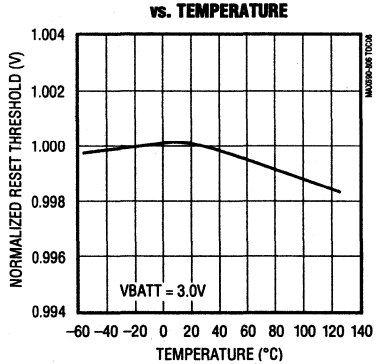
RESET-COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



PFI THRESHOLD vs. TEMPERATURE



NORMALIZED RESET THRESHOLD vs. TEMPERATURE



3.0V/3.3V Microprocessor Supervisory Circuits

Pin Description

PIN MAX690 MAX802	PIN MAX704 MAX806	PIN MAX804 MAX805	NAME	FUNCTION
1	1	1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} is connected to V_{CC} through a P-channel MOSFET switch. When V_{CC} falls below V_{SW} and VBATT, VBATT connects to V_{OUT}. Connect to V_{CC} if no battery is used.
2	2	2	V_{CC}	Main Supply Input
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Input. When PFI is less than V_{PFT} or when V_{CC} falls below V_{SW}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Connect to ground if unused.
5	5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than V_{PFT}, or V_{CC} falls below V_{SW}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Leave open if unused.
6	—	6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge. The watchdog function cannot be disabled.
—	6	—	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is low and for 200ms after $\overline{MR}$ returns high. This active-low input has an internal 70µA pull-up current. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.
7	7	—	$\overline{RESET}$	Active-Low Reset Output. Pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes from low to high.
—	—	7	RESET	Active-High, Open-Drain Reset Output is the inverse of $\overline{RESET}$.
8	8	8	VBATT	Backup-Battery Input. When V_{CC} falls below V_{SW} and VBATT, V_{OUT} switches from V_{CC} to VBATT. When V_{CC} rises above the reset threshold, V_{OUT} reconnects to V_{CC}. VBATT may exceed V_{CC}. Connect to GND if no battery is used.

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, brownout conditions, or a watchdog timeout.

$\overline{RESET}$ is guaranteed to be a logic low for $0V < V_{CC} < V_{RST}$, provided that VBATT is greater than 1V. Without a backup battery, $\overline{RESET}$ is guaranteed valid for $V_{CC} > 1V$. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period; after this interval, $\overline{RESET}$ goes high (Figure 2).

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts.

The watchdog timer can also initiate a reset. See the *Watchdog Input* section.

The MAX804_/MAX805_ active-high RESET output is open drain, and the inverse of the MAX690_/MAX704_/MAX802_/MAX806_ $\overline{RESET}$ output.

Reset Threshold

The MAX690T/MAX704T/MAX805T are intended for 3.3V systems with a ±5% power-supply tolerance and a 10% system tolerance. Except for watchdog faults, reset will not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V.

The MAX690S/MAX704S/MAX805S are designed for 3.3V ±10% power supplies. Except for watchdog faults, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.3V - 10%). Reset is guaranteed to assert before the power supply falls below 2.85V (V_{CC} - 14%).

The MAX690R/MAX704R/MAX805R are optimized for monitoring 3.0V ±10% power supplies. Reset will not occur until V_{CC} falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.59V (3.0V - 14%).

The MAX802R/S/T, MAX804R/S/T, and MAX806R/S/T are respectively similar to the MAX690R/S/T, MAX805R/S/T, and MAX704R/S/T, but with tightened reset and power-fail threshold tolerances.

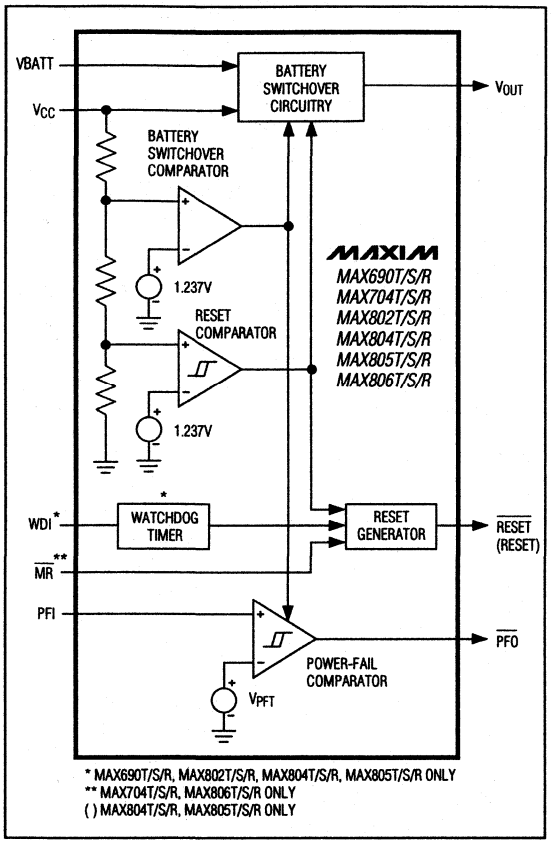


Figure 1. Block Diagram

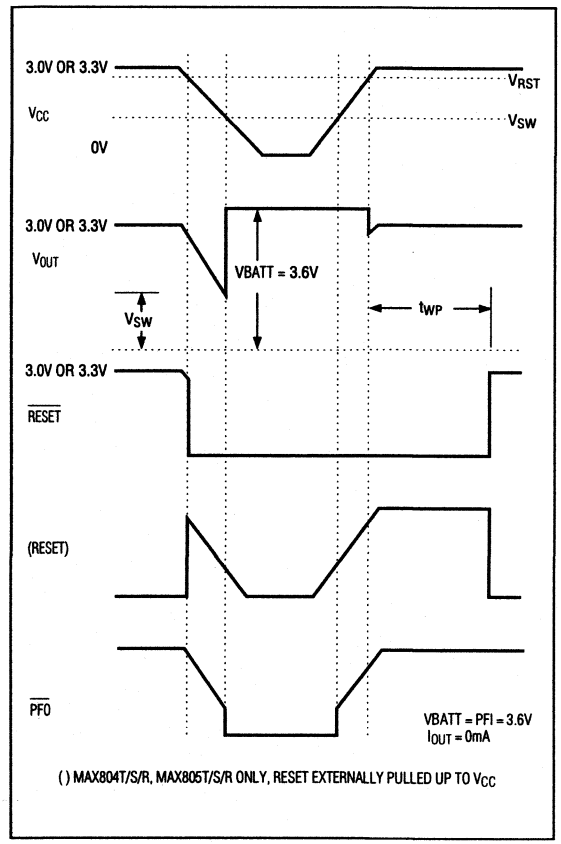


Figure 2. Timing Diagram

Watchdog Input (MAX690_/802_/804_/805_)

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by a transition (low-to-high or high-to-low) at WDI. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8sec (t_{WD} plus t_{RS}).

As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is deasserted, the timer starts counting. Unlike the 5V MAX690 family, the watchdog function **cannot** be disabled.

Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than V_{PFT}, $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply. However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

The power-fail comparator turns off and $\overline{PFO}$ goes low when V_{CC} falls below V_{SW} on power-down. The power-fail comparator turns on as V_{CC} crosses V_{SW} on power-up. If the comparator is not used, connect PFI to ground and leave $\overline{PFO}$ unconnected. $\overline{PFO}$ may be connected to $\overline{MR}$ on the MAX704_/MAX806_ so that a low voltage on PFI will generate a reset (Figure 5b).

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at VBATT, the devices automatically switch RAM to backup power when V_{CC} falls.

This family of µP supervisors (designed for 3.3V and 3V systems) doesn't always connect VBATT to V_{OUT} when VBATT is greater than V_{CC}. VBATT connects to V_{OUT} (through a 140Ω switch) when V_{CC} is below V_{SW} **and** VBATT is greater than V_{CC}, or when V_{CC} falls below 1.75V (typ) regardless of the VBATT voltage. This is done to allow the backup battery (e.g., a 3.6V lithium cell) to have a higher voltage than V_{CC}.

Switchover at V_{SW} (2.40V) ensures that battery-backup mode is entered before V_{OUT} gets too close to the 2.0V minimum required to reliably retain data in CMOS RAM. Switchover at higher V_{CC} voltages would decrease backup-battery life. When V_{CC} recovers, switchover is deferred until V_{CC} rises above the reset threshold (V_{RST}) to ensure a stable supply. V_{OUT} is connected to V_{CC} through a 3Ω PMOS power switch.

Manual Reset

A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{WP} (200ms) after $\overline{MR}$ returns high. This input has an internal 70µA pull-up current, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required.

Table 1. Input and Output Status in Battery-Backup Mode

PIN NAME	STATUS
V_{OUT}	Connected to VBATT through an internal 140Ω switch
V_{CC}	Disconnected from V_{OUT}
PFI	The power-fail comparator is disabled when $V_{CC} < V_{SW}$
$\overline{PFO}$	Logic low when $V_{CC} < V_{SW}$ or PFI < V_{PFT}
WDI	The watchdog timer is disabled
$\overline{MR}$	Disabled
$\overline{RESET}$	Low logic
RESET	High impedance
VBATT	Connected to V_{OUT}

Applications Information

These µP supervisory circuits are not short-circuit protected. Shorting V_{OUT} to ground—excluding power-up transients such as charging a decoupling capacitor—destroys the device. Decouple both V_{CC} and VBATT pins to ground by placing 0.1µF capacitors as close to the device as possible.

Using a SuperCap as a Backup Power Source

SuperCaps™ are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 3 shows two ways to use a SuperCap as a backup power source. The SuperCap may be connected through a diode to the 3V input (Figure 3a) or, if a 5V supply is also available, the SuperCap may be charged up to the 5V supply (Figure 3b) allowing a longer backup period. Since VBATT can exceed V_{CC} while V_{CC} is above the reset threshold, there are no special precautions when using these µP supervisors with a SuperCap.

Operation without a Backup Power Source

These µP supervisors were designed for battery-backed applications. If a backup battery is not used, ground VBATT and connect V_{OUT} to V_{CC}, or use a different µP supervisor such as the MAX706T/S/R or MAX708T/S/R.

Replacing the Backup Battery

The backup power source can be removed while V_{CC} remains valid, if VBATT is decoupled with a 0.1µF capacitor to ground, without danger of triggering $\overline{RESET}$/RESET. As long as V_{CC} stays above V_{SW}, battery-backup mode cannot be entered.

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see the section *Monitoring an Additional Power Supply*).

If additional noise margin is desired, connect a resistor between $\overline{PFO}$ and PFI as shown in Figure 4a. Select the ratio of R1 and R2 such that PFI sees 1.237V (V_{PFT}) when V_{IN} falls to its trip point (V_{TRIP}). R3 adds the hysteresis and will typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above (V_H) and below (V_L) the original trip point (V_{TRIP}).

™ SuperCap is a trademark of Baknor Industries.

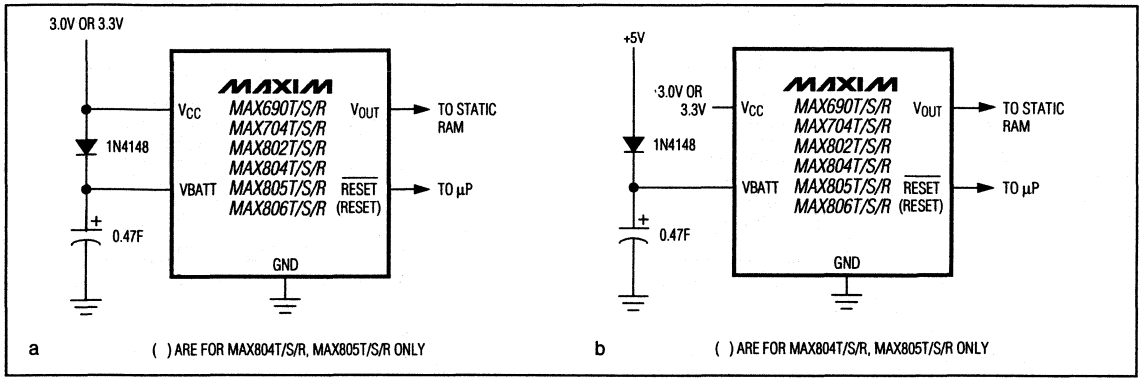


Figure 3. Using a SuperCap as a Backup Power Source

Connecting an ordinary signal diode in series with R3, as shown in Figure 4b, causes the lower trip point (V_L) to coincide with the trip point without hysteresis (V_{TRIP}), so the entire hysteresis window occurs above V_{TRIP}. This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold.

The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max over extended temperature range) PFI input current does not shift the trip point. R3 should be larger than 10kΩ so it does not load down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring an Additional Power Supply

These µP supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. $\overline{PFO}$ can be used to generate an interrupt to the µP (Figure 5). Connecting $\overline{PFO}$ to $\overline{MR}$ on the MAX704 and MAX806 causes reset to assert when the monitored supply goes out of tolerance. Reset remains asserted as long as $\overline{PFO}$ holds $\overline{MR}$ low, and for 200ms after $\overline{PFO}$ goes high.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX690_/MAX704_/MAX802_/MAX806_ $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 6. Buffer the $\overline{RESET}$ output to other system components.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 7 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

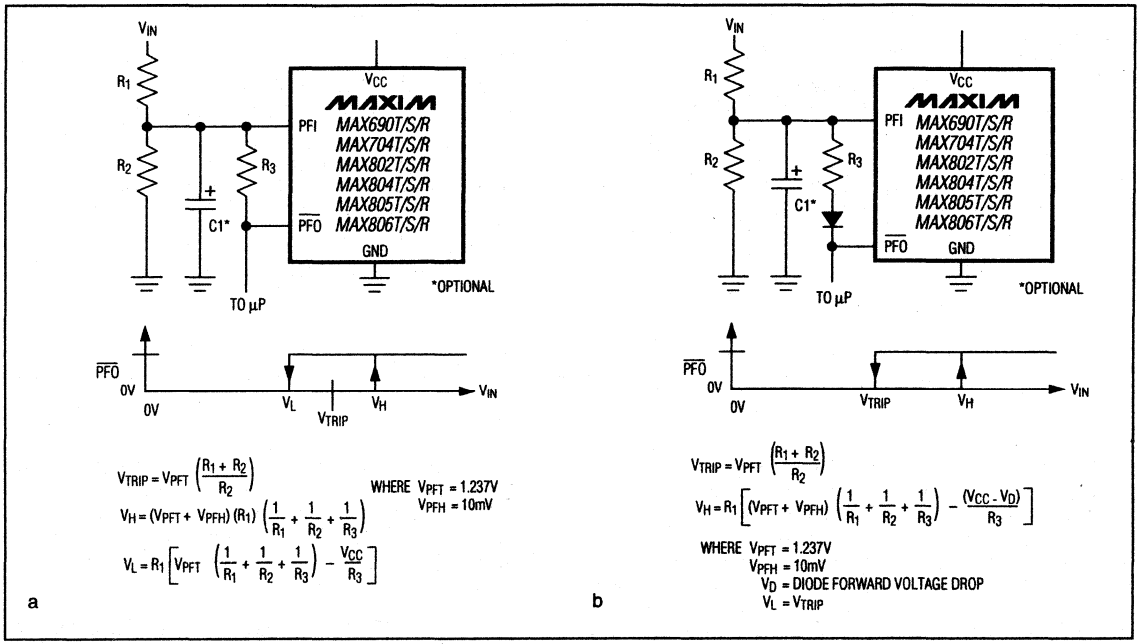


Figure 4. a) Adding Additional Hysteresis to the Power-Fail Comparator b) Shifting the Additional Hysteresis above V_{PFT}

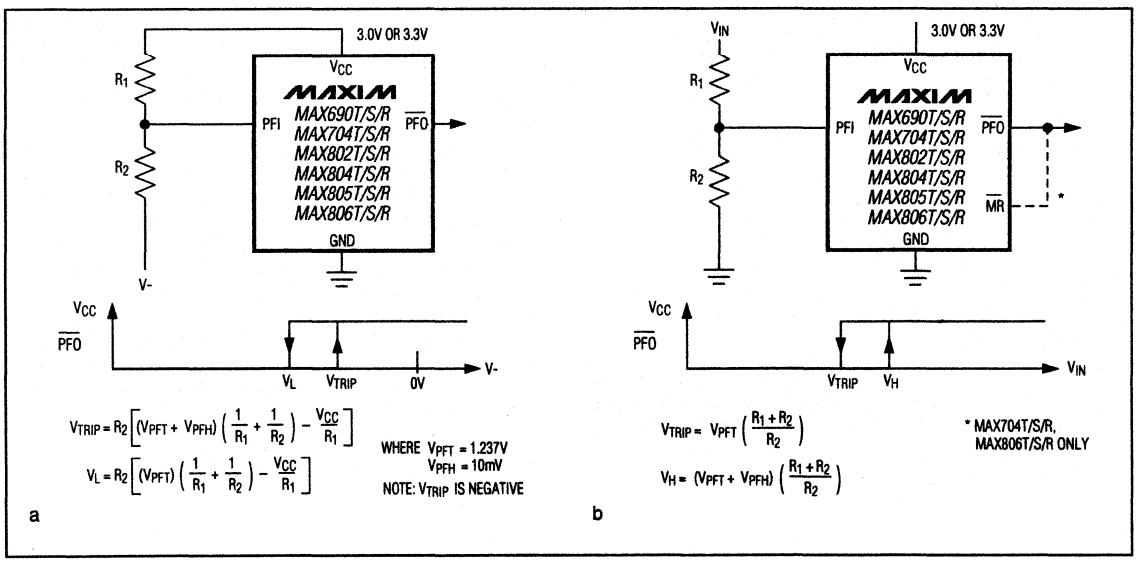


Figure 5. Using the Power-Fail Comparator to Monitor an Additional Power Supply

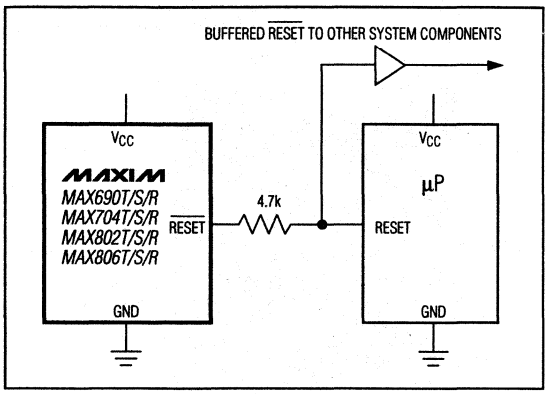
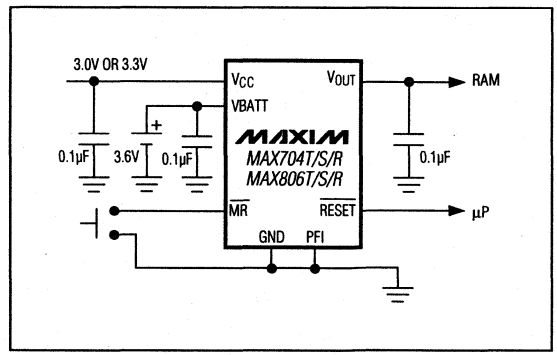


Figure 6. Interfacing to µPs with Bidirectional Reset I/O

Typical Operating Circuits (cont.)



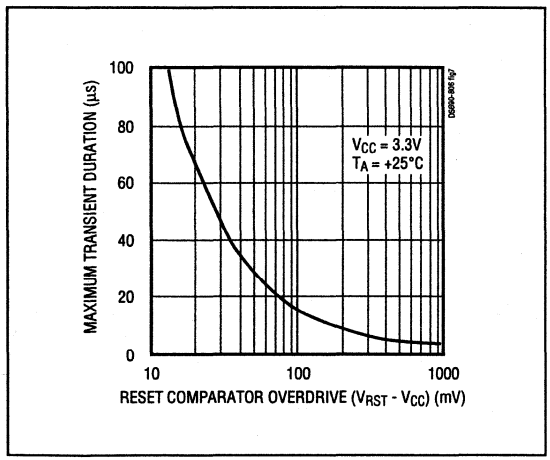


Figure 7. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

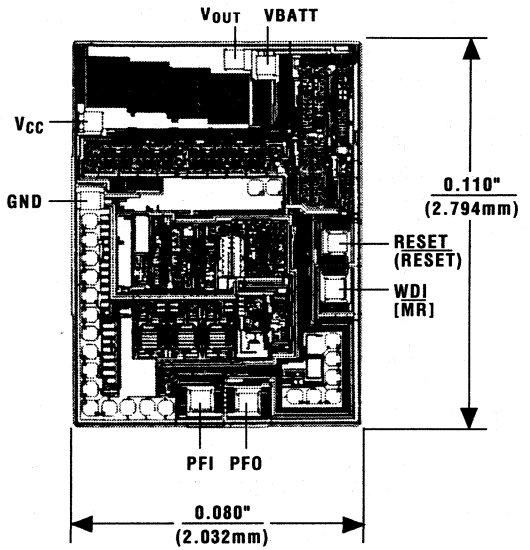
Ordering Information (continued)

PART**	TEMP. RANGE	PIN-PACKAGE
MAX704_CPA	0°C to +70°C	8 Plastic DIP
MAX704_CSA	0°C to +70°C	8 SO
MAX704_C/D	0°C to +70°C	Dice*
MAX704_EPA	-40°C to +85°C	8 Plastic DIP
MAX704_ESA	-40°C to +85°C	8 SO
MAX704_MJA	-55°C to +125°C	8 CERDIP
MAX802_CPA	0°C to +70°C	8 Plastic DIP
MAX802_CSA	0°C to +70°C	8 SO
MAX802_C/D	0°C to +70°C	Dice*
MAX802_EPA	-40°C to +85°C	8 Plastic DIP
MAX802_ESA	-40°C to +85°C	8 SO
MAX802_MJA	-55°C to +125°C	8 CERDIP
MAX804_CPA	0°C to +70°C	8 Plastic DIP
MAX804_CSA	0°C to +70°C	8 SO
MAX804_C/D	0°C to +70°C	Dice*
MAX804_EPA	-40°C to +85°C	8 Plastic DIP
MAX804_ESA	-40°C to +85°C	8 SO
MAX804_MJA	-55°C to +125°C	8 CERDIP
MAX805_CPA	0°C to +70°C	8 Plastic DIP
MAX805_CSA	0°C to +70°C	8 SO
MAX805_C/D	0°C to +70°C	Dice*
MAX805_EPA	-40°C to +85°C	8 Plastic DIP
MAX805_ESA	-40°C to +85°C	8 SO
MAX805_MJA	-55°C to +125°C	8 CERDIP
MAX806_CPA	0°C to +70°C	8 Plastic DIP
MAX806_CSA	0°C to +70°C	8 SO
MAX806_C/D	0°C to +70°C	Dice*
MAX806_EPA	-40°C to +85°C	8 Plastic DIP
MAX806_ESA	-40°C to +85°C	8 SO
MAX806_MJA	-55°C to +125°C	8 CERDIP

** Contact factory for dice specifications.*

*** These parts offer a choice of reset threshold voltage. Select the letter corresponding to the desired nominal reset threshold voltage (T = 3.075V, S = 2.925V, R = 2.625V) and insert it into the blank to complete the part number.*

Chip Topography



( ) ARE FOR MAX804T/S/R, MAX805T/S/R.
[ ] ARE FOR MAX704T/S/R, MAX806T/S/R.

TRANSISTOR COUNT: 802;

SUBSTRATE IS CONNECTED TO THE HIGHER OF V_{CC} OR VBATT, AND MUST BE FLOATED IN ANY HYBRID DESIGN.

19-0094; Rev 4; 3/94

MAXIM

Microprocessor Supervisory Circuits

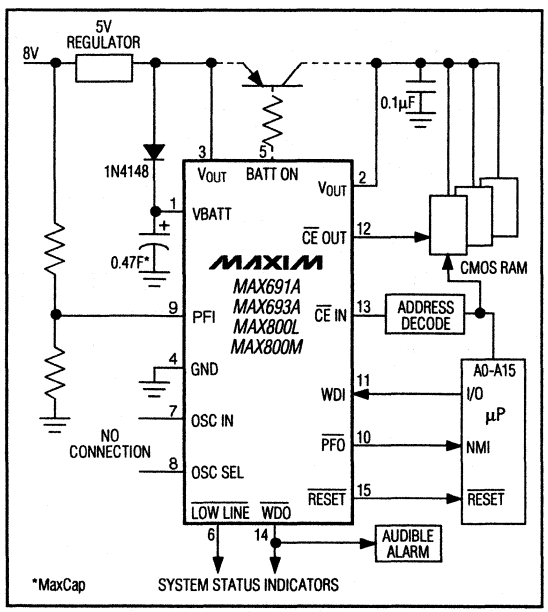
General Description

The MAX691A/MAX693A/MAX800L/MAX800M microprocessor (µP) supervisory circuits are pin-compatible upgrades to the MAX691, MAX693, and MAX695. They improve performance with 30µA supply current, 200ms typ reset active delay on power-up, and 6ns chip-enable propagation delay. Features include write protection of CMOS RAM or EEPROM, separate watchdog outputs, backup-battery switchover, and a $\overline{\text{RESET}}$ output that is valid with V_{CC} down to 1V. The MAX691A/MAX800L have a 4.65V typ reset-threshold voltage, and the MAX693A/MAX800M's reset threshold is 4.4V typ. The MAX800L/MAX800M guarantee power-fail accuracies to ±2%.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



® SuperCap is a registered trademark of Baknor Industries.

Features

- ♦ **200ms Power OK/Reset Timeout Period**
- ♦ **1µA Standby Current, 30µA Operating Current**
- ♦ **On-Board Gating of Chip-Enable Signals, 10ns Max Delay**
- ♦ **MaxCap® or SuperCap® Compatible**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Power-Fail Accuracy Guaranteed to ±2% (MAX800L/M)**
- ♦ **Available in 16-Pin Narrow SO and Plastic DIP Packages**

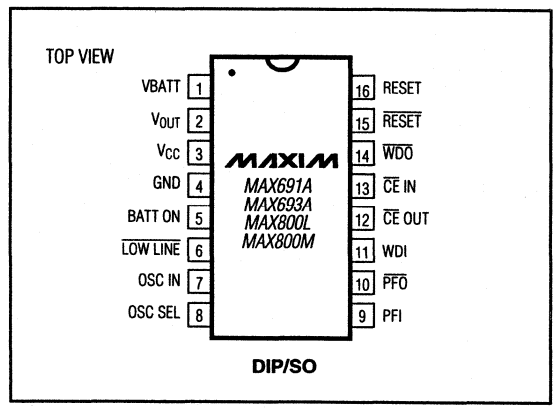
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX691ACPE	0°C to +70°C	16 Plastic DIP
MAX691ACSE	0°C to +70°C	16 Narrow SO
MAX691ACWE	0°C to +70°C	16 Wide SO
MAX691AC/D	0°C to +70°C	Dice*
MAX691AEPE	-40°C to +85°C	16 Plastic SO
MAX691AESE	-40°C to +85°C	16 Narrow SO
MAX691AEWE	-40°C to +85°C	16 Wide SO
MAX691AEJE	-40°C to +85°C	16 CERDIP
MAX691AMJE	-55°C to +125°C	16 CERDIP

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C.*

Pin Configuration



® MaxCap is a registered trademark of Carborundum Corp.

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- VBATT ..... -0.3V to +6V
- All Other Inputs ..... -0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 250mA
- VBATT Peak 250mA
- VBATT Continuous 25mA
- GND, BATT ON 100mA
- All Other Outputs 25mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Narrow SO (derate 8.70mW/°C above +70°C) 696mW
- Wide SO (derate 9.52mW/°C above +70°C) 762mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
- MAX69_AC_ _/MAX800_C_ _ ..... 0°C to +70°C
- MAX69_AE_ _/MAX800_E_ _ ..... -40°C to +85°C
- MAX69_AMJE ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX691A, MAX800L: V_{CC} = 4.75V to 5.5V, MAX693A, MAX800M: V_{CC} = 4.5V to 5.5V, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, VBATT (Note 1)				0		5.5	V
V_{OUT} Output	V_{CC} = 4.5V	I_{OUT} = 25mA		V_{CC} - 0.05	V_{CC} - 0.02		V
		I_{OUT} = 250mA	MAX69_AC/AE, MAX800_C/E	V_{CC} - 0.3	V_{CC} - 0.2		
			MAX69_AM	V_{CC} - 0.40			
V_{CC}-to-V_{OUT} On Resistance	V_{CC} = 4.5V	MAX69_AC/AE, MAX800_C/E			0.8	1.2	Ω
		MAX69_AM			0.8	1.6	
V_{OUT} in Battery-Backup Mode	VBATT = 4.5V, I_{OUT} = 20mA			VBATT - 0.3			V
	VBATT = 2.8V, I_{OUT} = 10mA			VBATT - 0.25			
	VBATT = 2.0V, I_{OUT} = 5mA			VBATT - 0.15			
VBATT-to-V_{OUT} On Resistance	VBATT = 4.5V					15	Ω
	VBATT = 2.8V					25	
	VBATT = 2.0V					30	
Supply Current in Normal Operating Mode (Excludes I_{OUT})	V_{CC} > VBATT - 1V				30	100	µA
Supply Current in Battery-Backup Mode (Excludes I_{OUT}) (Note 2)	V_{CC} < VBATT - 1.2V VBATT = 2.8V	T_A = +25°C			0.04	1	µA
		T_A = T_{MIN} + T_{MIN}				5	
VBATT Standby Current (Note 3)	VBATT + 0.2V ≤ V_{CC}	T_A = +25°C		-0.1		0.02	µA
		T_A = T_{MIN} + T_{MIN}		-1.0		0.02	
Battery Switchover Threshold	Power-up				VBATT + 0.3		V
	Power-down				VBATT - 0.3		
Battery Switchover Hysteresis					60		mV
BATT ON Output Low Voltage	I_{SINK} = 3.2mA				0.1	0.4	V
	I_{SINK} = 25mA				0.7	1.5	
BATT ON Output Short-Circuit Current	Sink current				60		mA
	Source current			1	15	100	µA

ELECTRICAL CHARACTERISTICS (continued)

(MAX691A, MAX800L: V_{CC} = 4.75V to 5.5V, MAX693A, MAX800M: V_{CC} = 4.5V to 5.5V, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET AND WATCHDOG TIMER					
Reset Threshold Voltage	MAX691A, MAX800L	4.50	4.65	4.75	V
	MAX693A, MAX800M	4.25	4.40	4.50	
	MAX800L, T_A = +25°C, V_{CC} falling	4.55		4.70	
	MAX800M, T_A = +25°C, V_{CC} falling	4.30		4.45	
Reset Threshold Hysteresis			15		mV
V_{CC} to RESET Delay	Power-down		80		µs
LOWLINE-to-RESET Delay			800		ns
Reset Active Timeout Period, Internal Oscillator	Power-up	140	200	280	ms
Reset Active Timeout Period, External Clock	Power-up		2048		Clock Cycles
Watchdog Timeout Period, Internal Oscillator	Long period	1.0	1.6	2.25	sec
	Short Period	70	100	140	ms
Watchdog Timeout Period, External Clock	Long Period		4096		Clock Cycles
	Short Period		1024		
Minimum Watchdog Input Pulse Width	V_{IL} = 0.8V, V_{IH} = 0.75 x V_{CC}	100			ns
RESET Output Voltage	I_{SINK} = 50µA, V_{CC} = 1V, VBATT = 0V, V_{CC} falling		0.004	0.3	V
	I_{SINK} = 3.2mA, V_{CC} = 4.25V		0.1	0.4	
	I_{SOURCE} = 1.6mA, V_{CC} = 5V	3.5			
RESET Output Short-Circuit Current	Output source current		7	20	mA
RESET Output Voltage Low (Note 4)	I_{SINK} = 3.2mA	0.1	0.4		mA
LOW LINE Output Voltage	I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
LOW LINE Output Short-Circuit Current	Output source current	1	15	100	µA
WDO Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 500µA, V_{CC} = 5V	3.5			
WDO Output Short-Circuit Current	Output source current		3	10	mA
WDI Threshold Voltage (Note 5)	V_{IH}	0.75 x V_{CC}			V
	V_{IL}			0.8	
WDI Input Current	WDI = 0V	-50	-10		µA
	WDI = V_{OUT}		20	50	

ELECTRICAL CHARACTERISTICS (continued)

(MAX691A, MAX800L: V_{CC} = 4.75V to 5.5V, MAX693A, MAX800M: V_{CC} = 4.5V to 5.5V, VBATT = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-FAIL COMPARATOR					
PFI Input Threshold	MAX69_AC/AE/AM, V_{CC} = 5V	1.2	1.25	1.3	V
	MAX800_C/E, V_{CC} = 5V	1.225	1.25	1.275	
PFI Leakage Current			±0.01	±25	nA
$\overline{PFO}$ Output Voltage	I_{SINK} = 3.2mA			0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V	3.5			
$\overline{PFO}$ Output Short-Circuit Current	Output source current	1	15	100	µA
PFI-to-PFO Delay	V_{IN} = -20mV, V_{OD} = 15mA		25		µs
	V_{IN} = 20mV, V_{OD} = 15mA		60		
CHIP-ENABLE GATING					
$\overline{CE}$ IN Leakage Current	Disable mode		±0.005	±1	µA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Resistance (Note 6)	Enable mode		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)	Disable mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN-to-$\overline{CE}$ OUT Propagation Delay (Note 7)	50Ω source impedance driver, C_{LOAD} = 50pF		6	10	ns
$\overline{CE}$ OUT Output Voltage High (Reset Active)	V_{CC} = 5V, I_{OUT} = -100µA	3.5			V
	V_{CC} = 0V, VBATT = 2.8V, I_{OUT} = 1µA	2.7			
RESET-to-$\overline{CE}$ OUT Delay	Power-down		12		µs
INTERNAL OSCILLATOR					
OSC IN Leakage Current	OSC SELL = 0V		0.10	±5	µA
OSC IN Input Pull-up Current	OSC SELL = V_{OUT} or floating, OSC IN = 0V		10	100	µA
OSC SEL Input Pull-up Current	OSC SELL = 0V		10	100	µA
OSC IN Frequency Range	OSC SELL = 0V		50		kHz
OSC IN External Oscillator Threshold Voltage	V_{IH}	V_{OUT} - 0.4	V_{OUT} - 0.6		V
	V_{IL}		3.65	2.00	
OSC IN Frequency with External Capacitor	OSC SELL = 0V, COSC = 47pF		100		kHz

Note 1: Either V_{CC} or VBATT can go to 0V, if the other is greater than 2.0V.

Note 2: The supply current drawn by the MAX691A/MAX800L/MAX800M from the battery excluding I_{OUT} typically goes to 10µA when (VBATT - 1V) < V_{CC} < VBATT. In most applications, this is a brief period as V_{CC} falls through this region.

Note 3: "+" = battery-discharging current, "-" = battery-charging current.

Note 4: RESET is an open-drain output and sinks current only.

Note 5: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V (typ), disabling the watchdog function.

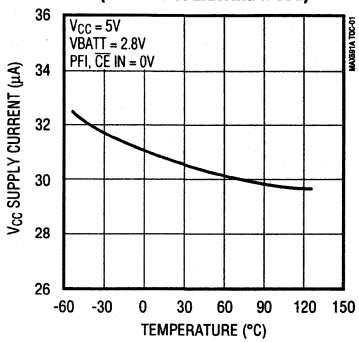
Note 6: The chip-enable resistance is tested with V_{CC} = 4.75V for the MAX691A/MAX800L and V_{CC} = 4.5 for the MAX693A/MAX800M. $\sqrt{CE\ IN}$ = $\sqrt{CE\ OUT}$ = $V_{CC}/2$.

Note 7: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

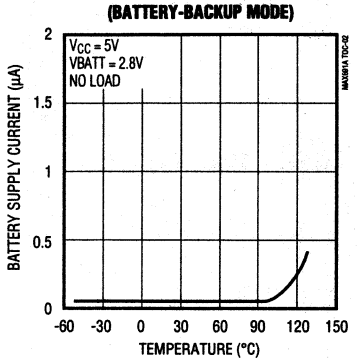
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

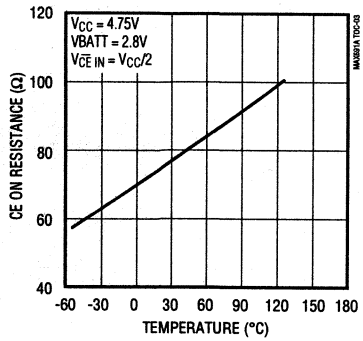
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



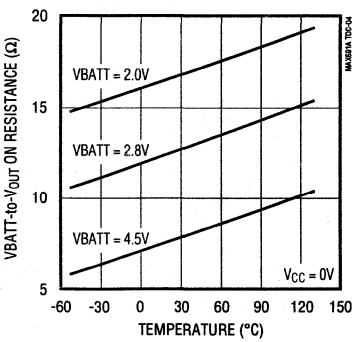
BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



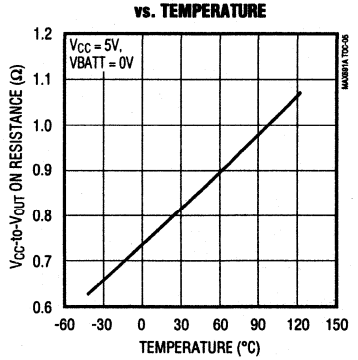
CHIP-ENABLE ON RESISTANCE vs. TEMPERATURE



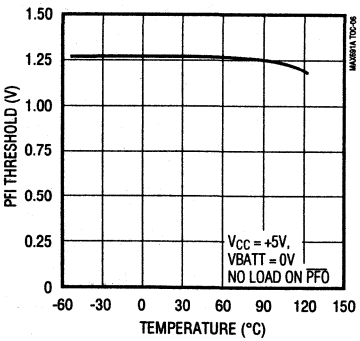
VBATT to V_{OUT} ON RESISTANCE vs. TEMPERATURE



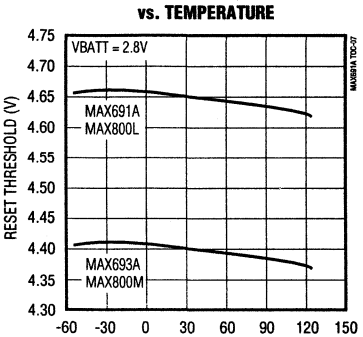
V_{CC} to V_{OUT} ON RESISTANCE vs. TEMPERATURE



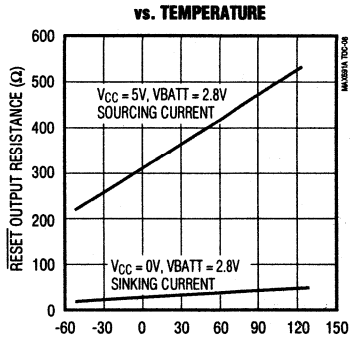
PFI THRESHOLD vs. TEMPERATURE



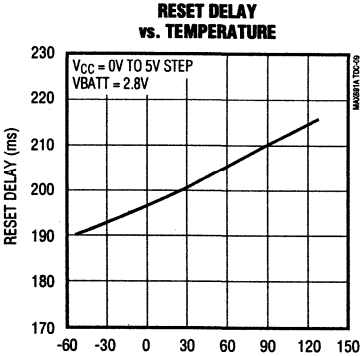
RESET THRESHOLD vs. TEMPERATURE



$\overline{RESET}$ OUTPUT RESISTANCE vs. TEMPERATURE



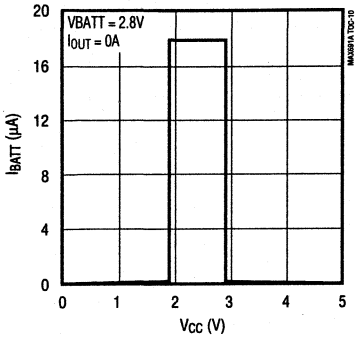
RESET DELAY vs. TEMPERATURE



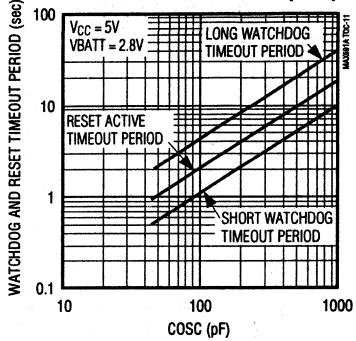
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

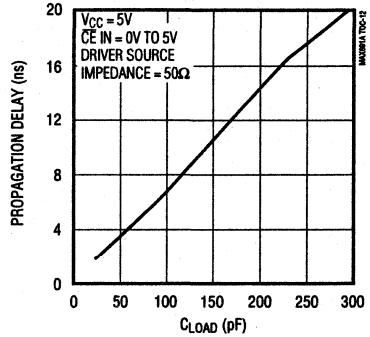
BATTERY CURRENT vs. INPUT SUPPLY VOLTAGE



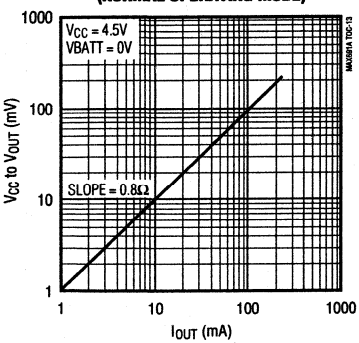
WATCHDOG AND RESET TIMEOUT PERIOD vs. OSC IN TIMING CAPACITOR (COSC)



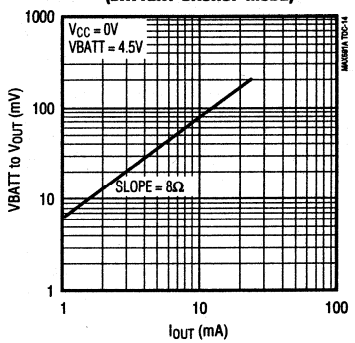
CHIP-ENABLE PROPOGATION DELAY vs. $\overline{CE}$ OUT LOAD CAPACITANCE



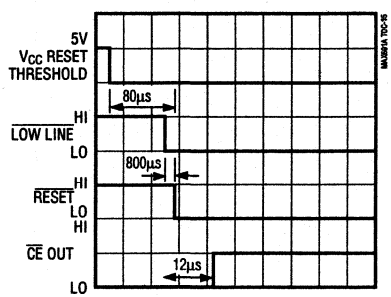
VCC to VOUT vs. OUTPUT CURRENT (NORMAL OPERATING MODE)



VBATT to VOUT vs. OUTPUT CURRENT (BATTERY-BACKUP MODE)



VCC to $\overline{LOW\ LINE}$ AND $\overline{CE}$ OUT DELAY



Pin Description

PIN	NAME	FUNCTION
1	VBATT	Battery-Backup Input. Connect to external battery or capacitor and charging circuit. If backup battery is not used, connect to GND.
2	VOUT	Output Supply Voltage. When V_{CC} is greater than VBATT and above the reset threshold, V_{OUT} connects to V_{CC}. When V_{CC} falls below VBATT and is below the reset threshold, V_{OUT} connects to VBATT. Connect a 0.1µF capacitor from V_{OUT} to GND. Connect V_{OUT} to V_{CC} if no backup battery is used.
3	VCC	Input Supply Voltage, 5V input.
4	GND	Ground. 0V reference for all signals.
5	BATT ON	Battery On Output. When V_{OUT} switches to VBATT, BATT ON goes high. When V_{OUT} switches to V_{CC}, BATT ON goes low. Connect the base of a PNP through a current-limiting resistor to BATT ON for V_{OUT} current requirements greater than 250mA.
6	$\overline{\text{LOW LINE}}$	$\overline{\text{LOW LINE}}$ output goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
7	OSC IN	External Oscillator Input. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. The timing can also be adjusted by connecting an external capacitor to this pin. (see Figure 3). When OSC SEL is high or floating, OSC IN selects between fast and slow watchdog timeout periods.
8	OSC SEL	Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period.When OSC SEL is low, the external oscillator input, OSC IN, is enabled (see Table 1). OSC SEL has a 10µA internal pull-up.
9	PFI	Power-Fail Input. This is the non-inverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. When PFI is not used, connect PFI to GND or V_{OUT} .
10	$\overline{\text{PFO}}$	Power-Fail Output. This is the output of the power-fail comparator. $\overline{\text{PFO}}$ goes low when PFI is less than 1.25V. This is an uncommited comparator, and has no effect on any other internal circuitry.
11	WDI	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected.
12	$\overline{\text{CE}}$ OUT	Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and V_{CC} is above the reset threshold. If CE IN is low when reset is asserted, $\overline{\text{CE}}$ OUT will stay low for 15µs or until $\overline{\text{CE}}$ IN goes high, whichever occurs first.
13	$\overline{\text{CE}}$ IN	Chip-Enable Input. The input to chip-enable gating circuit. If $\overline{\text{CE}}$ IN is not used, connect $\overline{\text{CE}}$ IN to GND or V_{OUT}.
14	$\overline{\text{WDO}}$	Watchdog Output. If WDI remains high or low longer than the watchdog timeout period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. $\overline{\text{WDO}}$ remains high if WDI is unconnected.
15	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output goes low whenever V_{CC} falls below the reset threshold. $\overline{\text{RESET}}$ will remain low typically for 200ms after V_{CC} crosses the reset threshold on power-up.
16	RESET	RESET is an active-high output. It is open drain, and the inverse of $\overline{\text{RESET}}$.

Detailed Description

$\overline{\text{RESET}}$ and RESET Outputs

TheMAX691A/MAX693A/MAX800L/MAX800M's $\overline{\text{RESET}}$ and RESET outputs ensure that the µP (with reset inputs asserted either high or low) powers up in a known state, and prevents code-execution errors during power-down or brownout conditions.

The $\overline{\text{RESET}}$ output is active low, and typically sinks 3.2mA at 0.1V saturation voltage in its active state. When deasserted, $\overline{\text{RESET}}$ sources 1.6mA at typically V_{OUT} - 0.5V. RESET output is open drain, active high, and typically sinks 3.2mA with a saturation voltage of 0.1V. When no backup battery is used, $\overline{\text{RESET}}$ output is guaranteed to be valid down to V_{CC} = 1V, and an external 10kΩ pull-down resistor on $\overline{\text{RESET}}$ insures that it will be valid with V_{CC} down to GND (Figure 1). As V_{CC} goes below 1V, the gate drive to the $\overline{\text{RESET}}$ output switch reduces accordingly, increasing the $r_{DS(ON)}$ and the saturation voltage. The 10kΩ pull-down resistor insures the parallel combination of switch plus resistor is around 10kΩ and the output saturation voltage is below 0.4V while sinking 40µA. When using a 10kΩ external pull-down resistor, the high state for $\overline{\text{RESET}}$ output with V_{CC} = 4.75V will be 4.5V typ. For battery voltages ≥ 2V connected to VBATT, RESET and $\overline{\text{RESET}}$ remain valid for V_{CC} from 0V to 5.5V.

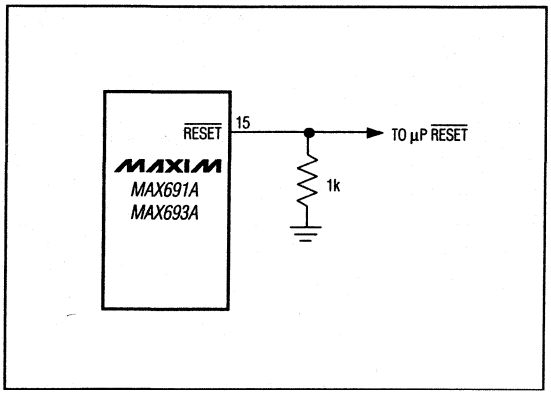


Figure 1. Adding an external pull-down resistor ensures RESET is valid with V_{CC} down to GND.

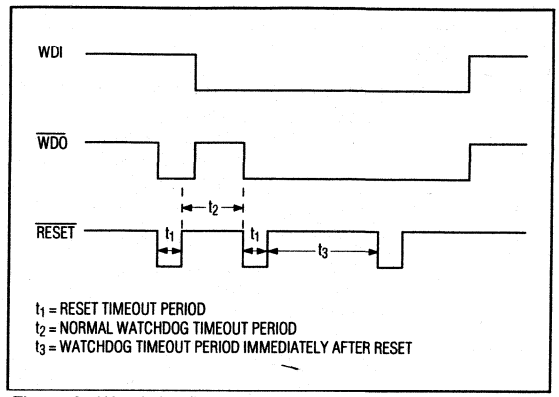


Figure 2. Watchdog Timeout Period and Reset Active Time

RESET and RESET are asserted when V_{CC} falls below the reset threshold (4.65V for the MAX691A/MAX800L, 4.4V for the MAX693A/MAX800M) and remain asserted for 200ms typ after V_{CC} rises above the reset threshold on power-up (Figure 5). The devices' battery-switchover comparator does not affect reset assertion. However, both reset outputs are asserted in battery-backup mode since V_{CC} must be below the reset threshold to enter this mode.

Watchdog Function

The watchdog monitors µP activity via the Watchdog Input (WDI). If the µP becomes inactive, RESET and RESET are asserted. To use the watchdog function, connect WDI to a bus line or µP I/O line. If WDI remains high or low for longer than the watchdog time-out period (1.6sec nominal), WDO, RESET, and RESET are asserted (see *RESET and RESET Outputs* section, and the *Watchdog Output* discussion on this page).

Watchdog Input

A change of state (high to low, low to high, or a minimum 100ns pulse) at the Watchdog Input (WDI) during the watchdog period resets the watchdog timer. The watchdog default timeout is 1.6sec.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the reset threshold, the watchdog function is disabled and WDI is disconnected from its internal resistor network, thus becoming high impedance.

Watchdog Output

The Watchdog Output (WDO) remains high if there is a transition or pulse at WDI during the watchdog timeout period. The watchdog function is disabled and WDO is a logic high when V_{CC} is below the reset threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog timeout period, RESET and RESET are asserted for the reset timeout period (200ms typ). WDO goes low and remains low until the next transition at WDI (Figure 2). If WDI is held high or low indefinitely, RESET and RESET will generate 200ms pulses every 1.6sec. WDO has a 2 x TTL output characteristic.

Selecting an Alternative Watchdog and Reset Timeout

OSC SEL and OSC IN inputs control the watchdog and reset timeout periods. Floating OSC SEL and OSC IN or tying them both to V_{OUT} selects the nominal 1.6sec watchdog timeout period and 200ms reset timeout period. Connecting OSC IN to GND and floating or connecting OSC SEL to V_{OUT} selects the 100ms normal watchdog timeout delay and 1.6sec delay immediately after reset. The reset timeout delay remains 200ms (Figure 2). Select alternative timeout periods by connecting OSC SEL to GND and a capacitor between OSC IN and GND, or externally driving OSC IN (Table 1 and Figure 3).

Chip-Enable Signal Gating

The MAX691A/MAX693A/MAX800L/MAX800M provide internal gating of chip-enable (CE) signals to prevent erroneous data from being written to CMOS RAM in the event of a power failure. During normal operation, the

Table 1. Reset Pulse Width and Watchdog Timeout Selections

OSC SEL	OSC IN	Watchdog Timeout Period		Reset Timeout Period
		Normal	Immediately After Reset	
Low	External Clock Input	1024 clks	4096 clks	2048 clks
Low	External Capacitor	(600/47pF x C)ms	(2.4/47pF x C)sec	(800/47pF x C)ms
Floating	Low	100ms	1.6sec	200ms
Floating	Floating	1.6sec	1.6sec	200ms

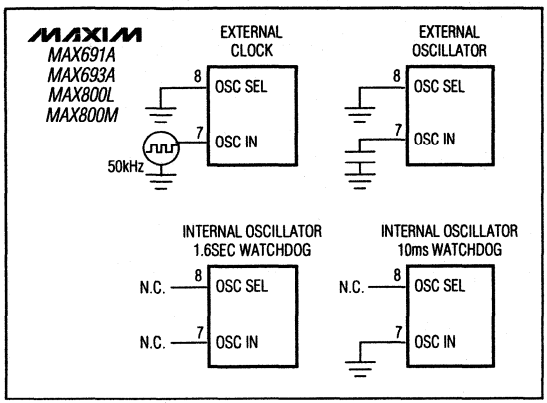


Figure 3. Oscillator Circuits

CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. All these parts use a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 4).

The 10ns max CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the parts to be used with most µPs.

Chip-Enable Input

The Chip-Enable Input ($\overline{CE}$ IN) is high impedance (disabled mode) while RESET and $\overline{RESET}$ are asserted.

During a power-down sequence where V_{CC} falls below the reset threshold or a watchdog fault, $\overline{CE}$ IN assumes a high-impedance state when the voltage at $\overline{CE}$ IN goes high or 15µs after reset is asserted, whichever occurs first (Figure 5).

During a power-up sequence, $\overline{CE}$ IN remains high impedance, regardless of $\overline{CE}$ IN activity, until reset is deasserted following the reset timeout period.

In the high-impedance mode, the leakage currents into this terminal are ±1µA max over temperature. In the low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on the Chip-Enable Output ($\overline{CE}$ OUT) (see Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point of $\overline{CE}$ IN to the 50% point of $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 6). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT, and use a low output-impedance driver.

Chip-Enable Output

In the enabled mode, the impedance of $\overline{CE}$ OUT is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In the disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to V_{OUT}. This source turns off when the transmission gate is enabled.

$\overline{LOW\ LINE}$ Output

$\overline{LOW\ LINE}$ is the buffered output of the reset threshold comparator. $\overline{LOW\ LINE}$ typically sinks 3.2mA at 0.1V. For normal operation (V_{CC} above the $\overline{LOW\ LINE}$ threshold), $\overline{LOW\ LINE}$ is pulled to V_{OUT}.

Power-Fail Comparator

The power-fail comparator is an uncommitted comparator that has no effect on the other functions of the IC. Common uses include low-battery indication (Figure 7), and early power-fail warning (see *Typical Operating Circuit*).

Power-Fail Input

PFI is the input to the power-fail comparator. PFI has a guaranteed input leakage of ±25nA max over temperature. The typical comparator delay is 25µs from V_{IL} to V_{OL} (power failing), and 60µs from V_{IH} to V_{OH} (power being restored). If unused, connect this input to ground.

Power-Fail Output

The Power-Fail Output ($\overline{PFO}$) goes low when PFI goes below 1.25V. It typically sinks 3.2mA with a saturation voltage of 0.1V. With PFI above 1.25V, $\overline{PFO}$ is actively pulled to V_{OUT}.

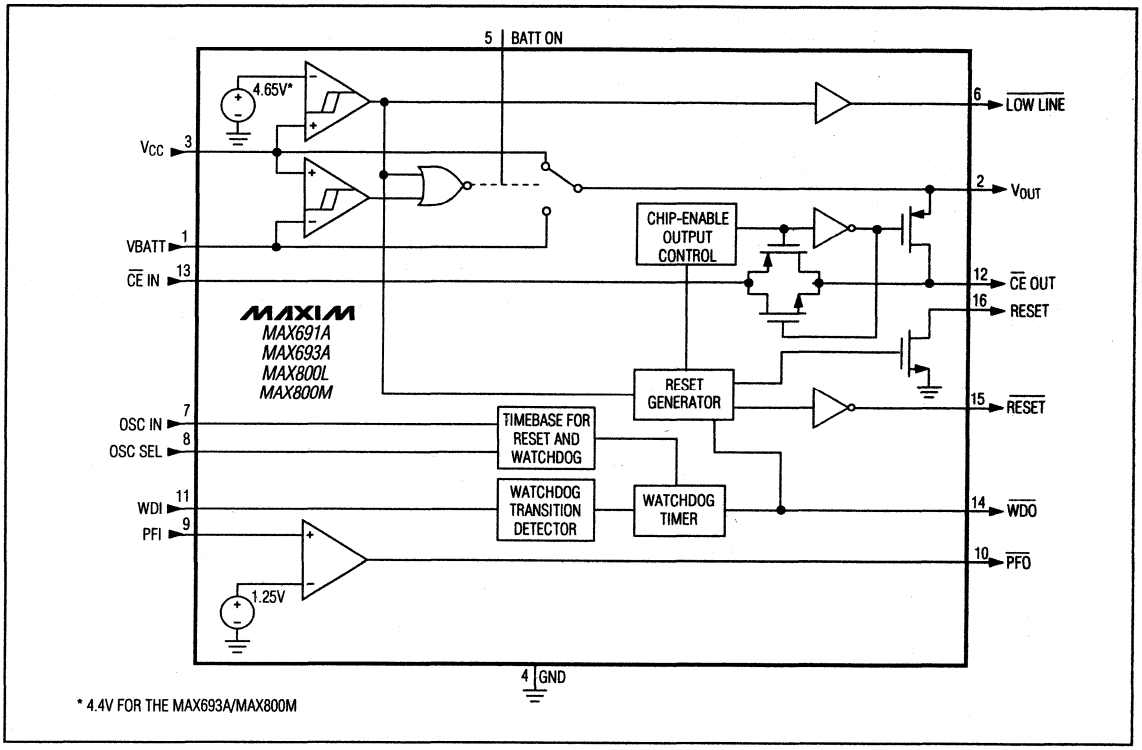


Figure 4. MAX691A/MAX693A/MAX800L/MAX800M Block Diagram

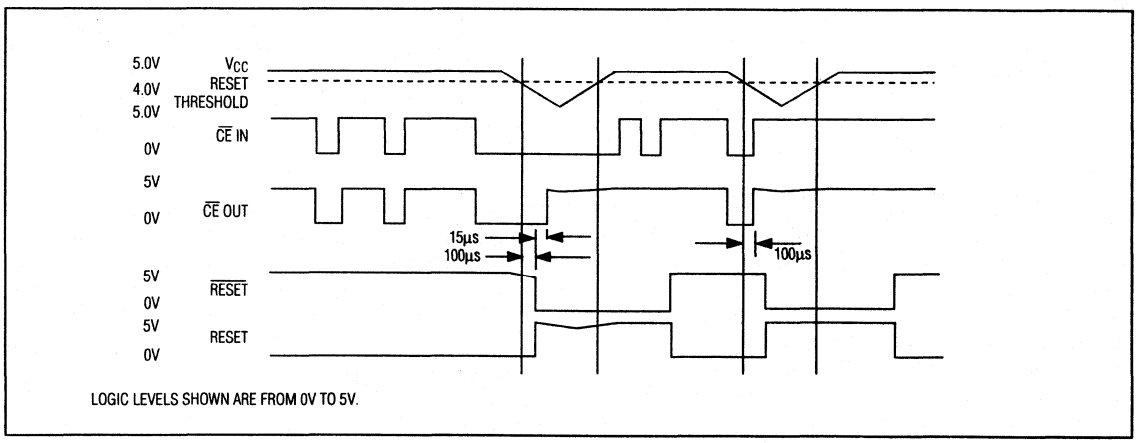


Figure 5. Reset and Chip-Enable Timing

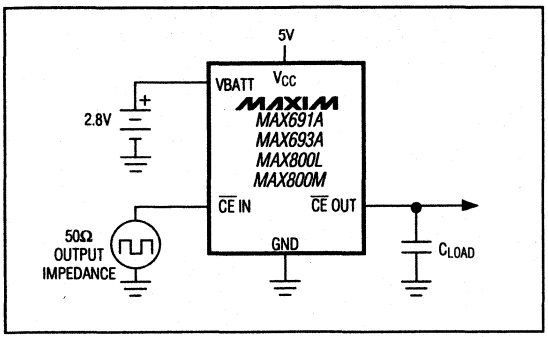


Figure 6. CE Propagation Delay Test Circuit

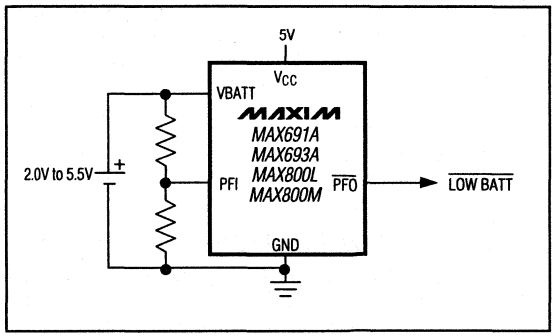


Figure 7. Low-Battery Indicator

Table 2. Input and Output Status in Battery-Backup Mode

PIN	NAME	STATUS
1	VBATT	Supply Current is 1µA max.
2	V_{OUT}	V_{OUT} is connected to VBATT through an internal PMOS switch.
3	V_{CC}	Battery switchover comparator monitors V_{CC} for active switchover.
4	GND	GND 0V, 0V reference for all signals.
5	BATT ON	Logic high. The open-circuit output is equal to V_{OUT}.
6	$\overline{\text{LOWLINE}}$	Logic Low*
7	OSC IN	OSC IN is ignored.
8	OSC SEL	OSC SEL is ignored.
9	PFI	The power-fail comparator remains active in the battery-backup mode for $V_{CC} \geq$ VBATT - 1.2V typ.
10	$\overline{\text{PFO}}$	The power-fail comparator remains active in the battery-backup mode for $V_{CC} \geq$ VBATT - 1.2V typ. Below this voltage, PFO is forced low.
11	WDI	Watchdog is ignored.
12	$\overline{\text{CE}}$ OUT	Logic high. The open-circuit voltage is equal to V_{OUT}.
13	$\overline{\text{CE}}$ IN	High Impedance.
14	$\overline{\text{WDO}}$	Logic high. The open-circuit voltage is equal to V_{OUT}.
15	$\overline{\text{RESET}}$	Logic low*
16	RESET	High Impedance*.

** V_{CC} must be below the reset threshold to enter battery-backup mode.*

Battery-Backup Mode

Two conditions are required to switch to battery-backup mode: 1) V_{CC} must be below the reset threshold, and 2) V_{CC} must be below VBATT. Table 2 lists the status of the inputs and outputs in battery-backup mode.

Battery On Output

The Battery On (BATT ON) output indicates the status of the internal V_{CC}/battery-switchover comparator, which controls the internal V_{CC} and VBATT switches. For V_{CC} greater that VBATT (ignoring the small hysteresis effect), BATT ON typically sinks 3.2mA at 0.1V saturation voltage. In battery-backup mode, this terminal sources approximately 10µA from V_{OUT}. Use BATT ON to indicate battery-switchover status or to supply base drive to an external pass transistor for higher-current applications (see *Typical Operating Circuit*).

Input Supply Voltage

The Input Supply Voltage (V_{CC}) should be a regulated 5V. V_{CC} connects to V_{OUT} via a parallel diode and a large PMOS switch. The switch carries the entire current load for currents less than 250mA. The parallel diode carries any current in excess of 250mA. Both the switch and the diode have impedances less than 1Ω each. The maximum continuous current is 250mA, but power-on transients may reach a maximum of 1A.

Backup-Battery Input

The Backup-Battery Input (VBATT) is similar to the V_{CC} input except the PMOS switch and parallel diode are much smaller. Accordingly, the on resistances of the diode and the switch are each approximately 10Ω. Continuous current should be limited to 25mA and peak currents (only during power-up) limited to 250mA. The reverse leakage of this input is less than 1µA over temperature and supply voltage (Figure 8).

Output Supply Voltage

The Output Supply Voltage (V_{OUT}) pin is internally connected to the substrate of the IC and supplies current to the external system and internal circuitry. All open-circuit outputs will, for example, assume the V_{OUT} voltage in their high states rather than the V_{CC} voltage. At the maximum source current of 250mA, V_{OUT} will typically be 200mV below V_{CC}. Decouple this terminal with a 0.1µF capacitor.

Applications Information

The MAX691A/MAX693A/MAX800L/MAX800M are not short-circuit protected. Shorting V_{OUT} to ground, other than power-up transients such as charging a decoupling capacitor, destroys the device.

All open-circuit outputs swing between V_{OUT} and GND rather than V_{CC} and GND.

If long leads connect to the chip inputs, insure that these leads are free from ringing and other conditions that would forward bias the chip's protection diodes.

There are three distinct modes of operation:

1) Normal operating mode with all circuitry powered up. Typical supply current from V_{CC} is 35µA while only leakage currents flow from the battery.
2) Battery-backup mode where V_{CC} is typically within 0.7V below VBATT. All circuitry is powered up and the supply current from the battery is typically less than 60µA.
3) Battery-backup mode where V_{CC} is less than VBATT by at least 0.7V. VBATT supply current is 1µA max.

Using SuperCaps or MaxCaps with the MAX691A/MAX693A/MAX800L/MAX800M

VBATT has the same operating voltage range as V_{CC}, and the battery switchover threshold voltages are typically ±30mV centered at VBATT, allowing use of a SuperCap and a simple charging circuit as a backup source (Figure 9).

If V_{CC} is above the reset threshold and VBATT is 0.5V above V_{CC}, current flows to V_{OUT} and V_{CC} from VBATT until the voltage at VBATT is less than 0.5V above V_{CC}. For example, with a SuperCap connected to VBATT and through a diode to V_{CC}, if V_{CC} quickly changes from 5.4V to 4.9V, the capacitor discharges through V_{OUT} and V_{CC} until VBATT reaches 5.1V typ. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to V_{CC}. Also, if V_{CC} and VBATT start from 0.1V above the reset threshold and power is lost at V_{CC}, the SuperCap on VBATT discharges through V_{CC} until VBATT reaches the reset threshold; then the battery-backup mode is initiated and the current through V_{CC} goes to zero.

Using Separate Power Supplies for VBATT and V_{CC}

If using separate power supplies for V_{CC} and VBATT, VBATT must be less than 0.3V above V_{CC} when V_{CC} is above the reset threshold. As described in the previous section, if VBATT exceeds this limit and power is lost at V_{CC}, current flows continuously from VBATT to V_{CC} via the VBATT-to-V_{OUT} diode and the V_{OUT}-to-V_{CC} switch until the circuit is broken (Figure 8).

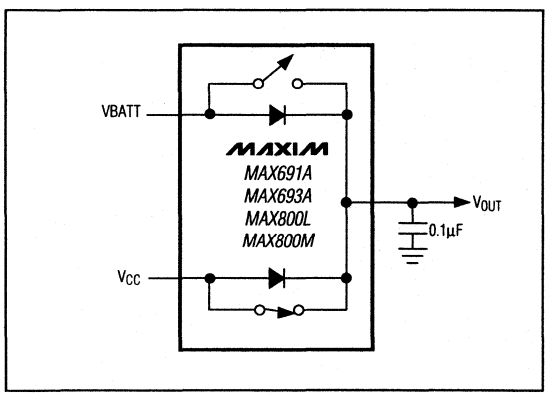


Figure 8. V_{CC} and VBATT to V_{OUT} Switch

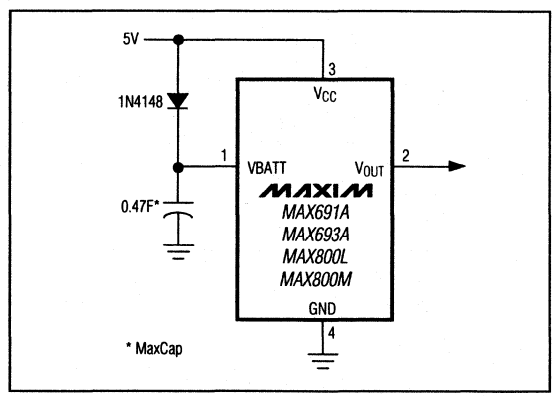


Figure 9. SuperCap or MaxCap on VBATT

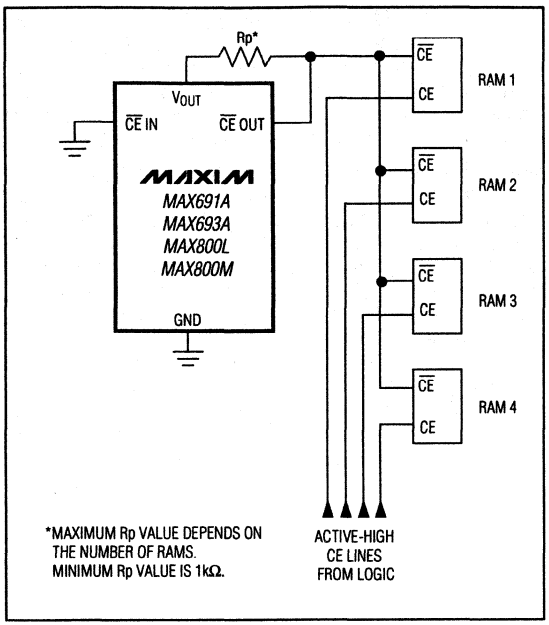


Figure 10. Alternate CE Gating

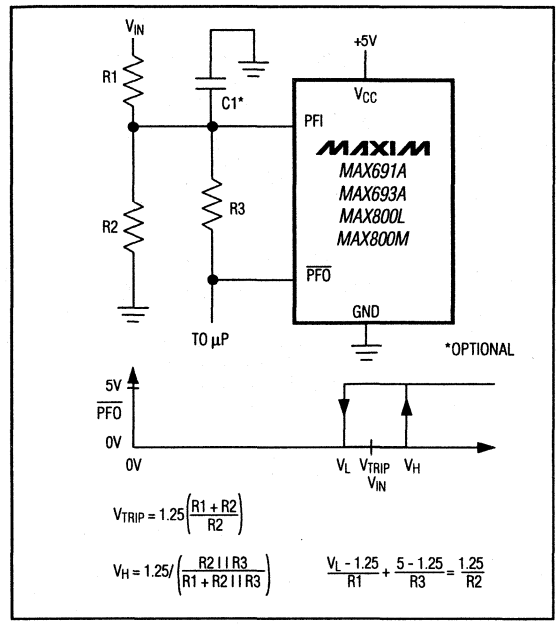


Figure 11. Adding Hysteresis to the Power-Fail Comparator

Alternative Chip-Enable Gating

Using memory devices with both CE and $\overline{CE}$ inputs allows the CE loop to be bypassed. To do this, connect $\overline{CE}$ IN to ground, pull-up $\overline{CE}$ OUT to V_{OUT}, and connect $\overline{CE}$ OUT to the $\overline{CE}$ input of each memory device (Figure 10). The CE input of each part then connects directly to the chip-select logic, which does not have to be gated.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of $\overline{PFO}$ when V_{IN} is near the power-fail comparator trip point. Figure 11 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

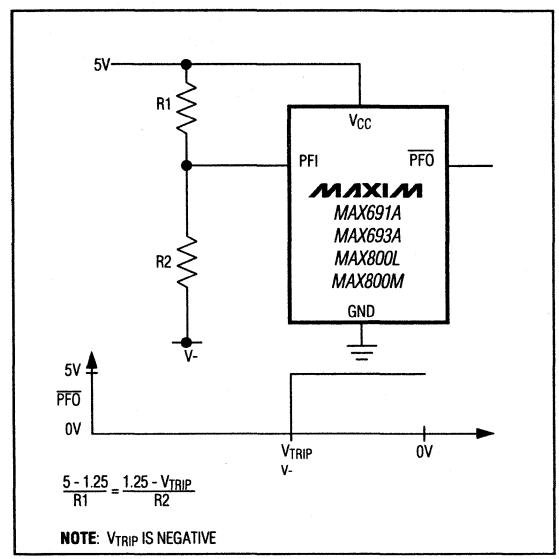


Figure 12. Monitoring a Negative Voltage

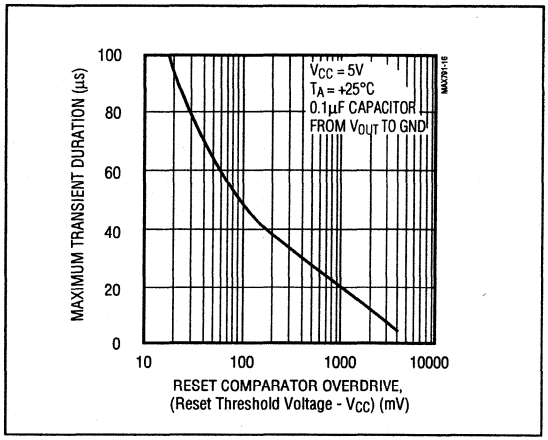


Figure 13. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using Figure 12's circuit. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

Backup-Battery Replacement

The backup battery may be disconnected while V_{CC} is above the reset threshold. No precautions are necessary to avoid spurious reset pulses.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 7 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX693ACPE	0°C to +70°C	16 Plastic DIP
MAX693ACSE	0°C to +70°C	16 Narrow SO
MAX693ACWE	0°C to +70°C	16 Wide SO
MAX693AC/D	0°C to +70°C	Dice*
MAX693AEPE	-40°C to +85°C	16 Plastic SO
MAX693AESE	-40°C to +85°C	16 Narrow SO
MAX693AEWE	-40°C to +85°C	16 Wide SO
MAX693AEJE	-40°C to +85°C	16 CERDIP
MAX693AMJE	-55°C to +125°C	16 CERDIP
MAX800LCPE	0°C to +70°C	16 Plastic DIP
MAX800LCSE	0°C to +70°C	16 Narrow SO
MAX800LEPE	-40°C to +85°C	16 Plastic DIP
MAX800LESE	-40°C to +85°C	16 Narrow SO
MAX800MCPE	0°C to +70°C	16 Plastic DIP
MAX800MCSE	0°C to +70°C	16 Narrow SO
MAX800MEPE	-40°C to +85°C	16 Plastic DIP
MAX800MESE	-40°C to +85°C	16 Narrow SO

** Dice are specified at T_A = +25°C, DC parameters only.*

19-0130; Rev 1; 4/94

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Low-Cost µP Supervisory Circuits with Battery Backup

General Description

The MAX703 and MAX704 microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX703/MAX704 are available in 8-pin DIP and SO packages and provide four functions:

1) An active-low reset during power-up, power-down, and brownout conditions.
2) Battery-backup switching for CMOS RAM, CMOS µPs, or other low-power logic circuitry.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual-reset input.

The MAX703 and MAX704 differ only in their supply-voltage monitor levels. The MAX703 generates a reset when the supply drops below 4.65V, while the MAX704 generates a reset below 4.4V.

Applications

Computers

Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

- ♦ **Battery-Backup Power Switching**
- ♦ **Precision Supply-Voltage Monitor**
  4.65V (MAX703)
  4.40V (MAX704)
- ♦ **200ms Reset Pulse Width**
- ♦ **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- ♦ **200µA Quiescent Current**
- ♦ **50nA Quiescent Current in Battery-Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **8-Pin DIP and SO Packages**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX703CPA	0°C to +70°C	8 Plastic DIP
MAX703CSA	0°C to +70°C	8 SO
MAX703C/D	0°C to +70°C	Dice*
MAX703EPA	-40°C to +85°C	8 Plastic DIP
MAX703ESA	-40°C to +85°C	8 SO
MAX703MJA	-55°C to +125°C	8 CERDIP**

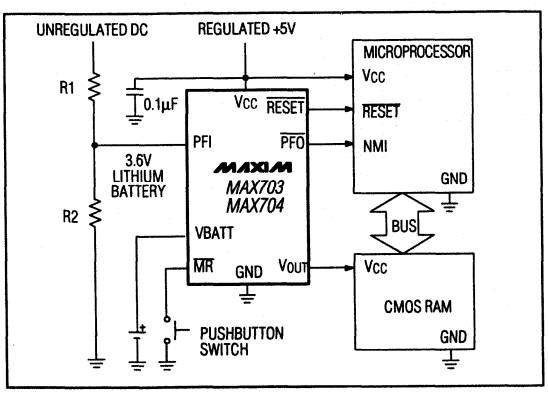
Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C only.*

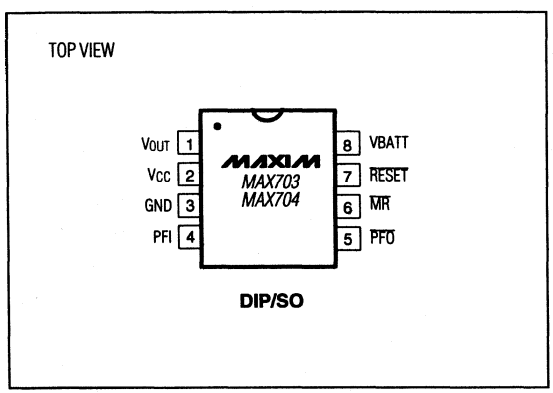
** *Contact factory for availability and processing to MIL-STD-883.*

5

Typical Operating Circuit



Pin Configuration



Low-Cost µP Supervisory Circuits with Battery Backup

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- VBATT ..... -0.3V to 6.0V
- All Other Inputs (Note 1) .....-0.3V to (V_{CB} + 0.3V)

Input Current
- V_{CC} 200mA
- VBATT 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10 sec
- All Other Outputs 20mA

Rate-of-Rise, V_{CC}, VBATT 100V/µs

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C__ .....0°C to +70°C
- MAX70_E__ ..... -40°C to +85°C
- MAX70_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: V_{CB} is the greater of V_{CC} and VBATT. The input voltage limits on PFI and $\overline{MR}$ may be exceeded if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX703, V_{CC} = +4.5V to +5.5V for MAX704, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOLS	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, VBATT (Note 2)				0		5.5	V
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX70_C			200	350	µA
		MAX70_E/M			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, VBATT = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A= T_{MIN} to T_{MAX}			5.0	
VBATT Standby Current (Note 3)		5.5V> V_{CC} > VBATT + 0.2V	T_A = +25°C	-0.1		0.02	µA
			T_A=T_{MIN} to T_{MAX}	-1.0		0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC}-0.05	V_{CC}-0.025		V
		I_{OUT} = 50mA		V_{CC}-0.5	V_{CC}-0.25		
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT}-0.2V		VBATT-0.1	VBATT-0.02		V
Battery-Switch Threshold (V_{CC} - VBATT)		V_{CC} < V_{RST}	Power-Up		20		mV
			Power-Down		-20		
Battery-Switchover Hysteresis					40		mV
$\overline{RESET}$ Threshold	V_{RST}	MAX703		4.50	4.65	4.75	V
		MAX704		4.25	4.40	4.50	
$\overline{RESET}$ Threshold Hysteresis					40		mV
$\overline{RESET}$ Pulse Width	t_{RST}			140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA		V_{CC}-1.5			V
	V_{OL}	I_{SINK} = 3.2mA				0.4	
		MAX70_C, V_{CC} = 1V, V_{CC} falling, VBATT = 0V, I_{SINK} = 50µA				0.3	
		MAX70_E/M, V_{CC} = 1.2V, V_{CC} falling, VBATT = 0V, I_{SINK} = 100µA				0.3	

19-4334; Rev. 3; 6/94

MAXIM

Low-Cost, µP Supervisory Circuits

General Description

The MAX705-MAX708/MAX813L microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX705/MAX706/MAX813L provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual-reset input.

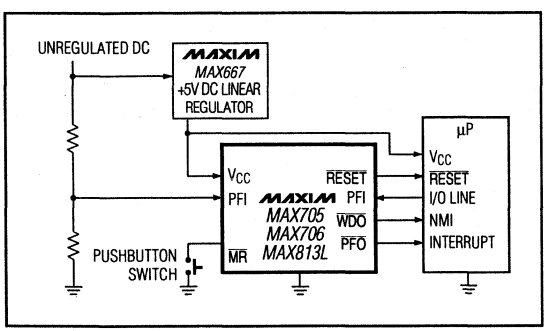
The MAX707/MAX708 are the same as the MAX705/MAX706, except an active-high reset is substituted for the watchdog timer. The MAX813L is the same as the MAX705, except RESET is provided instead of $\overline{\text{RESET}}$.

Two supply-voltage monitor levels are available: The MAX705/MAX707/MAX813L generate a reset pulse when the supply voltage drops below 4.65V, while the MAX706/MAX708 generate a reset pulse below 4.40V. All four parts are available in 8-pin DIP, SO and µMax packages.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

- **µMax Package: smallest 8-pin SO**
- **Guaranteed $\overline{\text{RESET}}$ Valid at V_{CC} = 1V**
- **Precision Supply-Voltage Monitor**
  4.65V in MAX705/MAX707/MAX813L
  4.40V in MAX706/MAX708
- **200ms Reset Pulse Width**
- **Debounced TTL/CMOS-Compatible Manual-Reset Input**
- **Independent Watchdog Timer – 1.6sec Timeout (MAX705/MAX706)**
- **Active-High Reset Output (MAX707/MAX708/MAX813L)**
- **200µA Quiescent Current**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**

Ordering Information

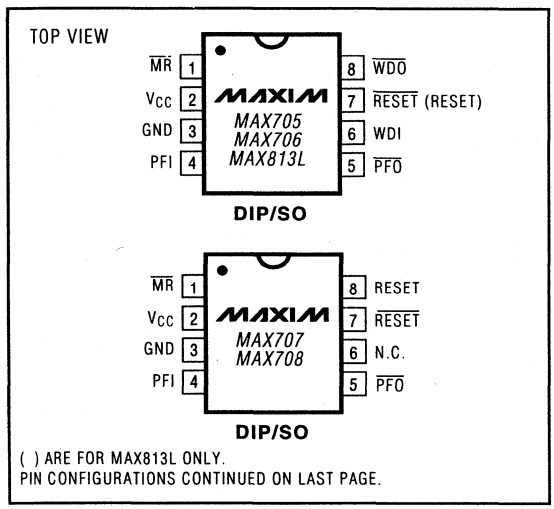
PART	TEMP. RANGE	PIN-PACKAGE
MAX705CPA	0°C to +70°C	8 Plastic DIP
MAX705CSA	0°C to +70°C	8 SO
MAX705CUA	0°C to +70°C	8 µMax
MAX705C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



( ) ARE FOR MAX813L ONLY.

PIN CONFIGURATIONS CONTINUED ON LAST PAGE.

Low-Cost, µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current (all outputs) 20mA

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- µMAX (derate 4.1mW/°C above +70°C) 330mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C__, MAX813LC__ ..... 0°C to +70°C
- MAX70_E__, MAX813LE__ ..... -40°C to +85°C
- MAX70_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.5V for MAX705/MAX707/MAX813L, V_{CC} = 4.5V to 5.5V for MAX706/MAX708 , T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	MAX70_C	1.0		5.5	V
		MAX813LC	1.1		5.5	
		MAX70_E/M, MAX813LE/M	1.2		5.5	
Supply Current	I_{SUPPLY}	MAX70_C, MAX813LC		200	350	µA
		MAX70_E/M, MAX813LE/M		200	500	
Reset Threshold (Note 2)	V_{RT}	MAX705, MAX707, MAX813L	4.50	4.65	4.75	V
		MAX706, MAX708	4.25	4.40	4.50	
Reset Threshold Hysteresis (Note 2)				40		mV
Reset Pulse Width (Note 2)	t_{RS}		140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		I_{SINK} = 3.2mA			0.4	
		MAX70_C, V_{CC} = 1V, I_{SINK} = 50µA			0.3	
		MAX70_E/M, V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
RESET Output Voltage		MAX707, MAX708, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		MAX707, MAX708, I_{SINK} = 1.2mA			0.4	
		MAX813LC, I_{SOURCE} = 4µA, V_{CC} = 1.1V	0.8			
		MAX813LE/M, I_{SOURCE} = 4µA, V_{CC} = 1.2V	0.9			
		MAX813L, I_{SOURCE} = 800µA	V_{CC} - 1.5			
		MAX813L, I_{SINK} = 3.2mA			0.4	
Watchdog Timeout Period	t_{WD}	MAX705, MAX706, MAX813L	1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (V_{CC}) (0.8)	50			ns
WDI Input Threshold — Low		MAX705, MAX706, MAX813L, V_{CC} = 5V			0.8	V
WDI Input Threshold — High			3.5			
WDI Input Current		MAX705, MAX706, MAX813L, WDI = V_{CC}		50	150	µA
		MAX705, MAX706, MAX813L, WDI = 0V	-150	-50		
$\overline{WDO}$ Output Voltage		MAX705, MAX706, MAX813L, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		MAX705, MAX706, MAX813L, I_{SINK} = 1.2mA			0.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

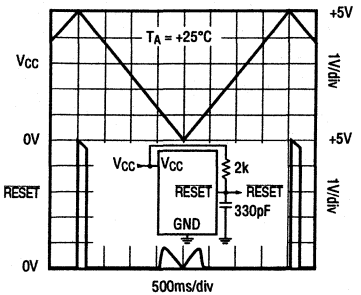
PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ Pull-Up Current			$\overline{MR}$ = 0V	100	250	600	µA
$\overline{MR}$ Pulse Width		t_{MR}		150			ns
$\overline{MR}$ Input Threshold	Low					0.8	V
	High			2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)		t_{MD}				250	ns
PFI Input Threshold			V_{CC} = 5V	1.20	1.25	1.30	V
PFI Input Current				-25.00	0.01	25.00	nA
$\overline{PFO}$ Output Voltage			I_{SOURCE} = 800µA	V_{CC} - 1.5			V
			I_{SINK} = 3.2mA			0.4	

Note 2: Applies to both $\overline{RESET}$ in the MAX705-MAX708 and RESET in the MAX707/MAX708/MAX813L.

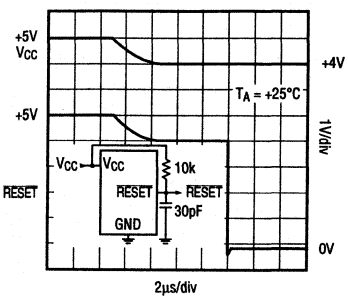
Low-Cost, µP Supervisory Circuits

Typical Operating Characteristics

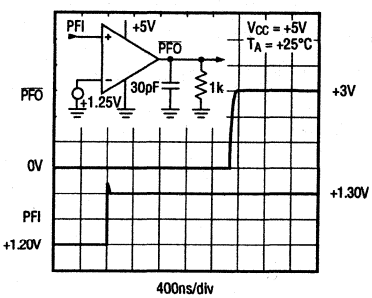
MAX705/MAX707
RESET OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



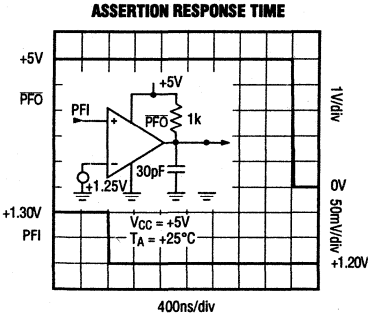
MAX705/MAX707
RESET RESPONSE TIME



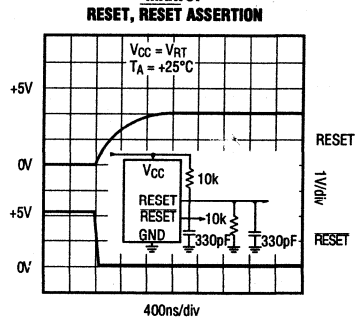
POWER-FAIL COMPARATOR
DE-ASSERTION RESPONSE TIME



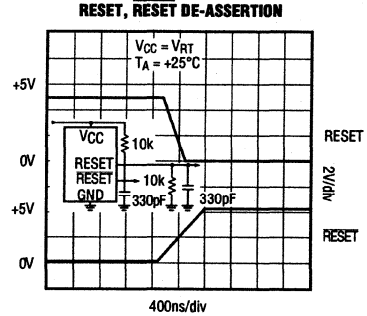
POWER-FAIL COMPARATOR
ASSERTION RESPONSE TIME



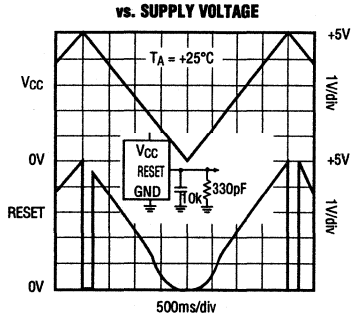
MAX707
RESET, RESET ASSERTION



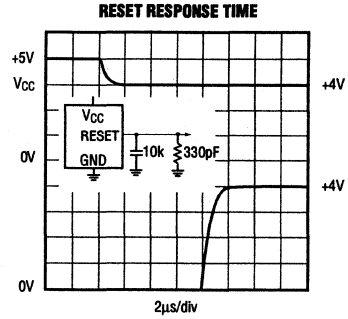
MAX707
RESET, RESET DE-ASSERTION



MAX707/MAX708/MAX813L
RESET OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE



MAX813L
RESET RESPONSE TIME



Pin Description

PIN						NAME	FUNCTION
MAX705/MAX706		MAX707/MAX708		MAX813L			
DIP/SO	µMax	DIP/SO	µMax	DIP/SO	µMax		
1	3	1	3	1	3	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250µA pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	4	2	4	2	4	V_{CC}	+5V Supply Input
3	5	3	5	3	5	GND	0V Ground Reference for all signals
4	6	4	6	4	6	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	7	5	7	5	7	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	8	-	-	6	8	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and WDO goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
-	-	6	-	-	-	N.C.	No Connect
7	1	7	1	-	-	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (4.65V in the MAX705 and 4.40V in the MAX706). It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high (Figure 3). A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	2	-	-	8	2	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.
-	-	8	2	7	1	RESET	Active-High Reset Output is the inverse of $\overline{RESET}$. Whenever $\overline{RESET}$ is high, RESET is low, and vice versa (Figure 2). The MAX813L has a RESET output only.

Low-Cost, µP Supervisory Circuits

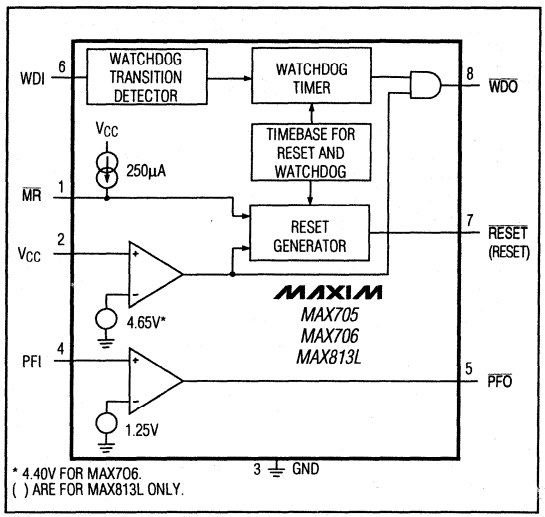


Figure 1. MAX705/MAX706/MAX813L Block Diagram

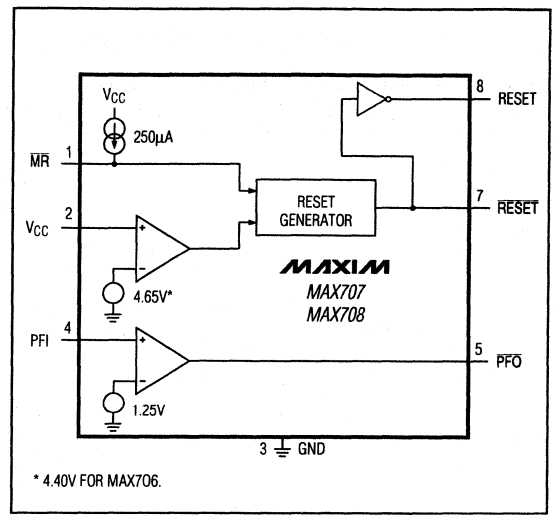


Figure 2. MAX707/MAX708 Block Diagram

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX705-MAX708/MAX813L assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} dips below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The MAX707/MAX708/MAX813L active-high RESET output is simply the complement of the $\overline{RESET}$ output, and is guaranteed to be valid with V_{CC} down to 1.1V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The MAX705/MAX706/MAX813L watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not three-stated, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is three-stated, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

The MAX705/MAX706 have a watchdog timer and a $\overline{RESET}$ output. The MAX707/MAX708 have both active-high and active-low reset outputs. The MAX813L has both an active-high reset output and a watchdog timer.

Manual Reset

The manual-reset input ($\overline{MR}$) allows reset to be triggered by a push button switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in the MAX705/MAX706/MAX813L. Simply connect $\overline{WDO}$ to $\overline{MR}$.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

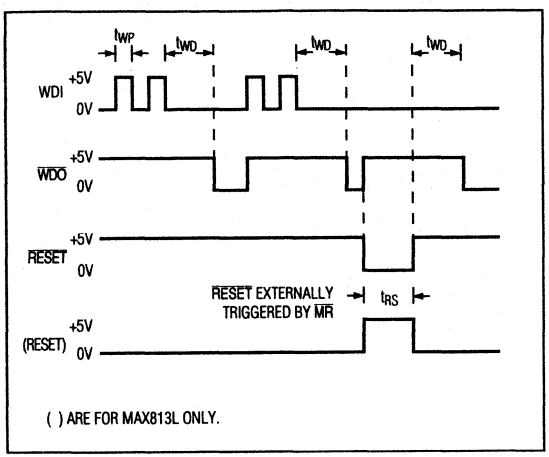


Figure 3. MAX705/MAX706/MAX813L Watchdog Timing

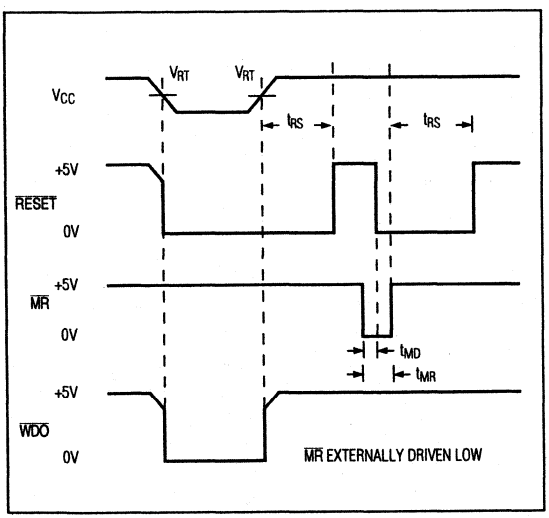


Figure 4. MAX705/MAX706 RESET, MR, and WDO Timing with WDI Three-Stated. The MAX707/MAX708/MAX813L RESET output is the inverse of RESET shown.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see *Typical Operating Circuit*). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

Applications Information

Ensuring a Valid RESET Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX705-MAX708 RESET output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load RESET and small enough to pull RESET to ground.

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on other voltages in addition to the +5V V_{CC} line. Connect PFO to MR to initiate a RESET pulse when PFI drops below 1.25V. Figure 6 shows the MAX705-MAX708 configured to assert RESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), PFO is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers reset. As long as PFO remains high, the MAX705-MAX708/MAX813L will keep reset asserted (RESET = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

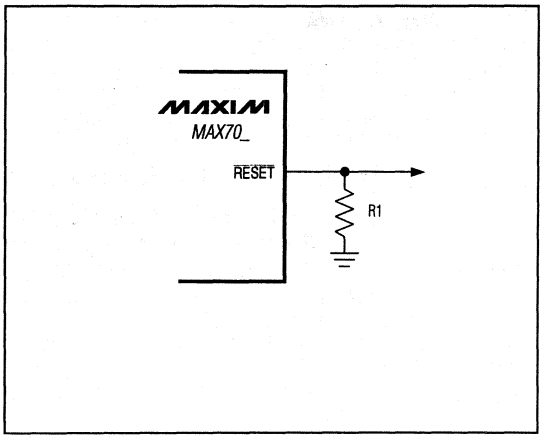
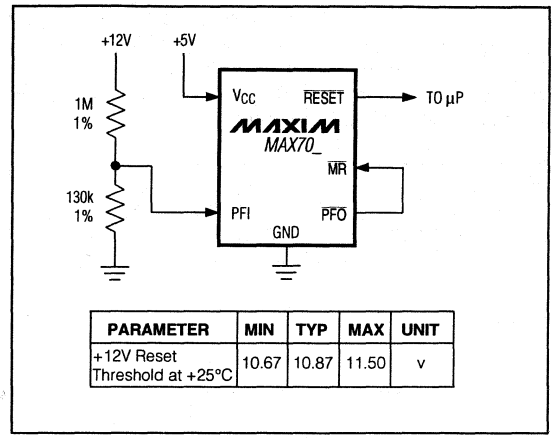


Figure 5. RESET Valid to Ground Circuit



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.67	10.87	11.50	v

Figure 6. Monitoring Both +5V and +12V

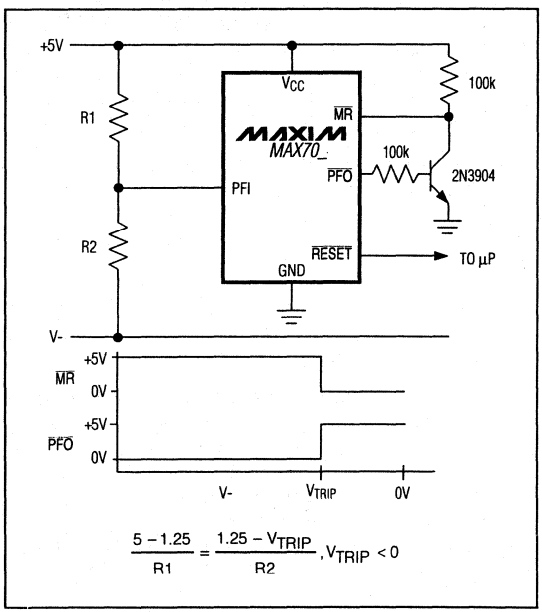


Figure 7. Monitoring a Negative Voltage

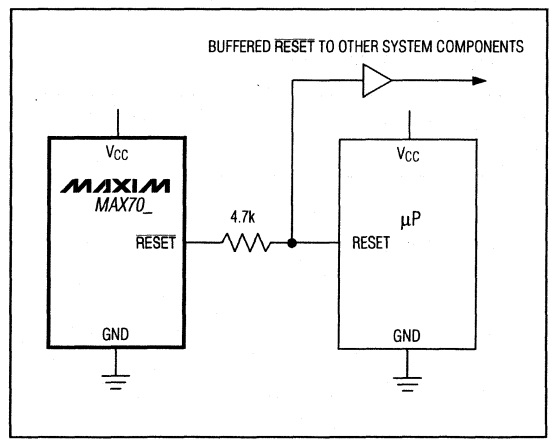


Figure 8. Interfacing to µPs with Bidirectional Reset I/O

Interfacing to µPs with Bidirectional Reset Pins

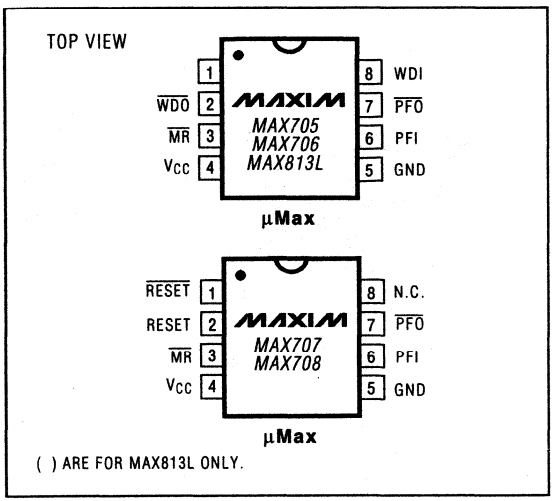
µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX705-MAX708 RESET output. If, for example, the RESET output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O, as in Figure 8. Buffer the RESET output to other system components.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX705EPA	-40°C to +85°C	8 Plastic DIP
MAX705ESA	-40°C to +85°C	8 SO
MAX705MJA	-55°C to +125°C	8 CERDIP**
MAX706CPA	0°C to +70°C	8 Plastic DIP
MAX706CSA	0°C to +70°C	8 SO
MAX706CUA	0°C to +70°C	8 µMax
MAX706C/D	0°C to +70°C	Dice*
MAX706EPA	-40°C to +85°C	8 Plastic DIP
MAX706ESA	-40°C to +85°C	8 SO
MAX706MJA	-55°C to +125°C	8 CERDIP**
MAX707CPA	0°C to +70°C	8 Plastic DIP
MAX707CSA	0°C to +70°C	8 SO
MAX707CUA	0°C to +70°C	8 µMax
MAX707C/D	0°C to +70°C	Dice*
MAX707EPA	-40°C to +85°C	8 Plastic DIP
MAX707ESA	-40°C to +85°C	8 SO
MAX707MJA	-55°C to +125°C	8 CERDIP**
MAX708CPA	0°C to +70°C	8 Plastic DIP
MAX708CSA	0°C to +70°C	8 SO
MAX708CUA	0°C to +70°C	8 µMax
MAX708C/D	0°C to +70°C	Dice*
MAX708EPA	-40°C to +85°C	8 Plastic DIP
MAX708ESA	-40°C to +85°C	8 SO
MAX708MJA	-55°C to +125°C	8 CERDIP**
MAX813LCPA	0°C to +70°C	8 Plastic DIP
MAX813LCSA	0°C to +70°C	8 SO
MAX813LCUA	0°C to +70°C	8 µMax
MAX813LC/D	0°C to +70°C	Dice*
MAX813LEPA	-40°C to +85°C	8 Plastic DIP
MAX813LESA	-40°C to +85°C	8 SO
MAX813LMJA	-55°C to +125°C	8 CERDIP**

*Dice are specified at T_A = +25°C.
**Contact factory for availability and processing to MIL-STD-883.

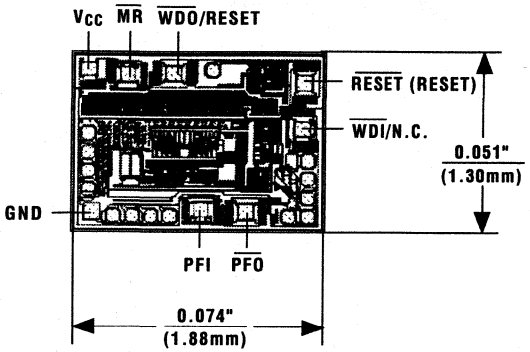
Pin Configuration (continued)



( ) ARE FOR MAX813L ONLY.

Low-Cost, µP Supervisory Circuits

Chip Topography



( ) ARE FOR MAX813L ONLY.
TRANSISTOR COUNT: 572
SUBSTRATE MUST BE LEFT UNCONNECTED.

19-0099; Rev 0; 10/92

MAXIM

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

General Description

The MAX706P/R/S/T and MAX708R/S/T microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor +3V power-supply levels in +3V to +5V µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX706P/R/S/T supervisory circuits provide the following four functions:

1) A reset output during power-up, power-down and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6sec.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than the main supply.
4) An active-low manual-reset input.

The only difference among the MAX706R, MAX706S, and MAX706T is the reset-threshold voltage levels, which are 2.63V, 2.93V, and 3.08V respectively. All have active-low reset output signals. The MAX706P is identical to the MAX706R, except its reset output signal is active-high.

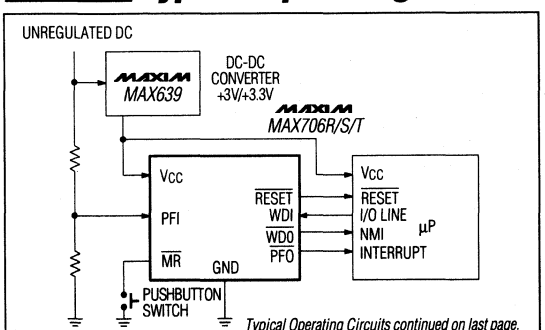
The MAX708R/S/T provide the same functions as the MAX706R/S/T, except they do not have a watchdog timer. Instead, they provide both $\overline{\text{RESET}}$ and RESET outputs. As with the MAX706, devices with R, S, and T suffixes have reset thresholds of 2.63V, 2.93V and 3.08V respectively.

All seven devices are packaged in 8-pin SO and DIP.

Applications

Battery-Powered Equipment
Portable Instruments
Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring

Typical Operating Circuits



Typical Operating Circuits continued on last page.

Features

- **Precision Supply-Voltage Monitor**
  2.63V (MAX706P/R, MAX708R)
  2.93V (MAX706S, MAX708S)
  3.08V (MAX706T, MAX708T)
- **200ms Reset Time Delay**
- **Debounced TTL-/CMOS-Compatible Manual-Reset Input**
- **100µA Quiescent Current**
- **Watchdog Timer (MAX706P/R/S/T only) – 1.6sec Timeout**
- **Reset Output Signal:**
  Active-High Only (MAX706P)
  Active-Low Only (MAX706R/S/T)
  Active-High and Active-Low (MAX708R/S/T)
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **8-Pin Surface-Mount Package**
- **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**

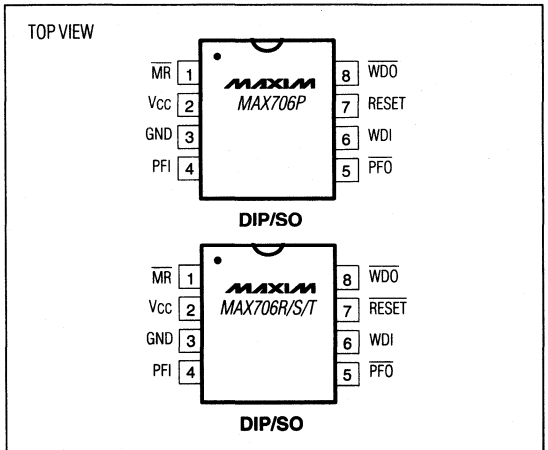
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX706PCPA	0°C to +70°C	8 Plastic DIP
MAX706PCSA	0°C to +70°C	8 SO
MAX706PC/D	0°C to +70°C	Dice*
MAX706PEPA	-40°C to +85°C	8 Plastic DIP
MAX706PESA	-40°C to +85°C	8 SO
MAX706PMJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

** Dice are tested at T_A = +25°C only.*
***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Pin Configurations continued on last page.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current (all outputs) 20mA

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70__C__ ..... 0°C to +70°C
- MAX70__E__ ..... -40°C to +85°C
- MAX70__M__ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The input voltage limits on PFI, WDI, and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX70_P/R: V_{CC} = 2.70V to 5.5V, MAX70_S: V_{CC} = 3.00V to 5.5V, MAX70_T: V_{CC} = 3.15V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		MAX70__C	1.0		5.5	V
			MAX70__E/M	1.2		5.5	
Supply Current	I_{SUPPLY}	V_{CC} < 3.6V	MAX70__C		100	200	µA
			MAX70__E/M		100	300	
		V_{CC} < 5.5V	MAX70__C		150	350	
			MAX70__E/M		150	500	
Reset Threshold (Note 2)	V_{RST}		MAX70_P/R	2.55	2.63	2.70	V
			MAX70_S	2.85	2.93	3.00	
			MAX70_T	3.00	3.08	3.15	
Reset Threshold Hysteresis (Note 2)					20		mV
Reset Pulse Width (Note 2)	t_{RST}	MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V		140	200	280	ms
		V_{CC} = 5.0V			200		
$\overline{RESET}$ Output Voltage (MAX70_R/S/T)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	
	V_{OL}	MAX70__C: V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		MAX70__E/M: V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
RESET Output Voltage (MAX706P)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 215µA	V_{CC} - 0.6			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		ISINK = 3.2mA			0.4	

ELECTRICAL CHARACTERISTICS (continued)

(MAX70_P/R: V_{CC} = 2.70V to 5.5V, MAX70_S: V_{CC} = 3.00V to 5.5V, MAX70_T: V_{CC} = 3.15V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

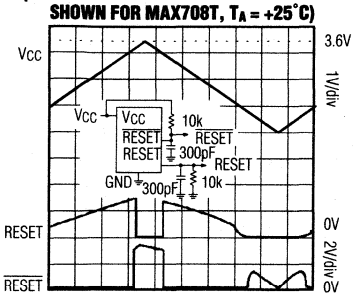
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX708_)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 1.2mA			0.4	
Watchdog Timeout Period (MAX706_)	t_{WD}	MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V		1.0	1.6	2.25	sec
WDI Pulse Width (MAX706_)	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}	V_{RST}(max) < V_{CC} < 3.6V	100			ns
			4.5V < V_{CC} < 5.5V	50			
WDI Input Threshold (MAX706_)	V_{IL}	V_{RST} (max) < V_{CC} < 3.6V	Low			0.6	V
	V_{IH}		High	0.7 x V_{CC}			
	V_{IL}	V_{CC} = 5.0V	Low			0.8	
	V_{IH}		High	3.5			
WDI Input Current (MAX706_)		WDI = 0V or V_{CC}		-1.0	0.02	1.0	µA
$\overline{WDO}$ Output Voltage (MAX706_)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 1.2mA			0.4	
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	V_{RST} (max) < V_{CC} < 3.6V	25	70	250	µA
			4.5V < V_{CC} < 5.5V	100	250	600	
$\overline{MR}$ Pulse Width	t_{MR}	V_{RST} (max) < V_{CC} < 3.6V		500			ns
		4.5V < V_{CC} < 5.5V		150			
$\overline{MR}$ Input Threshold	V_{IL}	V_{RST} (max) < V_{CC} < 3.6V	Low			0.6	V
	V_{IH}		High	0.7 x V_{CC}			
	V_{IL}	4.5V < V_{CC} < 5.5V	Low			0.8	
	V_{IH}		High	2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)	t_{MD}	V_{RST} (max) < V_{CC} < 3.6V				750	ns
		4.5V < V_{CC} < 5.5V				250	
PFI Input Threshold		MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V, PFI falling		1.20	1.25	1.30	V
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	

Note 2: Applies to both $\overline{RESET}$ in the MAX70_R/S/T, and RESET in the MAX706P and MAX708R/S/T.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

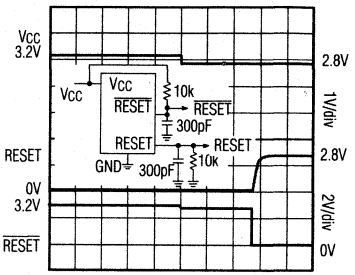
Typical Operating Characteristics

RESET, $\overline{\text{RESET}}$ OUTPUT VOLTAGES vs. SUPPLY VOLTAGE (RESET OUTPUTS AND RESET THRESHOLDS SHOWN FOR MAX708T, T_A = +25°C)



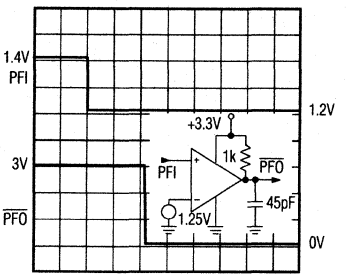
500ms/div

RESET, $\overline{\text{RESET}}$ RESPONSE TIMES



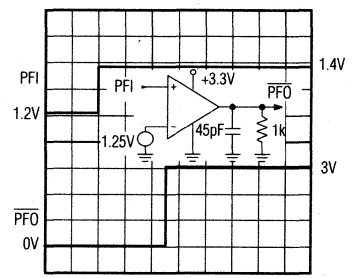
2µs/div

POWER-FAIL COMPARATOR ASSERTION RESPONSE TIME



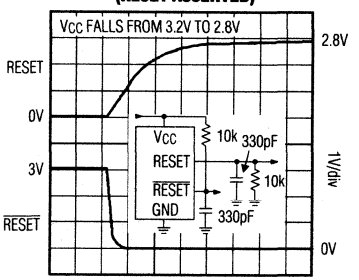
1µs/div

POWER-FAIL COMPARATOR DEASSERTION RESPONSE TIME



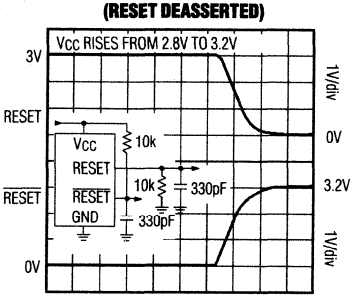
500ns/div

RESET, $\overline{\text{RESET}}$ RISE AND FALL TIMES (RESET ASSERTED)



200ns/div

RESET, $\overline{\text{RESET}}$ RISE AND FALL TIMES (RESET DEASSERTED)



200ns/div

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

Pin Description

PIN			NAME	FUNCTION
MAX706P	MAX706R/S/T	MAX708R/S/T		
1	1	1	$\overline{MR}$	Manual-Reset Input. When pulled below 0.6V, $\overline{MR}$ triggers a reset pulse. It is TTL/CMOS compatible when V_{CC} = 5V and can be shorted to ground with a switch. This active-low input has an internal 70µA pull-up current. Leave floating or connect to V_{CC} if not used.
2	2	2	V_{CC}	Supply-Voltage Input
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND when not used.
5	5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low and sinks current; otherwise, $\overline{PFO}$ remains high. Leave unconnected if not used.
6	6	–	WDI	Watchdog Input. A rising or falling edge must occur at WDI within 1.6sec or $\overline{WDO}$ goes low (Figure 4). The internal watchdog timer is reset to zero when reset is asserted or when a transition occurs at WDI. The watchdog function cannot be disabled.
–	–	6	N.C.	No Connect – not internally connected.
–	7	7	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ remains low while V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains low for 200ms after the reset conditions are terminated (Figure 3).
7	–	8	RESET	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains high for 200ms after the reset conditions are terminated (Figure 3).
8	8	–	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low when a transition does not occur at WDI within 1.6sec, and remains low until a transition occurs at WDI (indicating the watchdog interrupt has been serviced). $\overline{WDO}$ also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output signal, $\overline{WDO}$ goes high as soon as V_{CC} exceeds the reset threshold.

Detailed Description

$\overline{RESET}$ and RESET Outputs

A microprocessor's (µP's) reset input starts it in a known state. When the µP is in an unknown state, it should be held in reset. The MAX706P/R/S/T and MAX708R/S/T assert reset when V_{CC} is low, preventing code execution errors during power-up, power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low and RESET is guaranteed to be a logic high. As V_{CC} rises, $\overline{RESET}$ and RESET remain asserted. Once V_{CC} exceeds the reset threshold, the internal timer causes $\overline{RESET}$ and RESET to be deasserted after a time equal to the reset pulse width, which is typically 200ms (Figure 3). If a power-fail or brownout condition occurs (i.e. V_{CC} drops below the reset threshold), $\overline{RESET}$ and RESET are asserted. As long as V_{CC} remains below the reset threshold, the internal timer is continually reset, causing the $\overline{RESET}$ and RESET outputs to remain asserted. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-down, once V_{CC} drops below the reset threshold, $\overline{RESET}$ and RESET are guaranteed to be asserted for $V_{CC} \geq 1V$.

The MAX706P provides a RESET signal, the MAX706R/S/T provide a $\overline{RESET}$ signal, and the MAX708R/S/T provide both RESET and $\overline{RESET}$.

Watchdog Timer (MAX706P/R/S/T)

The MAX706P/R/S/T watchdog circuit monitors the µP's activity. If the µP does not toggle the Watchdog Input (WDI) within 1.6sec, the Watchdog Output ($\overline{WDO}$) goes low (Figure 4). If the reset signal is asserted, the watchdog timer will be reset to zero and disabled. As soon as reset is released, the timer starts counting. WDI can detect pulses as narrow as 100ns with a 2.7V supply and 50ns with a 4.5V supply.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

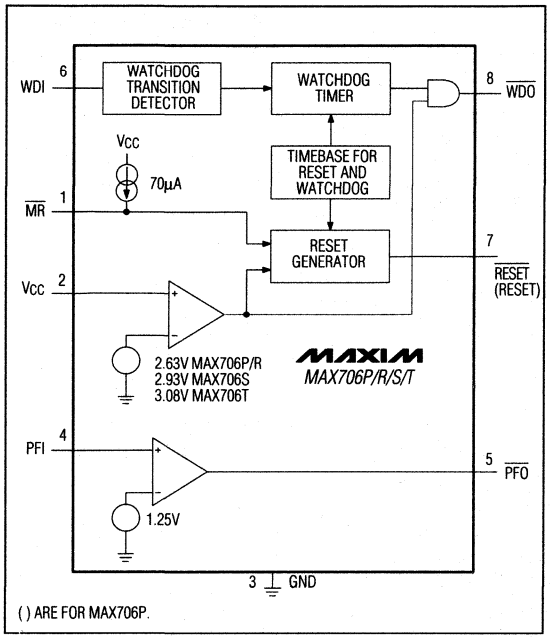


Figure 1. MAX706P/R/S/T Block Diagram

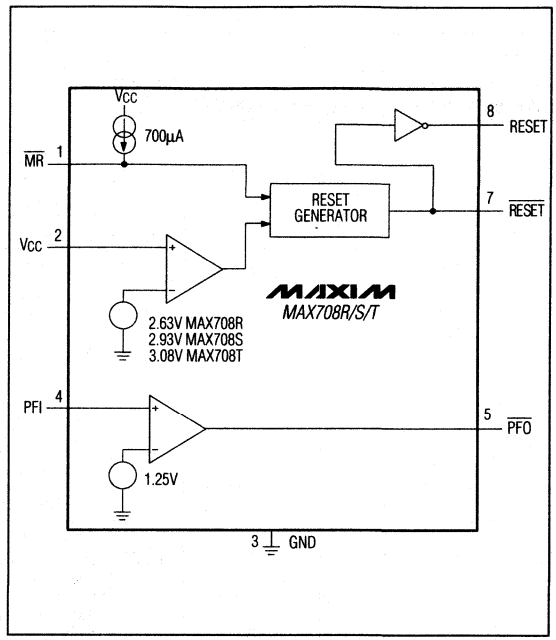


Figure 2. MAX708R/S/T Block Diagram

WDO can be connected to the non-maskable interrupt (NMI) input of a µP. When VCC drops below the reset threshold, WDO immediately goes low, even if the watchdog timer has not timed out (Figure 3). Normally, this would trigger an NMI, but since reset is asserted simultaneously, the NMI is overridden. WDO can instead be connected to MR to generate a reset pulse when the watchdog times out.

Manual Reset

The Manual-Reset (MR) input allows RESET and RESET to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. MR can be driven by an external logic line since it is TTL/CMOS compatible. The minimum MR input pulse width is 500ns when VCC = +3V and 150ns when VCC = +5V. Leave MR floating or tie to VCC when not used.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference. The power-fail comparator has 10mV of hysteresis which prevents repeated triggering of the Power-Fail Output (PFO).

To build an early-warning power-failure circuit, use the Power- Fail Comparator Input (PFI) to monitor the unregulated DC supply voltage (see *Typical Operating Circuit*). Connect the PFI pin to a resistor-divider network such that the voltage at PFI falls below 1.25V just before the regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

Regulated and unregulated voltages can be monitored by simply adjusting the PFI resistor-divider network values to the appropriate ratio. In addition, the reset signal can be asserted at voltages other than the VCC reset threshold, as shown in Figure 5. Connect PFO to MR to initiate a reset pulse when the 12V supply drops below a user-specified threshold (11V in this example) or when VCC falls below the reset threshold.

Applications Information

Operation with +3V and +5V Supplies

The MAX706P/R/S/T and MAX708R/S/T provide voltage monitoring at the reset threshold (2.63V to 3.08V) when powered from either +3V or +5V. They are ideal in porta-

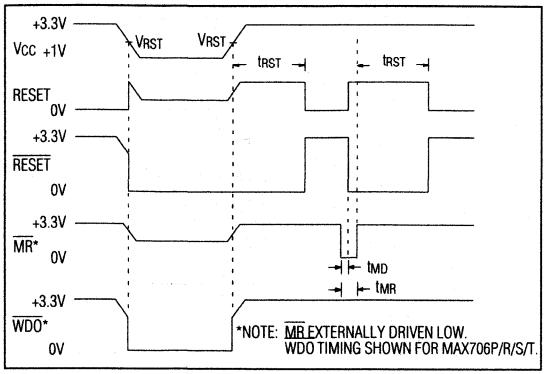


Figure 3. RESET, RESET, MR and WDO Timing

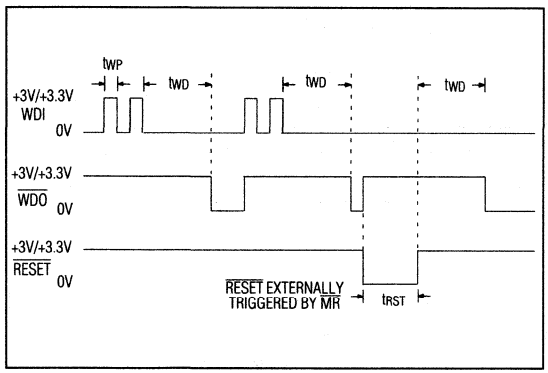
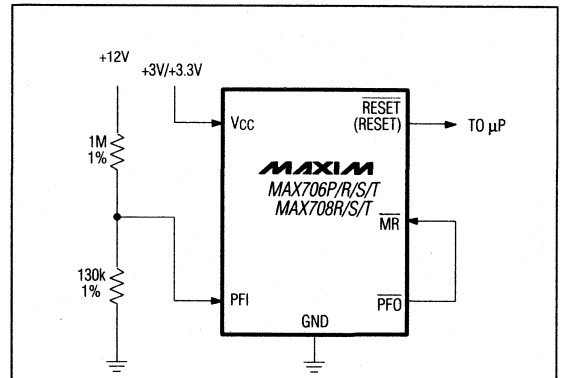


Figure 4. MAX706P/R/S/T Watchdog Timing

ble-instrument applications where power can be supplied from either a +3V battery or an AC- DC wall adapter that generates +5V (a +5V supply allows a µP or a microcontroller to run faster than a +3V supply). With a +3V supply, these ICs consume less power, but output drive capability is reduced, the MR-to-RESET delay time increases, and the MR minimum pulse width increases. The *Electrical Characteristics* table provides specifications for operation with both +3V and +5V supplies.

Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX706R/S/T and MAX708R/S/T RESET output no longer sinks current; it becomes an open circuit. High-impedance, CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the RESET pin, as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding RESET low. Resistor



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.24	10.87	11.50	V

( ) ARE FOR MAX706P.

Figure 5. Monitoring Both +3V/+3.3V and +12V

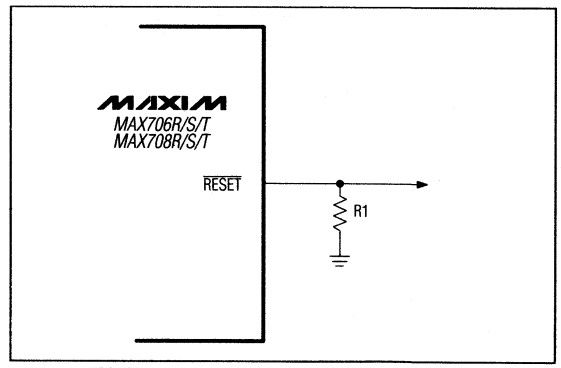


Figure 6. RESET Valid to Ground Circuit

value R1 is not critical, but it should not load RESET and should be small enough to pull RESET and the input it is driving to ground. 100kΩ is suggested for R1.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. R3 will typically be an order of

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA max PFI input current does not shift the trip point significantly. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit of Figure 8. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage droops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

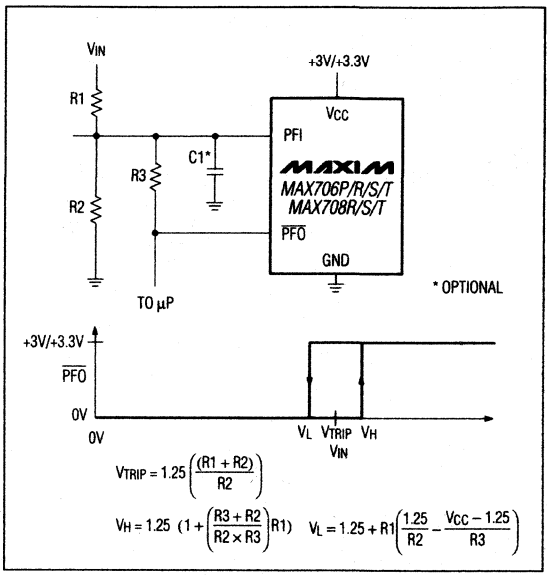


Figure 7. Adding Hysteresis to the Power-Fail Comparator

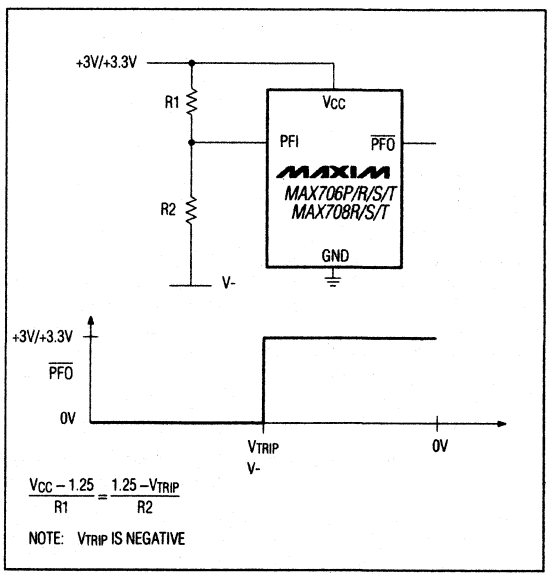


Figure 8. Monitoring a Negative Voltage

Table 1. Maxim µP Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt-On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706 R/S/T	4.40/2.63 2.93/3.08	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706P	2.63	140	1.6	no	no	yes	yes	yes	no	yes	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708 R/S/T	4.40/2.63 2.93/3.08	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.50/4.75	250	0.15/0.60/ 1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

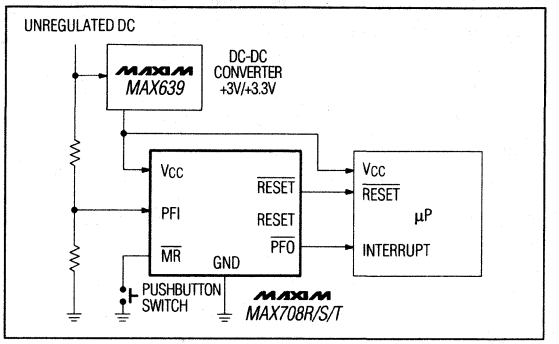
+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

Ordering Information (continued)

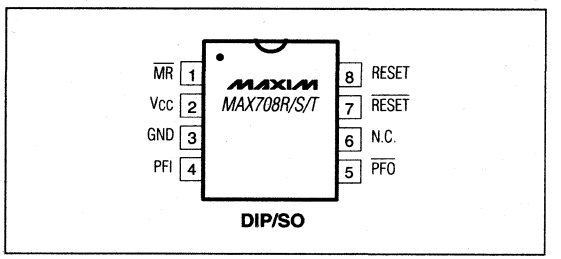
PART	TEMP. RANGE	PIN-PACKAGE
MAX706RCPA	0°C to +70°C	8 Plastic DIP
MAX706RCSA	0°C to +70°C	8 SO
MAX706RC/D	0°C to +70°C	Dice*
MAX706REPA	-40°C to +85°C	8 Plastic DIP
MAX706RESA	-40°C to +85°C	8 SO
MAX706RMJA	-55°C to +125°C	8 CERDIP**
MAX706SCPA	0°C to +70°C	8 Plastic DIP
MAX706SCSA	0°C to +70°C	8 SO
MAX706SC/D	0°C to +70°C	Dice*
MAX706SEPA	-40°C to +85°C	8 Plastic DIP
MAX706SESA	-40°C to +85°C	8 SO
MAX706SMJA	-55°C to +125°C	8 CERDIP**
MAX706TCPA	0°C to +70°C	8 Plastic DIP
MAX706TCSA	0°C to +70°C	8 SO
MAX706TC/D	0°C to +70°C	Dice*
MAX706TEPA	-40°C to +85°C	8 Plastic DIP
MAX706TESA	-40°C to +85°C	8 SO
MAX706TMJA	-55°C to +125°C	8 CERDIP**
MAX708RCPA	0°C to +70°C	8 Plastic DIP
MAX708RCSA	0°C to +70°C	8 SO
MAX708RC/D	0°C to +70°C	Dice*
MAX708REPA	-40°C to +85°C	8 Plastic DIP
MAX708RESA	-40°C to +85°C	8 SO
MAX708RMJA	-55°C to +125°C	8 CERDIP**
MAX708SCPA	0°C to +70°C	8 Plastic DIP
MAX708SCSA	0°C to +70°C	8 SO
MAX708SC/D	0°C to +70°C	Dice*
MAX708SEPA	-40°C to +85°C	8 Plastic DIP
MAX708SESA	-40°C to +85°C	8 SO
MAX708SMJA	-55°C to +125°C	8 CERDIP**
MAX708TCPA	0°C to +70°C	8 Plastic DIP
MAX708TCSA	0°C to +70°C	8 SO
MAX708TC/D	0°C to +70°C	Dice*
MAX708TEPA	-40°C to +85°C	8 Plastic DIP
MAX708TESA	-40°C to +85°C	8 SO
MAX708TMJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuits (continued)



Pin Configurations (continued)



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

+3V-Voltage-Monitoring µP Supervisory Circuits

General Description

The MAX793/MAX794/MAX795 monitor and control the activities of +3V microprocessors (µPs) by providing backup-battery switchover, as well as low-line resets, write protection for CMOS RAM, and watchdog functions. The backup-battery voltage can exceed V_{CC}, permitting the use of 3.6V lithium batteries in systems using 3.0V or 3.3V for V_{CC}.

The MAX795 comes in 8-pin packages and provides the following three functions:

1) Precision active-low $\overline{RESET}$ during power-up, power-down, and brownout conditions.
2) Backup-battery switching for CMOS RAM, CMOS µPs, or other low-power logic circuitry. 75mA is available from VOUT in normal mode, and 1mA is available in battery-backup mode. The normal-mode output can be boosted with an external transistor controlled by BATT ON.
3) Write protection of CMOS RAM or EEPROM.

The MAX793/MAX794 come in 16-pin packages and perform the same functions as the MAX795, plus the following:

1) Active-high RESET (in addition to active-low $\overline{RESET}$).
2) Separate watchdog output pulse if the watchdog timer has not been toggled within 1.6sec, which can optionally be wired to generate a reset.
3) 1.23V threshold detector for power-fail warning, low-battery detection, or monitoring a power supply other than +3V.
4) Low-line output indicating when the power supply falls to a point 45mV above the reset threshold.
5) Active-low manual-reset input, $\overline{MR}$.
6) Ship mode that protects the backup battery until the end-user activates the device.
7) Backup-battery level monitor (MAX793 only).

The MAX793/MAX795 are available in four versions, each with a unique reset trip voltage. The MAX794 has a user-defined reset threshold, and so is available in only one version.

Applications

Battery-Powered Computers and Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

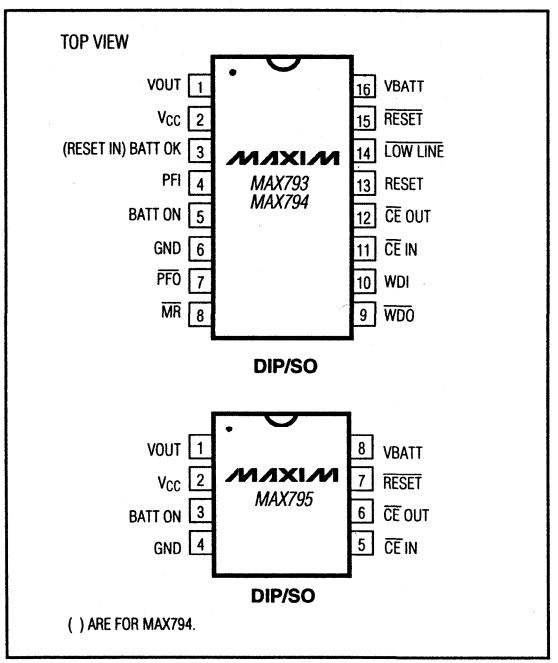
MAX793/MAX794/MAX795

- **Precision Supply-Voltage Monitor**
  Fixed Reset Trip Voltage (MAX793/MAX795)
  Adjustable Reset Trip Voltage (MAX794)
- **Guaranteed Reset Assertion to V_{CC} = 1V**
- **Backup-Battery Power Switching—Battery Voltage Can Exceed V_{CC}**
- **On-Board Gating of Chip-Enable Signals—10ns Max Propagation Delay**

MAX793/MAX794 Only

- **Active-High and Active-Low Reset Outputs**
- **Separate Watchdog Timer Output—1.6sec Timeout**
- **Low-Line Output Allows Early Warning of Power Failure**
- **Power-Fail Comparator**
- **Manual Reset Input**
- **Ship Mode Protects Battery Until Unit Activates**
- **Battery OK Monitor (MAX793 only)**

Pin Configurations



+3V-Voltage-Monitoring µP Supervisory Circuits

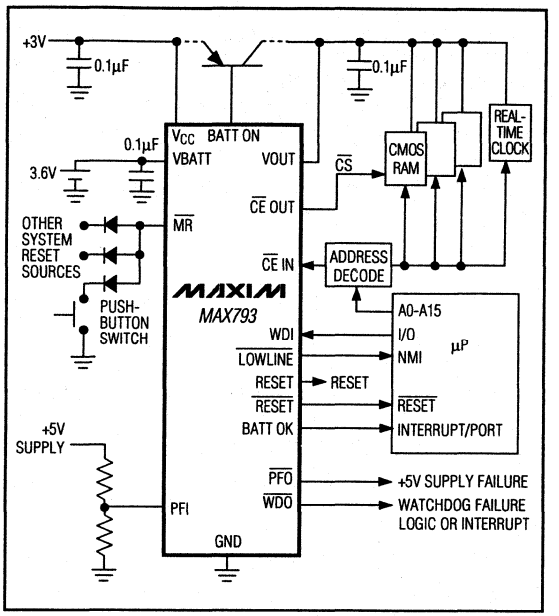
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX793_CPE	0°C to +70°C	16 Plastic DIP
MAX793_CSE	0°C to +70°C	16 Narrow SO
MAX793_EPE	-40°C to +85°C	16 Plastic DIP
MAX793_ESE	-40°C to +85°C	16 Narrow SO
MAX793_MJE	-55°C to +125°C	16 CERDIP
MAX794CPE	0°C to +70°C	16 Plastic DIP
MAX794CSE	0°C to +70°C	16 Narrow SO
MAX794EPE	-40°C to +85°C	16 Plastic DIP
MAX794ESE	-40°C to +85°C	16 Narrow SO
MAX794MJE	-55°C to +125°C	16 CERDIP
MAX795_CPA	0°C to +70°C	8 Plastic DIP
MAX795_CSA	0°C to +70°C	8 Narrow SO
MAX795_EPA	-40°C to +85°C	8 Plastic DIP
MAX795_ESA	-40°C to +85°C	8 Narrow SO
MAX795_MJA	-55°C to +125°C	8 CERDIP

†*For the MAX793 and MAX795, insert the desired suffix into the blank to complete the part number:*

SUFFIX	RESET THRESHOLD (V)	
	MIN	MAX
T	3.00	3.15
U	3.00	3.13
S	2.85	3.00
R	2.55	2.70

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

µP Supervisory Circuit with ±1.5% Reset Accuracy

General Description

The MAX807 microprocessor (µP) supervisory circuit reduces the complexity and number of components needed to monitor power-supply and battery-control functions in µP systems. A 60µA supply current makes the MAX807 ideal for use in portable equipment, while a 6ns chip-enable propagation delay and 250mA output current capability (20mA in battery-backup mode) make it suitable for larger, higher-performance equipment.

The MAX807 comes in 16-pin DIP and SO packages, and provides the following functions:

1) µP reset. The active-low $\overline{\text{RESET}}$ output is asserted during power-up, power-down, and brownout conditions, and is guaranteed to be in the correct state for V_{CC} down to 1V.
2) Active-high RESET output.
3) Manual-reset input.
4) Two-stage power-fail warning. A separate low-line comparator compares V_{CC} to a threshold 30mV above the reset threshold. This low-line comparator is more accurate than those in previous µP supervisors.
5) Backup-battery switchover for CMOS RAM, real-time clocks, µPs, or other low-power logic.
6) Write protection of CMOS RAM or EEPROM.
7) 2.275V threshold detector—provides for power-fail warning and low-battery detection, or monitors a power supply other than +5V.
8) BATT OK status flag indicates that the backup-battery voltage is above 2.275V.
9) Watchdog-fault output—asserted if the watchdog input has not been toggled within a preset timeout period.

Features

- **Precision 4.675V (MAX807L) or 4.425V (MAX807M), or 4.575V (MAX807N) Voltage Monitoring**
- **140ms Power OK / Reset Time Delay**
- **$\overline{\text{RESET}}$ and RESET Outputs**
- **Independent Watchdog Timer**
- **1µA Standby Current**
- **Power Switching:**
  250mA in V_{CC} Mode
  20mA in Battery-Backup Mode
- **On-Board Gating of Chip-Enable Signals:**
  Memory Write-Cycle Completion
  6ns CE Gate Propagation Delay
- **MaxCap™ and SuperCap™ Compatible**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **Backup-Battery Monitor**
- **Guaranteed $\overline{\text{RESET}}$ Valid to V_{CC} = 1V**

Applications

Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring
Portable/Battery-Powered Equipment

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX807_CPE	0°C to +70°C	16 Plastic DIP
MAX807_CSE	0°C to +70°C	16 Wide SO

Ordering Information continued on last page.

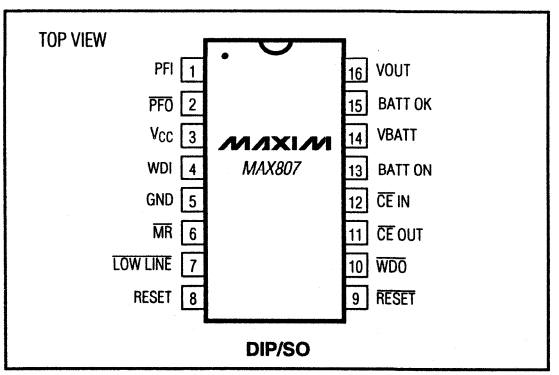
** Contact factory for dice specifications.*

† Insert the desired suffix into blank to complete the part number.

SUFFIX	RESET THRESHOLD (V) MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50

™ SuperCap is a registered trademark of Baknor Industries
MaxCap is a registed trademark of the Carborundum Corp.

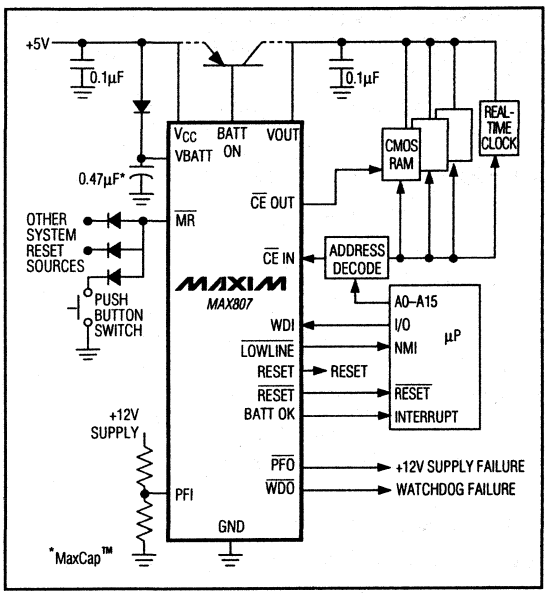
Pin Configuration



Typical Operating Circuit on next page.

µP Supervisory Circuit with ±1.5% Reset Accuracy

Typical Operating Circuit



Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX807_EPE	-40°C to +85°C	16 Plastic DIP
MAX807_EWE	-40°C to +85°C	16 Wide SO
MAX807_MJE	-55°C to +125°C	16 CERDIP

** Contact factory for dice specifications.*
† Insert the desired suffix into blank to complete the part number.

SUFFIX	RESET THRESHOLD (V) MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MA 809 LEUR

MAXIM

3-Pin µP Reset Monitor

General Description

The MAX809/MAX810 are microprocessor (µP) supervisory circuits used to monitor the power supplies in µP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered or 3V-powered circuits.

These circuits perform a single function: They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The only difference between the two devices is that the MAX809 has an active-low $\overline{RESET}$ output (which is guaranteed to be in the correct state for V_{CC} down to 1V), while the MAX810 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}. Reset thresholds suitable for operation with a variety of supply voltages are available.

The MAX809/MAX810 come in an 8-pin DIP package as well as a 3-pin SOT-23 package.

Applications

Computers

Controllers

Intelligent Instruments

Critical µP Power Monitoring

Portable/Battery-Powered Equipment

Features

- **Precision Monitoring of 3V, 3.3V, and 5V Power-Supply Voltages**
- **140ms Min Power-On Reset Pulse Width**
  $\overline{RESET}$ Output (MAX809)
  RESET Output (MAX810)
- **Guaranteed $\overline{RESET}$ Valid to V_{CC} = 1V (MAX809)**
- **Transient Immunity**
- **No External Components**
- **8-Pin DIP Package**
  3-Pin SOT-23 Package

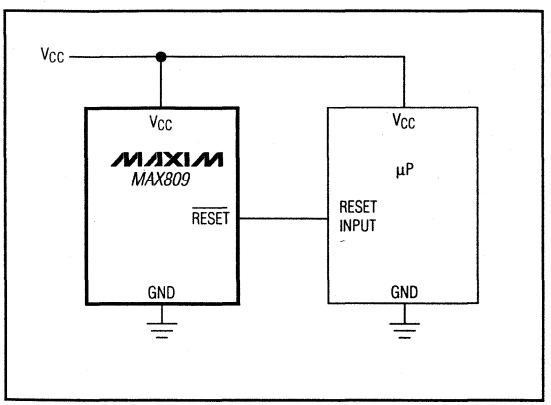
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX809_CPA	0°C to +70°C	8 Plastic DIP
MAX809_CUR	0°C to +70°C	3 SOT-23
MAX810_CPA	0°C to +70°C	8 Plastic DIP
MAX810_CUR	0°C to +70°C	3 SOT-23

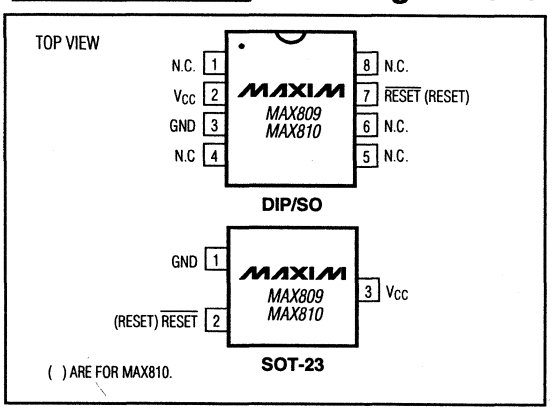
†*Insert the desired suffix into blank to complete the part number:*

SUFFIX	RESET THRESHOLD (V)
L	4.65
M	4.40
T	3.08
S	2.93
R	2.63

Typical Operating Circuit



Pin Configurations



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

High-Accuracy, ±1%, Low-Power, +3V and +5V µP Supervisory Circuits

General Description

The MAX814/MAX815/MAX816 high-accuracy microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. They eliminate manual trimming and improve reliability in critical applications needing high-accuracy reset trip thresholds.

All members of this device family provide the following three functions:

1) Active-low $\overline{\text{RESET}}$ output, asserted during power-up, power-down, and brownout conditions. The reset threshold is accurate to ±1%, over temperature.
2) Threshold detector for power-fail warning, low-battery detection, or monitoring another power-supply voltage.
3) Active-low manual-reset input.

Additional device functions are listed below.

MAX814:

1) Choice of reset thresholds: 4.8V, 4.7V, 4.55V, or 3.03V.
2) Active-high RESET output.
3) Two-stage power-fail warning. A separate low-line comparator compares V_{CC} to a threshold 60mV above the reset threshold. This low-line comparator is more accurate than those in previous µP supervisors, and facilitates early warning of power failure so the system can be put into a safe condition before reset is asserted.

MAX815:

1) Choice of reset thresholds: 4.8V, 4.7V, 4.55V, or 3.03V.
2) Independent watchdog output that goes low if the watchdog input has not been toggled within 1.56sec.

MAX816:

1) Active-high RESET output.
2) Adjustable reset threshold, set with an external resistor divider. In this device, the voltage on the RESET IN pin is monitored, not the voltage on V_{CC}.

The $\overline{\text{RESET}}$ output is guaranteed to be in the correct state for V_{CC} down to 1V. The reset comparator is designed to ignore fast transients on V_{CC}. Reset thresholds suitable for operation with a variety of 3V and 5V supply voltages are available.

A 75µA max supply current makes the MAX814/MAX815/MAX816 ideal for use in portable equipment. All three devices are available in 8-pin DIP and SO packages.

Typical Operating Circuit on next page.

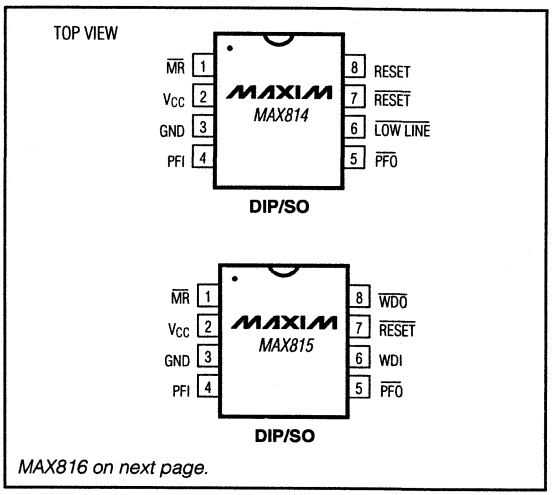
Features

- ♦ **±1% Reset Threshold Accuracy over Temperature**
- ♦ **4.8V, 4.7V, 4.55V, 3.03V, or Adjustable Reset Thresholds**
- ♦ **±1% Low-Line Threshold Accuracy (MAX814)**
- ♦ **200ms Reset Pulse Width**
- ♦ **Active-Low $\overline{\text{RESET}}$ Output**
- ♦ **Active-High RESET Output (MAX814/MAX816)**
- ♦ **75µA Max Supply Current**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Valid to V_{CC} = 1V**
- ♦ **Manual Reset Input**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Independent Watchdog (MAX815) with 1.56sec Timeout**
- ♦ **Power-Supply Glitch Immunity**
- ♦ **8-Pin SO and DIP Packages**

Applications

Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring
Portable/Battery-Powered Equipment

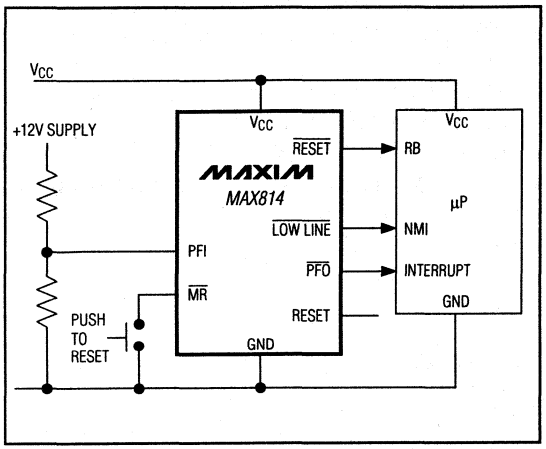
Pin Configurations



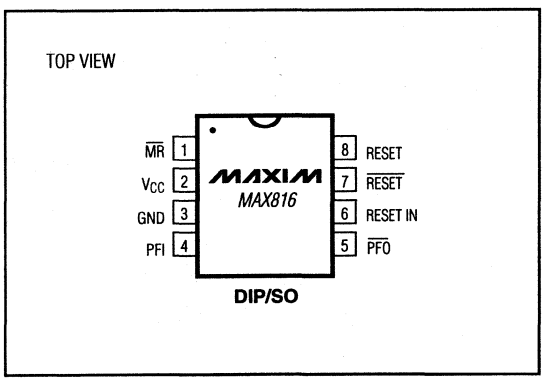
MAX816 on next page.

High-Accuracy, ±1%, Low-Power, +3V and +5V µP Supervisory Circuits

Typical Operating Circuit

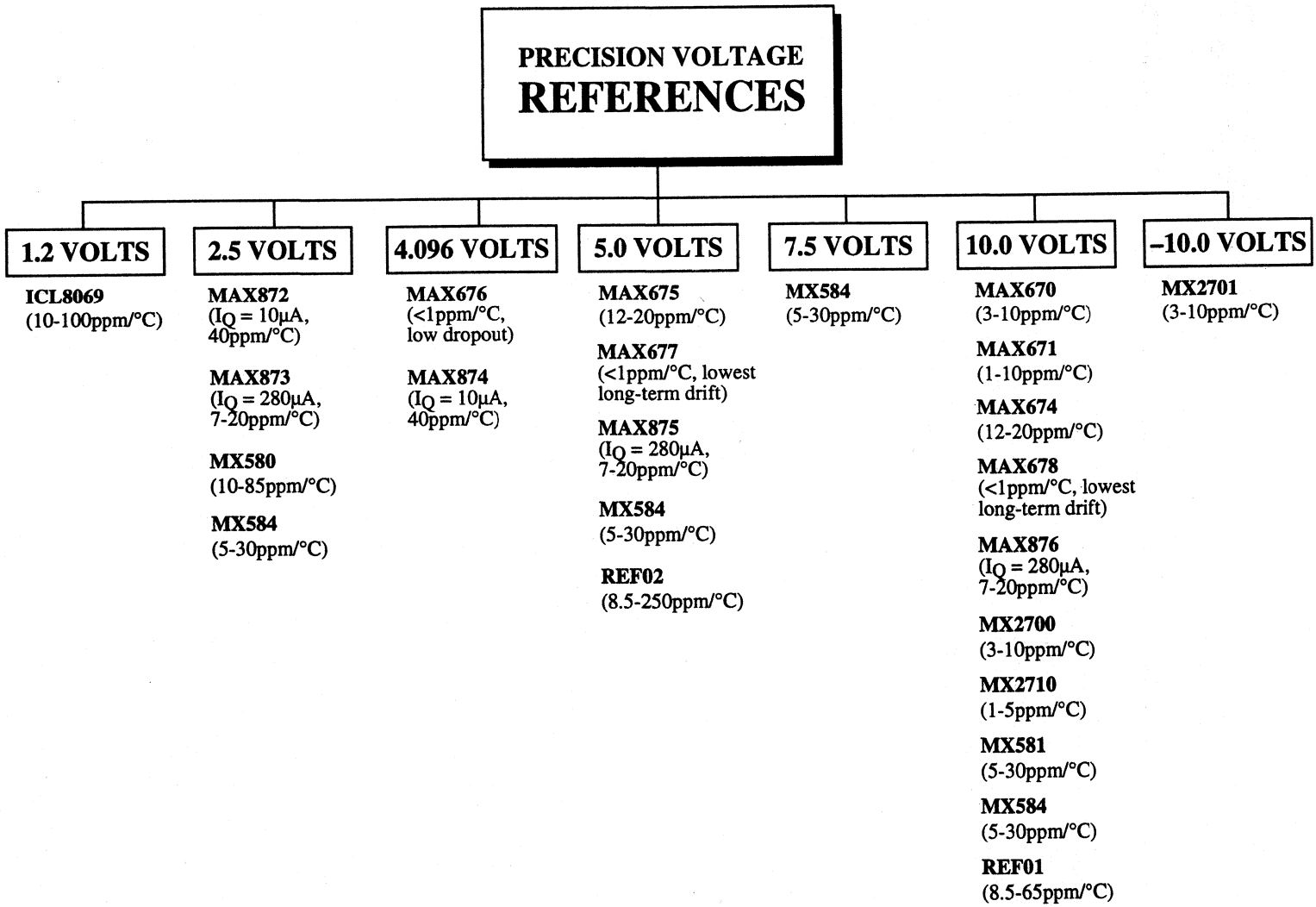


Pin Configurations (continued)



Voltage References

*Advance Information–first page of data sheet in preparation.


PRECISION VOLTAGE
REFERENCES
1.2 VOLTS
ICL8069
(10-100ppm/°C)
2.5 VOLTS
MAX872
(IQ = 10µA,
40ppm/°C)
MAX873
(IQ = 280µA,
7-20ppm/°C)
MX580
(10-85ppm/°C)
MX584
(5-30ppm/°C)
4.096 VOLTS
MAX676
(<1ppm/°C,
low dropout)
MAX874
(IQ = 10µA,
40ppm/°C)
5.0 VOLTS
MAX675
(12-20ppm/°C)
MAX677
(<1ppm/°C, lowest
long-term drift)
MAX875
(IQ = 280µA,
7-20ppm/°C)
MX584
(5-30ppm/°C)
REF02
(8.5-250ppm/°C)
7.5 VOLTS
MX584
(5-30ppm/°C)
10.0 VOLTS
MAX670
(3-10ppm/°C)
MAX671
(1-10ppm/°C)
MAX674
(12-20ppm/°C)
MAX678
(<1ppm/°C, lowest
long-term drift)
MAX876
(IQ = 280µA,
7-20ppm/°C)
MX2700
(3-10ppm/°C)
MX2710
(1-5ppm/°C)
MX581
(5-30ppm/°C)
MX584
(5-30ppm/°C)
REF01
(8.5-65ppm/°C)
–10.0 VOLTS
MX2701
(3-10ppm/°C)

Part Number	Voltage (V)	Temp. Drift (ppm/°C max)	Initial Accuracy T_A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz-10Hz (μV_{p-p}), max(typ)	Package Options[1]	Temp. Ranges[2]	Features	Price† 1000-up ($)
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz to 10kHz)	TO-52,TO-92,SO*	C,E,M	Micropower two-terminal reference	0.65
MAX872	2.5	40	0.2	10µA	(60)	DIP,SO	C,E	Lowest power, lowest dropout precision reference. $V_{CC} = V_{OUT} + 200mV$	2.12
MAX873	2.5	7 to 20	0.06 to 0.1	0.28	(16)	DIP,SO	C,E,M	Low power/drift, REF43 upgrade	2.95
MX580	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52,SO**	C,M	Low-drift bandgap reference	2.33
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift programmable reference	3.09
MAX676	4.096	1 to 2	0.01	10	(1.5)	DIP/SO	C,E,M	Lowest temperature drift in SO package, lowest long-term drift, low dropout	5.23
MAX874	4.096	40	0.2	10µA	(60)	DIP,SO	C,E	Lowest power, lowest dropout precision reference. $V_{CC} = V_{OUT} + 200mV$	2.12
MAX675	5.0	12 to 20	0.15	1.4	15	TO-99,DIP,SO,CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX677	5.0	1 to 2	0.01	10	(2)	DIP/SO	C,E,M	Lowest temperature drift in SO package, lowest long-term drift	5.23
MAX875	5.0	7 to 20	0.06 to 0.1	0.28	(32)	DIP,SO	C,E,M	Low power/drift, REF02 upgrade	2.95
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	TO-99,DIP,SO,CERDIP	C,M	Low-drift bandgap reference	1.80
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift programmable reference	3.09
MAX670	10.0	3 to 10	0.025	14	50	SB Ceramic	E,M	Kelvin connected, ultra low-drift reference	38.51
MAX671	10.0	1 to 10	0.01	14	50	SB Ceramic	C,E,M	Kelvin connected, ultra low-drift reference	37.41
MAX674	10.0	12 to 20	0.15	1.4	30	TO-99,DIP,SO,CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX678	10.0	1 to 2	0.01	10	(3)	DIP/SO	C,E,M	Lowest temperature drift in SO package, lowest long-term drift	5.23
MAX876	10.0	7 to 20	0.06 to 0.1	0.28	(64)	DIP,SO	C,E,M	Low power/drift, REF01 upgrade	2.95
MX2700	10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I,M	Ultra low-drift voltage reference	19.61
MX2710	10.0	1 to 5	0.01	14	(30)	SB Ceramic	C	Ultra low-drift voltage reference	24.74
MX581	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39,SO***	C,M	Low-drift bandgap reference	2.90
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99,DIP,SO,CERDIP	C,M	Low-drift programmable reference	3.09
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	TO-99,DIP,SO,CERDIP	C,M	Low-drift bandgap reference	2.05
MX2701	-10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I,M	Ultra low-drift voltage reference	24.02

* The ICL8069 is available in 2-pin TO-52, 2-pin TO-92, and 8-pin SO packages.
** The MX580 is available in 3-pin TO-52 and 8-pin SO packages.
*** The MX581 is available in 3-pin TO-39 and 8-pin SO packages.
1 Package Options: DIP = Dual-In-Line Package, PLCC = Plastic Leadless Chip Carrier (quad pack), FP = Flat Pack
2 Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ADVANCE INFORMATION

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MAXIM

Calibrated, Low-Drift, +4.096V/+5V/+10V Precision Voltage References

General Description

The MAX676/MAX677/MAX678 precision +4.096V, +5V, and +10V voltage references feature a factory-programmed on-chip ROM that calibrates each reference at specific temperatures, and reduces the temperature drift to less than 1ppm/°C over temperature—the lowest in the industry.

The MAX676/MAX677/MAX678 have excellent line and load regulation: 20ppm/V and 3ppm/mA, respectively. Load regulation specifications are guaranteed for source currents up to 5mA and sink currents up to 500µA. The 4.096V MAX676 operates from a supply voltage as low as 4.75V, making it an ideal reference for single 5V, high resolution ADCs.

Applications

High Resolution 16-Bit ADCs and DACs

Precision Test and Measurement Systems

Precision, Calibrated Voltage-Reference Standard

High-Accuracy Transducers

Features

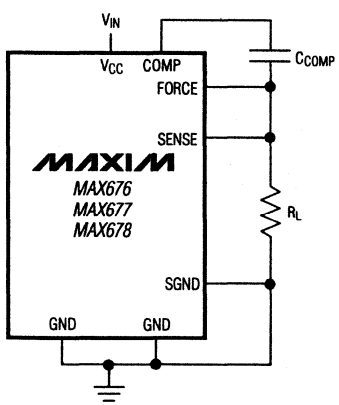
- **Lowest Temperature Drift:**
  1ppm/°C Max Over -40°C to +85°C
  1.5ppm/°C Max Over -55°C to +125°C
- **0.02% Initial Accuracy**
- **3ppm/mA Max Load Regulation**
- **20ppm/V Max Line Regulation**
- **4.096V Reference Operates from 5V ±5% Supply**
- **Available in Surface-Mount Package**

Ordering Information

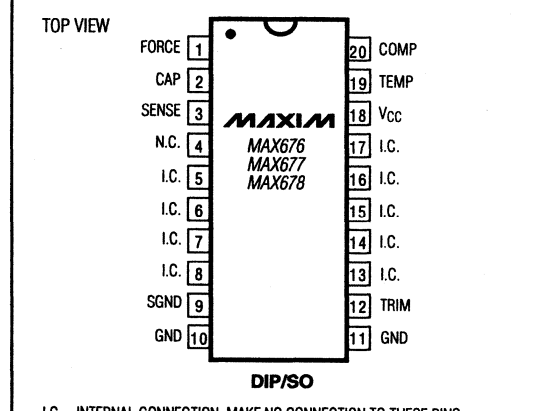
PART	TEMP. RANGE	PIN-PACKAGE	MAX DRIFT (ppm/°C)
MAX676ACPP	0°C to +70°C	20 Plastic DIP	1.0
MAX676BCPP	0°C to +70°C	20 Plastic DIP	2.0
MAX676ACWP	0°C to +70°C	20 Wide SO	1.0
MAX676BCWP	0°C to +70°C	20 Wide SO	2.0
MAX676ACJP	0°C to +70°C	20 CERDIP	1.0
MAX676AEPP	-40°C to +85°C	20 Plastic DIP	1.0
MAX676BEPP	-40°C to +85°C	20 Plastic DIP	2.0
MAX676AEWP	-40°C to +85°C	20 Wide SO	1.0
MAX676BEWP	-40°C to +85°C	20 Wide SO	2.0
MAX676AEJP	-40°C to +85°C	20 CERDIP	1.0
MAX676AMJP	-55°C to +125°C	20 CERDIP	1.5
MAX676BMJP	-55°C to +125°C	20 CERDIP	3.0

Ordering Information continued on next page.

Typical Operating Circuit



Pin Configuration



I.C. = INTERNAL CONNECTION. MAKE NO CONNECTION TO THESE PINS.

Calibrated, Low-Drift, +4.096V/+5V/+10V Precision Voltage References

Ordering Information (continued)

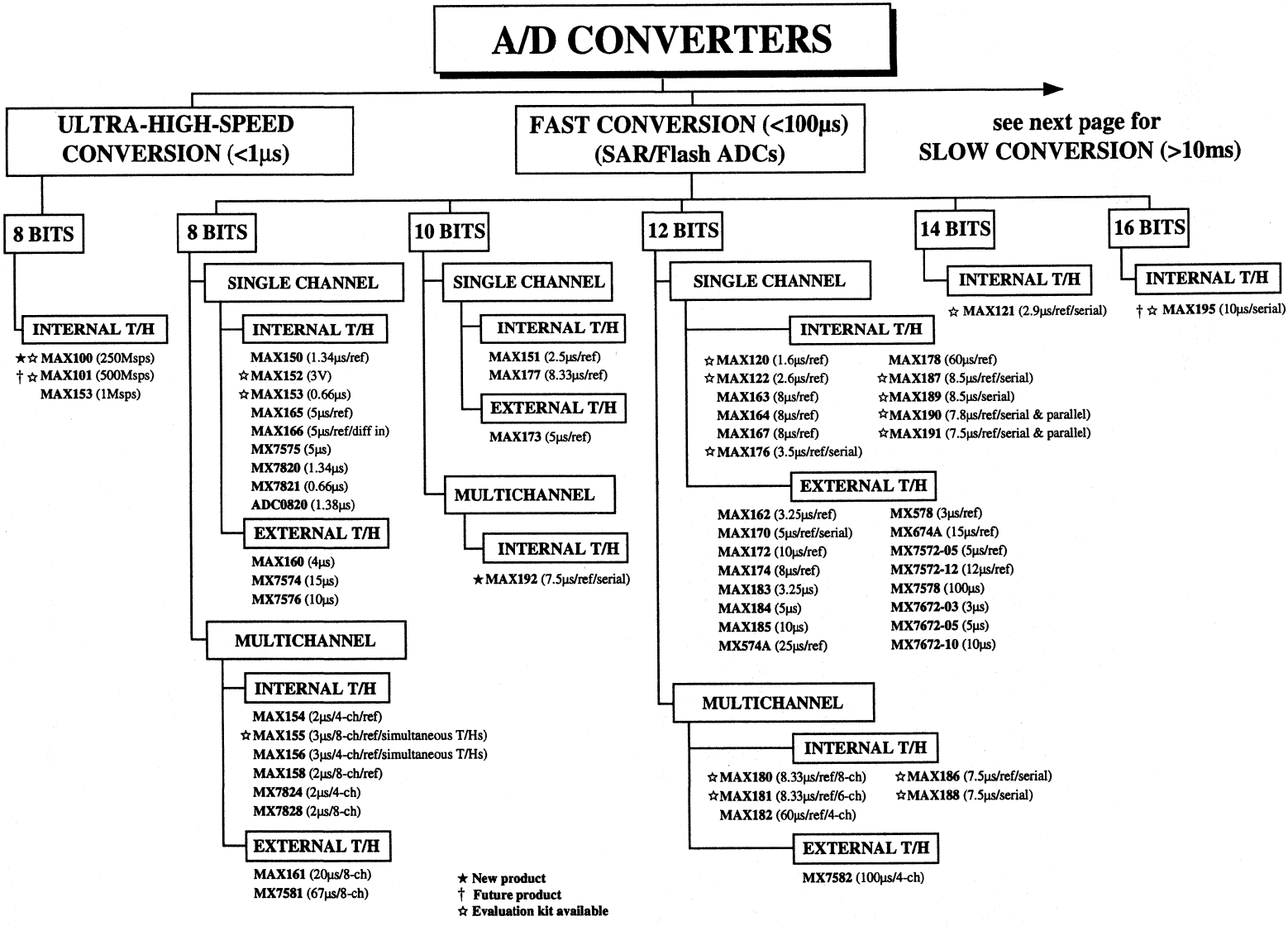
PART	TEMP. RANGE	PIN-PACKAGE	MAX DRIFT (ppm/°C)
MAX677ACPP	0°C to +70°C	20 Plastic DIP	1.0
MAX677BCPP	0°C to +70°C	20 Plastic DIP	2.0
MAX677ACWP	0°C to +70°C	20 Wide SO	1.0
MAX677BCWP	0°C to +70°C	20 Wide SO	2.0
MAX677ACJP	0°C to +70°C	20 CERDIP	1.0
MAX677AEPP	-40°C to +85°C	20 Plastic DIP	1.0
MAX677BEPP	-40°C to +85°C	20 Plastic DIP	2.0
MAX677AEWP	-40°C to +85°C	20 Wide SO	1.0
MAX677BEWP	-40°C to +85°C	20 Wide SO	2.0
MAX677AEJP	-40°C to +85°C	20 CERDIP	1.0
MAX677AMJP	-55°C to +125°C	20 CERDIP	1.5
MAX677BMJP	-55°C to +125°C	20 CERDIP	3.0
MAX678ACPP	0°C to +70°C	20 Plastic DIP	1.0
MAX678BCPP	0°C to +70°C	20 Plastic DIP	2.0
MAX678ACWP	0°C to +70°C	20 Wide SO	1.0
MAX678BCWP	0°C to +70°C	20 Wide SO	2.0
MAX678ACJP	0°C to +70°C	20 CERDIP	1.0
MAX678AEPP	-40°C to +85°C	20 Plastic DIP	1.0
MAX678BEPP	-40°C to +85°C	20 Plastic DIP	2.0
MAX678AEWP	-40°C to +85°C	20 Wide SO	1.0
MAX678BEWP	-40°C to +85°C	20 Wide SO	2.0
MAX678AEJP	-40°C to +85°C	20 CERDIP	1.0
MAX678AMJP	-55°C to +125°C	20 CERDIP	1.5
MAX678BMJP	-55°C to +125°C	20 CERDIP	3.0

MAXIM

A/D Converters

7

*Advance Information–first page of data sheet in preparation.


A/D CONVERTERS
ULTRA-HIGH-SPEED CONVERSION (<1µs)
FAST CONVERSION (<100µs) (SAR/Flash ADCs)
see next page for SLOW CONVERSION (>10ms)
8 BITS
INTERNAL T/H
★☆ MAX100 (250Msps)
† ☆ MAX101 (500Msps)
MAX153 (1Msps)
8 BITS
SINGLE CHANNEL
INTERNAL T/H
MAX150 (1.34µs/ref)
☆ MAX152 (3V)
☆ MAX153 (0.66µs)
MAX165 (5µs/ref)
MAX166 (5µs/ref/diff in)
MX7575 (5µs)
MX7820 (1.34µs)
MX7821 (0.66µs)
ADC0820 (1.38µs)
EXTERNAL T/H
MAX160 (4µs)
MX7574 (15µs)
MX7576 (10µs)
MULTICHANNEL
INTERNAL T/H
MAX154 (2µs/4-ch/ref)
☆ MAX155 (3µs/8-ch/ref/simultaneous T/Hs)
MAX156 (3µs/4-ch/ref/simultaneous T/Hs)
MAX158 (2µs/8-ch/ref)
MX7824 (2µs/4-ch)
MX7828 (2µs/8-ch)
EXTERNAL T/H
MAX161 (20µs/8-ch)
MX7581 (67µs/8-ch)
10 BITS
SINGLE CHANNEL
INTERNAL T/H
MAX151 (2.5µs/ref)
MAX177 (8.33µs/ref)
EXTERNAL T/H
MAX173 (5µs/ref)
MULTICHANNEL
INTERNAL T/H
★ MAX192 (7.5µs/ref/serial)
12 BITS
SINGLE CHANNEL
INTERNAL T/H
☆ MAX120 (1.6µs/ref)
☆ MAX122 (2.6µs/ref)
MAX163 (8µs/ref)
MAX164 (8µs/ref)
MAX167 (8µs/ref)
☆ MAX176 (3.5µs/ref/serial)
MAX178 (60µs/ref)
☆ MAX187 (8.5µs/ref/serial)
☆ MAX189 (8.5µs/serial)
☆ MAX190 (7.8µs/ref/serial & parallel)
☆ MAX191 (7.5µs/ref/serial & parallel)
EXTERNAL T/H
MAX162 (3.25µs/ref)
MAX170 (5µs/ref/serial)
MAX172 (10µs/ref)
MAX174 (8µs/ref)
MAX183 (3.25µs)
MAX184 (5µs)
MAX185 (10µs)
MX574A (25µs/ref)
MX578 (3µs/ref)
MX674A (15µs/ref)
MX7572-05 (5µs/ref)
MX7572-12 (12µs/ref)
MX7578 (100µs)
MX7672-03 (3µs)
MX7672-05 (5µs)
MX7672-10 (10µs)
MULTICHANNEL
INTERNAL T/H
☆ MAX180 (8.33µs/ref/8-ch)
☆ MAX181 (8.33µs/ref/6-ch)
MAX182 (60µs/ref/4-ch)
☆ MAX186 (7.5µs/ref/serial)
☆ MAX188 (7.5µs/serial)
EXTERNAL T/H
MX7582 (100µs/4-ch)
14 BITS
INTERNAL T/H
☆ MAX121 (2.9µs/ref/serial)
16 BITS
INTERNAL T/H
† ☆ MAX195 (10µs/serial)
★ New product
† Future product
☆ Evaluation kit available

A/D CONVERTERS

see previous page for
FAST CONVERSION (< 100µs)
and ULTRA-HIGH-SPEED
CONVERSION (<1µs)

SLOW CONVERSION (>10ms) (Integrating & Σ - Δ ADCs)

LCD DISPLAY

MAX130 (3 1/2 D, B/G)
MAX131 (3 1/2 D, B/G, L)
MAX136 (3 1/2 D, B/G, HOLD, L)
MAX138 (3 1/2 D, B/G, S/S)
ICL7106 (3 1/2 D, Z)
ICL7116 (3 1/2 D, Z, HOLD)
ICL7126 (3 1/2 D, Z, L)
ICL7129A (4 1/2 D)
ICL7136 (3 1/2 D, Z, L)

LED DISPLAY

MAX139 (3 1/2 D, B/G, S/S)
MAX140 (3 1/2 D, B/G, S/S)
ICL7107 (3 1/2 D, Z)
ICL7117 (3 1/2 D, Z, HOLD)
ICL7137 (3 1/2 D, Z, L)

µP INTERFACE

☆ **MAX132** (±18 bit, serial, L)
☆ **MAX133** (±40,000 count, L)
☆ **MAX134** (±40,000 count, L)
MAX135 (±15 bit, L)
ICL7109 (12 bit, Z)
ICL7135 (±20,000 count)

Σ - Δ ADCs

☆★ **MAX110** (±14 bit, serial, no ext. components, L)
☆★ **MAX111** (±14 bit, serial, no ext. components, L)

NOTES: HOLD – Has display-hold input
S/S – Has +5V single supply
B/G – Has bandgap reference
Z – Has zener reference
L – Low power

☆ Evaluation kit available
★ New product

General-Purpose A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX153	8	0.660	1	1000	E	µP/8	+5 or ±5	+5 or ±2.5	Yes	High-speed ADC with 1µA power-down	6.63
MX7821	8	0.660	1	500	E	µP/8	+5 or ±5	+5 or ±2.5		Complete ADC with T/H	7.54
MAX150	8	1.34	1	500	E or I/+2.5	µP/8	+5	+5		Complete ADC with T/H and ref	5.85
MX7820	8	1.34	1	500	E	µP/8	+5	+5		Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	µP/8	+5	+5		Complete ADC with T/H	7.16
MAX152	8	1.8	1	400	E	µP/8	+3 or ±3	+3 or ±1.5	Yes	3V ADC with 1µA power-down	4.25
MAX154	8	2	4	400	E or I/+2.5	µP/8	+5	+5		4-Ch ADC with T/H and ref	6.45
MAX158	8	2	8	400	E or I/+2.5	µP/8	+5	+5		8-Ch ADC with T/H and ref	6.85
MX7824	8	2	4	400	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MX7828	8	2	8	400	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	3.6	8	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-Ch ADC with simult. T/Hs and ref	9.50
MAX156	8	3.6	4	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-Ch ADC with simult. T/Hs and ref	7.19
MAX160	8	4	1	–	E	µP/8	+5	+10 or ±5		Ratiometric single-supply ADC	7.20
MAX165	8	5	1	200	E or I/+1.23	µP/8	+5	+5		Low-cost sampling ADC with ref	3.95
MAX166	8	5	1	200	E or I/+1.23	µP/8	+5	+5		Differential-input complete ADC	4.20
MX7575	8	5	1	200	E	µP/8	+5	+5		Plug-in replacement for AD7575	3.74
MX7576	8	10	1	–	E	µP/8	+5	+5		Plug-in replacement for AD7576	3.52
MX7574	8	15	1	–	E	µP/8	+5	+10 or ±5		Plug-in replacement for AD7574	4.80
MAX161	8	20	8	–	E	µP/8	+5	+10		8-Ch ADC with RAM buffer	11.12
MX7581	8	66.6	8	–	E	µP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX151	10	2.5	1	300	E or I/+4.0	µP/10	±5	+5		Sampling ADC with ref	7.95
MAX173	10 or 12	5	1	–	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5		MAX172 with 10-bit accuracy	5.26
MAX192	10	7.5	8	133	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX177	10 or 12	8.33	1	100	I/-5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX120	12	1.6	1	500	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	16.00
MAX122	12	2.6	1	333	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	12.00
MX578	12	3	1	–	E or I/+10.0	Logic	+5 & ±15	±10		Parallel/serial outputs	88.71
MAX162	12	3.25	1	–	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5		High-speed ADC with internal ref	19.20
MAX183	12	3.25	1	–	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed ADC	9.00
MX7672-03	12	3.25	1	–	E	µP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-03	57.38
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	13.20
MAX170	12	5	1	–	I/-5.25	Serial	+5 & -12 to -15	+5		Serial ADC, 8-pin miniDIP with T/H	11.96
MAX184	12	5	1	–	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed ADC with external ref	8.25
MX7572-05	12	5	1	–	I/-5.25	µP/8 or 12	+5 & -15	+5		Plug-in replacement for AD7572-05	20.00
MX7672-05	12	5	1	–	E	µP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-05	33.66
MAX186	12	7.5	8	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	8.95
MAX188	12	7.5	8	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	8.45
MAX191	12	7.5	1	100	E or I/+4.096	Serial or µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX190	12	7.8	1	75	E or I/+4.096	Serial or µP/8	+5	+5	Yes	Use MAX191 for new designs	10.00

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

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General-Purpose A/D Converters (continued)

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX174	12	8	1	–	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20		Upgrades AD574A/AD674A	28.13
MAX163	12	8.33	1	100	I/-5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling ADC with ref	14.40
MAX164	12	8.33	1	100	I/-5.0	µP/8 or 12	+5 & -12 to -15	±5		Complete sampling ADC with ref	14.40
MAX167	12	8.33	1	100	I/-5.0	µP/8 or 12	+5 & -12 to -15	±2.5		Complete sampling ADC with ref	14.40
MAX180	12	8.33	8	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	8.33	6	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX187	12	8.5	1	75	E or I/+4.096	Serial	+5	+5	Yes	7mW, 8-pin package	7.45
MAX189	12	8.5	1	75	E	Serial	+5	+5	Yes	MAX187 without reference	6.95
MAX172	12	10	1	–	I/-5.25	µP/8 or 12	+5 & -12 to -15	+5		Plug-in upgrade for AD7572-12	9.60
MAX185	12	10.4	1	–	E	µP/8 or 12	+5 & -12 to -15	+5, ±5 or +10		High-speed ADC with external ref	7.20
MX7672-10	12	10.4	1	–	E	µP/8 or 12	+5 & -12	+5, ±5 or +10		Plug-in replacement for AD7672-05	25.25
MX7572-12	12	12	1	–	I/-5.25	µP/8 or 12	+5 & -15	+5		Plug-in replacement for AD7572-12	14.00
MX674A	12	15	1	–	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20		Plug-in replacement for AD574A	23.44
MX574A	12	25	1	–	E or I/+10.0	µP/8 or 12	+5 & ±12 to ±15	±5, ±10, +10 or +20		Plug-in replacement for AD674A	11.97
MAX178	12	60	1	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	15.24
MAX182	12	60	4	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	17.55
MX7578	12	100	1	–	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7578	16.96
MX7582	12	100	4	–	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX121	14	2.9	1	308	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC with DSP interface, 16-pin pkg.	12.00
MAX110	14 + sign	20ms	2	–	E	Serial	±5	±3	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	20ms	2	–	E	Serial	+5	±2	Yes	Low-power, shutdown mode, single supply	4.80
MAX135	15 + sign	10ms	1	–	E	µP/8	±5	±0.5		High-resolution ADC, <1mW	8.00
MAX195	16	10	1	100	E	Serial	±5	+5 or ±5	Yes	High-speed serial 16-pin ADC, 50mW	††
MAX132	18 + sign	10ms	1	–	E	Serial	±5	±0.5	Yes	Serial high-resolution ADC, <1mW	8.00

Ultra-High-Speed A/D Converters

Part Number	Resolution (Bits)	Sample Rate (Msps max)	Input Channels	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX100	8	250	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P	227.90
MAX101	8	500	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P	††

* E = external reference, I = internal reference

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Sampling A/D Converters

Part Number	Resolution (Bits)	Sample Rate (kHz max)	Input Channels	Conversion Time (µs max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX153	8	1000	1	0.660	E	µP/8	+5 or ±5	+5 or ±2.5	Yes	High-speed ADC with 1µA power-down	6.63
MAX150	8	500	1	1.34	E or I/+2.5	µP/8	+5	+5		Complete ADC with T/H and ref	5.85
MX7821	8	500	1	0.660	E	µP/8	+5 or ±5	+5 or ±2.5		Complete ADC with T/H	7.54
MX7820	8	500	1	1.34	E	µP/8	+5	+5		Plug-in replacement for AD7820	7.93
MAX152	8	400	1	1.8	E	µP/8	+3 or ±3	+3 or ±1.5	Yes	3V ADC with 1µA power-down	4.25
ADC0820	8	400	1	1.38	E	µP/8	+5	+5		Complete ADC with T/H	7.16
MAX154	8	400	4	2	E or I/+2.5	µP/8	+5	+5		4-Ch ADC with T/H and ref	6.45
MAX158	8	400	8	2	E or I/+2.5	µP/8	+5	+5		8-Ch ADC with T/H and ref	6.85
MX7824	8	400	4	2	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MX7828	8	400	8	2	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	250	8	3.6	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-Ch ADC with simult. T/Hs and ref	9.50
MAX156	8	250	4	3.6	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-Ch ADC with simult. T/Hs and ref	7.19
MAX165	8	200	1	5	E or I/+1.23	µP/8	+5	+5		Low-cost sampling ADC with ref	3.95
MAX166	8	200	1	5	E or I/+1.23	µP/8	+5	+5		Differential-input complete ADC	4.20
MX7575	8	200	1	5	E	µP/8	+5	+5		Plug-in replacement for AD7575	3.74
MAX151	10	300	1	2.5	E or I/+4.0	µP/10	±5	+5		Sampling ADC with ref	7.95
MAX192	10	133	8	7.5	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX177	10 or 12	100	1	8.33	I/-5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX120	12	500	1	1.6	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	16.00
MAX122	12	333	1	2.6	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed complete sampling ADC	12.00
MAX176	12	250	1	3.5	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	13.20
MAX186	12	133	8	7.5	E or I/+4.096	Serial	+5	+5	Yes	7mW, 10µA power-down	8.95
MAX188	12	133	8	7.5	E	Serial	+5	+5	Yes	MAX186 without reference	8.45
MAX163	12	100	1	8.33	I/-5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling ADC with ref	14.40
MAX164	12	100	1	8.33	I/-5.0	µP/8 or 12	+5 & -12 to -15	±5		Complete sampling ADC with ref	14.40
MAX167	12	100	1	8.33	I/-5.0	µP/8 or 12	+5 & -12 to -15	±2.5		Complete sampling ADC wirh ref	14.40
MAX180	12	100	8	8.33	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	100	6	8.33	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX191	12	100	1	7.5	E or I/+4.096	Serial or µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX187	12	75	1	8.5	E or I/+4.096	Serial	+5	+5	Yes	7mW, 8-pin package	7.45
MAX189	12	75	1	8.5	E	Serial	+5	+5	Yes	MAX187 without reference	6.95
MAX190	12	75	1	7.8	E or I/+4.096	Serial or µP/8	+5	+5	Yes	Use MAX191 for new designs	10.00
MAX178	12	20	1	60	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	15.24
MAX182	12	20	4	60	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	17.55
MAX121	14	308	1	2.9	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC with DSP interface, 16-pin pkg.	12.00
MAX195	16	100	1	10	E	Serial	±5	+5 or ±5	Yes	High-speed serial 16-pin ADC	††

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

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Low-Power A/D Converters

Part Number	Resolution (Bits)	Input Channels	Data-Bus Interface (Bits)	Supply Voltage (V)	Supply Current (mA)	Power-Down Current (µA)	Conversion Time (µs max)	Reference Voltage* (V)	EV Kit	Features	Price† 1000-up ($)
MAX152	8	1	µP/8	+3 or ±3	1.5	1	1.8	E	Yes	3V ADC with 1µA power-down	4.25
MAX153	8	1	µP/8	+5 or ±5	8	1	0.660	E	Yes	High-speed ADC with 1µA power-down	6.63
MAX192	10	8	Serial	+5	1.5	2	7.5	I/+4.096		Low power, low cost, small package	2.95**
MAX186	12	8	Serial	+5 or ±5	1.5	2	7.5	I/+4.096	Yes	7mW, 10µA power-down	8.95
MAX187	12	1	Serial	+5	1.5	2	8.5	I/+4.096	Yes	7mW, 8-pin package	7.45
MAX188	12	8	Serial	+5 or ±5	1.0	2	7.5	E	Yes	MAX186 without reference	8.45
MAX189	12	1	Serial	+5	1.0	2	8.5	E	Yes	MAX187 without reference	6.95
MAX191	12	1	Serial or µP/8	+5 or ±5	2.5	20	7.5	E or I/+4.096	Yes	15mW, 20µA power-down	9.60
MAX110	14 + sign	2	Serial	±5	550µA	1	20ms	E	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	Serial	+5	640µA	1	20ms	E	Yes	Low-power, shutdown mode, single supply	4.80
MAX135	15 + sign	1	µP/8	±5	60µA	1	10ms	E		High-resolution ADC, <1mW	8.00
MAX195	16	1	Serial	±5	5.5	–	10	E	Yes	High-speed serial 16-pin ADC	††
MAX132	18 + sign	1	Serial	±5	60µA	1	10ms	E	Yes	Serial high-resolution ADC, <1mW	8.00

Multi-Channel A/D Converters

Part Number	Resolution (Bits)	Input Channels	Conversion Time (µs max)	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX154	8	4	2	400	E or I/+2.5	µP/8	+5	+5		4-Ch ADC with T/H and ref	6.45
MX7824	8	4	2	400	E	µP/8	+5	+5		Plug-in replacement for AD7824	8.33
MAX156	8	4	3.6	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5		4-Ch ADC with simult. T/Hs and ref	7.19
MAX158	8	8	2	400	E or I/+2.5	µP/8	+5	+5		8-Ch ADC with T/H and ref	6.85
MX7828	8	8	2	400	E	µP/8	+5	+5		Plug-in replacement for AD7828	8.73
MAX155	8	8	3.6	250	E or I/+2.5	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-Ch ADC with simult. T/Hs and ref	9.50
MAX161	8	8	20	–	E	µP/8	+5	+10		8-Ch ADC with RAM buffer	11.12
MX7581	8	8	66.6	–	E	µP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX192	10	8	133	7.5	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX182	12	4	60	20	E or I/+5.0	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and ref	17.55
MX7582	12	4	100	–	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX181	12	6	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX186	12	8	7.5	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	8.95
MAX188	12	8	7.5	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	8.45
MAX180	12	8	8.33	100	E or I/-5.0	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX110	14 + sign	2	20ms	–	E	Serial	±5	±3	Yes	Low power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	20ms	–	E	Serial	+5	±2	Yes	Low power, shutdown mode, single supply	4.80

* E = external reference, I = internal reference

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Serial A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX192	10	7.5	8	133	I/+4.096	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	13.20
MAX170	12	5	1	–	I/-5.25	Serial	+5 & -12 to -15	+5		Serial ADC, 8-pin miniDIP with T/H	11.96
MAX186	12	7.5	8	133	E or I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	8.95
MAX188	12	7.5	8	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	8.45
MAX191	12	7.5	1	100	E or I/+4.096	Serial or µP/8	+5 or ±5	+5 or ±2.5	Yes	15mW, 20µA power-down	9.60
MAX190	12	7.8	1	75	E or I/+4.096	Serial or µP/8	+5	+5	Yes	Use MAX191 for new designs	10.00
MAX187	12	8.5	1	75	E or I/+4.096	Serial	+5	+5	Yes	7mW, 8-pin package	7.45
MAX189	12	8.5	1	75	E	Serial	+5	+5	Yes	MAX187 without reference	6.95
MAX121	14	2.9	1	308 –	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC with DSP interface	12.00
MAX110	14 + sign	20ms	2	–	E	Serial	±5	±3	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	20ms	2	–	E	Serial	+5	±2	Yes	Low-power, shutdown mode, single supply	4.80
MAX195	16	10	1	100	E	Serial	±5	+5 or ±5	Yes	High-speed, serial, 16-pin ADC, 50mW	††
MAX132	18 + sign	10ms	1	–	E	Serial	±5	±0.5	Yes	Serial high-resolution ADC, <1mW	8.00

Integrating and Sigma-Delta A/D Converters

Part Number	Resolution (digits)	Resolution (counts)	Output Type	Supply Voltage (V)	Supply Current (mA), max(typ)	References	EV Kit	Features	Price† 1000-up ($)
INTEGRATING ADCs									
MAX130	3 1/2	±2000	LCD	+4.5 to +14	0.25(0.1)	Bandgap		Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to +14	0.1(0.06)	Bandgap		Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15(0.06)	Bandgap		Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to +7	0.8(0.2)	Bandgap		± inputs with single supply	4.40
ICL7106	3 1/2	±2000	LCD	+9	1.8(0.6)	Zener		For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8(0.8)	Zener		ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		± inputs with single supply	4.40
MAX140	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		Low segment current (2mA)	4.40
ICL7107	3 1/2	±2000	LED	+9	1.8(0.6)	Zener		For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	±5	1.8(0.8)	Zener		ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	±5	0.2(0.06)	Zener		Low power when LEDs off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
MAX134	3 3/4	±40,000	µP	±5	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
ICL7109	12 bits + sign	±4096	8-/16-bit µP/UART	±5	1.5(0.7)	Zener		3-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4(1.0)	External		Lowest noise ±3µV	7.96
ICL7135	4 1/2	±20,000	Multiplexed BCD	±5	2.0(1.0)	External		For DMM, DPM, data loggers	5.48
MAX135	15 bits + sign	±20,000	µP/8	±5	0.125(0.06)	External		Three-state twos-complement outputs	8.00
MAX132	18 bits + sign	±260,000	Serial µP	±5	0.125(0.06)	External	Yes	Serial high-resolution ADC, <1mW	8.00
SIGMA-DELTA ADCs									
MAX110	14 bits + sign	–	Serial	±5	1.2(0.8)	External	Yes	No external components, low power, dual supplies	4.80
MAX111	14 bits + sign	–	Serial	+5	1.5(1.0)	External	Yes	No external components, low power, single supply	4.80

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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EVALUATION KIT AVAILABLE

MAXIM

250Msps, 8-Bit ADC with Track/Hold

General Description

The MAX100 ECL-compatible, 250Msps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 125MHz (Nyquist frequency). Designed with Maxim's proprietary advanced bipolar processes, the MAX100 contains a high-performance track/hold (T/H) amplifier and a quantizer in a single ceramic strip-line package.

The innovative design of the internal T/H assures an exceptionally wide input bandwidth of 1.2GHz and aperture delay uncertainty of less than 2ps, resulting in a high 6.8 effective bits performance. Special comparator output design and decoding circuitry reduce out-of-sequence code errors. The probability of erroneous codes occurring due to metastable states is reduced to less than 1 error per 10^{15} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX100 keeps the magnitude to less than 1LSB.

The analog input is designed for either differential or single-ended use with a ±270mV range. Sense pins for the reference input allow full-scale calibration of the input range or facilitate ratiometric use. Midpoint tap for the reference string is available for applications that need to modify the output coding for a user-defined bilinear response. Use of separate high-current and low-current ground pins provides better noise immunity and highest device accuracy.

Dual output data paths provide several data output modes for easy interfacing. These modes can be configured as either one or two identical latched ECL outputs. An 8:16 demultiplexer mode that reduces the output data rates to one-half the clock rate is also available.

For applications that require faster data rates, refer to Maxim's MAX101, which allows conversion rates up to 500Msps.

Features

- ♦ **250Msps Conversion Rate**
- ♦ **6.8 Effective Bits at 125MHz**
- ♦ **Less than ±1/2LSB INL**
- ♦ **50Ω Differential or Single-Ended Inputs**
- ♦ **±270mV Input Signal Range**
- ♦ **Reference Sense Inputs**
- ♦ **Ratiometric Reference Inputs**
- ♦ **Configurable Dual-Output Data Paths**
- ♦ **Latched, ECL-Compatible Outputs**
- ♦ **Low Error Rate, Less than 10^{-15} Metastable States**
- ♦ **Selectable On-Chip 8:16 Demultiplexer**
- ♦ **84-Pin Ceramic Flat Pack**

Applications

High-Speed Digital Instrumentation
High-Speed Signal Processing
Medical Systems
Radar/Sonar
High-Energy Physics
Communications

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX100CFR*	0°C to +70°C	84 Ceramic Flat Pack (with heatsink)

**Contact factory for 84-Pin Ceramic Flat Pack without heatsink.*

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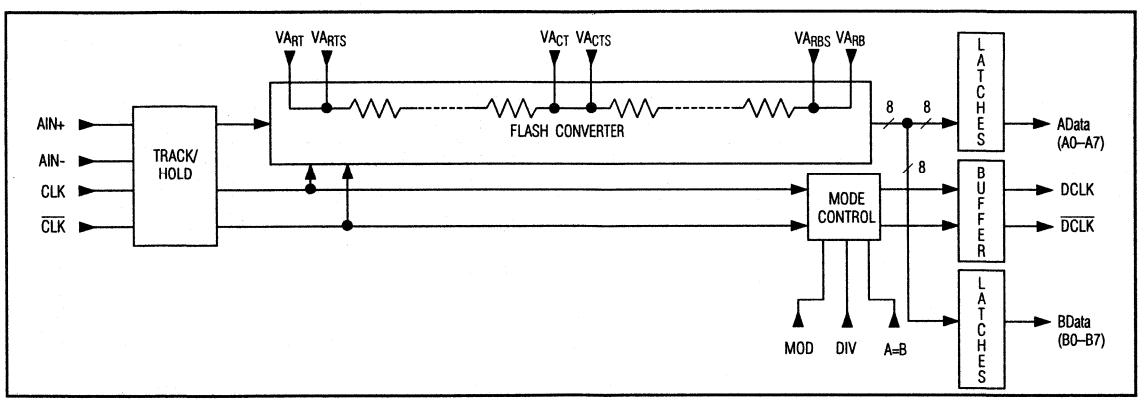
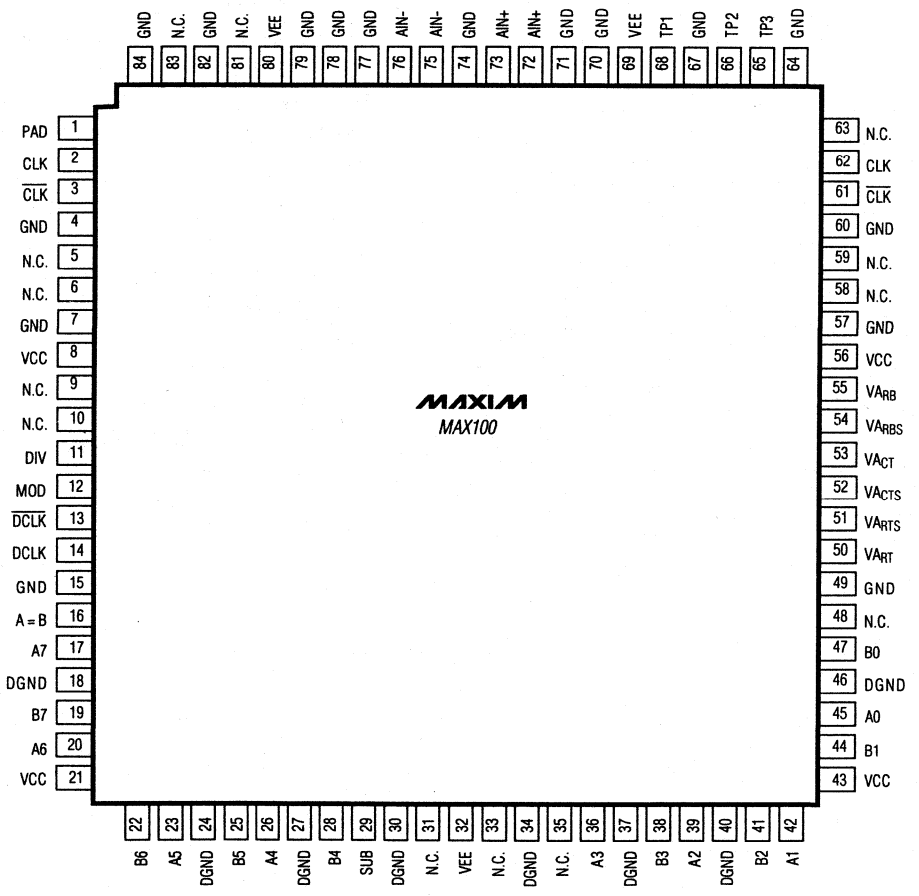
Functional Diagram



250Msps, 8-Bit ADC with Track/Hold

Pin Configuration

TOP VIEW



Ceramic Flat Pack

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

500Msps, 8-Bit ADC with Track/Hold

General Description

The MAX101 ECL-compatible, 500Msps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 250MHz (Nyquist frequency). Designed with Maxim's proprietary advanced bipolar process, the MAX101 contains a high-performance track/hold (T/H) amplifier and a pair of time-interleaved quantizers in a single ceramic strip-line package. These dual monolithic converters, driven by the T/H, operate on opposite clock edges and provide alternate 8-bit outputs on two ports.

The innovative design of the internal T/H assures an exceptionally wide input bandwidth of 1.2GHz and aperture uncertainty of less than 2ps, resulting in seven effective bits of performance at the Nyquist frequency. Special comparator output design and decoding circuitry reduce out-of-sequence code errors. The probability of erroneous codes occurring due to metastable states is reduced to less than one error per 10^{15} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX101 keeps the magnitude to less than 1LSB.

The device's analog input is designed for either differential or single-ended use and has a ±270mV range. Sense pins for the reference input allow full-scale calibration of the input range or facilitate ratiometric operation.

Phase adjustment (for adjusting the relative sampling of the converter halves) is available to optimize converter performance. Input clock phasing is also available for interleaving several MAX101s for higher effective sampling rates. For breadboarding, the output data and clock rates may be reduced by a factor of five, resulting in a sampling mode of one out of every five input values.

Features

- **500Msps Conversion Rate**
- **Seven Effective Bits at 250MHz**
- **±1/2LSB Integral Nonlinearity**
- **50Ω Differential or Single-Ended Inputs**
- **±270mV Input Signal Range**
- **1.2GHz Input Bandwidth**
- **Ratiometric Reference Inputs**
- **Latched, ECL-Compatible Outputs**
- **Low Error Rate, <10^{-15} Metastable States**
- **84-Pin Ceramic Flat Pack**

Applications

High-Speed Digital Instrumentation
High-Speed Signal Processing
Medical Systems
Radar/Sonar
High-Energy Physics
Communications

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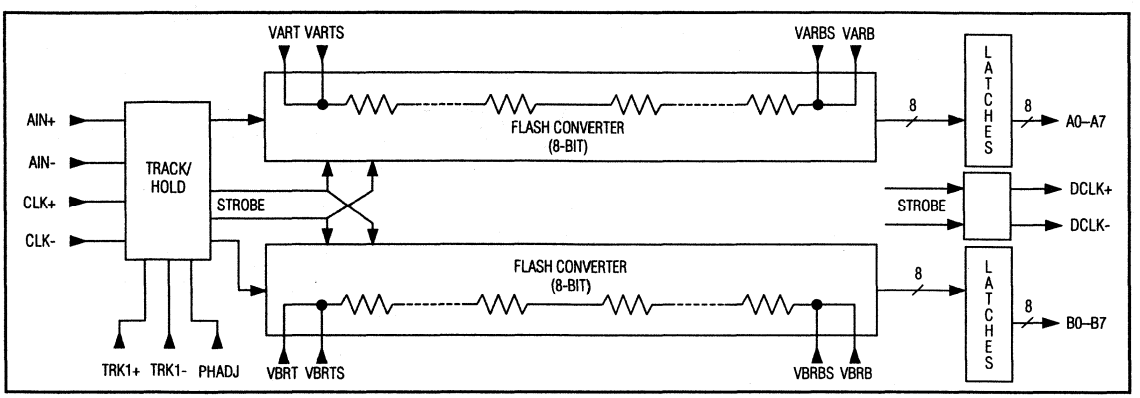
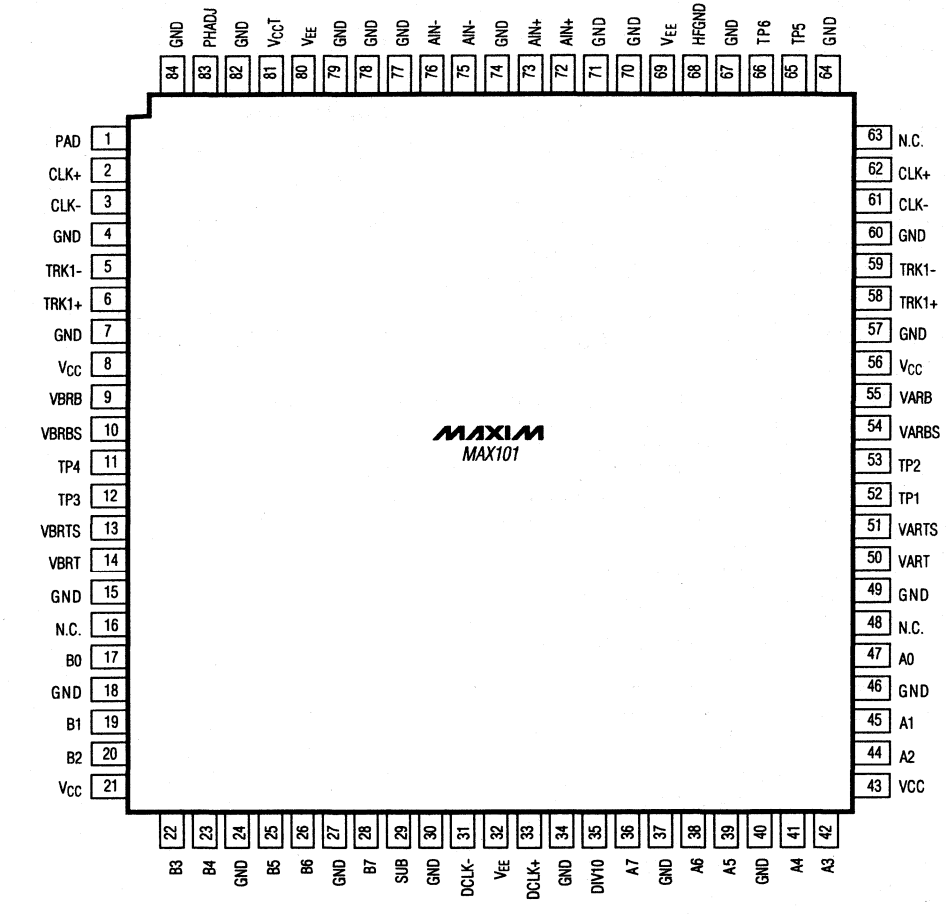
Functional Diagram



Pin Configuration on next page.

500Msps, 8-Bit ADC with Track/Hold

Pin Configuration



Ceramic Flat Pack

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
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EVALUATION KIT AVAILABLE

MAXIM

Low-Cost, 2-Channel, ±14-Bit Serial ADCs

General Description

The MAX110/MAX111 analog-to-digital converters (ADCs) use an internal auto-calibration technique to achieve 15-bit resolution plus overrange, with no external components. Operating supply current is only 550µA, and reduces to 1µA in power-down mode, making these ADCs ideal for high-resolution battery-powered or remote sensing applications. A fast serial interface simplifies signal routing and opto-isolation, saves microcontroller pins, and offers compatibility with SPI™, QSPI™, and Microwire™. The MAX110 operates with ±5V supplies and converts single-ended or differential analog signals in the -2.5V to +2.5V range, while the MAX111 operates with a single +5V supply and converts differential signals in the ±2V range, or single-ended signals in the 0V to 2V range.

Internal calibration allows for both offset and gain-error correction under microprocessor (µP) control. Both devices are available in space-saving 16-pin DIP and SO packages, as well as an even smaller 20-pin SSOP package.

Applications

Process Control
Weigh Scales
Panel Meters
Data-Acquisition Systems
Temperature Measurement

Features

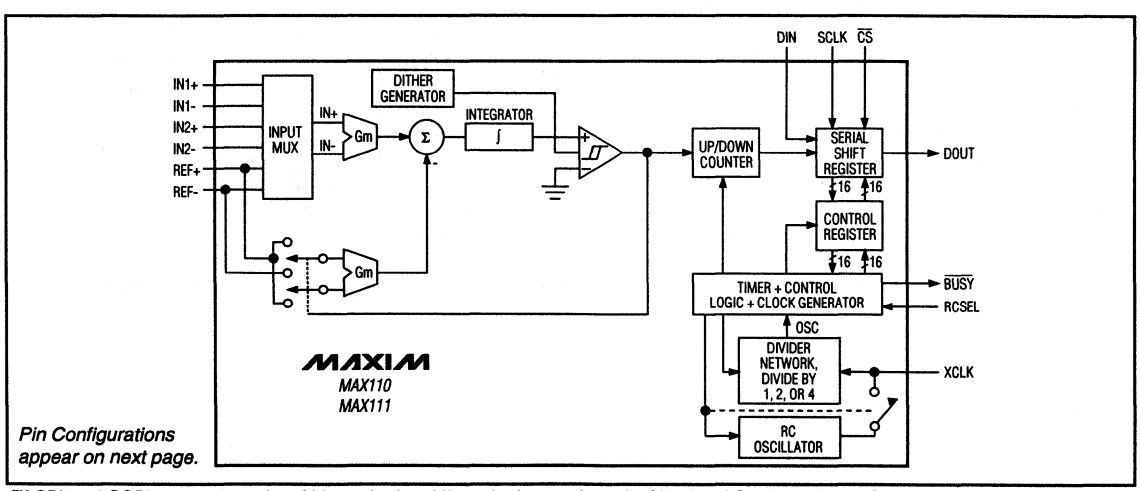
- **14-Bit Resolution Plus Sign and Overrange**
- **12-Bit Accuracy**
- **Low Power Consumption:**
  400µA Operating Current
  1µA Shutdown Current
- **High Input Impedance**
- **50Hz/60Hz Rejection**
- **Calibration µP Control**
- **No External Components Required**
- **16-Pin DIP/SO, 20-Pin SSOP**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX110CPE	0°C to +70°C	16 Plastic DIP
MAX110CWE	0°C to +70°C	16 Wide SO
MAX110CAP	0°C to +70°C	20 SSOP
MAX110C/D	0°C to +70°C	Dice*
MAX110EPE	-40°C to +85°C	16 Plastic DIP
MAX110EWE	-40°C to +85°C	16 Wide SO
MAX110EAP	-40°C to +85°C	20 SSOP
MAX110MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued on next page.
** Contact factory for dice specifications.*

Functional Diagram



Pin Configurations appear on next page.

™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Low-Cost, 2-Channel, ±14-Bit Serial ADCs

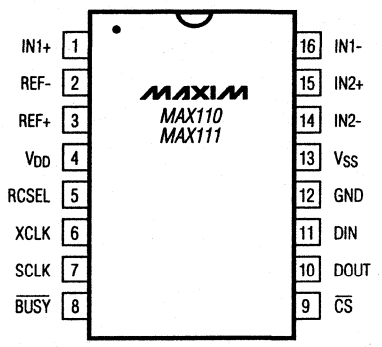
_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX111CPE	0°C to +70°C	16 Plastic DIP
MAX111CWE	0°C to +70°C	16 Wide SO
MAX111CAP	0°C to +70°C	20 SSOP
MAX111C/D	0°C to +70°C	Dice*
MAX111EPE	-40°C to +85°C	16 Plastic DIP
MAX111EWE	-40°C to +85°C	16 Wide SO
MAX111EAP	-40°C to +85°C	20 SSOP
MAX111MJE	-55°C to +125°C	16 CERDIP

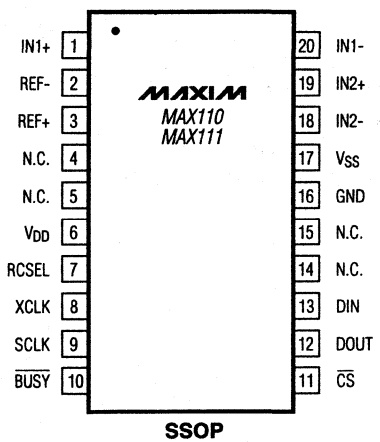
** Contact factory for dice specifications.*

_Pin Configurations

TOP VIEW



DIP/SO



SSOP

19-0030; Rev 0; 9/92

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

500ksps, 12-Bit ADCs with Track/Hold and Reference

General Description

The MAX120 and MAX122 complete, BiCMOS, sampling 12-bit analog-to-digital converters (ADCs) combine an on-chip track/hold (T/H) and a low-drift voltage reference with fast conversion speeds and low power consumption. The T/H's 350ns acquisition time combined with the MAX120's 1.6µs conversion time results in throughput rates as high as 500k samples per second (ksps). Throughput rates of 333ksps are possible with the 2.6µs conversion time of the MAX122.

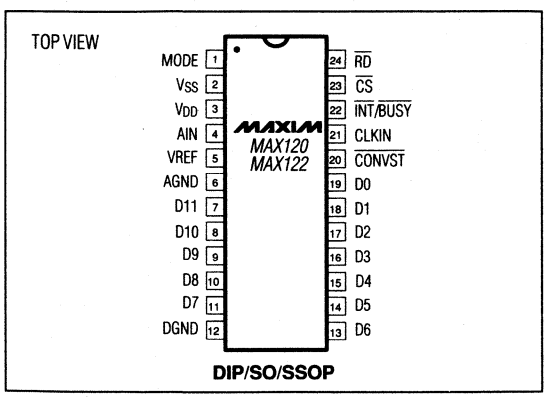
The MAX120/MAX122 accept analog input voltages from -5V to +5V. The only external components needed are decoupling capacitors for the power-supply and reference voltages. The MAX120 operates with clocks in the 0.1MHz to 8MHz frequency range. The MAX122 accepts 0.1MHz to 5MHz clock frequencies.

The MAX120/MAX122 employ a standard microprocessor (µP) interface. Three-state data outputs are configured to operate with 12-bit data buses. Data-access and bus-release timing specifications are compatible with most popular µPs without resorting to wait states. In addition, the MAX120/MAX122 can interface directly to a first in, first out (FIFO) buffer, virtually eliminating µP interrupt overhead. All logic inputs and outputs are TTL/CMOS compatible. For applications requiring a serial interface, refer to the new MAX121.

Applications

Digital-Signal Processing
Audio and Telecom Processing
Speech Recognition and Synthesis
High-Speed Data Acquisition
Spectrum Analysis
Data Logging Systems

Pin Configuration



DIP/SO/SSOP

Features

- ♦ 12-Bit Resolution
- ♦ No Missing Codes Over Temperature
- ♦ 20ppm°/C -5V Internal Reference
- ♦ 1.6µs Conversion Time/500ksps Throughput (MAX120)
- ♦ 2.6µs Conversion Time/333ksps Throughput (MAX122)
- ♦ Low Noise and Distortion:
  70 dB Min SINAD;
  -77 dB Max THD (MAX122)
- ♦ Low Power Dissipation: 210mW
- ♦ Separate Track/Hold Control Input
- ♦ Continuous-Conversion Mode Available
- ♦ ±5V Input Range, Overvoltage Tolerant to ±15V
- ♦ 24-Pin Narrow DIP, Wide SO and SSOP Packages

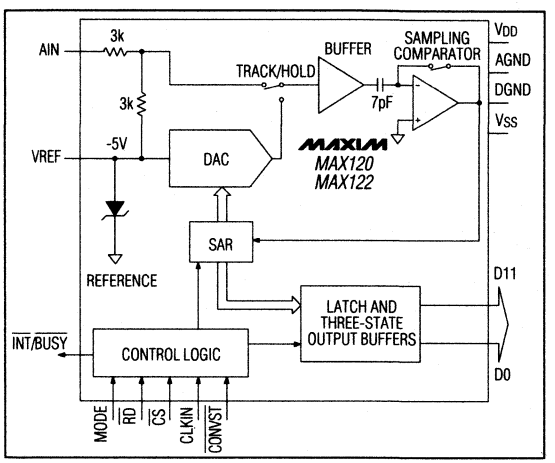
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX120CNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX120CWG	0°C to +70°C	24 Wide SO	±1
MAX120CAG	0°C to +70°C	24 SSOP	±1
MAX120C/D	0°C to +70°C	Dice*	±1
MAX120ENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX120EWG	-40°C to +85°C	24 Wide SO	±1

Ordering Information continued on last page.

**Contact factory for dice specifications.*

Functional Diagram



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500ksps, 12-Bit ADCs with Track/Hold and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs/Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Narrow CERDIP (derate 12.50W/°C above +70°C) .. 1000mW

Operating Temperature Ranges:
MAX12_C__ ..... 0°C to +70°C
MAX12_E__ ..... -40°C to +85°C
MAX12_MRG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Differential Nonlinearity (Note 1)	DNL	12-bit no missing codes over temp. range	MAX122AC/AE			±3/4	LSB
			MAX120C/E, MAX122BC/BE/BM			±1	
		11-bit no missing codes over temp. range	MAX120M			±2	
Integral Nonlinearity (Note 1)	INL		MAX122AC/AE			±3/4	LSB
			MAX120C/E, MAX122BC/BE/BM			±1	
			MAX120M			±2	
Bipolar Zero Error (Note 1)		Code 00..00 to 00..01 transition, near AIN = 0V				±3	LSB
		Temperature drift			±0.005		LSB/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±8	LSB
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection Ratio (Change in FS, Note 3)	PSRR	V_{DD} only, 5V ±5%			±1/4	±3/4	LSB
		V_{SS} only, -12V ±10%			±1/4	±1	
		V_{SS} only, -15V ±5%			±1/4	±1	
ANALOG INPUT							
Input Range				-5		5	V
Input Current		AIN = +5V (approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 4)						10	pF
Full-Power Input Bandwidth					1.5		MHz
REFERENCE							
Output Voltage		No external load, AIN = 5V, T_A = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 5)		MAX12_C/E				±25	ppm/°C
		MAX12_M				±30	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX120: f_S = 500kHz, A_{IN} = ±5Vp-p, 100kHz; MAX122: f_S = 333kHz, A_{IN} = ±5Vp-p, 50kHz							
Signal-to-Noise Plus Distortion	SINAD	T_A = +25°C	MAX120, MAX122	70	72		dB
			MAX122AC/AE	70			
			MAX122BC/BE/BM	69			
Total Harmonic Distortion (First Five Harmonics)	THD	T_A = +25°C	MAX120		-82	-77	dB
			MAX122		-85	-78	
			MAX122AC/AE			-77	
			MAX122BC/BE/BM			-75	
Spurious-Free Dynamic Range	SFDR	T_A = +25°C	MAX120	77	82		dB
			MAX122	78	85		
			MAX122AC/AE	77			
			MAX122BC/BE/BM	75			
CONVERSION TIME							
Synchronous	t_{CONV}	$13t_{CLK}$	MAX120			1.63	µs
			MAX122			2.60	
Clock Frequency	f_{CLK}		MAX120	0.1		8	MHz
			MAX122	0.1		5	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 4)						10	pF
Input Current		V_{IN} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS ($\overline{INT}$/$\overline{BUSY}$, D11-D0)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD} - 0.5			V
Leakage Current	I_{LKG}	V_{IN} = 0V or V_{DD}, D11-D0				±5	µA
Output Capacitance (Note 4)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	Guaranteed by supply rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	Guaranteed by supply rejection test		-10.80		-15.75	V
Positive Supply Current (Note 6)	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V			9	15	mA
Negative Supply Current (Note 6)	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V			14	20	mA
Power Dissipation (Note 6)		V_{DD} = 5V, V_{SS} = -12V, AIN = 0V			210	315	mW

Note 1: These tests are performed at V_{DD} = 5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.
Note 2: Ideal full-scale transition is at +5V - 3/2LSB = +4.9963V, adjusted for offset error.
Note 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage = (FS at nominal supply) - (FS at nominal supply ± tolerance), expressed in LSBs.
Note 4: For design guidance only, not tested.
Note 5: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as $TC = (\Delta VREF/VREF)/(\Delta T)$
Note 6: $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V

500ksps, 12-Bit ADCs with Track/Hold and Reference

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -12V to -15V, 100% tested, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX12_C/E			MAX12_M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}		0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0			0			ns
$\overline{CONVST}$ Pulse Width	t_{CW}		30			30			30			ns
$\overline{RD}$ Pulse Width	t_{RW}		t_{DA}			t_{DA}			t_{DA}			ns
Data-Access Time	t_{DA}	C_L = 100pF		40	75			100			120	ns
Bus-Relinquish Time	t_{DH}			30	50			65			80	ns
$\overline{RD}$ or $\overline{CONVST}$ to $\overline{BUSY}$	t_{B0}	C_L = 50pF		30	75			100			120	ns
CLKIN to $\overline{BUSY}$ or $\overline{INT}$	t_{B1}	C_L = 50pF		70	110			150			180	ns
CLKIN to $\overline{BUSY}$ Low	t_{B2}	In mode 5		45	90			120			150	ns
$\overline{RD}$ to $\overline{INT}$ High	t_{IH}	C_L = 50pF		30	50			75			90	ns
$\overline{BUSY}$ or $\overline{INT}$ to Data Valid	t_{BD}	C_L (Data) = 100pF, C_L ($\overline{INT}$, $\overline{BUSY}$) = 50pF			20			30			35	ns
Acquisition Time (Note 8)	t_{AQ}		350			350			400			ns
Aperture Delay (Note 8)	t_{AP}			10								ns
Aperture Jitter (Note 8)				30								ps

Note 7: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Figures 1 and 2 for load circuits.

Note 8: For design guidance only, not tested.

19-0108; Rev 1; 8/93

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

308ksps ADC with DSP Interface and 78dB SINAD

General Description

The MAX121 is a complete, BiCMOS, serial-output, sampling 14-bit analog-to-digital converter (ADC) that combines an on-chip track/hold and a low-drift, low-noise, buried-zener voltage reference with fast conversion speed and low power consumption. The throughput rate is as high as 308k samples per second (ksps). The full-scale analog input range is ±5V.

The MAX121 utilizes the successive-approximation architecture with a high-speed DAC to achieve both fast conversion speeds and low-power operation. Operating with +5V and -12V or -15V power supplies, power consumption is only 210mW.

The MAX121 can be directly interfaced to the serial port of most popular digital-signal processors, and comes in space-saving 16-pin DIP and SO and smaller 20-pin SSOP packages. The MAX121 operates with TTL-/CMOS-compatible clocks in the frequency range from 0.1MHz to 5.5MHz. All logic inputs and outputs are TTL/CMOS compatible. This data sheet includes application notes for easy interface to TMS320, µPD77230, and ADSP2101 digital-signal processors, as well as µPs using the Motorola SPI and QSPI interface standards.

Applications

Digital Signal Processing

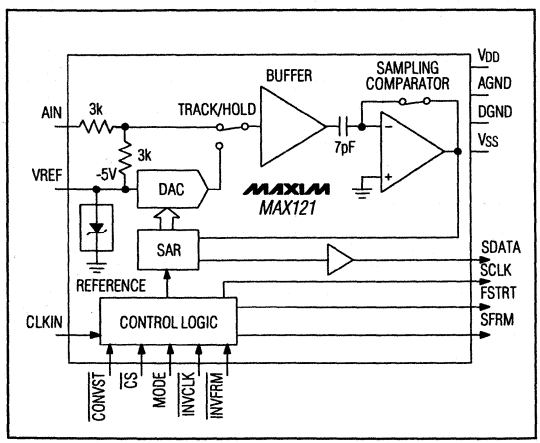
Audio and Telecom Processing

Speech Recognition and Synthesis

DSP Servo Control

Spectrum Analysis

Functional Diagram



Features

- ♦ **14-Bit Resolution**
- ♦ **2.9µs Conversion Time/308ksps Throughput**
- ♦ **400ns Acquisition Time**
- ♦ **Low Noise and Distortion:**
  78dB SINAD
  -85dB THD
- ♦ **±5V Bipolar Input Range, Overvoltage Tolerant to ±15V**
- ♦ **210mW Power Dissipation**
- ♦ **Continuous-Conversion Mode Available**
- ♦ **30ppm/°C, -5V Internal Reference**
- ♦ **Interfaces to DSP Processors**
- ♦ **16-Pin DIP and SO Packages, 20-Pin SSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX121CPE	0°C to +70°C	16 Plastic DIP
MAX121CWE	0°C to +70°C	16 Wide SO
MAX121CAP	0°C to +70°C	20 SSOP**
MAX121C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *20-pin SSOP is 50% smaller than 16-pin SOIC.*

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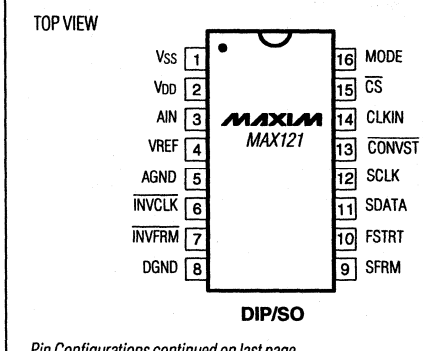
Pin Configurations



DIP/SO

Pin Configurations continued on last page.

308ksps ADC with DSP Interface and 78dB SINAD

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs to DGND ..... -0.3V, (V_{DD} + 0.3V)
(CS, CONVST, MODE, CLKIN, INVCLK, INVFRM)
Digital Outputs to DGND ..... +0.3V, (V_{DD} + 0.3V)
(SFRM, FSTRT, SCLK, SDATA)

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
Operating Temperature Ranges:
MAX121C_ ..... 0°C to +70°C
MAX121E_ ..... -40°C to +85°C
MAX121MJE ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = -10.8V to -15.75V, MAX121C/E f_{CLK} = 5.5MHz, MAX121M f_{CLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX121C/E: f_S = 308kHz, AIN = 10Vp-p, 50kHz) (MAX121M: f_S 278kHz, AIN = 10Vp-p, 50kHz)							
Signal-to-Noise Ratio	SINAD	Including distortion	MAX121C	75	78		dB
			MAX121E/M	73	77		
Total Harmonic Distortion	THD	First five harmonics	MAX121C/E		-85	-77	dB
			MAX121M		-83	-76	
Spurious-Free Dynamic Range	SFDR		MAX121C/E	77	86		dB
			MAX121M	76	84		
ACCURACY							
Resolution	RES			14			Bits
Differential Nonlinearity (Note 1)	DNL	12 bits no missing codes over temp. range			±1.5		LSB
Integral Nonlinearity	INL				±2		LSB
Bipolar Zero Error		Code 00..00 to 00..01 transition, near AIN = 0V				±10	mV
		Temperature drift			±1		ppm/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±0.2	%
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection		V_{DD} only, 5V ±5%			±1/2	±2	LSB
		V_{SS} only, -12V ±10%			±1	±2	
		V_{SS} only, -15V ±5%			±1	±2	
ANALOG INPUT							
Input Range				-5		+5	V
Input Current		AIN = 5V (R_{IN} approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 3)						10	pF
Full-Power Bandwidth					1.5		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 4.75V to 5.25V, V_{SS} = -10.8V to -15.75V, MAX121C/E f_{CLK} = 5.5MHz, MAX121M f_{CLK} = 5MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Output Voltage		No external load, AIN = 5V, T_A = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 4)		MAX121C/E				±30	ppm/°C
		MAX121M				±35	
CONVERSION TIME							
Synchronous	t_{CONV}	16 t_{CLK}	MAX121C/E			2.91	µs
			MAX121M			3.20	
Clock Frequency	f_{CLK}		MAX121C/E	0.1		5.5	MHz
			MAX121M	0.1		5.0	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 3)						10	pF
Input Current		V_{DD} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS (SCLK, SDATA, FSTRT, SFRM)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD}-0.5			V
Leakage Current	I_{LKG}	V_{OUT} = 0V or V_{DD}				±5	µA
Output Capacitance (Note 3)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	By supply-rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	By supply-rejection test		-10.8		-15.75	V
Positive Supply Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			9	15	mA
Negative Supply Current	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			14	20	mA
Power Dissipation		V_{DD} = 5V, V_{SS} = -12V, AIN = 0V, $\overline{CS}$ = $\overline{CONVST}$ = MODE = 5V			213	315	mW

Note 1: These tests are performed at V_{DD} = +5V, V_{SS} = -15V. Operation over supply is guaranteed by supply-rejection tests.
Note 2: Ideal full-scale transition is at +5V - 3/2LSB = +4.9991V, adjusted for offset error.
Note 3: Guaranteed, not tested.
Note 4: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as TC = (ΔVREF/VREF) / ΔT.

308ksps ADC with DSP Interface and 78dB SINAD

TIMING CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX121C/E		MAX121M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CONVST}$ Pulse Width (Note 6)	t_{CW}		20			30		35		ns
Data-Access Time	t_{DA}	C_L = 50pF		25	50		65		80	ns
Data-Hold Time	t_{DH}			25	50		65		80	ns
CLKIN to SCLK	t_{CD}	C_L = 50pF		40	65		85		105	ns
SCLK to SDATA Skew	t_{SC}	C_L = 50pF			±65		±80		±100	ns
SCLK to SFRM or FSTRT Skew	t_{SC}	C_L = 50pF			±25		±35		±40	ns
Acquisition Time (Note 6)	t_{AQ}		400			400		400		ns
Aperture Delay	t_{AP}			10						ns
Aperture Jitter				30						ps
Clock Setup/Hold Time	t_{CK}		10		50	10	50	10	50	ns

Note 5: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V. Output delays are measured to +0.8V if going low, or +2.4V if going high. For a data-hold time, a change of 0.5V is measured. See Figures 4 and 5 for load circuits.

Note 6: Guaranteed, but not tested.

Pin Description

PIN		NAME	FUNCTION
DIP/SO	SSOP		
1	1	V_{SS}	Negative Power Supply: -12V or -15V
2	2	V_{DD}	Positive Power Supply: +5V
3	3	AIN	Sampling Analog Input: ±5V bipolar input range
4	4	VREF	-5V Reference Output. Bypass to AGND with 22µF II 0.1µF.
5	7	AGND	Analog Ground
6	8	$\overline{INVCLK}$	Invert Serial Clock. Connect to DGND to invert the SCLK output (relative to CLKIN).
7	9	$\overline{INVFRM}$	Invert Serial Frame. This input sets the polarity of the SFRM output as follows: If $\overline{INVFRM}$ = DGND, SFRM is high during a conversion. If $\overline{INVFRM}$ = V_{DD}, SFRM is low during a conversion.
8	10	DGND	Digital Ground
9	11	SFRM	Serial Frame Output. Normally high ($\overline{INVFRM}$ = V_{DD}), falls at the beginning of the conversion and rises at the end (after 16 t_{CLK}) signaling the end of a 16-bit frame.
10	12	FSTRT	Frame Start Output. High pulse that lasts one clock cycle, falling edge indicates that a valid MSB is available.
11	13	SDATA	Serial Data Output. MSB first, twos-complement binary output code.
12	14	SCLK	Serial Clock Output. Same polarity as CLKIN if $\overline{INVCLK}$ = V_{DD}, inverted CLKIN if $\overline{INVCLK}$ = DGND. Note that SCLK runs whenever CLKIN is active.
13	17	$\overline{CONVST}$	Active-Low Convert Start Input. Conversions are initiated on falling edges.
14	18	CLKIN	Clock Input. Supply a TTL-/CMOS-compatible clock from 0.1MHz to 5.5MHz, 40%-60% duty cycle.
15	19	$\overline{CS}$	Active-Low Chip-Select Input. $\overline{CS}$ = DGND enables the three-state outputs. Also, if $\overline{CONVST}$ is low, initiates a conversion on the falling edge of $\overline{CS}$.
16	20	MODE	Hardwire to set operational mode: V_{DD}: single conversions, DGND: continuous conversions
—	5, 6, 15, 16	N.C.	No Connect – not internally connected.

19-0009; Rev. 1; 7/92

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

±18-Bit ADC with Serial Interface

General Description

The MAX132 is a CMOS, 18-bit plus sign, serial-output, analog-to-digital converter (ADC). Multi-slope integration provides high-resolution conversions in less time than standard integrating ADCs, allowing operation up to 100 conversions per second. Low conversion noise provides guaranteed operation with ±512mV full-scale input range (2µV/LSB). A simple 4-wire serial interface connects easily to all common microprocessors, and twos-complement output coding simplifies bipolar measurements. Typical supply current is only 60µA and is reduced to 1µA in sleep mode. Four serially programmed digital outputs can be used to control an external multiplexer or programmable-gain amplifier. The MAX132 comes in 24-pin narrow DIP and wide SO packages, and is available in commercial and extended temperature grades.

High resolution, compact size, and low power make this device ideal for data loggers, weigh scales, data-acquisition systems, and panel meters.

Applications

Remote Data Acquisition

Battery-Powered Instruments

Industrial Process Control

Transducer-Signal Measurement
Pressure, Flow, Temperature, Voltage, Current, Resistance, Weight

Features

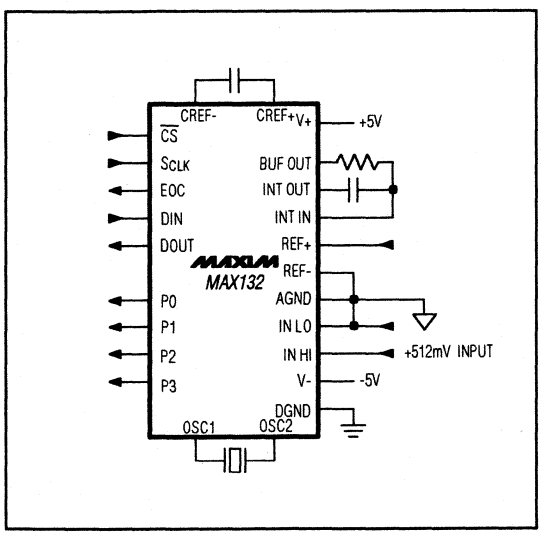
- **Low Supply Current**
  60µA (Normal Operation)
  1µA (Sleep-Mode Operation)
- **±0.006% FSR Accuracy at 16 Conv/Sec**
- **Low Noise: 15µVRMS**
- **Serial I/O Interface with Programmed Output for Mux and PGA**
- **Performs up to 100 Conv/Sec**
- **±10pA Input Current**
- **50Hz/60Hz Rejection**

Ordering Information

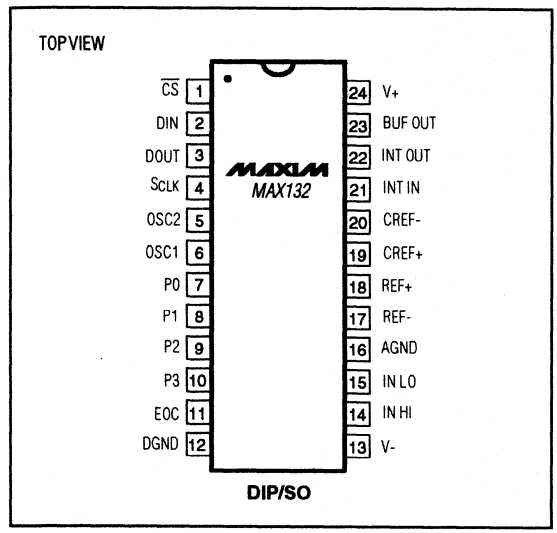
PART	TEMP. RANGE	PIN-PACKAGE
MAX132CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX132CWG	0°C to +70°C	24 Wide SO
MAX132C/D	0°C to +70°C	Dice*
MAX132ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX132EWG	-40°C to +85°C	24 Wide SO
MAX132MRG	-55°C to +125°C	24 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



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±18-Bit ADC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V+ to DGND ..... -0.3V < V+ < +6.0V
V- to DGND ..... +0.3V < V- < -9.0V
V+ to V- ..... +15V
Analog Input Voltage (any input) ..... V+ to V-
Digital Input Voltage ..... (DGND - 0.3V) to (V+ + 0.3V)
Continuous Power Dissipation
Narrow Plastic DIP (derate 8.70mW/°C above +70°C) 478mW
Wide SO (derate 11.76mW/°C above +70°C) 647mW

Operating Temperature Ranges:
MAX132C_ _ ..... 0°C to +70°C
MAX132E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF LO = 0V, REF HI = 545mV, RINT = 602kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY						
Resolution					±18	Bits
Zero Error	V_{IN} HI = 0V	T_A = +25°C		0	±0.0076	% of FSR
		T_A = T_{MIN} to T_{MAX}			±0.0168	
Integral Nonlinearity	(Notes 1, 2)	T_A = +25°C		±0.0015	±0.006	% of FSR
Rollover Error	(Note 3)	T_A = +25°C		0	±0.010	% of FSR
		T_A = T_{MIN} to T_{MAX}			±0.032	
Input Voltage Range	IN HI to IN LO, for specified accuracy				±512	mV
	See *Typical Operating Characteristics*				±2	V
Leakage Current	IN HI, IN LO	T_A = +25°C		±2	±10	pA
		T_A = T_{MIN} to T_{MAX}		±12	±250	
Common-Mode Rejection Ratio	IN HI = IN LO	V_{CM} = ±500mV		±0.009	±0.032	% of FSR
		V_{CM} = ±3.0V		±0.25	±0.50	
Common-Mode Range	IN HI = IN LO				±3.0	V
Read-Zero 50Hz/60Hz Range					±3.1	% of FSR
RMS Noise		T_A = +25°C		15		µV
Zero-Reading Drift	(Note 2)			±0.15	±1.5	ppm/°C
Scale Factor Temp. Coefficient	(Note 2)				±5	ppm/°C
POWER REQUIREMENTS						
Positive Supply Voltage			4.5		5.5	V
Negative Supply Voltage			-5.5		-4.5	V
Positive Supply Rejection	V_{IN} HI = 400mV, V- = -5.0V, 4.5V ≤ V+ ≤ 5.5V	T_A = +25°C		±0.003	±0.0061	% of FSR
		T_A = T_{MIN} to T_{MAX}		±0.003	±0.0168	
Negative Supply Rejection	V_{IN} HI = 400mV, V+ = 5.0V, -5.5V ≤ V- ≤ -4.5V	T_A = +25°C		±0.003	±0.0061	% of FSR
		T_A = T_{MIN} to T_{MAX}		±0.003	±0.0168	
Positive Supply Current	Digital input = 0V or V+			60	125	µA
Negative Supply Current	Digital input = 0V or V+			-35	-65	µA
Digital Ground Supply Current	Digital input = 0V or V+			-25	-60	µA
Positive Sleep-Mode Current	Digital input = 0V or V+			1	10	µA
Negative Sleep-Mode Current	Digital input = 0V or V+			-1	-10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF LO = 0V, REF HI = 545mV, RINT = 602kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SECTION						
Output High	V_{OH}	DOUT, I_{OUT} = -1mA	3.5	4.3		V
		DOUT, I_{OUT} = -100µA	4.0	4.5		
		EOC, P0-P3, I_{OUT} = -100µA	4.0	4.7		
Output Low	V_{OL}	DOUT, I_{OUT} = 1.6mA		0.1	0.4	V
		EOC, P0-P3, I_{OUT} = 100µA		0.1	0.4	
Input High	V_{IH}	Referred to DGND, 4.5V ≤ V+ ≤ 5.5V, $\overline{CS}$, DIN, S_{CLK}	2.4			V
Input Low	V_{IL}	Referred to DGND, 4.5V ≤ V+ ≤ 5.5V, $\overline{CS}$, DIN, S_{CLK}			0.8	V
Input Current	I_{IN}	$\overline{CS}$, DIN, S_{CLK}, and DOUT when three-stated		±10	±500	nA
Input Capacitance	C_{IN}	$\overline{CS}$, DIN, S_{CLK}, and DOUT when three-stated			5	pF

INTERFACE TIMING

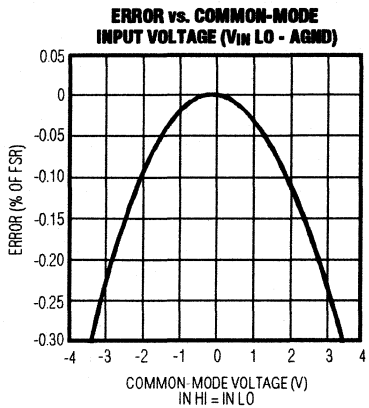
(Test Circuit of Figure 1, Figure 2, V+ = 5V, V- = -5V, DGND = AGND = 0V, T_A = +25°C, unless otherwise noted.) (Note 2)

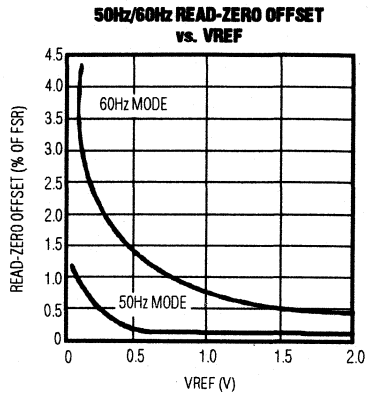
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Lead Time	t_1		500			ns
$\overline{CS}$ Lag Time	t_2		400			ns
S_{CLK} High Time	t_3		400			ns
S_{CLK} Low Time	t_4		300			ns
$\overline{CS}$ High Pulse Width	t_5		1			µs
DIN to S_{CLK} Setup Time	t_6		0			ns
DIN to S_{CLK} Hold Time	t_7		200			ns
DOUT Access Time from Three-State	t_8	See Figure 3			320	ns
Data Valid	t_9				60	ns
DOUT Disable Time to Three-State	t_{10}	See Figure 4			320	ns
Delay to P0-P3 High	t_{11}			230	350	ns
Delay to P0-P3 Low	t_{12}			230	350	ns

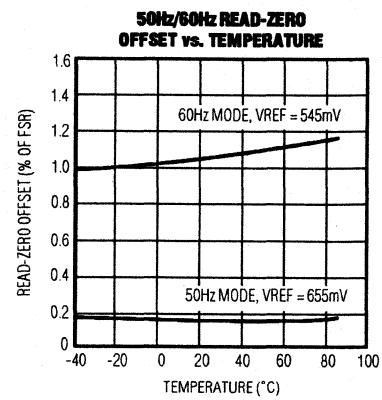
Note 1: Maximum deviation from best straight-line fit.
Note 2: Guaranteed by design, not tested.

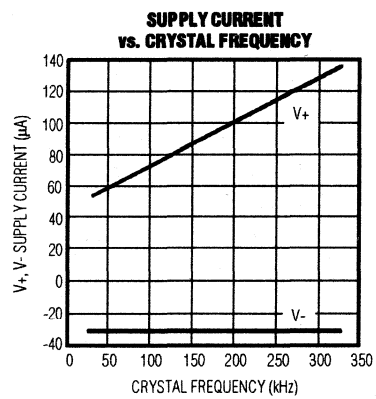
±18-Bit ADC with Serial Interface

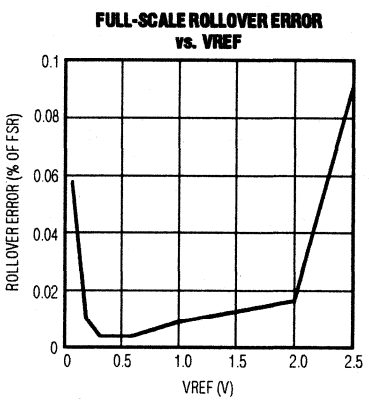
Typical Operating Characteristics

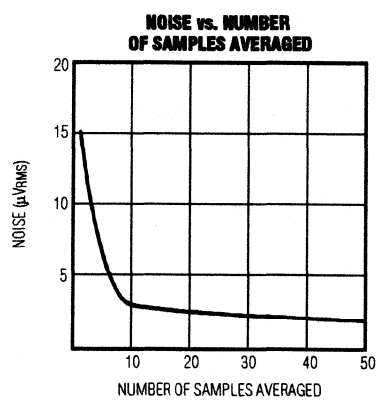












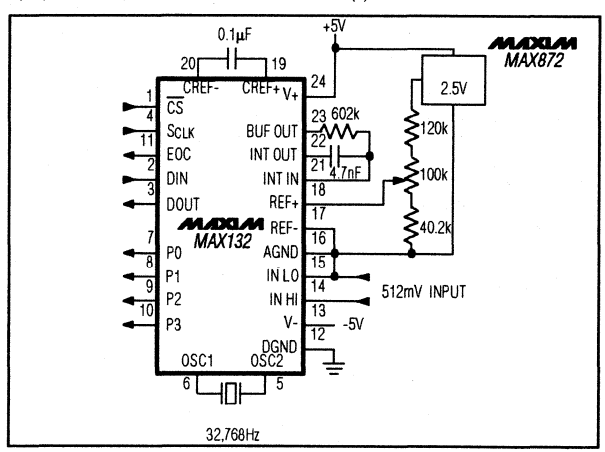


Figure 1. Test and Typical Application Circuit

19-0119; Rev. 1; 12/93

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

+3V, 8-Bit ADC with 1µA Power-Down

General Description

The MAX152 high-speed, microprocessor (µP)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 1.8µs conversion time, and digitizes at a rate of 400k samples per second (ksps). It operates with single +3V or dual ±3V supplies and accepts either unipolar or bipolar inputs. A $\overline{\text{POWERDOWN}}$ pin reduces current consumption to a typical value of 1µA. The part returns from power-down and acquires an input signal in less than 900ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX152 is DC and dynamically tested. Its µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation. A fully-assembled evaluation kit provides a proven PC board layout to speed prototyping and design.

Applications

Cellular Telephones
Portable Radios
Battery-Powered Systems
Burst-Mode Data Acquisition
Digital Signal Processing
Telecommunications
High-Speed Servo Loops

Features

- ♦ **Single +3.0V to +3.6V Supply**
- ♦ **1.8µs Conversion Time**
- ♦ **Power-Up in 900ns**
- ♦ **Internal Track/Hold**
- ♦ **400ksps Throughput**
- ♦ **Low Power: 1.5mA (Operating Mode)**
  1µA (Power-Down Mode)
- ♦ **300kHz Full-Power Bandwidth**
- ♦ **20-Pin DIP, SO and SSOP Packages**
- ♦ **No External Clock Required**
- ♦ **Unipolar/Bipolar Inputs**
- ♦ **Ratiometric Reference Inputs**
- ♦ **2.7V Version Available – Contact Factory**

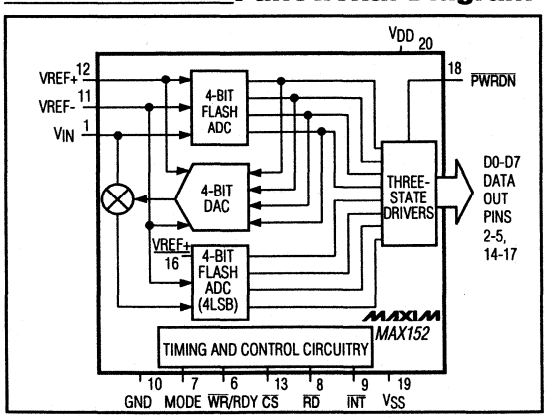
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX152CPP	0°C to +70°C	20 Plastic DIP
MAX152CWP	0°C to +70°C	20 Wide SO
MAX152CAP	0°C to +70°C	20 SSOP
MAX152C/D	0°C to +70°C	Dice*
MAX152EPP	-40°C to +85°C	20 Plastic DIP
MAX152EWP	-40°C to +85°C	20 Wide SO
MAX152EAP	-40°C to +85°C	20 SSOP
MAX152MJP	-55°C to +125°C	20 CERDIP**

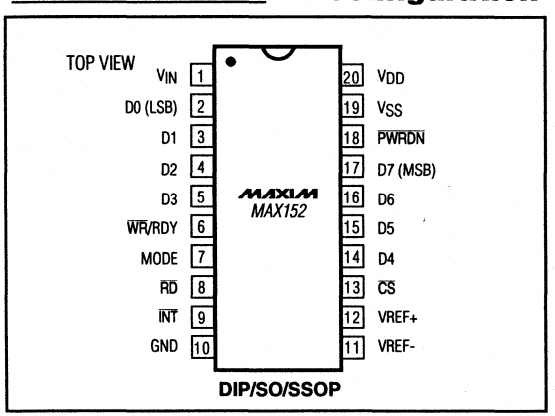
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



+3V, 8-Bit ADC with 1µA Power-Down

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +7V
V_{SS} to GND .....+0.3V to -7V
Digital Input Voltage to GND .....-0.3V, (V_{DD} + 0.3V)
Digital Output Voltage to GND .....-0.3V, (V_{DD} + 0.3V)
VREF+ to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
VREF- to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
V_{IN} to GND.....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C).....800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C).....889mW
Operating Temperature Ranges:
MAX152C__ .....0°C to +70°C
MAX152E__ .....-40°C to +85°C
MAX152MJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Unipolar input range, V_{DD} = 3.0V to 3.6V, GND = 0V, V_{SS} = GND, VREF+ = 3.0V, VREF- = GND, specifications are given for RD mode (pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE	Unipolar range			±1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±1	LSB
Zero-Code Error (Note 2)		Unipolar and bipolar modes			±1	LSB
Full-Scale Error (Note 2)		Unipolar and bipolar modes			±1	LSB
DYNAMIC PERFORMANCE (Note 3)						
Signal-to-Noise Plus Distortion Ratio	S/(N+D)	MAX152C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	45			dB
		MAX152M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	45			
Total Harmonic Distortion	THD	MAX152C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz			-50	dB
		MAX152M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz			-50	
Spurious-Free Dynamic Range		MAX152C/E, f_{SAMPLE} = 400kHz, f_{IN} = 30.273kHz	50			dB
		MAX152M, f_{SAMPLE} = 340kHz, f_{IN} = 30.725kHz	50			
Input Full-Power Bandwidth		V_{IN} = 3.0V_{p-p}		0.3		MHz
Maximum Input Slew Rate, Tracking			0.28	0.5		V/µs
ANALOG INPUT						
Input Voltage Range	V_{IN}		VREF-		VREF+	V
Input Leakage Current	I_{IN}	V_{SS} < V_{IN} < V_{DD}			±3	µA
Input Capacitance	C_{IN}			22		pF
REFERENCE INPUT						
Reference Resistance	RREF		1	2	4	kΩ
VREF+ Input Voltage Range			VREF-		V_{DD}	V
VREF- Input Voltage Range			V_{SS}		VREF+	V

ELECTRICAL CHARACTERISTICS (continued)

(Unipolar input range, V_{DD} = 3.0V to 3.6V, GND = 0V, V_{SS} = GND, VREF+ = 3.0V, VREF- = GND, specifications are given for RD mode (pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$		2.0			V
		MODE		2.4			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$				0.66	V
		MODE				0.8	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$				±1	μA
		$\overline{WR}$				±3	
		MODE			15	100	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE				±1	μA
Input Capacitance (Note 4)	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$, MODE			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	$\overline{INT}$, D0-D7, I_{SINK} = 20μA				0.1	V
		$\overline{INT}$, D0-D7, I_{SINK} = 400μA				0.4	
		RDY, I_{SINK} = 1mA				0.4	
Output High Voltage	V_{OH}	$\overline{INT}$, D0-D7, I_{SOURCE} = 20μA		V_{DD}-0.1			V
		$\overline{INT}$, D0-D7, I_{SOURCE} = 400μA		V_{DD}-0.4			
Floating-State Current	I_{LKG}	D0-D7, RDY				±3	μA
Floating Capacitance (Note 4)	C_{OUT}	D0-D7, RDY			5	8	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			3.0		3.6	V
Negative Supply Voltage	V_{SS}	Unipolar operation			GND		V
		Bipolar operation (Note 2)		-3.6		-3.0	
Positive Supply Current	I_{DD}	V_{DD} = 3.6V	MAX152C, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		2.5	5	mA
			MAX152E/M, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		2.5	6	
		V_{DD} = 3.0V	MAX152C, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		1.5	3	
			MAX152E/M, $\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}		1.5	3.5	
Power-Down V_{DD} Current (Note 5)		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0	MAX152C/E/M		1	50	μA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0, $\overline{PWRDN}$ = V_{DD}			1	50	μA
Power-Down V_{SS} Current		$\overline{CS}$ = $\overline{RD}$ = V_{DD}, $\overline{PWRDN}$ = 0			1	25	μA
Power-Supply Rejection	PSR	V_{DD} = 3.3V ±10%			±1/16	±1/4	LSB

Note 1: Accuracy measurements performed at V_{DD} = 3.0V, unipolar mode. Operation over supply range is guaranteed by power-supply rejection test.
Note 2: Bipolar tests are performed with VREF+ = +1.5V, VREF- = -1.5V, V_{SS} = -3.0V.
Note 3: Unipolar input range, V_{IN} = $3.0V_{P-P}$, WR-RD mode, V_{DD} = 3.0V
Note 4: Guaranteed by design.
Note 5: Power-down current increases if control inputs are not driven to ground or V_{DD}.

+3V, 8-Bit ADC with 1µA Power-Down

TIMING CHARACTERISTICS

(Unipolar input range, V_{DD} = 3V, V_{SS} = 0V, T_A = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES T_A = +25°C MIN	TYP	MAX	MAX152C/E T_A = T_{MIN} to T_{MAX} MIN	MAX	MAX152M T_A = T_{MIN} to T_{MAX} MIN	MAX	UNITS
Conversion Time (WR-RD Mode)	t_{CWR}	$t_{RD} < t_{INTL}$, C_L = 100pF			1.8		2.06		2.4	µs
Conversion Time (RD Mode)	t_{CRD}				2.0		2.3		2.6	µs
Power-Up Time	t_{UP}				0.9		1.2		1.4	µs
$\overline{CS}$ to $\overline{RD}$,$\overline{WR}$ Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$,$\overline{WR}$ Hold Time	t_{CSH}		0			0		0		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R_L = 5.1kΩ to V_{DD}			100		120		140	ns
Data Access Time (RD Mode) (Note 7)	t_{ACC0}	C_L = 100pF			t_{CRD} +100		t_{CRD} +130		t_{CRD} +150	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF		100	160		170		180	ns
Data Hold Time (Note 8)	t_{DH}				100		130		150	ns
Delay Time Between Conversions	t_P		450			600		700		ns
$\overline{WR}$ Pulse Width	t_{WR}		0.6		10	0.66	10	0.8	10	µs
Delay Time Between $\overline{WR}$ and $\overline{RD}$ Pulses	t_{RD}		0.8			0.9		1.0		µs
$\overline{RD}$ Pulse Width	t_{READ1}	WR-RD mode, determined by t_{ACC1} (Figure 6)	400			500		600		ns
Data Access Time (Note 7)	t_{ACC1}	WR-RD mode, $t_{RD} < t_{INTL}$, C_L = 100pF (Figure 6)			400		500		600	ns
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}				300		340		400	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF		0.7	1.45		1.6		1.8	µs
$\overline{RD}$ Pulse Width	t_{READ2}	WR-RD mode, $t_{RD} > t_{INTL}$, determined by t_{ACC2} (Figure 5)	180			220		250		ns
Data Access Time (Note 7)	t_{ACC2}	WR-RD mode, $t_{RD} < t_{INTL}$, C_L = 100pF (Figure 5)			180		220		250	ns
$\overline{WR}$ to $\overline{INT}$ Delay	t_{IHWR}	Stand-alone mode, C_L = 50pF			180		200		240	ns
Data Access Time After $\overline{INT}$ (Note 7)	t_{ID}	Stand-alone mode, C_L = 100pF			100		130		150	ns

Note 6: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of +3.0V, and timed from a voltage level of 1.3V. Timing delays get shorter at higher supply voltages. See the Converson Time vs. Supply Voltage graph in the *Typical Operating Characteristics* to extrapolate timing delays at other power-supply voltages.

Note 7: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.66V or 2.0V.

Note 8: See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

19-4740; Rev 1; 10/9?

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down

General Description

The MAX153 high-speed, microprocessor (µP)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 660ns conversion time, and digitizes at a rate of 1M samples per second (Msps). It operates with single +5V or dual ±5V supplies and accepts either unipolar or bipolar inputs. A POWER-DOWN pin reduces current consumption to a typical value of 1µA (with 5V supply). The part returns from power-down to normal operating mode in less than 200ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX153 is DC and dynamically tested. Its µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

Applications

Cellular Telephones

Portable Radios

Battery-Powered Systems

Burst-Mode Data Acquisition

Digital-Signal Processing

Telecommunications

High-Speed Servo Loops

Features

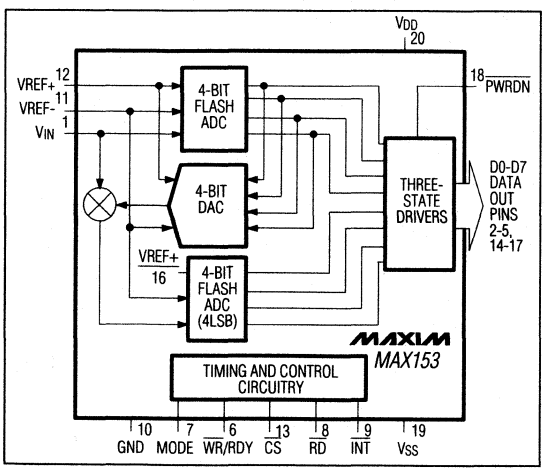
- ♦ **660ns Conversion Time**
- ♦ **Power-Up/Power-Down in 200ns**
- ♦ **Internal Track/Hold**
- ♦ **1Msps Throughput**
- ♦ **Low Power: 40mW (Operating Mode)**
  5µW (Powerdown Mode)
- ♦ **1MHz Full-Power Bandwidth**
- ♦ **20-Pin Narrow DIP, SO and SSOP Packages**
- ♦ **No External Clock Required**
- ♦ **Unipolar/Bipolar Inputs**
- ♦ **Single +5V or Dual ±5V Supplies**
- ♦ **Ratiometric Reference Inputs**

Ordering Information

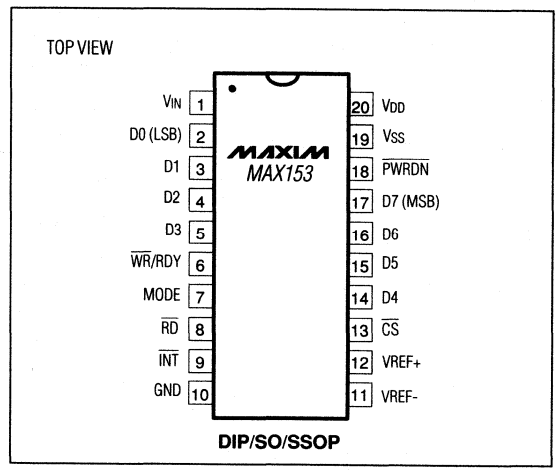
PART	TEMP. RANGE	PIN-PACKAGE
MAX153CPP	0°C to +70°C	20 Plastic DIP
MAX153CWP	0°C to +70°C	20 Wide SO
MAX153CAP	0°C to +70°C	20 SSOP***
MAX153C/D	0°C to +70°C	Dice*
MAX153EPP	-40°C to +85°C	20 Plastic DIP
MAX153EWP	-40°C to +85°C	20 Wide SO
MAX153EAP	-40°C to +85°C	20 SSOP***
MAX153MJP	-55°C to +125°C	20 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*
*** *Contact factory for availability of SSOP packages.*

Functional Diagram



Pin Configuration



DIP/SO/SSOP

7

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to +7V
V_{SS} to GND ..... +0.3V to -7V
Digital Input Voltage to GND ..... +0.3V, V_{DD} + 0.3V
Digital Output Voltage to GND ..... -0.3V, V_{DD} + 0.3V
VREF+ to GND ..... V_{SS} -0.3V to V_{DD} + 0.3V
VREF- to GND ..... V_{SS} -0.3V to V_{DD} + 0.3V
V_{IN} to GND ..... V_{SS} -0.3V to V_{DD} + 0.3V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 600mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX153C_ _ ..... 0°C to +70°C
MAX153E_ _ ..... -40°C to +85°C
MAX153MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, GND = 0V; Unipolar Input Range: V_{SS} = GND, VREF+ = 5V, VREF- = GND; Bipolar Input Range: V_{SS} = -5V ±5%, VREF+ = 2.5V, VREF- = -2.5V; 100% production tested, specifications are given for RD Mode (Pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	N			8			Bits
Total Unadjusted Error	TUE	Unipolar range				±1	LSB
Differential Nonlinearity	DNL	No missing codes guaranteed				±1	LSB
Zero-Code Error		Bipolar input range				±1	LSB
Full-Scale Error		Bipolar input range				±1	LSB
DYNAMIC PERFORMANCE (Note 1)							
Signal-to-Noise Plus Distortion Ratio	S/(N+D)	MAX153C/E, f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz		45			dB
		MAX153M, f_{SAMPLE} = 740kHz, f_{IN} = 195.7kHz					
Total Harmonic Distortion	THD	MAX153C/E, f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz				-50	dB
		MAX153M, f_{SAMPLE} = 740kHz, f_{IN} = 195.7kHz					
Peak Harmonic or Spurious Noise		MAX153C/E, f_{SAMPLE} = 1MHz, f_{IN} = 195.8kHz				-50	dB
		MAX153M, f_{SAMPLE} = 740kHz, f_{IN} = 195.7kHz					
Conversion Time (WR-RD Mode) (Note 2)	t_{CWR}	T_A = +25°C, t_{RD} < t_{INTL}, C_L = 20pF				660	ns
Conversion Time (RD Mode)	t_{CRD}	T_A = +25°C				700	ns
		T_A = T_{MIN} to T_{MAX}	MAX153C/E			875	
			MAX153M			975	
Full-Power Input Bandwidth		V_{IN} = $5V_{p-p}$			1		MHz
Input Slew Rate				3.14	15		V/µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, GND = 0V; Unipolar Input Range: V_{SS} = GND, VREF+ = 5V, VREF- = GND; Bipolar Input Range: V_{SS} = -5V ±5%, VREF+ = 2.5V, VREF- = -2.5V; 100% production tested, specifications are given for RD Mode (Pin 7 = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Input Voltage Range	V_{IN}			VREF-		VREF+	V
Input Leakage Current	I_{IN}	-5V ≤ V_{IN} ≤ 5V				±3	µA
Input Capacitance	C_{IN}				22		pF
REFERENCE INPUT							
Reference Resistance	RREF			1	2	4	kΩ
VREF+ Input Voltage Range				VREF-		V_{DD}	V
VREF- Input Voltage Range				V_{SS}		VREF+	V
LOGIC INPUTS							
Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$		2.4			V
		MODE		3.5			
Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$				0.8	V
		MODE				1.5	
Input High Current	I_{INH}	$\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$				1	µA
		$\overline{WR}$				3	
		MODE			50	200	
Input Low Current	I_{INL}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{PWRDN}$				±1	µA
Input Capacitance (Note 3)	C_{IN}	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{PWRDN}$, MODE			5	8	pF
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA, $\overline{INT}$, D0-D7				0.4	V
		RDY, I_{SINK} = 2.6mA				0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 360µA, $\overline{INT}$, D0-D7		4			V
Floating State Current	I_{LKG}	D0-D7, RDY				±3	µA
Floating Capacitance (Note 3)	C_{OUT}	D7-D0, RDY			5	8	pF
POWER REQUIREMENTS							
V_{DD}	V_{DD}	±5% for specified accuracy			5		V
V_{SS} (Unipolar Operation)	V_{SS}				GND		V
V_{SS} (Bipolar Operation)	V_{SS}	±5% for specified accuracy			-5		V
V_{DD} Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = 0V, PWRDN = 5V	MAX153C		8	15	mA
			MAX153E/M		8	20	
Power-Down V_{DD} Current		$\overline{CS}$ = $\overline{RD}$ = 5V, $\overline{PWRDN}$ = 0V (Note 4)			1	100	µA
V_{SS} Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = 0V, $\overline{PWRDN}$ = 5V			25	100	µA
Power-Down V_{SS} Current		$\overline{CS}$ = $\overline{RD}$ = 5V, $\overline{PWRDN}$ = 0V			12	100	µA
Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V, VREF+ = 4.75V max, unipolar mode			±1/16	±1/4	LSB

Note 1: Bipolar input range, V_{IN} = ±2.5V_{p-p}, WR-RD mode
Note 2: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross +0.8V or +2.4V.
Note 3: Guaranteed by design.
Note 4: Tested with $\overline{CS}$, $\overline{RD}$, $\overline{PWRDN}$ at CMOS logic levels. Power-down current increases to several hundred µA at TTL levels.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +5V ±5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V ±5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time	t_{CSS}			0			ns
$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time	t_{CSH}			0			ns
$\overline{CS}$ to $\overline{RDY}$ Delay (Note 6)	t_{RDY}	C_L = 50pF				70	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			85	
			MAX153M			100	
Data-Access Time (RD Mode) (Note 2)	t_{ACC0}	C_L = 20pF				t_{CRD}+25	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF	MAX153C/E			t_{CRD}+30	
			MAX153M			t_{CRD}+35	
		C_L = 100pF				t_{CRD}+50	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF	MAX153C/E			t_{CRD}+65	
			MAX153M			t_{CRD}+75	
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t_{INTH}	C_L = 50pF			50	80	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			85	
			MAX153M			90	
Data-Hold Time (Note 7)	t_{DH}					60	ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E			70	
			MAX153M			80	
Delay Time Between Conversions (Acquisition Time)	t_P			160			ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E	185			
			MAX153M	260			
Write Pulse Width	t_{WR}			0.250		10	µs
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E	0.280		10	
			MAX153M	0.400		10	
Delay Time Between WR and RD Pulses	t_{RD}			250			ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E	350			
			MAX153M	450			
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC1}	t_{READ1}	Figure 6		160			ns
		$T_A = T_{MIN}$ to T_{MAX}, Figure 6	MAX153C/E	205			
			MAX153M	240			

TIMING CHARACTERISTICS (Note 4) (continued)

(V_{DD} = +5V ±5%, V_{SS} = 0V for Unipolar Input Range, V_{SS} = -5V ±5% for Bipolar Input Range, 100% production tested, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data-Access Time (WR-RD Mode) (Note 2) $t_{RD} < t_{INL}$	t_{ACC1}	C_L = 20pF, Figure 6				160	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF, Figure 6	MAX153C/E			205	
			MAX153M			240	
		C_L = 100pF, Figure 6				185	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF, Figure 6	MAX153C/E			235	
			MAX153M			275	
$\overline{RD}$ to $\overline{INT}$ Delay	t_{RI}					150	ns
		$T_A = T_{MIN}$ to T_{MAX}	MAX153C/E			185	
			MAX153M			220	
$\overline{WR}$ to $\overline{INT}$ Delay	t_{INTL}	C_L = 50pF			380	500	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			610	
			MAX153M			700	
$\overline{RD}$ Pulse Width (WR-RD Mode) Determined by t_{ACC2} $t_{RD} > t_{INTL}$	tREAD2	Figure 5		65			ns
		$T_A = T_{MIN}$ to T_{MAX}, Figure 5	MAX153C/E	75			
			MAX153M	85			
Data-Access Time (WR-RD Mode) (Note 2) $t_{RD} > t_{INTL}$	tACC2	C_L = 20pF, Figure 5				65	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF, Figure 5	MAX153C/E			75	
			MAX153M			85	
		C_L = 100pF, Figure 5				90	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF, Figure 5	MAX153C/E			110	
			MAX153M			130	
$\overline{WR}$ to $\overline{INT}$ Delay (Pipe-Lined Mode)	t_{IHWR}	C_L = 50pF				80	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 50pF	MAX153C/E			100	
			MAX153M			120	
Data-Access Time After $\overline{INT}$ (Note 2)	t_{ID}	C_L = 20pF				30	ns
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 20pF	MAX153C/E			35	
			MAX153M			40	
		C_L = 100pF				45	
		$T_A = T_{MIN}$ to T_{MAX}, C_L = 100pF	MAX153C/E			60	
			MAX153M			70	

Note 5: Input control signals are specified with $t_r = t_f$ = 5ns, 10% to 90% of +5V and timed from a 1.6V voltage level.
Note 6: R_L = 5.1kΩ pull-up resistor.
Note 7: See Figure 2 for load circuit. Parameter defined as the time required for data lines to change 0.5V.

1Msps, µP-Compatible, 8-Bit ADC with 1µA Powerdown

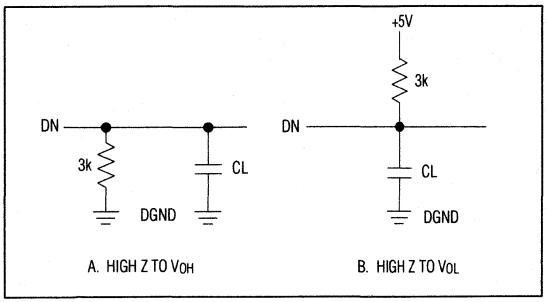


Figure 1. Load Circuits for Data-Access Time Test

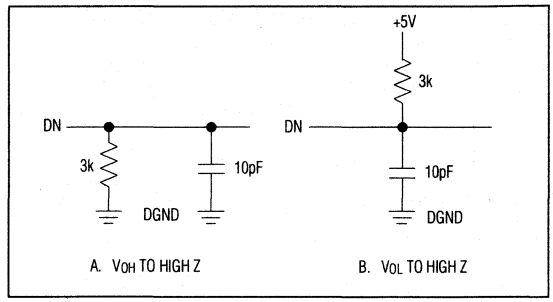
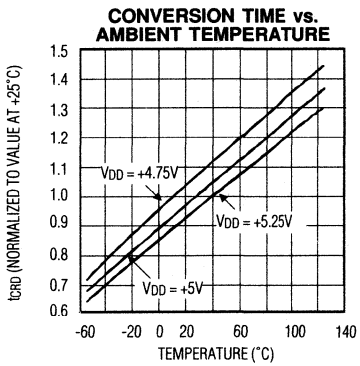
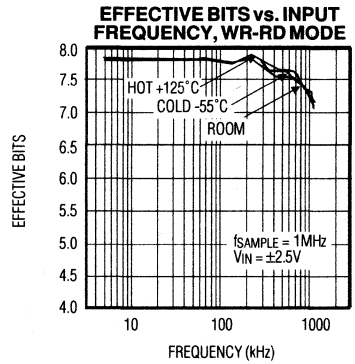
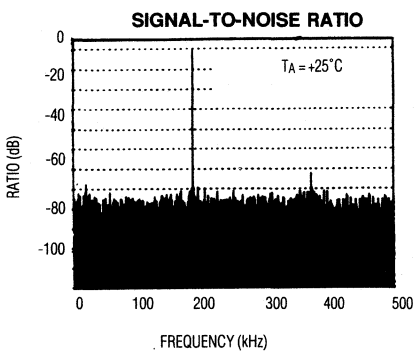


Figure 2. Load Circuits for Data-Hold Time Test

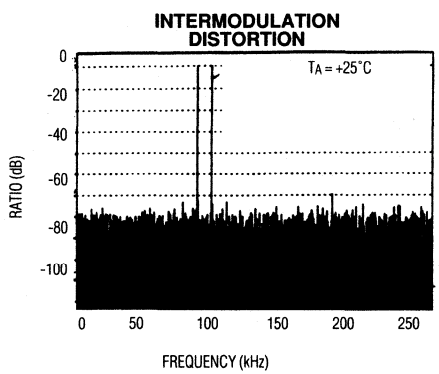
Typical Operating Characteristics







INPUT FREQUENCY = 195.8ksps (±2.5V)
SAMPLE FREQUENCY = 1MHz
SNR = 49.1dB



INPUT FREQUENCY = 94.97kHz
84.72kHz (±2.5V)
SAMPLE FREQUENCY = 500kHz
IMD: 2ND-ORDER TERMS = -66.2dB
3RD-ORDER TERMS = -60.0dB

19-0123; Rev. 1; 8/93

CONTACT FACTORY FOR COMPLETE DATA SHEET

MAXIM

Low-Power, 8-Channel, Serial 12-Bit ADCs

General Description

The MAX186/MAX188 are 12-bit data-acquisition systems that combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface together with high conversion speed and ultra-low power consumption. The devices operate with a single +5V supply or dual ±5V supplies. The analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface directly connects to SPI™, QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX186/MAX188 use either the internal clock or an external serial-interface clock to perform successive-approximation A/D conversions. The serial interface can operate beyond 4MHz when the internal clock is used.

The MAX186 has an internal 4.096V reference while the MAX188 requires an external reference. Both parts have a reference-buffer amplifier that simplifies gain trim .

The MAX186/MAX188 provide a hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the devices, and the quick turn-on time allows the MAX186/MAX188 to be shut down between every conversion. Using this technique of powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX186/MAX188 are available in 20-pin DIP and SO packages, and in a shrink small-outline package (SSOP), that occupies 30% less area than an 8-pin DIP. For applications that call for a parallel interface, see the MAX180/MAX181 data sheet. For anti-aliasing filters, consult the MAX274/MAX275 data sheet.

Applications

Portable Data Logging
Data-Acquisition
High-Accuracy Process Control
Automatic Testing
Robotics
Battery-Powered Instruments
Medical Instruments

Features

- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Single +5V or ±5V Operation**
- ♦ **Low Power: 1.5mA (operating mode)**
  2µA (power-down mode)
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **Internal 4.096V Reference (MAX186)**
- ♦ **SPI-, QSPI-, Microwire-, TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **20-Pin DIP, SO, SSOP Packages**
- ♦ **Evaluation Kit Available**

Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE
MAX186_CPP	0°C to +70°C	20 Plastic DIP
MAX186_CWP	0°C to +70°C	20 SO
MAX186_CAP	0°C to +70°C	20 SSOP
MAX186DC/D	0°C to +70°C	Dice*
MAX186_EPP	-40°C to +85°C	20 Plastic DIP
MAX186_EWP	-40°C to +85°C	20 SO
MAX186_EAP	-40°C to +85°C	20 SSOP
MAX186_MJP	-55°C to +125°C	20 CERDIP**

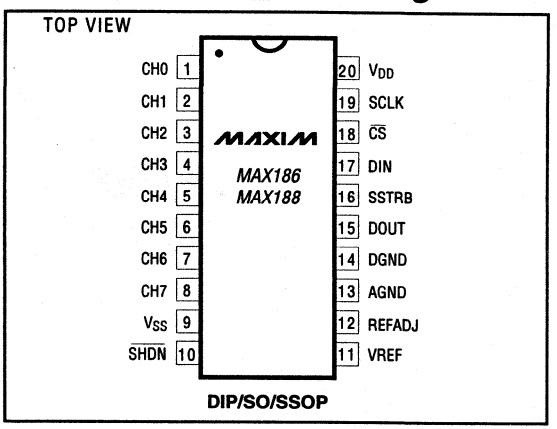
Ordering Information continued on last page.

† *NOTE: Parts are offered in grades A, B, C and D (grades defined in Electrical Characteristics). When ordering, please specify grade. Contact factory for availability of A-grade in SSOP package.*

* *Dice are specified at +25°C, DC parameters only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



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Low-Power, 8-Channel, Serial 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V to +6V
V_{SS} to AGND ..... +0.3V to -6V
V_{DD} to V_{SS} ..... -0.3V to +12V
AGND to DGND ..... -0.3V to +0.3V
CH0-CH7 to AGND, DGND ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
REFADJ to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX186_C/MAX188_C ..... 0°C to +70°C
MAX186_E/MAX188_E ..... -40°C to +85°C
MAX186_M/MAX188_M ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)		MAX186A/MAX188A				±0.5	LSB
		MAX186B/MAX188B				±0.5	
		MAX186C				±1.0	
		MAX188C				±0.75	
		MAX186D/MAX188D				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		MAX186A/MAX188A				±1.0	LSB
		MAX186B				±3.0	
		MAX188B				±1.5	
		MAX186C				±1.0	
		MAX188C				±1.5	
		MAX186D/MAX188D				±3.0	
Gain Error (Note 3)		MAX186 (all grades)				±3.0	LSB
		External reference, 4.096V (MAX188)	MAX188A			±0.5	
			MAX188B			±1.5	
			MAX188C			±2.0	
			MAX188D			±3.0	
Gain Temperature Coefficient		External reference, 4.096V			±0.8		ppm/°C
Channel-to-Channel Offset Matching					±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 4.096V_{p-p}, 133ksps, 2.0MHz external clock, bipolar input mode)							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD					-80	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		65kHz, V_{IN} = 4.096V_{p-p} (Note 4)			-85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth		-3dB rolloff		4.5		MHz
Full-Power Bandwidth				800		kHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{AZ}				1.5	µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz
External Clock Frequency Range		External compensation, 4.7µF	0.1		2.0	MHz
		Internal compensation (Note 6)	0.1		0.4	
		Used for data transfer only		10		
ANALOG INPUT						
Input Voltage Range, Single-Ended and Differential (Note 9)		Unipolar, V_{SS} = 0V			0 to VREF	V
		Bipolar, V_{SS} = -5V			±VREF/2	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = ±5V		±0.01	±1	µA
Input Capacitance		(Note 6)		16		pF
INTERNAL REFERENCE (MAX186 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
VREF Short-Circuit Current					30	mA
VREF Tempco		MAX186A, MAX186B, MAX186C — MAX186_C		±30	±50	ppm/°C
		MAX186A, MAX186B, MAX186C — MAX186_E		±30	±60	
		MAX186A, MAX186B, MAX186C — MAX186_M		±30	±80	
		MAX186D		±30		
Load Regulation (Note 7)		0mA to 0.5mA output load		2.5		mV
Capacitive Bypass at VREF		Internal compensation	0			µF
		External compensation	4.7			
Capacitive Bypass at REFADJ		Internal compensation	0.01			µF
		External compensation	0.01			
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled, VREF = 4.096V)						
Input Voltage Range			2.50		V_{DD} + 50mV	V
Input Current				200	350	µA
Input Resistance			12	20		kΩ
Shutdown VREF Input Current				1.5	10	µA
Buffer Disable Threshold REFADJ			V_{DD} - 50mV			V

Low-Power, 8-Channel, Serial 12-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX186		1.678		V/V
		MAX188		1.638		
REFADJ Input Current		MAX186			±50	µA
		MAX188			±5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.4			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{INH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{INL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.5		V_{DD} -1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 6)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down		30	70	µA
		Full power-down		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; V_{SS} = 0V or -5V; f_{CLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX186 - 4.7µF capacitor at VREF pin; MAX188 - external reference, VREF = 4.096V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Rejection (Note 8)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 8)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV

Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX186 – internal reference, offset nulled; MAX188 – external reference (VREF = +4.096V), offset nulled.
Note 4: Ground on-channel; sine wave applied to all off channels.
Note 5: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.
Note 9: The common-mode range for the analog inputs is from V_{SS} to V_{DD}.

TIMING CHARACTERISTICS

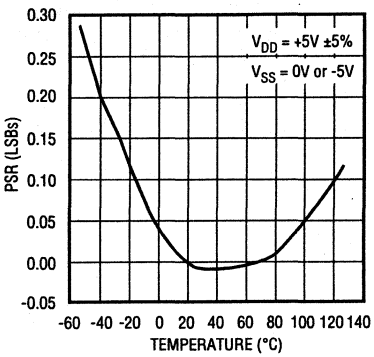
(V_{DD} = 5V ±5%; V_{SS} =0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{AZ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX188_C/E	20		150	ns
			MAX188_M	20		200	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF				200	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF				200	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only		0			ns

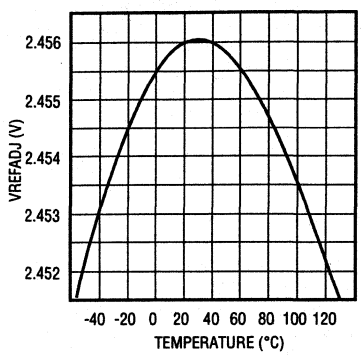
Low-Power, 8-Channel, Serial 12-Bit ADCs

Typical Operating Characteristics

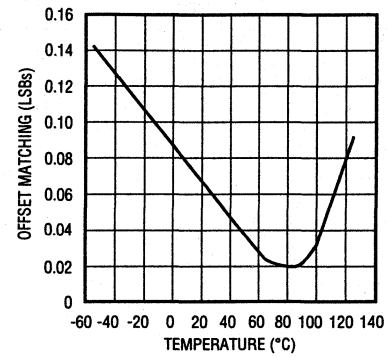
POWER-SUPPLY REJECTION vs. TEMPERATURE



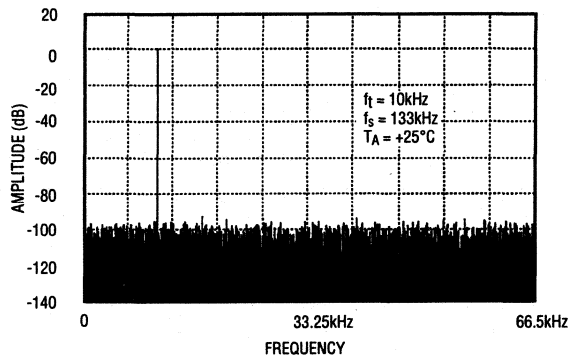
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



MAX186/MAX188 FFT PLOT – 133kHz



19-0196; Rev 0; 10/93

MAXIM

+5V, Low-Power, 12-Bit Serial ADCs

General Description

The MAX187/MAX189 serial 12-bit analog-to-digital converters (ADCs) operate from a single +5V supply and accept a 0V to 5V analog input. Both parts feature an 8.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed 3-wire serial interface.

The MAX187/MAX189 digitize signals at a 75ksps throughput rate. An external clock accesses data from the interface, which communicates without external hardware to most digital signal processors and microcontrollers. The interface is compatible with SPI™, QSPI™, and Microwire™.

The MAX187 has an on-chip buffered reference, and the MAX189 requires an external reference. Both the MAX187 and MAX189 save space with 8-pin DIP and 16-pin SO packages. Power consumption is 7.5mW and reduces to only 10µW in shutdown.

Excellent AC characteristics and very low power consumption combined with ease of use and small package size make these converters ideal for remote DSP and sensor applications, or for circuits where power consumption and space are crucial.

Applications

Portable Data Logging

Remote Digital Signal Processing

Isolated Data Acquisition

High-Accuracy Process Control

Features

- **12-Bit Resolution**
- **±½ LSB Integral Nonlinearity (MAX187A/MAX189A)**
- **Internal Track/Hold, 75kHz Sampling Rate**
- **Single +5V Operation**
- **Low Power: 2µA Shutdown Current**
  1.5mA Operating Current
- **Internal 4.096V Buffered Reference (MAX187)**
- **3-Wire Serial Interface, Compatible with SPI, QSPI, and Microwire**
- **Small-Footprint 8-Pin DIP and 16-Pin SO**

Ordering Information

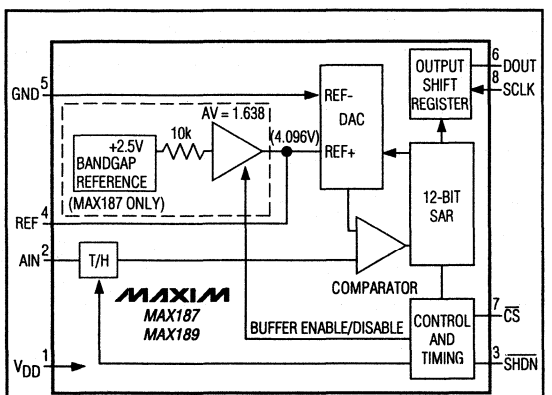
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX187ACPA	0°C to +70°C	8 Plastic DIP	±½
MAX187BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX187CCPA	0°C to +70°C	8 Plastic DIP	±2
MAX187ACWE	0°C to +70°C	16 Wide SO	±½
MAX187BCWE	0°C to +70°C	16 Wide SO	±1
MAX187CCWE	0°C to +70°C	16 Wide SO	±2
MAX187BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

* *Dice are specified at T_A = +25°C, DC parameters only.*

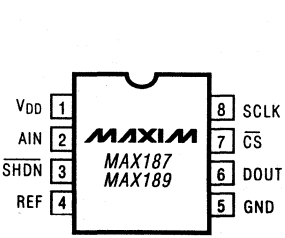
** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



NOTE: PIN NUMBERS SHOWN ARE FOR 8-PIN DIPs ONLY.

Pin Configurations



Pin Configurations continued on last page.

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+5V, Low-Power, 12-Bit Serial ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to GND .....-0.3V to (V_{DD} + 0.3V)
$\overline{SHDN}$ to GND .....-0.3V to (V_{DD} + 0.3V)
REF Load Current (MAX187) .....4.0mA Continuous
REF Short-Circuit Duration (MAX187) 20sec
DOUT Current .....±20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ..500mW
16-Pin Wide SO (derate 8.70mW/°C above +70°C) ...478mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 440mW
Operating Temperature Ranges:
MAX187_C_ _/MAX189_C_ _ .....0°C to +70°C
MAX187_E_ _/MAX189_E_ _ .....-40°C to +85°C
MAX187_MJA/MAX189_MJA .....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%; GND = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution					12	Bits
Relative Accuracy (Note 2)		MAX18_A			±½	LSB
		MAX18_B			±1	
		MAX18_C			±2	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX18_A			±1½	LSB
		MAX18_B/C			±3	
Gain Error (Note 3)		MAX187			±3	LSB
		MAX189A			±1	
		MAX189B/C			±3	
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine wave input, 0V to 4.096V_{p-p}, 75ksps)						
Signal-to-Noise plus Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD				-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Small-Signal Bandwidth		Rolloff -3dB		4.5		MHz
Full-Power Bandwidth				0.8		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; GND = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CONVERSION RATE							
Conversion Time	t_{CONV}			5.5		8.5	µs
Track/Hold Acquisition Time	t_{ACQ}			1.5			µs
Throughput Rate		External clock, 4MHz, 13 clocks				75	ksps
Aperture Delay	t_{APR}				10		ns
Aperture Jitter					<50		ps
ANALOG INPUT							
Input Voltage Range						0 to V_{REF}	V
Input Capacitance (Note 4)					16		pF
INTERNAL REFERENCE (MAX187 only, reference buffer enabled)							
REF Output Voltage	V_{REF}	T_A = +25°C		4.076	4.096	4.116	V
		T_A = T_{MIN} to T_{MAX}	MAX187_C	4.060		4.132	
			MAX187_E	4.050		4.140	
			MAX187_M	4.040		4.150	
REF Short-Circuit Current						30	mA
REF Tempco		MAX187AC/BC			±30	±50	ppm/°C
		MAX187AE/BE			±30	±60	
		MAX187AM/BM			±30	±80	
		MAX187C			±30		
Load Regulation (Note 5)		0mA to 0.6mA output load			1		mV
EXTERNAL REFERENCE AT REF (Buffer disabled, V_{REF} = 4.096V)							
Input Voltage Range				2.50		V_{DD} + 50mV	V
Input Current					200	350	µA
Input Resistance				12	20		kΩ
Shutdown REF Input Current					1.5	10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%; GND = 0V; unipolar input mode; 75ksps, f_{CLK} = 4.0MHz, external clock (50% duty cycle); MAX187—internal reference: V_{REF} = 4.096V, 4.7µF capacitor at REF pin, or MAX189—external reference: V_{REF} = 4.096V applied to REF pin, 4.7µF capacitor at REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, $\overline{CS}$, $\overline{SHDN}$)							
SCLK, $\overline{CS}$ Input High Voltage	V_{INH}			2.4			V
SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}					0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.15		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 4)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{INSH}			V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INSL}					0.5	V
$\overline{SHDN}$ Input Current	I_{INS}	$\overline{SHDN}$ = V_{DD} or 0V				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}			1.5		V_{DD} -1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open			2.75		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = open		-100		100	nA
DIGITAL OUTPUT (DOUT)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA			0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V				±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 4)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Operating mode	MAX187		1.5	2.5	mA
			MAX189		1.0	2.0	
		Power-down mode			2	10	µA
Power-Supply Rejection	PSR	V_{DD} = +5V, ±5%; external reference, 4.096V; full-scale input (Note 6)			±0.06	±0.5	mV

TIMING CHARACTERISTICS

(V_{DD} = +5.0V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time	t_{ACQ}	$\overline{CS}$ = high (Note 7)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	MAX18_ _C/E	20		150	ns
			MAX18_ _M	20		200	
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF				100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF				100	ns
SCLK Clock Frequency	f_{SCLK}					5	MHz
SCLK Pulse Width High	t_{CH}			100			ns
SCLK Pulse Width Low	t_{CL}			100			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CSO}			50			ns
$\overline{CS}$ Pulse Width	t_{CS}			500			ns

Note 1: Tested at V_{DD} = +5V.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: MAX187—internal reference, offset nulled; MAX189–external +4.096V reference, offset nulled. Excludes reference errors.

Note 4: Guaranteed by design. Not subject to production testing.

Note 5: External load should not change during conversion for specified ADC accuracy.

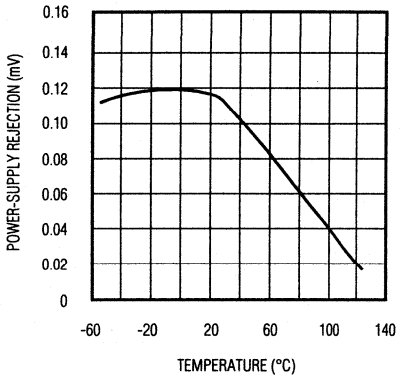
Note 6: DC test, measured at 4.75V and 5.25V only.

Note 7: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.

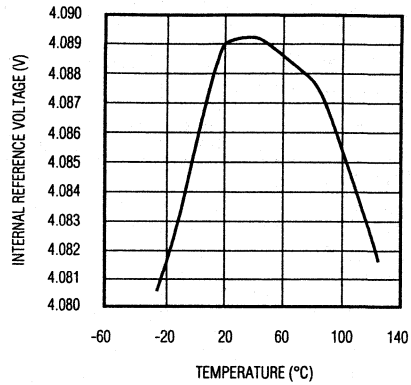
+5V, Low-Power, 12-Bit Serial ADCs

Typical Operating Characteristics

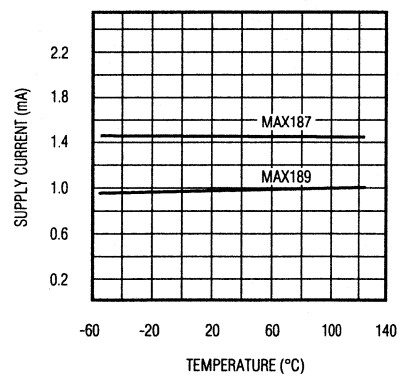
POWER-SUPPLY REJECTION vs. TEMPERATURE



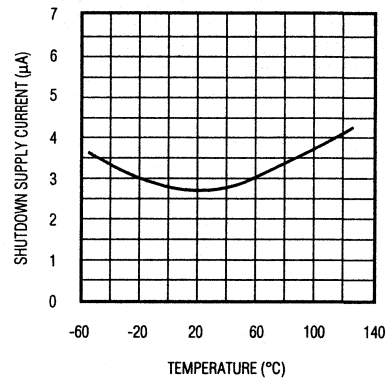
V_{REF} vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
DIP	WIDE SO		
1	1	V_{DD}	Supply voltage, +5V ±5%
2	3	AIN	Sampling analog input, 0V to V_{REF} range
3	6	$\overline{SHDN}$	Three-level shutdown input. Pulling $\overline{SHDN}$ low shuts the MAX187/MAX189 down to 10µA (max) supply current. Both MAX187 and MAX189 are fully operational with either $\overline{SHDN}$ high or floating. For the MAX187, pulling $\overline{SHDN}$ high enables the internal reference, and letting $\overline{SHDN}$ float disables the internal reference and allows for the use of an external reference.
4	8	REF	Reference voltage—sets analog voltage range and functions as a 4.096V output for the MAX187 with enabled internal reference. REF also serves as a +2.5V to V_{DD} input for a precision reference for both MAX187 (disabled internal reference) and MAX189. Bypass with 4.7µF if internal reference is used, and with 0.1µF if an external reference is applied.
5	—	GND	Analog and digital ground
—	10	AGND	Analog ground
—	11	DGND	Digital ground
6	12	DOUT	Serial data output. Data changes state at SCLK's falling edge.
7	15	$\overline{CS}$	Active-low chip select initiates conversions on the falling edge. When $\overline{CS}$ is high, DOUT is high impedance.
8	16	SCLK	Serial clock input. Clocks data out with rates up to 5MHz.
—	2,4,5,7,9,13,14	N.C.	Not internally connected. Connect to AGND for best noise performance.

Detailed Description

Converter Operation

The MAX187/MAX189 use input track/hold (T/H) and successive approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. No external hold capacitor is needed for the T/H. Figures 3a and 3b show the MAX187/MAX189 in their simplest configuration. The MAX187/MAX189 convert input signals in the 0V to V_{REF} range in 10µs, including T/H acquisition time. The MAX187's internal reference is trimmed to 4.096V, while the MAX189 requires an external reference. Both devices accept external reference voltages from +2.5V to V_{DD}. The serial interface requires only three digital lines, SCLK, $\overline{CS}$, and DOUT, and provides easy interface to microprocessors (µPs).

Both converters have two modes: normal and shutdown. Pulling $\overline{SHDN}$ low shuts the device down and reduces supply current to below 10µA, while pulling $\overline{SHDN}$ high or leaving it floating puts the device into the operational mode. A conversion is initiated by $\overline{CS}$ falling. The conversion result is available at DOUT in unipolar serial format. A high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first), make up the serial data stream.

The MAX187 operates in one of two states: (1) internal reference and (2) external reference. Select internal reference operation by forcing $\overline{SHDN}$ high, and external reference operation by floating $\overline{SHDN}$.

Analog Input

Figure 4 illustrates the sampling architecture of the ADC's analog comparator. The full-scale input voltage depends on the voltage at REF.

REFERENCE	ZERO SCALE	FULL SCALE
Internal Reference (MAX187 only)	0V	+4.096V
External Reference	0V	V_{REF}

For specified accuracy, the external reference voltage range spans from +2.5V to V_{DD}.

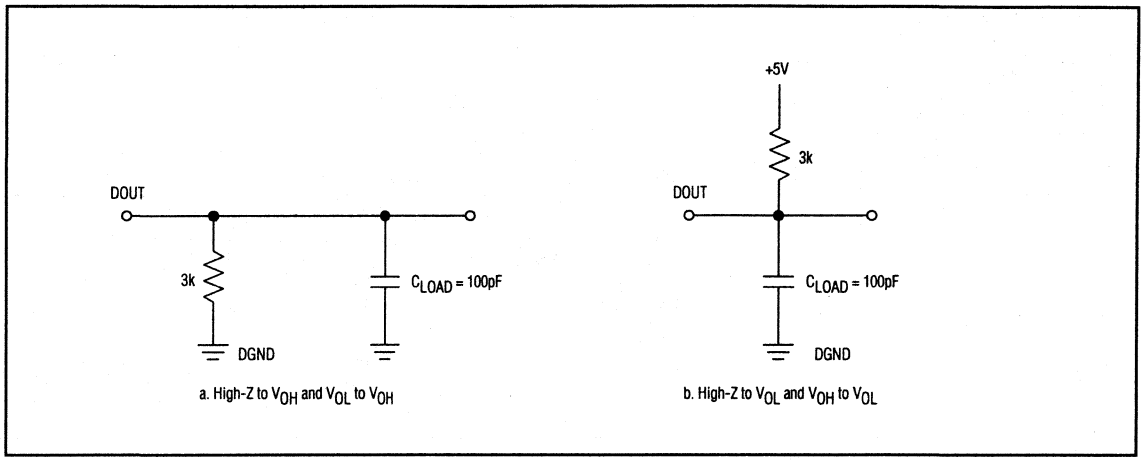


Figure 1. Load Circuits for DOUT Enable Time

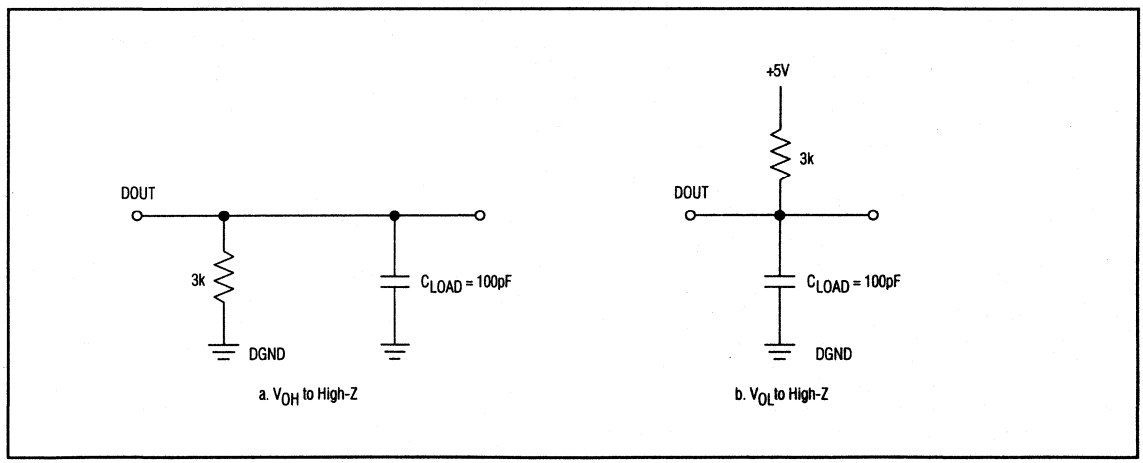


Figure 2. Load Circuits for DOUT Disable Time

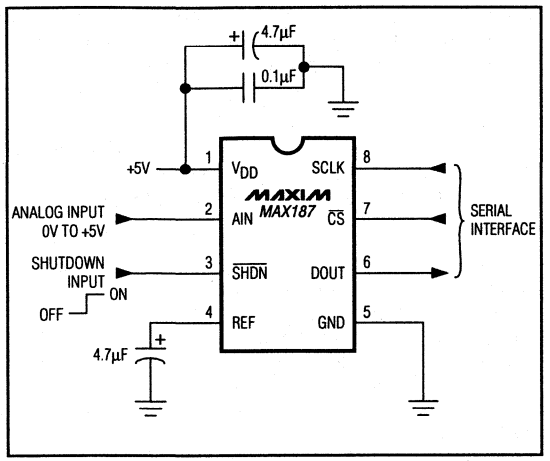


Figure 3a. MAX187 Operational Diagram

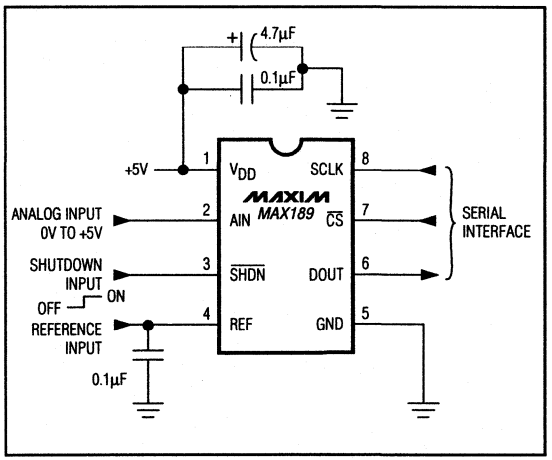


Figure 3b. MAX189 Operational Diagram

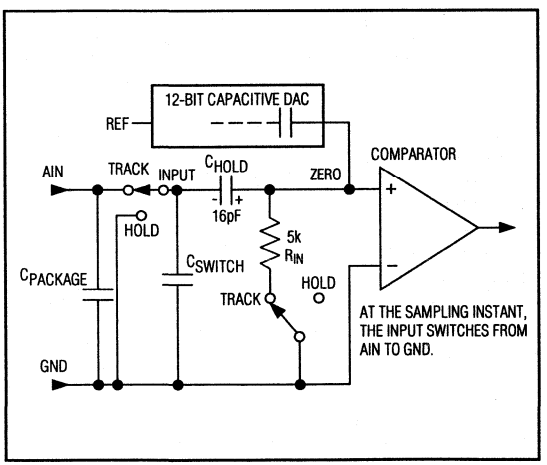


Figure 4. Equivalent Input Circuit

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input AIN charges capacitor C_{HOLD}. Bringing $\overline{CS}$ low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing the node ZERO at the comparator's input.

In hold mode, the capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of a 12-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 9\ (R_S + R_{IN})\ 16pF,$$

where R_{IN} = 5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Source impedances below 5kΩ do not significantly affect the AC performance of the ADC.

+5V, Low-Power, 12-Bit Serial ADCs

Input Bandwidth

The ADCs' input tracking circuitry has a 4.5MHz small-signal bandwidth, and an 8V/µs slew rate. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, an anti-alias filter is recommended. See the MAX274/MAX275 continuous-time filters data sheet.

Input Protection

Internal protection diodes that clamp the analog input allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds the supplies by more than 50mV beyond the supplies, limit the input current to 2mA, since larger currents degrade conversion accuracy.

Driving the Analog Input

The input lines to AIN and GND should be kept as short as possible to minimize noise pickup. Shield longer leads. Also see the *Input Protection* section.

Because the MAX187/MAX189 incorporate a T/H, the drive requirements of the op amp driving AIN are less stringent than those for a successive-approximation ADC without a T/H. The typical input capacitance is 16pF. The amplifier bandwidth should be sufficient to handle the frequency of the input signal. The MAX400 and OP07 work well at lower frequencies. For higher-frequency operation, the MAX427 and OP27 are practical choices. The allowed input frequency range is limited by the 75ksps sample rate of the MAX187/MAX189. Therefore, the maximum sinusoidal input frequency allowed is 37.5kHz. Higher-frequency signals cause aliasing problems unless undersampling techniques are used.

Reference

The MAX187 can be used with an internal or external reference, while the MAX189 requires an external reference.

Internal Reference

The MAX187 has an on-chip reference with a buffered temperature-compensated bandgap diode, laser-trimmed to +4.096V ±0.5%. Its output is connected to REF and also drives the internal DAC. The output can be used as a reference voltage source for other components and can source up to 0.6mA. Decouple REF with a 4.7µF capacitor. The internal reference is enabled by pulling the $\overline{SHDN}$ pin high. Letting $\overline{SHDN}$ float disables the internal reference, which allows the use of an external reference, as described in the *External Reference* section.

External Reference

The MAX189 operates with an external reference at the REF pin. To use the MAX187 with an external reference, disable the internal reference by letting $\overline{SHDN}$ float. Stay within the voltage range +2.5V to V_{DD} to achieve specified accuracy. The minimum input impedance is 12kΩ for DC currents. During conversion, the external reference must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

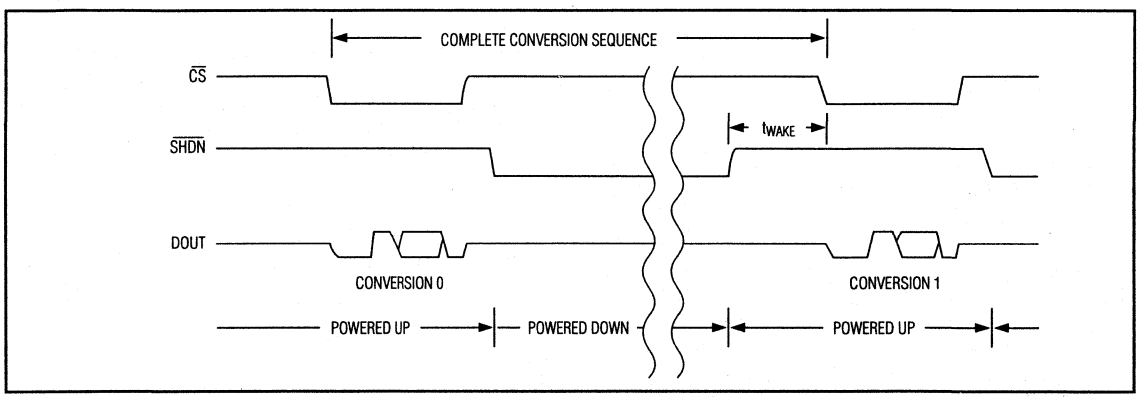


Figure 5. MAX187/MAX189 Shutdown Sequence

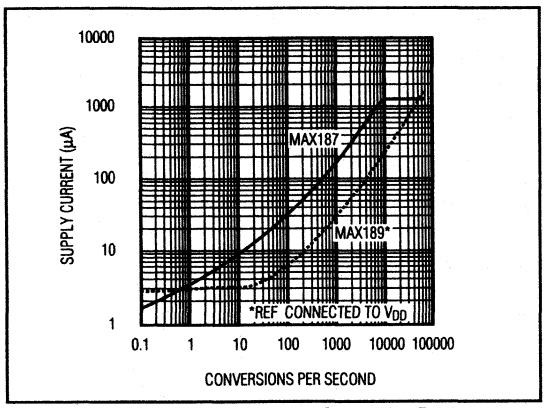


Figure 6. Average Supply Current vs. Conversion Rate

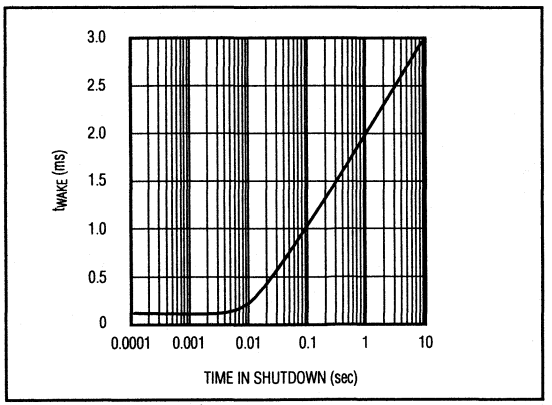


Figure 7. t_{WAKE} vs. Time in Shutdown (MAX187 only)

Serial Interface

Initialization After Power-Up and Starting a Conversion

When power is first applied, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy. With $\overline{SHDN}$ not pulled low, the MAX187/MAX189 are now ready to convert.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed 8.5µs conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using $\overline{SHDN}$ to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX187/MAX189 between conversions. This is shown in Figure 6, a plot of average supply current vs. conversion rate. Because the MAX189 uses an external reference voltage (assumed to be present continuously), it "wakes up" from shutdown more quickly, and therefore provides lower average supply currents. The wakeup-time, t_{WAKE}, is the time from $\overline{SHDN}$ deasserted to the time when a conversion may be initiated. For the MAX187, this time is 2µs. For the MAX189, this time depends on the time in shutdown (see Figure 7) because the external 4.7µF reference bypass capacitor loses charge slowly during shutdown (see the specifications for shutdown, REF Input Current = 10µA max).

External Clock

The actual conversion does not require the external clock. This frees the µP from the burden of running the SAR conversion clock, and allows the conversion result to be read back at the µP's convenience at any clock rate from 0MHz to 5MHz. The clock duty cycle is unrestricted if each clock phase is at least 100ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline the operation of the serial interface.

A $\overline{CS}$ falling edge initiates a conversion sequence: The T/H stage holds input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept inactive during the conversion. An internal register stores the data when the conversion is in progress.

End of conversion (EOC) is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing 0s at DOUT and have no effect on converter operation.

+5V, Low-Power, 12-Bit Serial ADCs

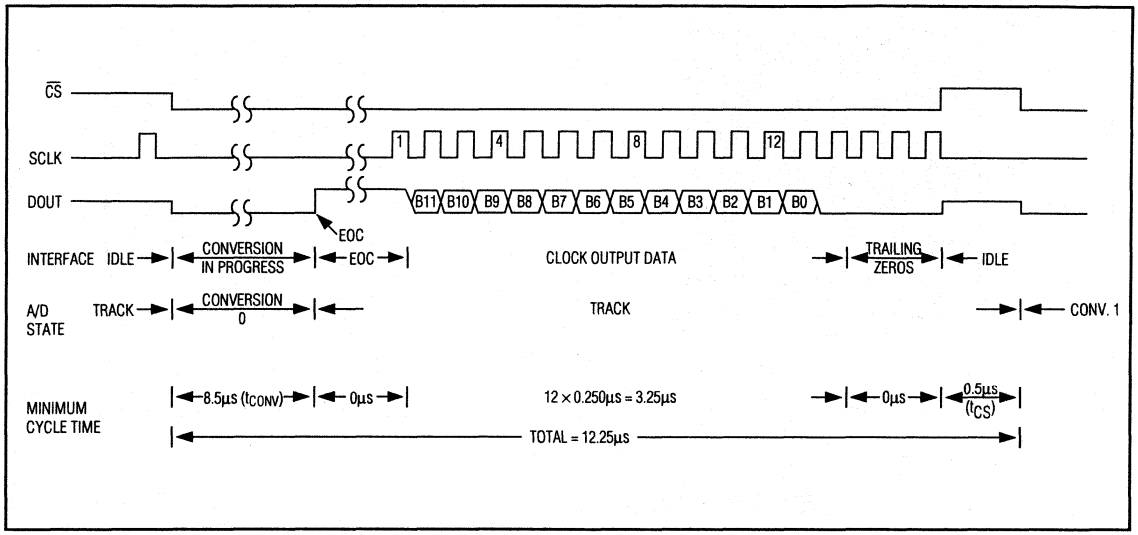


Figure 8. MAX187/MAX189 Interface Timing Sequence

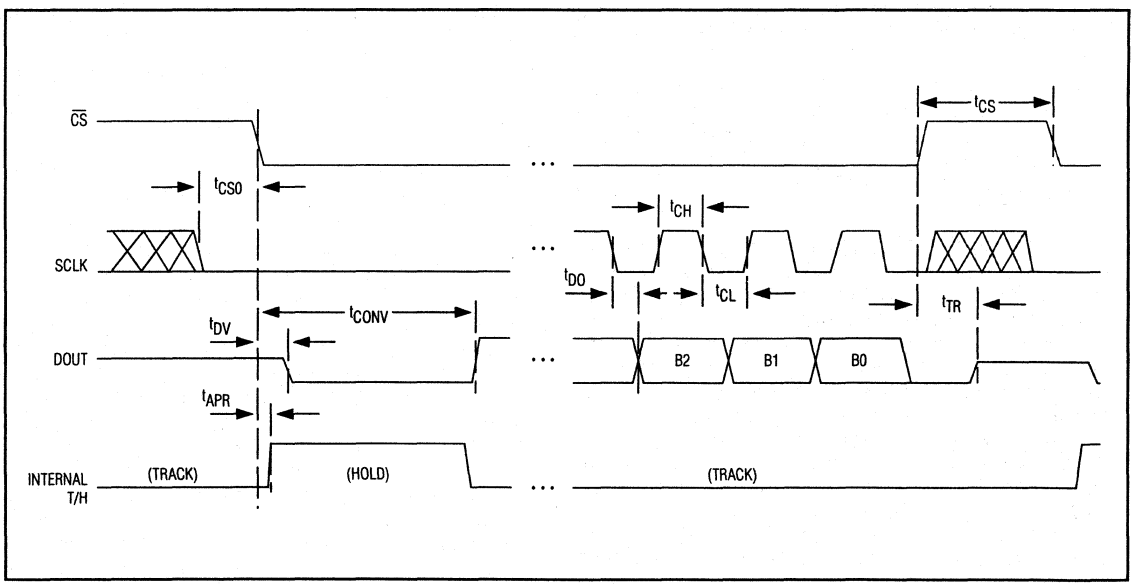


Figure 9. MAX187/MAX189 Detailed Serial-Interface Timing

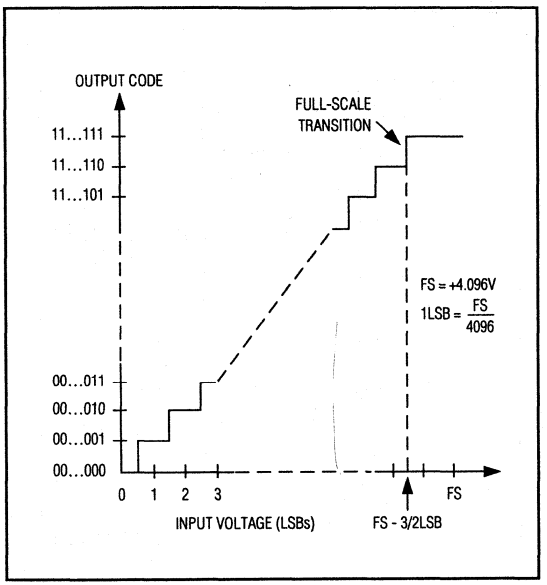


Figure 10. MAX187/MAX189 Unipolar Transfer Function, 4.096V = Full Scale

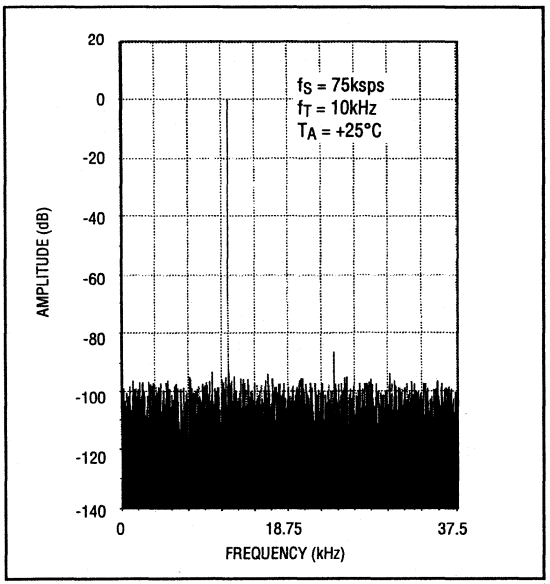


Figure 11. MAX187/MAX189 FFT plot

Minimum cycle time is accomplished by using DOUT's rising edge as the EOC signal. Clock out the data with 13 clock cycles at full speed. Raise $\overline{CS}$ after the conversion's LSB has been read. After the specified minimum time, t_{ACQ}, $\overline{CS}$ can be pulled low again to initiate the next conversion.

Output Coding and Transfer Function

The data output from the MAX187/MAX189 is binary, and Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive integer LSB values. If V_{REF} = +4.096V, then 1 LSB = 1.00mV or 4.096V/4096.

Dynamic Performance

High-speed sampling capability and a 75ksps throughput make the MAX187/MAX189 ideal for wideband signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques are used to guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm that determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency. ADCs have traditionally been evaluated by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications, where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS amplitude of all other ADC output signals. The input bandwidth is limited to frequencies above DC and below one-half the ADC sample (conversion) rate.

The theoretical minimum ADC noise is caused by quantization error and is a direct result of the ADC's resolution: SINAD = (6.02N + 1.76)dB, where N is the number of bits of resolution. An ideal 12-bit ADC can, therefore, do no better than 74dB. An FFT plot of the output shows the output level in various spectral bands. Figure 11 shows the result of sampling a pure 10kHz sine wave at a 75ksps rate with the MAX187/MAX189.

+5V, Low-Power, 12-Bit Serial ADCs

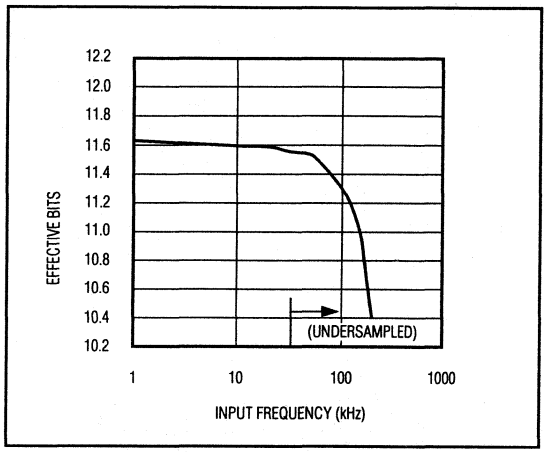


Figure 12. Effective Bits vs. Input Frequency

The effective resolution (effective number of bits) the ADC provides can be determined by transposing the above equation and substituting in the measured SINAD: N = (SINAD - 1.76)/6.02. Figure 12 shows the effective number of bits as a function of the input frequency for the MAX187/MAX189.

Total Harmonic Distortion

If a pure sine wave is sampled by an ADC at greater than the Nyquist frequency, the nonlinearities in the ADC's transfer function create harmonics of the input frequency present in the sampled output data.

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all the harmonics (in the frequency band above DC and below one-half the sample rate, but not including the DC component) to the RMS amplitude of the fundamental frequency. This is expressed as follows:

$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_N^2}}{V_1}$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics. The THD specification in the *Electrical Characteristics* includes the 2nd through 5th harmonics.

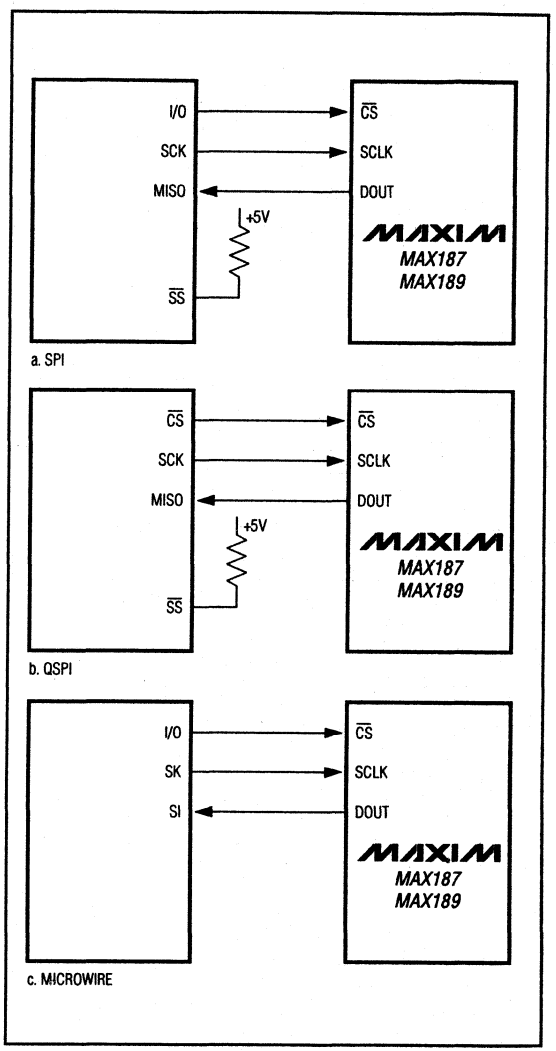


Figure 13. Common Serial-Interface Connections to the MAX187/MAX189

Applications Information

Connection to Standard Interfaces

The MAX187/MAX189 serial interface is fully compatible with SPI, QSPI, and Microwire standard serial interfaces.

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.5MHz.

1. Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2. Wait the for the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3. Activate SCLK for a minimum of 13 clock cycles. The first falling clock edge will produce the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4. Pull $\overline{CS}$ high at or after the 13th falling clock edge. If $\overline{CS}$ remains low, trailing zeros are clocked out after the LSB.
5. With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, before launching a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversions end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in 1-byte chunks or continuously, as shown in Figure 8. The bytes will contain the result of the conversion padded with one leading 1, and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

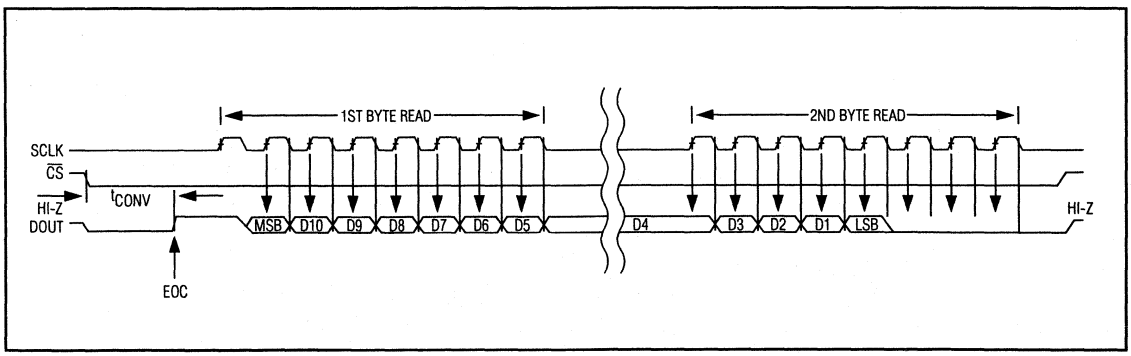


Figure 14. SPI/Microwire Serial Interface Timing (CPOL = CPHA = 0)

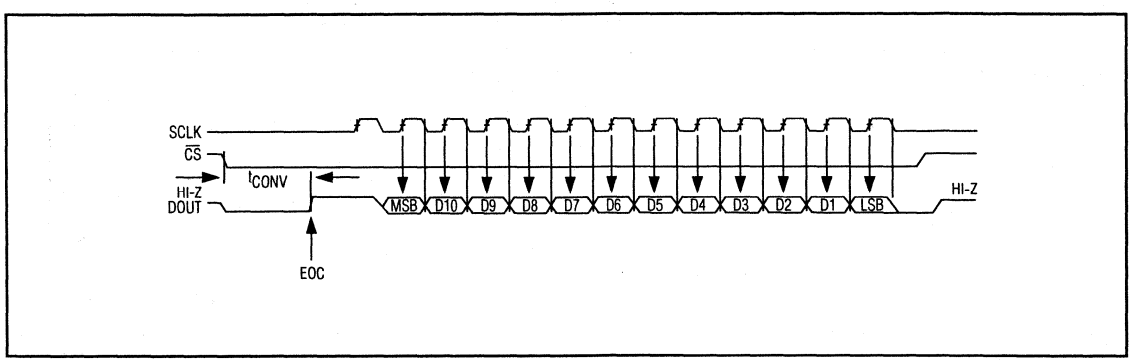


Figure 15. QSPI Serial Interface Timing (CPOL = CPHA = 0)

+5V, Low-Power, 12-Bit Serial ADCs

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion in progress. Wait until DOUT goes high or the maximum specified 8.5µs conversion time. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1 and 7 bits of conversion result. The second byte contains the remaining 5 bits and 3 trailing 0s. See Figure 13 for connections and Figure 14 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX187/MAX189 require 13 clock cycles from the µP to clock out the 12 bits of data with no trailing 0s (Figure 15). The maximum clock frequency to ensure compatibility with QSPI is 2.77MHz.

Opto-Isolated Interface, Serial-to-Parallel Conversion

Many industrial applications require electrical isolation to separate the control electronics from hazardous electrical conditions, provide noise immunity, or prevent excessive current flow where ground disparities exist between the ADC and the rest of the system. Isolation amplifiers typically used to accomplish these tasks are expensive. In cases where the signal is eventually converted to a digital form, it is cost effective to isolate the input using opto-couplers in a serial link.

The MAX187 is ideal in this application because it includes both T/H amplifier and voltage reference, operates from a single supply, and consumes very little power (Figure 16).

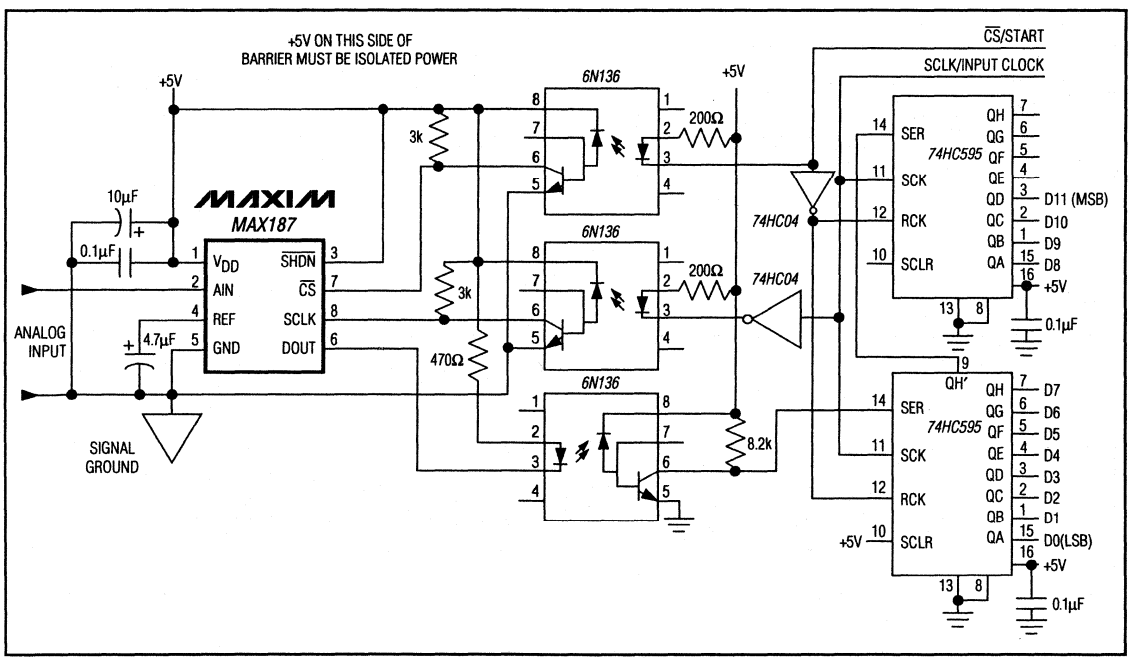


Figure 16. 12-Bit Isolated ADC

The ADC results are transmitted across a 1500V isolation barrier provided by three 6N136 opto-isolators. Isolated power must be supplied to the converter and the isolated side of the opto-couplers. 74HC595 three-state shift registers are used to construct a 12-bit parallel data output. The timing sequence is identical to the timing shown in Figure 8. Conversion speed is limited by the delay through the opto-isolators. With a 140kHz clock, conversion time is 100µs.

The universal 12-bit parallel data output can also be used without the isolation stage when a parallel interface is required. Clock frequencies up to 2.9MHz are possible without violating the 20ns shift-register setup time. Delay or invert the clock signal to the shift registers beyond 2.9MHz.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at GND, separate from the logic ground. All other analog grounds should be connected to this ground. The 16-pin versions also have a dedicated DGND pin available. Connect DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass this supply to the single-point analog ground with 0.01µF and 4.7µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise (Figure 17).

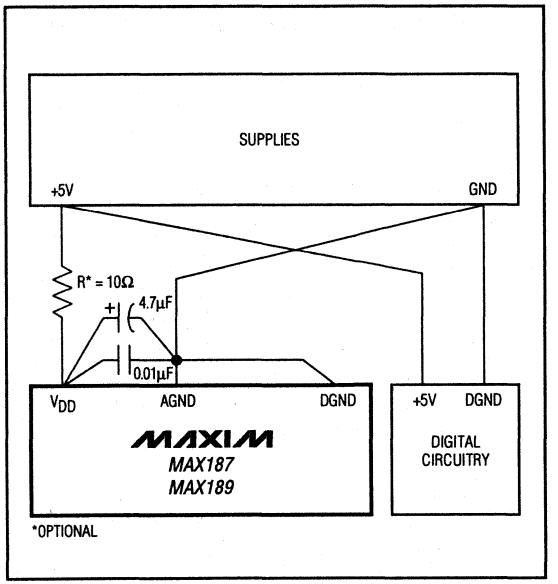


Figure 17. Power-Supply Grounding Condition

+5V, Low-Power, 12-Bit Serial ADCs

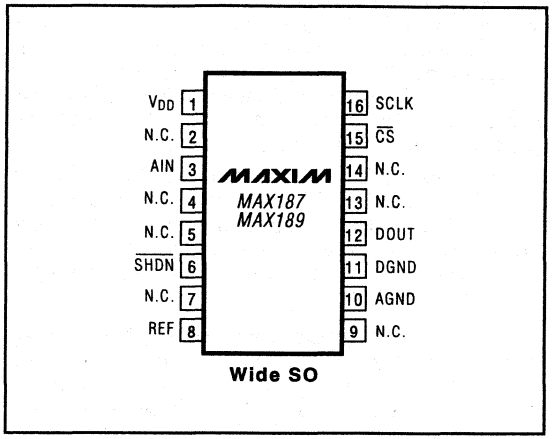
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX187AEPA	-40°C to +85°C	8 Plastic DIP	±½
MAX187BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX187CEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX187AEWE	-40°C to +85°C	16 Wide SO	±½
MAX187BEWE	-40°C to +85°C	16 Wide SO	±1
MAX187CEWE	-40°C to +85°C	16 Wide SO	±2
MAX187AMJA	-55°C to +125°C	8 CERDIP**	±½
MAX187BMJA	-55°C to +125°C	8 CERDIP**	±1
MAX189ACPA	0°C to +70°C	8 Plastic DIP	±½
MAX189BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX189CCPA	0°C to +70°C	8 Plastic DIP	±2
MAX189ACWE	0°C to +70°C	16 Wide SO	±½
MAX189BCWE	0°C to +70°C	16 Wide SO	±1
MAX189CCWE	0°C to +70°C	16 Wide SO	±2
MAX189BC/D	0°C to +70°C	Dice*	±1
MAX189AEPA	-40°C to +85°C	8 Plastic DIP	±½
MAX189BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX189CEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX189AEWE	-40°C to +85°C	16 Wide SO	±½
MAX189BEWE	-40°C to +85°C	16 Wide SO	±1
MAX189CEWE	-40°C to +85°C	16 Wide SO	±2
MAX189AMJA	-55°C to +125°C	8 CERDIP**	±½
MAX189BMJA	-55°C to +125°C	8 CERDIP**	±1

** Dice are specified at T_A = +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



19-0247; Rev. 0; 3/94

MAXIM

Low-Power, 8-Channel, Serial 10-Bit ADC

General Description

The MAX192 is a low-cost, 10-bit data-acquisition system that combines an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and ultra-low power consumption. The device operates with a single +5V supply. The analog inputs are software configurable for single-ended and differential (unipolar/bipolar) operation.

The 4-wire serial interface connects directly to SPI™, QSPI™, and Microwire™ devices, without using external logic. A serial strobe output allows direct connection to TMS320 family digital signal processors. The MAX192 uses either the internal clock or an external serial-interface clock to perform successive approximation A/D conversions. The serial interface can operate beyond 4MHz when the internal clock is used. The MAX192 has an internal 4.096V reference with a drift of ±30ppm typical. A reference-buffer amplifier simplifies gain trim and two sub-LSBs reduce quantization errors.

The MAX192 provides a hardwired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the device, and the quick turn-on time allows the MAX192 to be shut down between conversions. By powering down between conversions, supply current can be cut to under 10µA at reduced sampling rates.

The MAX192 is available in 20-pin DIP and SO packages, and in a shrink-small-outline package (SSOP) that occupies 30% less area than an 8-pin DIP. The data format provides hardware and software compatibility with the MAX186/MAX188. For anti-aliasing filters, consult the data sheets for the MAX291–MAX297.

Applications

Automotive
Pen-Entry Systems
Consumer Electronics
Portable Data Logging
Robotics
Battery-Powered Instruments, Battery Management
Medical Instruments

See last page for Typical Operating Circuit.

™ SPI and QSPI are trademarks of Motorola Corp.
Microwire is a trademark of National Semiconductor Corp.

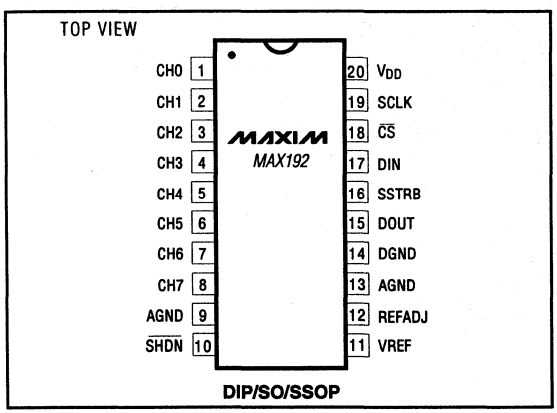
Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single +5V Operation**
- **Low Power: 1.5mA (operating)**
  2µA (power-down)
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 4.096V Reference**
- **4-Wire Serial Interface is Compatible with SPI, QSPI, Microwire, and TMS320**
- **20-Pin DIP, SO, SSOP Packages**
- **Pin-Compatible 12-Bit Upgrade (MAX186/MAX188)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL(LSBs)
MAX192ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX192BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX192ACWP	0°C to +70°C	20 Wide SO	±1/2
MAX192BCWP	0°C to +70°C	20 Wide SO	±1
MAX192ACAP	0°C to +70°C	20 SSOP	±1/2
MAX192BCAP	0°C to +70°C	20 SSOP	±1
MAX192AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX192BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX192AEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX192BEWP	-40°C to +85°C	20 Wide SO	±1
MAX192AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX192BEAP	-40°C to +85°C	20 SSOP	±1
MAX192AMJP	-55°C to +125°C	20 CERDIP	±1/2
MAX192BMJP	-55°C to +125°C	20 CERDIP	±1

Pin Configuration



Low-Power, 8-Channel, Serial 10-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH7 to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
REFADJ to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX192_C_P ..... 0°C to +70°C
MAX192_E_P ..... -40°C to +85°C
MAX192_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), 4.7µF capacitor at VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)		MAX192A			±1/2	LSB
		MAX192B			±1	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error					±2	LSB
Gain Error		External reference, 4.096V			±2	LSB
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 4.096V_{p-p}, 133ksps, 2.0MHz external clock)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		65kHz, V_{IN} = 4.096V_{p-p} (Note 3)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		4.5		MHz
Full-Power Bandwidth				800		kHz
CONVERSION RATE						
Conversion Time (Note 4)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{AZ}				1.5	µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), 4.7µF capacitor at VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
External Clock Frequency		External compensation, 4.7µF		0.1		2.0	MHz
		Internal compensation (Note 5)		0.1		0.4	
		Used for data transfer only			10		
ANALOG INPUT							
Analog Input Voltage		Common-mode range (any input) (Note 6)		0		V_{DD}	V
		Single-ended range (unipolar only)		0		V_{REF}	
		Differential range	Unipolar	0		V_{REF}	
			Bipolar	$\frac{-V_{REF}}{2}$		$\frac{+V_{REF}}{2}$	
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0V, 5V			±0.01	±1	µA
Input Capacitance		(Note 5)			16		pF
INTERNAL REFERENCE (reference buffer enabled)							
VREF Output Voltage		T_A = +25°C		4.076	4.096	4.116	V
VREF Short-Circuit Current						30	mA
VREF Tempco					±30		ppm/°C
Load Regulation (Note 7)		0mA to 0.5mA output load			2.5		mV
Capacitive Bypass at VREF		Internal compensation		0			µF
		External compensation		4.7			
Capacitive Bypass at REFADJ		Internal compensation		0.01			µF
		External compensation		0.01			
REFADJ Adjustment Range					±1.5		%
EXTERNAL REFERENCE AT VREF (buffer disabled, VREF = 4.096V)							
Input Voltage Range				2.5		V_{DD} + 50mV	V
Input Current					200	350	µA
Input Resistance				12	20		kΩ
Shutdown VREF Input Current					1.5	10	µA
Buffer Disable Threshold REFADJ				V_{DD} - 50mV			V
EXTERNAL REFERENCE AT REFADJ							
Capacitive Bypass at VREF		Internal compensation mode		0			µF
		External compensation mode		4.7			
Reference-Buffer Gain					1.678		V/V
REFADJ Input Current						±50	µA

Low-Power, 8-Channel, Serial 10-Bit ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%, f_{CLK} = 2.0MHz, external clock (50% duty cycle), 15 clocks/conversion cycle (133ksps), 4.7µF capacitor at VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{INH}		2.4			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{INL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 5)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{INH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Low Voltage	V_{INL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{INH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{INL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Input Mid Voltage	V_{IM}		1.5		V_{DD} - 1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Leakage Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 5)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down		30	70	µA
		Full power-down		2	10	
Positive Supply Rejection (Note 8)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV

Note 1: Tested at V_{DD} = 5.0V; single-ended, unipolar.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: Grounded on-channel; sine wave applied to all off channels.
Note 4: Conversion time defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 5: Guaranteed by design. Not subject to production testing.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.

TIMING CHARACTERISTICS

(V_{DD} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

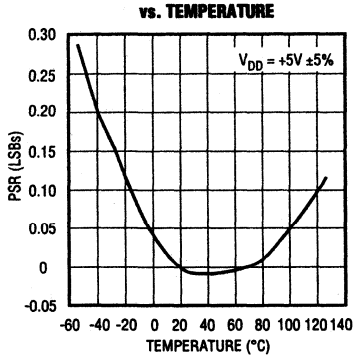
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{AZ}		1.5			µs
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	20		150	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF			200	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 5)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF			200	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 5)	t_{STR}	External clock mode only, C_{LOAD} = 100pF			200	ns
SSTRB Rise to SCLK Rise (Note 5)	t_{SCK}	Internal clock mode only	0			ns

Note 5: Guaranteed by design. Not subject to production testing.

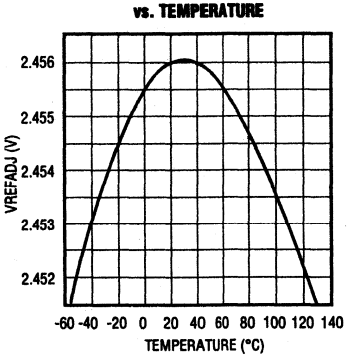
Typical Operating Characteristics

7

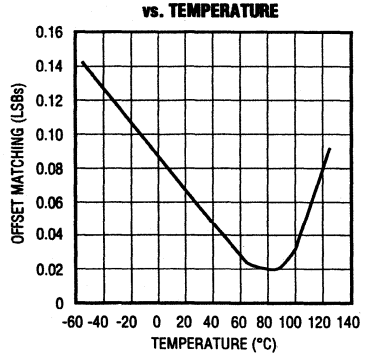
POWER-SUPPLY REJECTION vs. TEMPERATURE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



Low-Power, 8-Channel, Serial 10-Bit ADC

Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9, 13	AGND	Analog Ground. Also IN- Input for single-enabled conversions. Connect both AGND pins to analog ground.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling SHDN low shuts the MAX192 down to 10µA (max) supply current, otherwise the MAX192 is fully operational. Pulling SHDN high puts the reference-buffer amplifier in internal compensation mode. Letting SHDN float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference Voltage for analog-to-digital conversion. Also, Output of the Reference Buffer Amplifier. Add a 4.7µF capacitor to ground when using external compensation mode. Also functions as an input when used with a precision external reference.
12	REFADJ	Reference-Buffer Amplifier Input. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX192 begins the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. SSTRB is high impedance when $\overline{CS}$ is high (external mode).
17	DIN	Serial Data Input. Data is clocked in at the rising edge of SCLK.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 45% to 55%.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

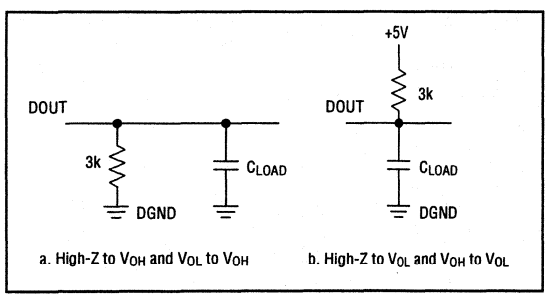


Figure 1. Load Circuits for Enable Time

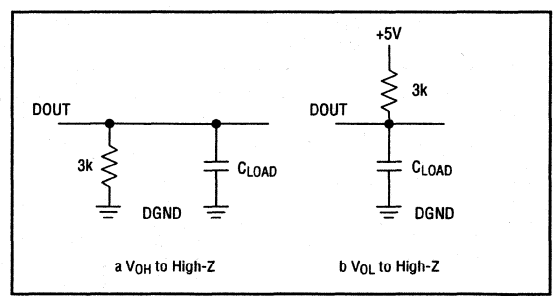


Figure 2. Load Circuits for Disabled Time

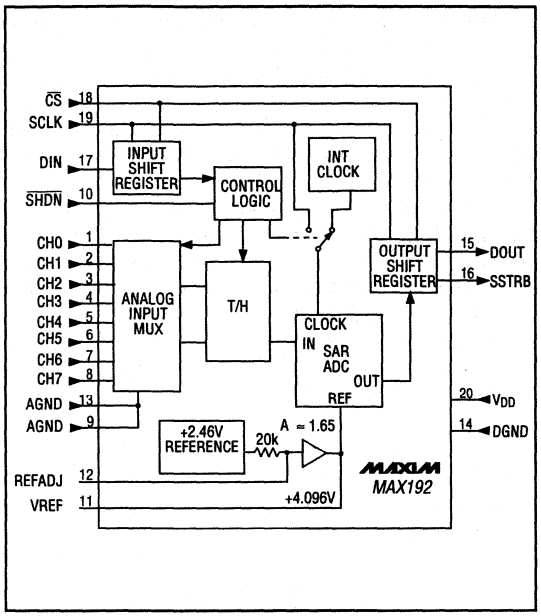


Figure 3. Block Diagram

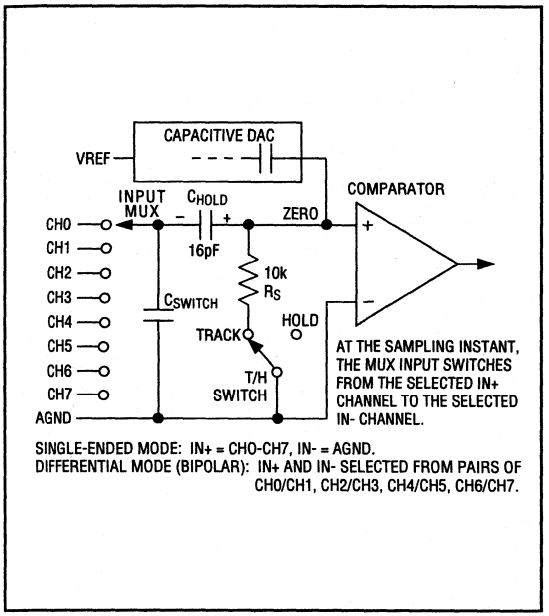


Figure 4. Equivalent Input Circuit

Detailed Description

The MAX192 uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors. No external hold capacitors are required. Figure 3 shows the block diagram for the MAX192.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7 and IN- is switched to AGND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5 and CH6/CH7. Refer to Tables 1 and 2 to configure the channels.

In differential mode, IN- and IN+ are internally switched to either one of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. Accomplish this by connecting a 0.1µF capacitor from AIN- (the selected analog input, respectively) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply AGND. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore its node ZERO to 0V within the limits of its resolution. This action is equivalent to transferring a charge of 16pF x (V_{IN+} - V_{IN-}) from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

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Low-Power, 8-Channel, Serial 10-Bit ADC

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. The T/H enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to AGND, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{AZ} = 9 (R_S + R_{IN}) 16pF$$

where $R_{IN} = 5k\Omega$, R_S = the source impedance of the input signal, and t_{AZ} is never less than 1.5µs. Note that source impedances below 5kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended. See the data sheets for the MAX291–MAX297 filters.

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than AGND by 50mV.

If an off-channel analog input exceeds the supplies by more than 50mV, current will flow through the protection diodes on that input. If this current exceeds 2mA, the accuracy of the on-channel's conversion will be degraded.

The MAX192 can be configured for differential (unipolar or bipolar) or single-ended (unipolar only) inputs, as selected by bits 2 and 3 of the control byte (Table 3).

In the single-ended mode, set the UNI/BIP bit to unipolar. In this mode, analog inputs are internally referenced to AGND, with a full-scale input range from 0V to V_{REF}.

In differential mode, both unipolar and bipolar settings can be used. Choosing unipolar mode sets the differential input range at 0V to V_{REF}. The output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to $\pm V_{REF} / 2$. Note that in this differential mode, the common-mode input range includes both supply rails. Refer to Tables 4a and 4b for input voltage ranges.

Quick Look

To evaluate the analog performance of the MAX192 quickly, use Figure 5's circuit. The MAX192 requires a control byte to be written to DIN before each

Table 1. Channel Selection in Single-Ended Mode (SGL/$\overline{DIFF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	AGND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 2. Channel Selection in Differential Mode (SGL/$\overline{DIFF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	−						
0	0	1			+	−				
0	1	0					+	−		
0	1	1							+	−
1	0	0	−	+						
1	0	1			−	+				
1	1	0					−	+		
1	1	1							−	+

Table 3. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7(MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion. See Tables 1 and 2.
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in differential bipolar mode, the differential signal can range from -VREF / 2 to +VREF / 2. Select differential operation if bipolar mode is used.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to AGND. In differential mode, the voltage difference between two channels is measured. Select unipolar operation if single-ended mode is used. See Tables 1 and 2.
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_Q = 2µA) **0** **1** Fast power-down (I_Q = 30µA) **1** **0** Internal clock mode **1** **1** External clock mode

Low-Power, 8-Channel, Serial 10-Bit ADC

Table 4a. Unipolar Full Scale and Zero Scale

REFERENCE		ZERO SCALE	FULL SCALE
Internal Reference		0V	+4.096V
External Reference	at REFADJ	0V	V_{REFADJ} (1.678)
	at VREF	0V	V_{REF}

Table 4b. Differential Bipolar Full Scale, Zero Scale, and Negative Full Scale

REFERENCE		NEGATIVE FULL SCALE	ZERO SCALE	FULL SCALE
Internal Reference		-4.096V / 2	0V	+4.096V / 2
External Reference	at REFADJ	-1/2V_{REFADJ} (1.678)	0V	+1/2V_{REFADJ} (1.678)
	at VREF	-1/2 V_{REF}	0V	+1/2 V_{REF}

conversion. Tying DIN to +5V feeds in control bytes of $FF (HEX), which trigger single-ended conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result comes out of DOUT. Varying the analog input to CH7 should alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

How to Start a Conversion

A conversion is started on the MAX192 by clocking a control byte into DIN. Each rising edge on SCLK, with $\overline{CS}$ low, clocks a bit from DIN into the MAX192's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the MSB of the control byte. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 3 shows the control-byte format.

The MAX192 is compatible with Microwire, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

Example: Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode, call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion-mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX192 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 HEX) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX192 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 will contain the result of the conversion padded with one leading zero, two sub-LSB bits, and three trailing zeros. The total conversion time is a function of the serial clock frequency and the amount of dead time between 8-bit transfers. Make sure that the total conversion time does not exceed 120µs, to avoid excessive T/H droop.

Digital Output

In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs in differential mode, the output is twos-complement (Figure 16). Data is clocked out at the falling edge of SCLK in MSB-first format.

Internal and External Clock Modes

The MAX192 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX192. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7 through 10 show the timing characteristics common to both modes.

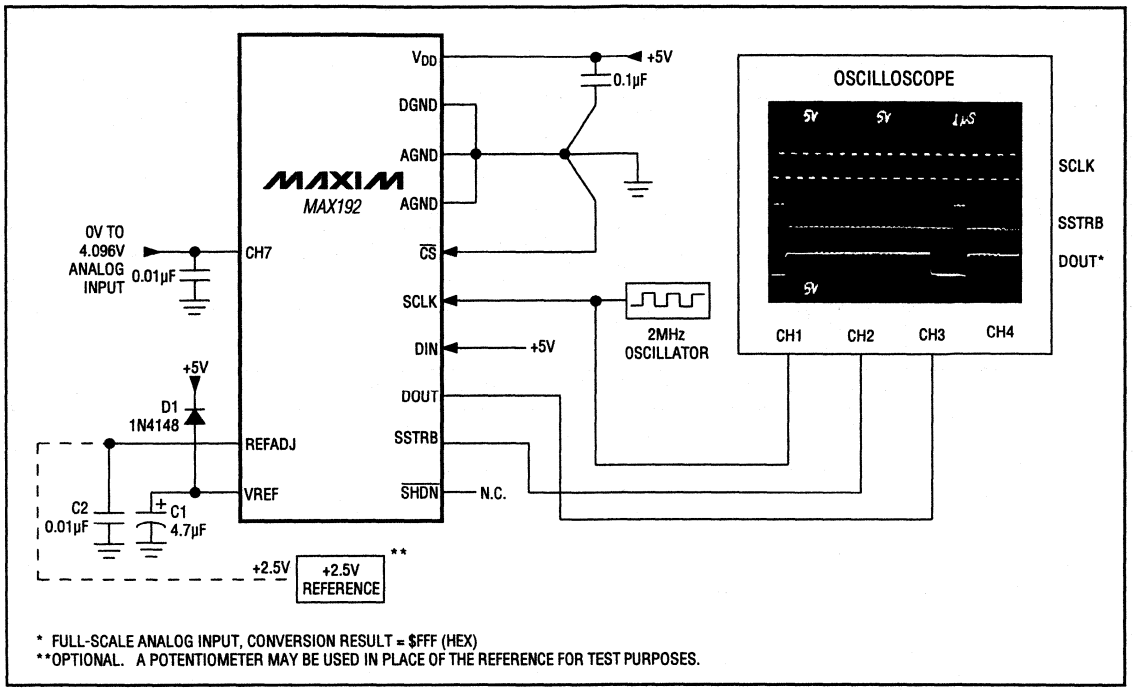

Figure 5. Quick-Look Circuit

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (see Figure 6). The first 10 bits are the true data bits, and the last two are sub-LSB bits.

SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or else droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the clock period exceeds 10µs, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX192 generates its own conversion clock internally. This frees the microprocessor from the burden of running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to typically 10MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB will be low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data when the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge will produce the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started.

Pulling $\overline{CS}$ high prevents data from being clocked into

Low-Power, 8-Channel, Serial 10-Bit ADC

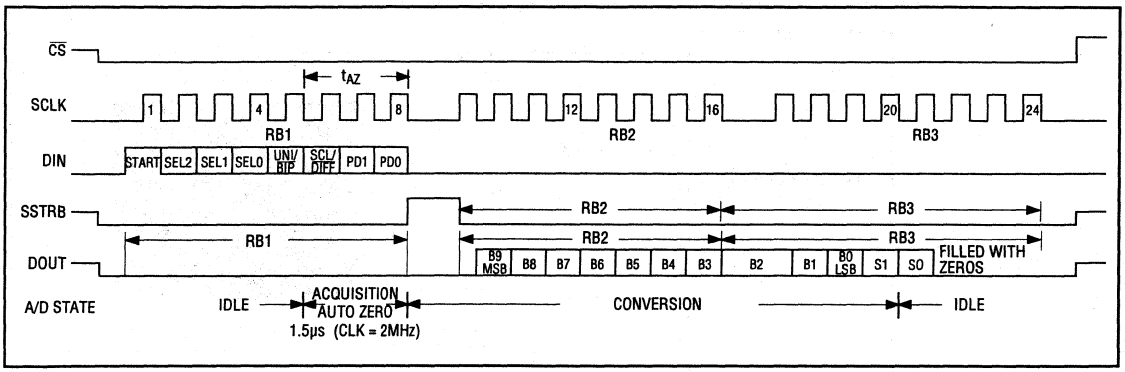

Figure 6. 24-Bit External Clock Mode Conversion Timing (SPI, QSPI and Microwire Compatible)

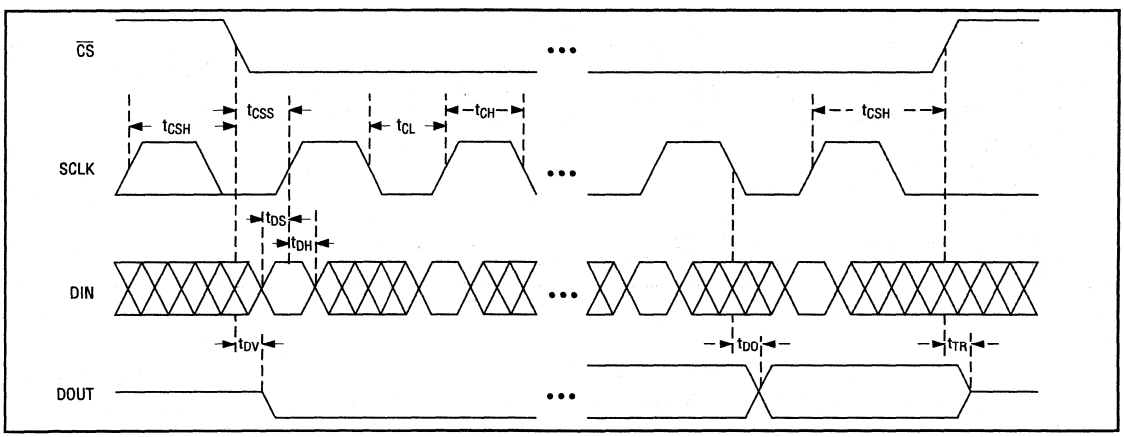

Figure 7. Detailed Serial-Interface Timing

the MAX192 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In internal clock mode, data can be shifted in and out of the MAX192 at clock rates exceeding 4.0MHz, provided that the minimum acquisition time, t_{AZ}, is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion on the MAX192. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle, e.g. after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If a falling edge on $\overline{CS}$ forces a start bit before bit 3 (B3) becomes available, then the current conversion will be terminated and a new one started. Thus, the fastest the MAX192 can run is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode.

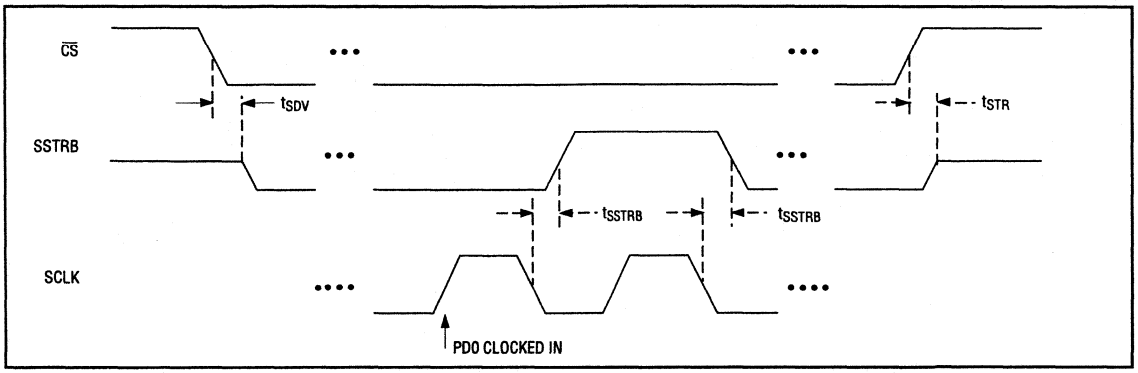

Figure 8. External Clock Mode SSTRB Detailed Timing

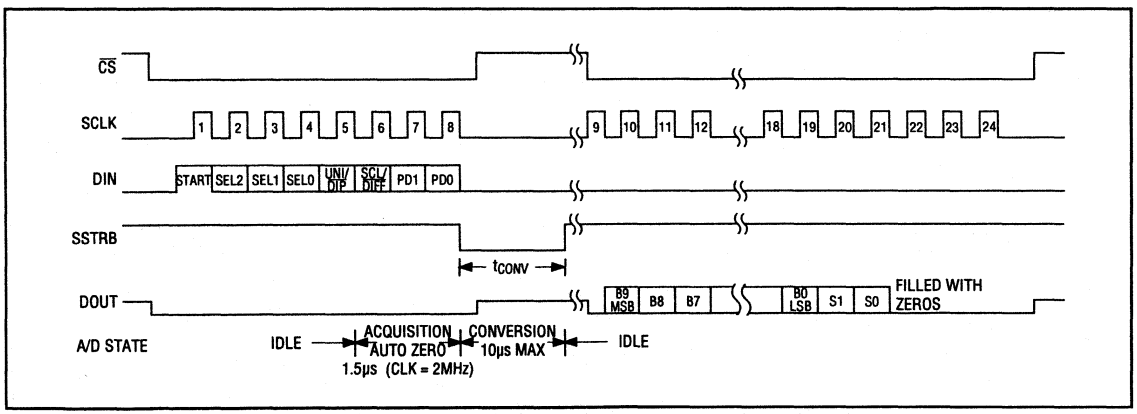

Figure 9. Internal Clock Mode Timing

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion will typically be the fastest that a microcontroller can drive the MAX192. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry will activate the MAX192 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have been stabilized, the internal reset time is 100µs and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN will be interpreted as a start bit. Until a conversion takes place, DOUT will shift out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, the $\overline{SHDN}$ pin also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

To select external compensation, float $\overline{SHDN}$. See the *Typical Operating Circuit*, which uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures stability and allows operation of the converter at the full clock speed of 2MHz. External compensation increases power-up time (see the *Choosing Power-Down Mode* section, and Table 5).

Internal compensation requires no external capacitor at VREF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for shortest power-up times, but is

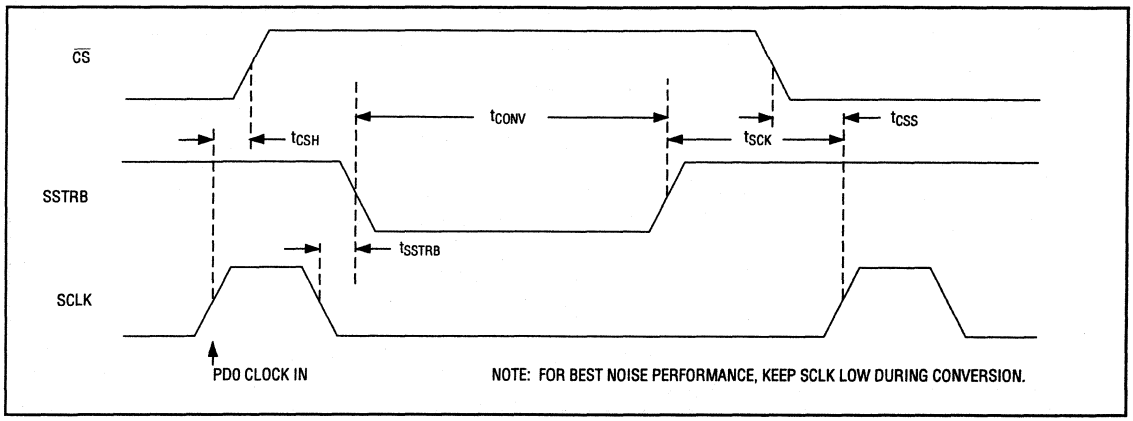

Figure 10. Internal Clock Mode SSTRB Detailed Timing

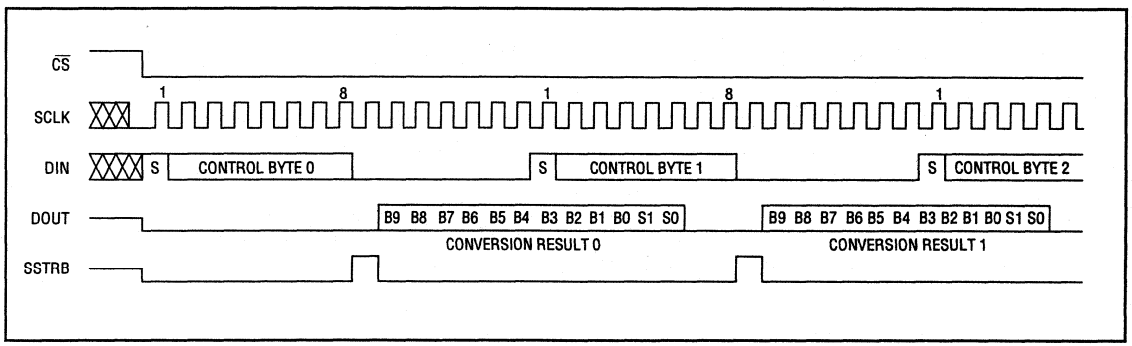

Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

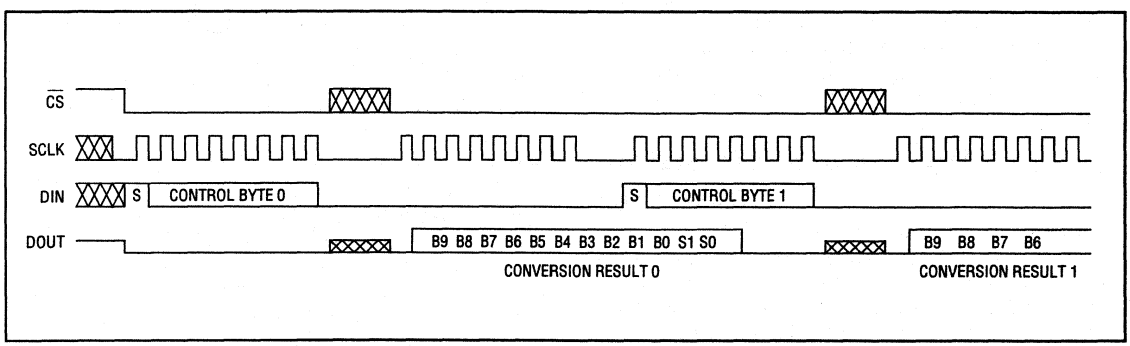

Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

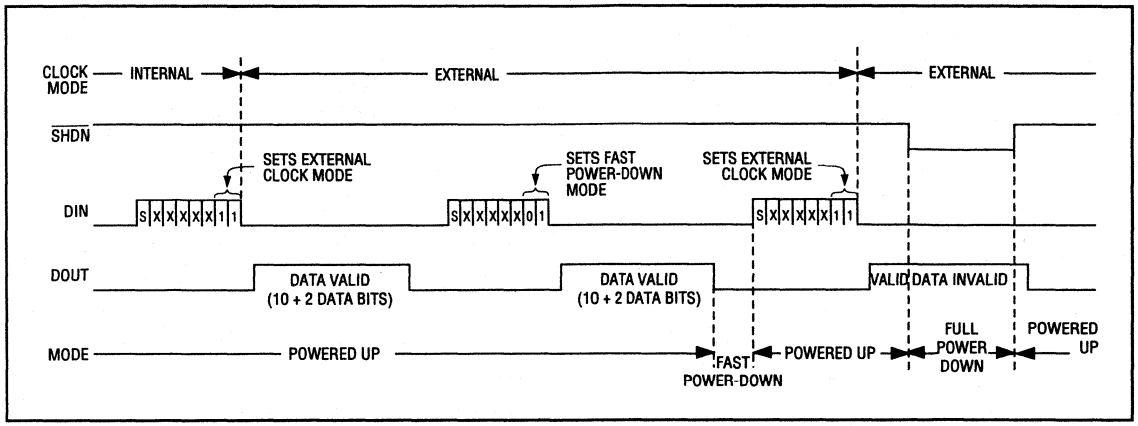

Figure 12a. Timing Diagram Power-Down Modes, External Clock

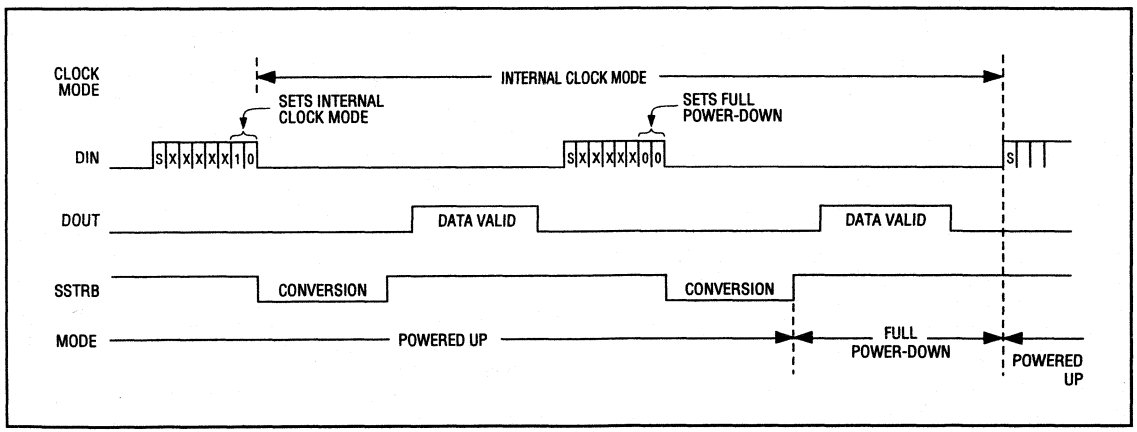

Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

only available using an external clock and reduces the maximum clock rate to 400kHz.

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 7 and 8 of the DIN control byte with $\overline{SHDN}$ high (see Tables 3 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 7 and 8 of DIN word (see Table 7).

Full power-down mode turns off all chip functions that draw quiescent current, typically reducing I_{DD} to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With the fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

In both software shutdown modes, the serial interface remains operational, however, the ADC will not convert. Table 5 illustrates how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

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Table 5. Worst-Case Power-Up Delay Times

Reference Buffer	Reference-Buffer Compensation Mode	VREF Capacitor (µF)	Power-Down Mode	Power-Up Delay (sec)	Maximum Sampling Rate (ksps)
Enabled	Internal		Fast	5µ	26
Enabled	Internal		Full	300µ	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled			Fast	2µ	133
Disabled			Full	2µ	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	Device Mode
1	1	External Clock Mode
1	0	Internal Clock Mode
0	1	Fast Power-Down Mode
0	0	Full Power-Down Mode

In external compensation mode, the power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is fully discharged. In fast power-down, you can eliminate start-up time by using low-leakage capacitors that will not discharge more than 1/2LSB while shut down. In shutdown, the capacitor has to supply the current into the reference (1.5µA typ) and the transient currents at power-up.

Figures 12a and 12b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC will continue to operate in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out while the MAX192 has already entered a software power-down.

The first logical 1 on DIN will be interpreted as a start bit, and powers up the MAX192. Following the start bit, the data input word or control byte also determines clock and power-down modes. For example, if the DIN word contains PD1 = 1, then the chip will remain powered up. If PD1 = 0, a power-down will resume after one conversion.

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ State	Device Mode	Reference-Buffer Compensation
1	Enabled	Internal Compensation
Floating	Enabled	External Compensation
0	Full Power-Down	N/A

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into the full power-down mode. Unlike with the software shutdown modes, conversion is not completed. It stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference is used and is not shut down. The $\overline{SHDN}$ pin also selects internal or external reference compensation (see Table 7).

Power-Down Sequencing

The MAX192 auto power-down modes can save considerable power when operating at less than maximum sample rates. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

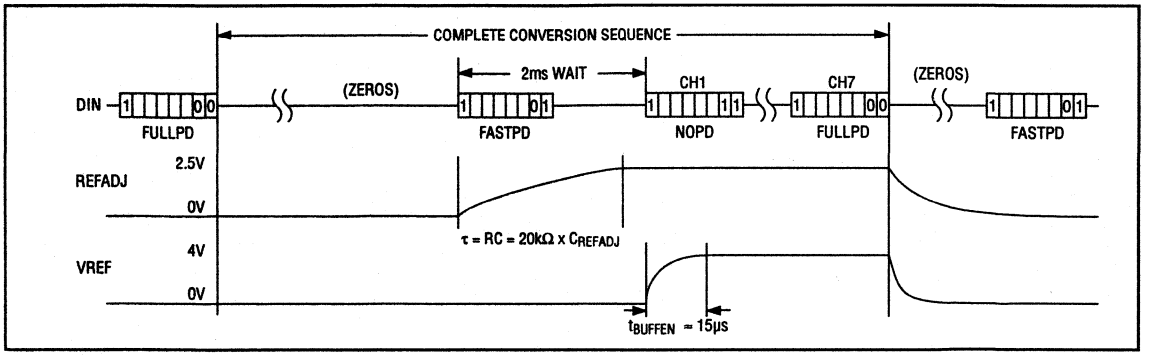

Figure 13. FULLPD/FASTPD Power-Up Sequence

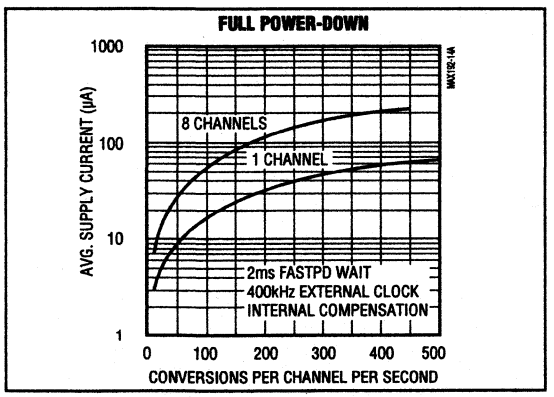

Figure 14a. Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

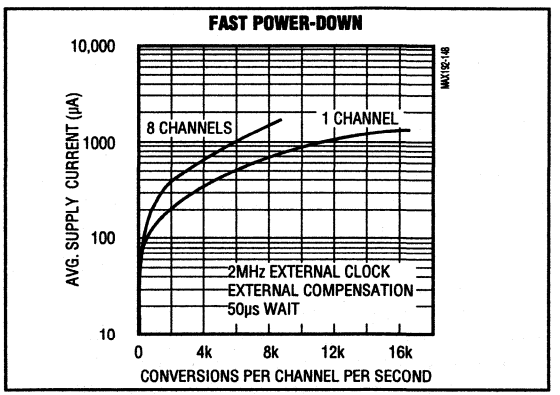

Figure 14b. Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

Figure 14a depicts the MAX192 power consumption for one or eight channel conversions utilizing full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 10-bit accuracy, 10 time constants or 2ms are required after power-up. Waiting 2ms in FASTPD mode instead of full power-up will reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 13.

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up, accomplished by 75 idle clocks after a

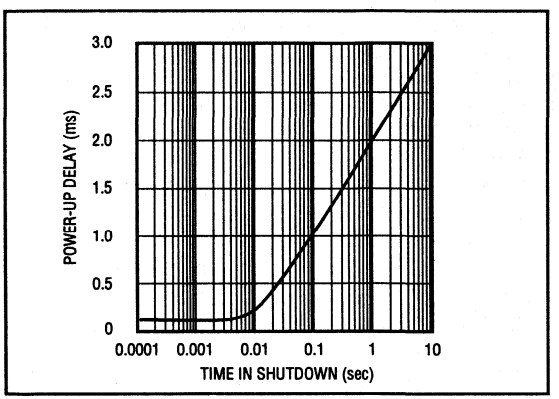

Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

Low-Power, 8-Channel, Serial 10-Bit ADC

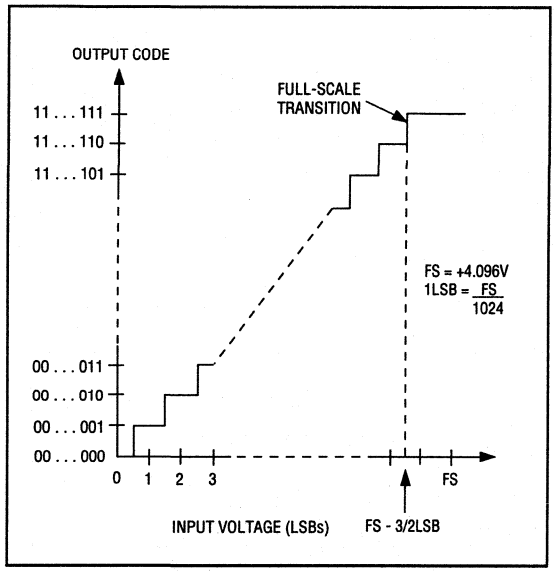

Figure 15. Unipolar Transfer Function, 4.096V = Full Scale

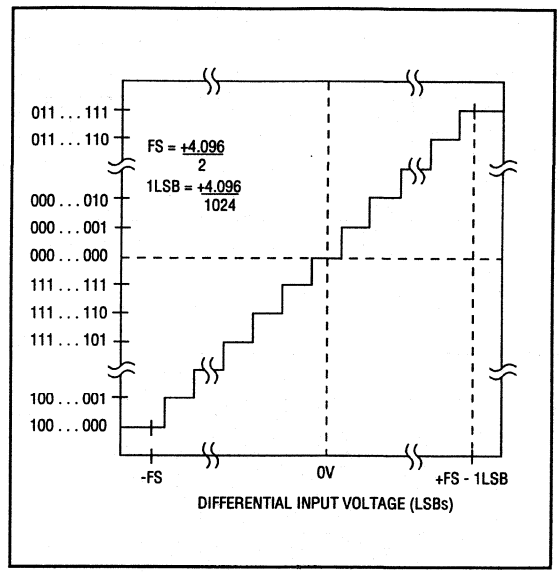

Figure 16. Differential Bipolar Transfer Function, ±4.096V / 2 = Full Scale

dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX192 is inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX192 can be used with an internal or external reference. Diode D1 shown in the *Typical Operating Circuit* ensures correct start-up. Any standard signal diode can be used. An external reference can either be connected directly at the VREF terminal or at the REFADJ pin.

The MAX192's internally trimmed 2.46V reference is buffered with a gain of 1.678 to scale an external 2.5V reference at REFADJ to 4.096V at VREF.

Internal Reference

The full-scale range of the MAX192 with internal reference is 4.096V with unipolar inputs, and ±2.048V with differential bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the Reference-Adjust Circuit of Figure 17.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal buffer amplifier. The REFADJ input impedance is typically 20kΩ. At VREF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at VREF must be able to deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the buffered REFADJ input avoids external buffering of the reference. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the differential bipolar input/output transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1LSB = 4.00mV (4.096V / 1024) for unipolar operation and 1LSB = 4.00mV [(4.096V / 2 - -4.096V / 2)/1024] for bipolar operation.

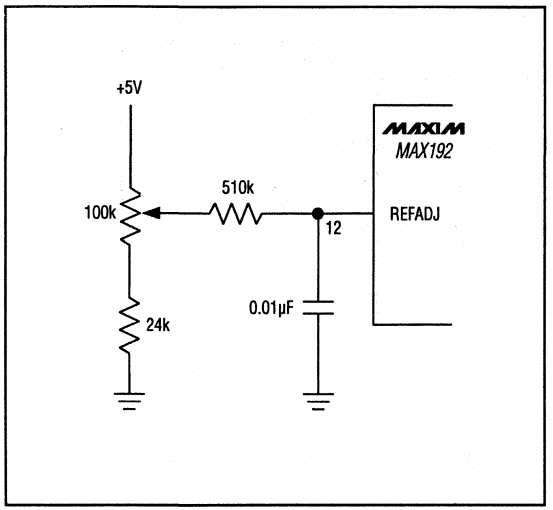

Figure 17. Reference-Adjust Circuit

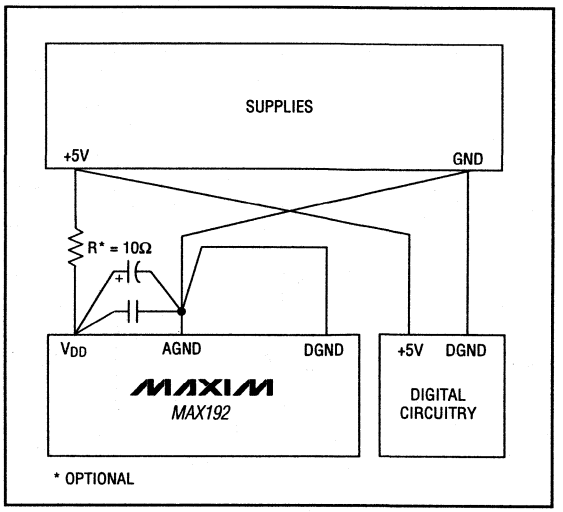

Figure 18. Power-Supply Grounding Connection

Figure 17, the Reference-Adjust Circuit, shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±15LSBs) of gain adjustment range.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX192. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter, as shown in Figure 18.

High-Speed Digital Interfacing

The MAX192 can interface with QSPI at high throughput rates using the circuit in Figure 19. This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU since QSPI incorporates its own micro-sequencer.

Figure 20 details the code that sets up QSPI for autonomous operation. In external clock mode, the MAX192 performs a single-ended, unipolar conversion on each of the eight analog input channels. Figure 21 shows the timing associated with the assembly code of Figure 20. The first byte clocked into the MAX192 is the control byte, which triggers the first conversion on CH0. The last two bytes clocked into the MAX192 are all zero, and clock out the results of the CH7 conversion.

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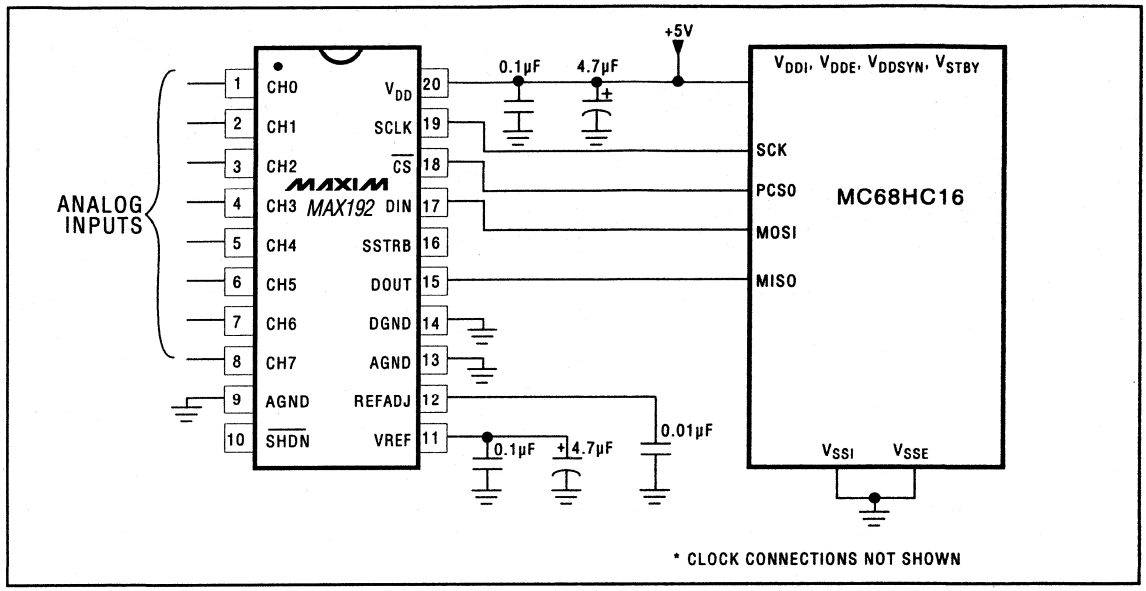


Figure 19. MAX192 QSPI Connection

TMS320 to MAX192 Interface

Figure 22 shows an application circuit to interface the MAX192 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 23.

Use the following steps to initiate a conversion in the MAX192 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR of the TMS320 are tied together with the SCLK input of the MAX192.
2) The MAX192 $\overline{CS}$ is driven low by the XF_ I/O port of the TMS320 to enable data to be clocked into DIN of the MAX192.
3) An 8-bit word (1XXXXX11) should be written to the MAX192 to initiate a conversion and place the device into external clock mode. Refer to Table 3 to select the proper XXXXX bit values for your specific application.
4) The SSTRB output of the MAX192 is monitored via the FSR input of the TMS320. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX192.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10-bit conversion result and two sub-LSBs, followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX192 until the next conversion is initiated.

```
* Description :
*           This is a shell program for using a stand-alone 68HC16 without any external memory. The internal 1K RAM
*           is put into bank $0F to maintain 68HC11 code compatibility. This program was written with software
*           provided in the Motorola 68HC16 Evaluation Kit.
*
* Roger J.A. Chen, Applications Engineer
* MAXIM Integrated Products
* November 20, 1992
*
*****************************************************************************************************************************************************

    INCLUDE     'EQUATES.ASM'   ;Equates for common reg addrs
    INCLUDE     'ORG00000.ASM'  ;initialize reset vector
    INCLUDE     'ORG00008.ASM'  ;initialize interrupt vectors
    ORG   $0200                 ;start program after interrupt vectors
    INCLUDE 'INITSYS.ASM'       ;set EK=F,XK=0,YK=0,ZK=0
                                ;set sys clock at 16.78 MHz, COP off
    INCLUDE 'INITRAM.ASM'       ;turn on internal SRAM at $10000
                                ;set stack (SK=1, SP=03FE)
MAIN:
    JSR   INITQSPI
MAINLOOP:
    JSR   READ192
WAIT:
    LDAA  SPSR
    ANDA  #$80
    BEQ   WAIT                  ;wait for QSPI to finish
    BRA MAINLOOP
ENDPROGRAM:

INITQSPI:

;This routine sets up the QSPI microsequencer to operate on its own.
;The sequencer will read all eight channels of a MAX192 each time
;it is triggered. The A/D converter results will be left in the
;receive data RAM. Each 16 bit receive data RAM location will
;have a leading zero, 10 + 2 bits of conversion result and three zeros.
;
;Receive RAM Bits 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
;A/D Result        0  MSB                                  LSB 0  0  0
***** Initialize the QSPI Registers  ******
    PSHA
    PSHB
    LDAA  #%01111000
    STAA  QPDR              ;idle state for PCS0-3 = high
    LDAA  #%01111011
    STAA  QPAR              ;assign port D to be QSPI
    LDAA  #%01111110
    STAA  QDDR              ;only MISO is an input
    LDD   #$8008
    STD   SPCR0             ;master mode,16 bits/transfer,
                            ;CPOL=CPHA=0,1MHz Ser Clock
    LDD   #$0000
    STD   SPCR1             ;set delay between PCS0 and SCK,
                            ;set delay between transfers
```

Figure 20. MAX192 Assembly-Code Listing

Low-Power, 8-Channel, Serial 10-Bit ADC

```
    LDD   #$0800
    STD   SPCR2          ;set ENDQP to $8 for 9 transfers
***** Initialize QSPI Command RAM *****

    LDAA  #$80       ;CONT=1,BITSE=0,DT=0,DSCK=0,PCS0=ACTIVE
    STAA  $FD40       ;store first byte in COMMAND RAM
    LDAA  #$C0       ;CONT=1,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
    STAA  $FD41
    STAA  $FD42
    STAA  $FD43
    STAA  $FD44
    STAA  $FD45
    STAA  $FD46
    STAA  $FD47
    LDAA  #$40       ;CONT=0,BITSE=1,DT=0,DSCK=0,PCS0=ACTIVE
    STAA  $FD48
***** Initialize QSPI Transmit RAM *****

    LDD   #$008F
                              STD   $FD20
    LDD   #$00CF
                              STD   $FD22
    LDD   #$009F
                              STD   $FD24
    LDD   #$00DF
                              STD   $FD26
    LDD   #$00AF
                              STD   $FD28
    LDD   #$00EF
                              STD   $FD2A
    LDD   #$00BF
                              STD   $FD2C
    LDD   #$00FF
                              STD   $FD2E
    LDD   #$0000
                              STD   $FD30
    PULB
    PULA
    RTS

READ192:
;This routine triggers the QSPI microsequencer to autonomously
;trigger conversions on all 8 channels of the MAX192. Each
;conversion result is stored in the receive data RAM.
    PSHA
    LDAA  #$80
    ORAA  SPCR1
    STAA  SPCR1       ;just set SPE
    PULA
    RTS

***** Interrupts/Exceptions *****

BDM: BGND             ;exception vectors point here
                      ;and put the user in background debug mode
```

Figure 20. MAX192 Assembly-Code Listing (continued)

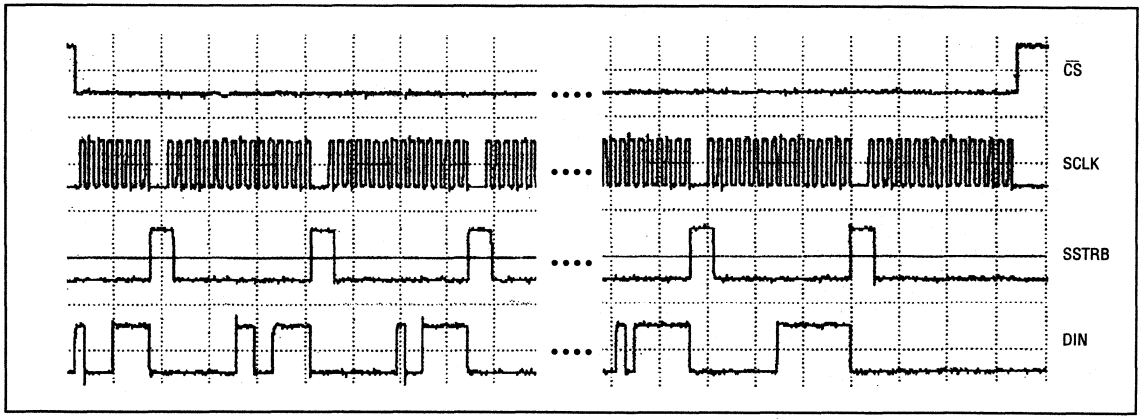


Figure 21. QSPI Assembly-Code Timing

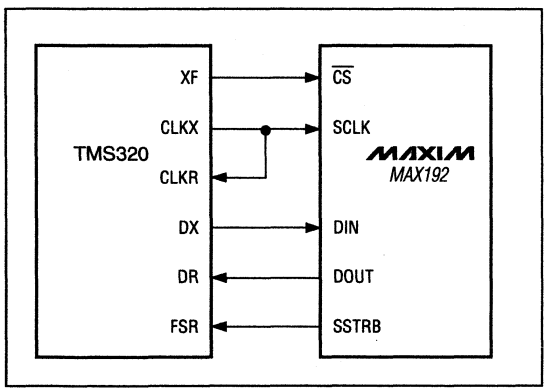


Figure 22. MAX192 to TMS320 Serial Interface

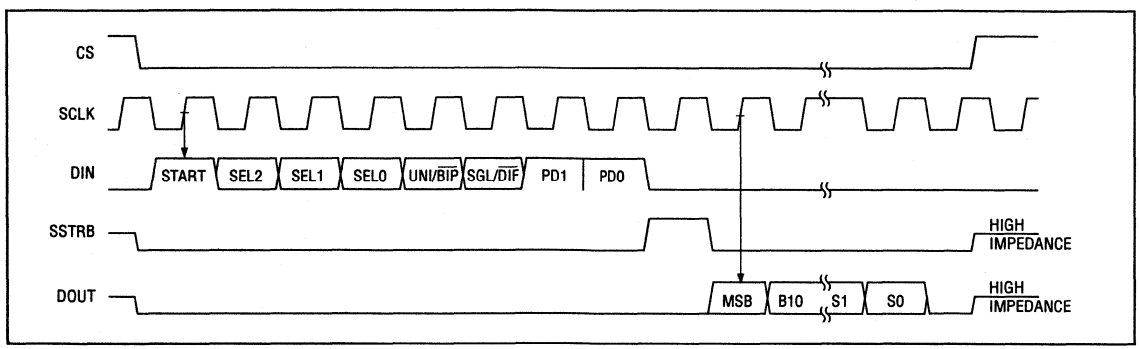
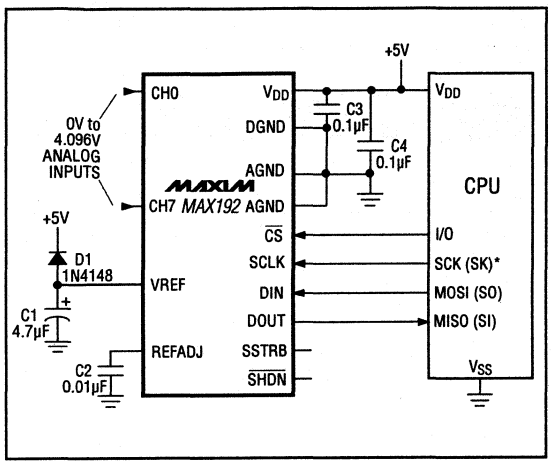


Figure 23. TMS320 Serial-Interface Timing Diagram

Low-Power, 8-Channel, Serial 10-Bit ADC

Typical Operating Circuit



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
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EVALUATION KIT AVAILABLE

MAXIM

16-Bit, Self-Calibrating, 10µs Sampling ADC with Shutdown

General Description

The MAX195 is a 16-bit successive-approximation analog-to-digital converter (ADC) that combines high speed, high accuracy, low power consumption, and a 10µA shutdown mode. Internal calibration circuitry corrects linearity and offset errors to maintain the full rated performance over the operating temperature without external adjustments. The capacitor-DAC architecture provides an inherent 100k samples per second track/hold function.

The MAX195, with an external reference (up to +5V), offers a unipolar (0V to REF) or bipolar (-REF to REF) pin-selectable input range. Separate analog and digital supplies minimize digital-noise coupling.

The chip-select input ($\overline{CS}$) controls the three-state serial-data output. The output can be read either during conversion as the bits are determined, or following conversion at up to 5MHz using the serial clock (SCLK). Calibration is performed at power-up and can be initiated at any time using the $\overline{RESET}$ pin. The end-of-conversion output ($\overline{EOC}$) can be either used to interrupt a processor, or connected directly to the convert input (CONV) for continuous, full-speed conversions.

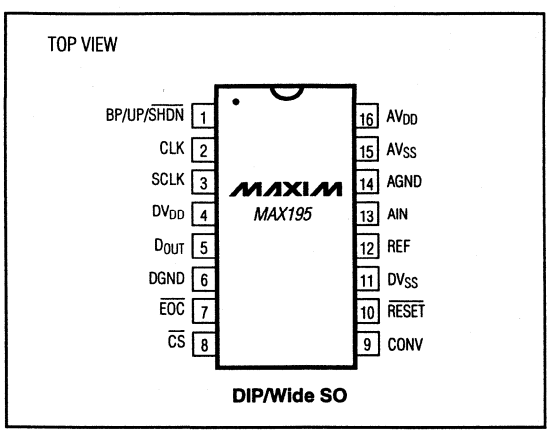
Applications

Industrial Controls
Robotics
Multiple Transducer Measurements
Vibration Analysis
Digital Signal Processing

Features

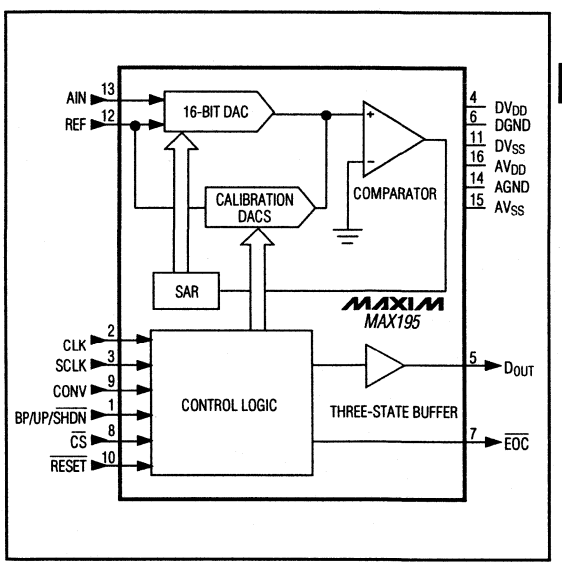
- **16-Bit Resolution and Linearity**
- **Internal Calibration of Linearity and Offset**
- **100ksps Sampling ADC**
- **Built-In Track/Hold**
- **AC and DC Specified**
- **Unipolar (0V to REF) and Bipolar (-REF to REF) Input Range**
- **Three-State Serial-Data Output**
- **Small 16-Pin DIP and SO Packages**
- **10µA Shutdown Mode**

Pin Configuration



DIP/Wide SO

Functional Diagram



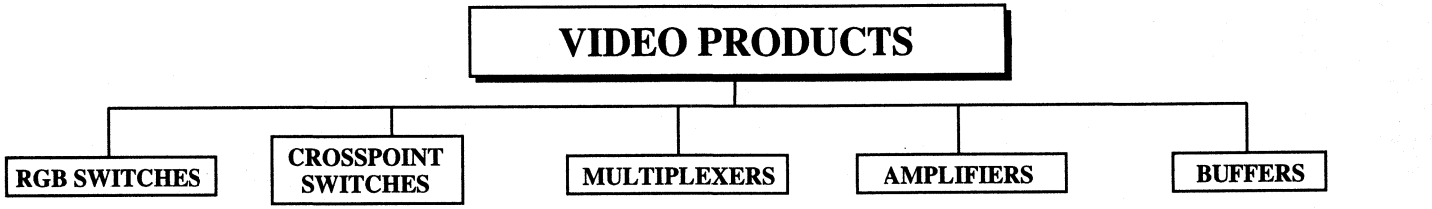
7

Video Products

8

*Advance Information–first page of data sheet in preparation.

VIDEO PRODUCTS



RGB SWITCHES

★ **MAX463**
(100MHz, output drivers)

☆★ **MAX464**
(100MHz, output drivers)

★ **MAX465**
(90MHz, AV = +2 output drivers)

☆★ **MAX466**
(90MHz, AV = +2 output drivers)

CROSSPOINT SWITCHES

MAX456
(8 x 8)

☆★ **MAX458**
(8 x 4, 100MHz, output drivers)

☆★ **MAX459**
(8 x 4, 90MHz, AV = +2 output drivers)

MULTIPLEXERS

MAX440
(160MHz, 8-ch mux + output amp)

MAX441
(160MHz, 4-ch mux + output amp)

MAX442
(160MHz, 2-ch mux + output amp)

MAX453
(50MHz, 2-ch mux + output amp)

MAX454
(50MHz, 4-ch mux + output amp)

MAX455
(50MHz, 8-ch mux + output amp)

AMPLIFIERS

MAX404
(80MHz, AV ≥ 2V/V)

MAX408
(100MHz, AV ≥ 3V/V)

MAX428
(dual MAX408)

MAX435
(275MHz, diff in/diff out)

MAX436
(200MHz, diff in/single out)

MAX448
(quad MAX408)

MAX452
(50MHz)

MAX453
(50MHz, 2-ch mux + amp)

MAX454
(50MHz, 4-ch mux + amp)

MAX455
(50MHz, 8-ch mux + amp)

MAX457
(70MHz dual)

† **MAX476**
(300MHz)

BUFFERS

MAX405
(160MHz, 0.998V/V gain)

MAX460
(140MHz, JFET input)

★ **MAX467**
(100MHz triple (RGB) buffer)

★ **MAX468**
(100MHz quad buffer)

★ **MAX469**
(90MHz, AV = +2 triple (RGB) buffer)

★ **MAX470**
(90MHz, AV = +2 quad buffer)

† **MAX477**
(300MHz, AV = +1/+2)

☆ Evaluation kit available
† Future product
★ New product

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	V_{OS} (mV max)	Output Current (mA min)	Supply Voltage (V)	I_{BIAS} (nA max)	Features	Price† 1000-up ($)
VIDEO AMPLIFIERS								
MAX404	80 ($A_V \geq 2$)	500	8	50	±5	3µA	Broadcast-quality video op amp, 0.01°/0.05% diff phase/gain, symmetrical inputs, 70dB CMRR, 66dB A_{VOL}	2.68
MAX408/428/448	100 ($A_V \geq 3$)	90	6 to 12	50/op amp	±5	1.1µA	Single/dual/quad op amp, high-output drive	3.02/4.06/6.74
MAX435/436	275	800	3	10	±5	3µA	Ultra high-speed differential input/output transconductance amp, no feedback required	2.75
MAX452	50	300	5	14	±5	10	Unity-gain stable, drives 75Ω coax cable	2.40
MAX457	70	300	5	15	±5	1	Dual, unity-gain stable, drives 75Ω coax cable	4.45
MAX476	300	3000	2	100	±5	5µA	Gain of +1 or +2 buffer, 0.01°/0.01% diff phase/gain error	††
BB3554	90	1200	1	125	±15	50pA	Fast-settling (150ns), differential JFET input	56.99
VIDEO BUFFERS								
MAX405	180	650	5	60	±5	2µA	Broadcast quality, 0.99V gain guaranteed over temp, 0.01°/0.03% diff phase/gain error	4.25
MAX460	140	1500	5 to 10	100	±15	0.05 to 0.1	FET input, EL2005/LH0033 upgrade	19.78
MAX467	100	200	10	20	±5	–	Triple (RGB) video buffer, 0.03°/0.01% diff phase/gain error	3.70
MAX468	100	200	10	20	±5	–	Quad, unity-gain video buffer, 0.03°/0.01% diff phase/gain error	4.20
MAX469	90	300	10	20	±5	–	Triple (RGB), gain of +2 video buffer, 0.03°/0.01% diff phase/gain error	3.70
MAX470	90	300	10	20	±5	–	Quad, gain of +2 (6dB) video buffer, 0.03°/0.01% diff phase/gain error	4.20
MAX477	500	3000	4	100	±5	5µA	Ultra high-speed amplifier, 0.01°/0.01% diff phase/gain error	††
LH0033	100	1400 to 1500	5 to 20	100	±15	0.1 to 0.5	FET input, improved industry standard	13.67
LH0063/BB3553	300	2000	25 to 50	200	±15	0.2 to 0.5	FET input, industry standard	23.51/24.99
VIDEO MULTIPLEXER/AMPLIFIERS								
MAX440	160 110 ($A_V \geq 2$)	370	10	35	±5	2µA	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain error,15ns switch time, high-Z output state	8.95
MAX441	160 110 ($A_V \geq 2$)	370	10	35	±5	2µA	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain error, 15ns switch time	5.90
MAX442	140	250	5	35	±5	2µA	Video amp with 2-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	300	5	14	±5	10	Video amp with 2-channel video mux	3.94
MAX454	50	300	5	14	±5	10	Video amp with 4-channel video mux	5.25
MAX455	50	300	5	14	±5	10	Video amp with 8-channel video mux	8.75

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Video/High-Speed Products (continued)

Part Number	Unity-Gain Bandwidth (MHz)	Slew Rate (v/µs)	Switching Time (ns)	Number of Inputs	Number of Outputs	Buffer Amp Gain (V/V)	Output Current (mA)	Features	Price† 1000-up ($)
RGB VIDEO SWITCHES									
MAX463/465	100	300	20	6 (RGB_A, RGB_B)	3 (RGB)	+1, +2	20	RGB switch with 75Ω cable drivers	6.97
MAX464/466	100	300	20	8 (RGB_A + Sync, RGB_B + Sync)	4 (RGB + Sync)	+1, +2	20	RGB + sync switch with 75Ω cable drivers	7.97

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	Diff Phase/Gain Error	Off Isolation (dB typ)	Crosstalk (dB typ)	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCHES							
MAX456	35	250	1°/0.5%	80 (5MHz)	70 (5MHz)	8 x 8 crosspoint switch array with 8 output buffers, high-Z output capability	19.98
MAX458/459	100	300	0.05°/0.01%	60 (10MHz)	55 (10MHz)	8 x 4 crosspoint switch array with four 75Ω cable drivers, high-Z output capability.	22.00

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Low-Cost, High-Resolution, Z-Axis Video Display Driver

General Description

The MAX445 is a high-performance, monolithic, variable-gain transconductance amplifier with a high-voltage open collector output capable of directly driving a video display (CRT cathode). Rise times of 2.5ns through 50V are achieved using a peaking network with a 200Ω load resistor and an 8pF total load (CRT and parasitic capacitance).

Differential inputs and a linear adjustable gain stage with an output offset adjustment make the versatile MAX445 well suited for many video display applications. A buffered bandgap reference voltage is available for the gain (contrast) and offset (brightness) adjustments along with a TTL BLANK input to turn off the output current, independent of signal input.

The MAX445 is available in a 24-pin power-tab DIP package. A suitable heatsink must be attached to maintain the junction temperature with the recommended operating range.

Applications

CRT Driver for High Resolution Monochrome and Color Displays

High-Voltage, Variable-Gain Transconductance Amplifier

Features

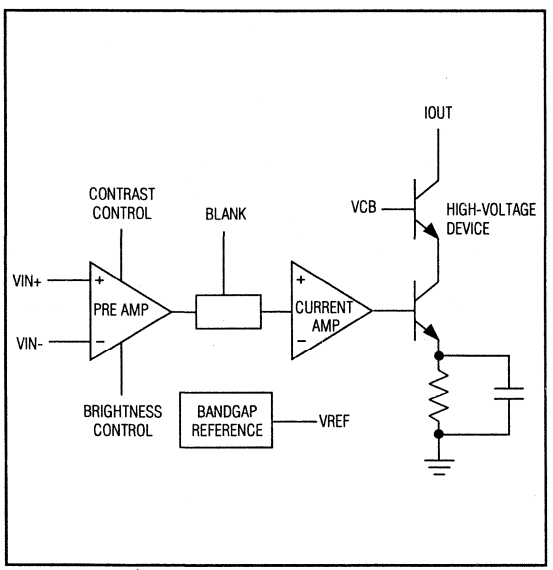
- ♦ **2.5ns Rise/Fall Time into an 8pF Load**
- ♦ **50Vp-p Output**
- ♦ **Ground Referenced Differential Inputs**
- ♦ **Linear Variable Gain For Contrast Control**
- ♦ **Offset Adjustment for Brightness Control**
- ♦ **5.5V Bandgap Reference**
- ♦ **Drives 1280 x 1024 and 1530 x 1280 Displays**

Ordering Information

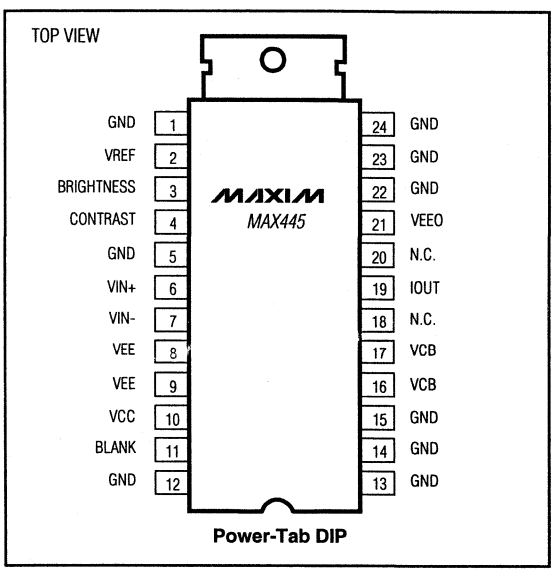
PART	TEMP. RANGE	PIN-PACKAGE
MAX445CPG	0°C to +70°C	24 Power-Tab DIP
MAX445C/D	0°C to +70°C	Dice*

** Dice are specified at T_A = +25°C, DC parameters only.*

Functional Diagram



Pin Configuration



Power-Tab DIP

19-0258; Rev 0; 5/94

EVALUATION KIT AVAILABLE

MAXIM

8x4 Video Crosspoint Switches with Buffers

General Description

The MAX458/MAX459 are crosspoint switches with eight input channels and four high-speed, buffered output channels. The MAX458 output buffer is configured with a gain of one, while the MAX459 buffer has a gain of two. In each device, any one of eight input lines can be connected to any of four output amplifiers. The output buffers are capable of driving loads of 75Ω.

Data interface can be accomplished by either a 16-bit serial or a 6-bit parallel connection. In the serial mode, the MAX458/MAX459 are SPI™, QSPI™, and Microwire™ compatible. In parallel mode, the MAX458/MAX459 are compatible with most microprocessor buses. Three-state amplifier output capability makes it possible to multiplex MAX458/MAX459s to form larger switch networks. The output buffers can be disabled individually or the entire device can be shut down to conserve power.

Applications

Video Test Equipment
Video Security Systems
Video Editing

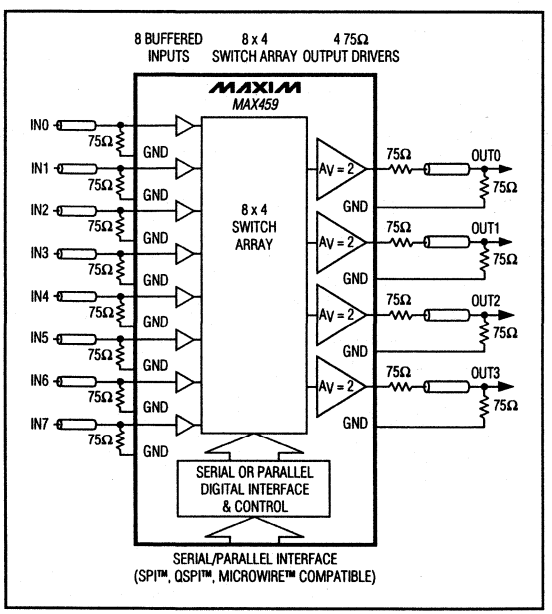
Features

- ♦ **100MHz Unity-Gain Bandwidth**
- ♦ **300V/µs Slew Rate**
- ♦ **Low 0.05° Differential Phase Error**
- ♦ **Low 0.01% Differential Gain Error**
- ♦ **Directly Drives 75Ω Cables**
- ♦ **Fast 60ns Switching Time**
- ♦ **High-Z Amplifier Output Capability**
- ♦ **Shutdown Capability**
- ♦ **16-Bit Serial and 6-Bit Parallel Address Modes**
- ♦ **40-Pin DIP and 44-Pin PLCC Packages**

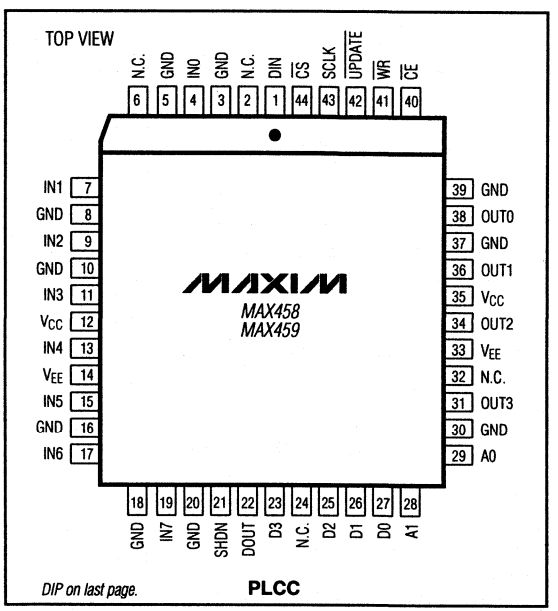
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX458CPL	0°C to +70°C	40 Plastic DIP
MAX458CQH	0°C to +70°C	44 PLCC
MAX458EPL	-40°C to +85°C	40 Plastic DIP
MAX459CPL	0°C to +70°C	40 Plastic DIP
MAX459CQH	0°C to +70°C	44 PLCC
MAX459EPL	-40°C to +85°C	40 Plastic DIP

Block Diagram



Pin Configurations



™ *SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.*

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8x4 Video Crosspoint Switches with Buffers

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{CC} to V_{EE}) 12V
Positive Supply Voltage (V_{CC} to GND) 6V
Negative Supply Voltage (V_{EE} to GND) 6V
Analog Input/Output Voltage ..... (V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Digital Input Voltage ..... (V_{CC} + 0.3V) to -0.3V
Duration of Output Short Circuit to GND (Note 1) ..... Continuous
Continuous Power Dissipation
  Plastic DIP (derate 17mW/°C above +70°C) 1333mW
  PLCC (derate 13mW/°C above +70°C) 1067mW

Operating Temperature Ranges
  MAX45_C_ _ ..... 0°C to +70°C
  MAX45_E_ _ ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Outputs may be shorted to any supply pin or ground as long as package power dissipation ratings are not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, -2V ≤ V_{IN} ≤ +2V, output load resistor (R_L) = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC SPECIFICATIONS							
Input Voltage Range				-2		+2	V
Input Offset Voltage	V_{OS}	Any channel	T_A = +25°C		5	15	mV
			T_A = T_{MIN} to T_{MAX}			20	
Input Offset Voltage Match	ΔV_{OS}	V_{IN} = 0V (Note 2)			3	10	mV
Power-Supply Rejection Ratio	PSRR	V_S = ±4.75V to ±5.25V		50	60		dB
On Input Bias Current	I_{IN}	V_{IN} = 0V, input programmed to one output			±1	±5	µA
On Input Resistance	R_{IN}	Input programmed to one output		0.50	5.0		MΩ
Input Capacitance	C_{IN}	Input channel on or off			7		pF
DC Voltage Gain Accuracy		MAX458 (Note 3)	T_A = +25°C		0.1	0.5	%
			T_A = T_{MIN} to T_{MAX}			1.0	
		MAX459 (Note 4)	T_A = +25°C		0.1	1.0	
			T_A = T_{MIN} to T_{MAX}			2.0	
Output Voltage Swing	V_{OUT}			±2	±3		V
Enabled Output Resistance	R_{OUT}	V_{IN} = 1kHz sine wave			0.05		Ω
		V_{IN} = 10MHz sine wave			4.0		
Disabled Output Resistance	R_{OUT}	MAX458		0.25	1.0		MΩ
		MAX459		0.70	1.0		kΩ
Disabled Output Capacitance	C_{OUT}				12		pF
Positive Power-Supply Current	I_{CC}	V_{IN} = 0V, all amplifiers enabled	T_A = +25°C	60	75	85	mA
			T_A = T_{MIN} to T_{MAX}	50		100	
Negative Power-Supply Current	I_{EE}	V_{IN} = 0V, all amplifiers enabled	T_A = +25°C	50	65	75	mA
			T_A = T_{MIN} to T_{MAX}	40		90	
Positive Supply Current in Shutdown					15	26	mA
Negative Supply Current in Shutdown					7	12	mA
Logic Input High Voltage	V_{IH}	(Note 5)				2.0	V
Logic Input Low Voltage	V_{IL}	(Note 5)		0.8			V

8x4 Video Crosspoint Switches with Buffers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, -2V ≤ V_{IN} ≤ +2V, output load resistor (R_L) = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Input High Current	I_{IH}	(Note 3)				10	µA
Logic Input Low Current	I_{IL}	(Note 3)				10	µA
Logic Output High Voltage	V_{OH}	I_{SOURCE} = 400µA (Note 5)		4.0			V
Logic Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA (Note 5)				0.5	V
DYNAMIC SPECIFICATIONS							
Differential Gain Error (Note 6)	DG	MAX458			0.01		%
		MAX459			0.13		
Differential Phase Error (Note 6)	DG	MAX458			0.05		degrees
		MAX459			0.14		
Slew Rate	SR	MAX458	Positive transition		200		V/µs
			Negative transition		150		
		MAX459	Positive transition		300		
			Negative transition		250		
Bandwidth (-3dB)	BW	MAX458, R_L = 75Ω			100		MHz
		MAX459, R_L = 150Ω			90		
Input Noise Density	e_n	f = 10kHz			20		nV/√Hz
Settling Time	t_S	To 0.1% of final value (Note 7)			40		ns
Amplifier Disable Time	t_{AOFF}				100		ns
Amplifier Enable Time	t_{AON}				120		ns
Channel Switching Time	t_{CSW}				60		ns
Channel Switching Propagation Delay	t_{CPD}				50		ns
Switching Transient Glitch		See *Typical Operating Characteristics*			100		mV_{p-p}
Adjacent Channel Crosstalk		(Note 8)			-65		dB
Non-Adjacent Channel Crosstalk		(Note 9)			-65		dB
All-Hostile Crosstalk		(Note 10)			-55		dB
All-Hostile Off Isolation		(Note 11)			-60		dB

Note 2: Defined as the DC offset shift when switching between input channels for a given output.

Note 3: Voltage Gain Accuracy for MAX458 calculated as $\frac{(V_{OUT} - V_{IN})\ @\ (V_{IN} = +2V) - (V_{OUT} - V_{IN})\ @\ (V_{IN} = -2V)}{4V}$

Note 4: Voltage Gain Accuracy for MAX459 calculated as $\frac{(V_{OUT}/2 - V_{IN})\ @\ (V_{IN} = +1V) - (V_{OUT}/2 - V_{IN})\ @\ (V_{IN} = -1V)}{2V}$

Note 5: All logic levels are guaranteed over the range of V_S = ±4.75V to ±5.25V.

Note 6: Differential phase and gain measured with a 40 IRE (285.7mV), 3.58MHz sine wave superimposed on a linear ramp of 0 IRE to 100 IRE (714.3mV). "The IRE scale is a linear scale for measuring, in arbitrary IRE units, the relative amplitudes of the various components of a television signal" (from the "Television Engineering Handbook", edited by K. Blair Benson, McGraw Hill). This system defines 100 IRE as reference white, 0 IRE as the blanking level, and -40 IRE as the sync peak. The equipment used for the test signal generated 714.3mV (100 IRE) as reference white and -285.7mV (-40 IRE) as sync. The modulation used was 285.7mV (40 IRE), which conforms to the EIA color signal standards.

Note 7: For MAX458, step input from +2V to 0V; for MAX459, step input from +1V to 0V. All unused channels grounded and all unused amplifiers disabled.

Note 8: Test input channel programmed to an output and grounded through a 75Ω resistor. Adjacent input is programmed to an adjacent output and driven by a 10MHz, 4Vp-p sine wave.

Note 9: Same as Note 6 above, except driven input and output are not adjacent to test input/output.

Note 10: All inputs but the test input are driven by a 10MHz 4Vp-p sine wave. All outputs except the test output are connected to driven inputs.

Note 11: Same as Note 9 above, except with test channel programmed off.

8x4 Video Crosspoint Switches with Buffers

TIMING CHARACTERISTICS (Note 12)

(V_{CC} = +5V, V_{EE} = -5V, -2V ≤ V_{IN} ≤ +2V, output load resistor (R_L) = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
PARALLEL-MODE TIMING (see Figure 1)					
Address to $\overline{WR}$ Fall Setup Time	t_{ADS}		20		ns
Address to $\overline{WR}$ Rise Hold Time	t_{ADH}		0		ns
$\overline{CE}$ Fall to $\overline{WR}$ Fall Setup Time	t_{CES}		0		ns
$\overline{CE}$ Rise to $\overline{WR}$ Rise Hold Time	t_{CEH}		0		ns
$\overline{WR}$ Pulse Width Low	t_{WR}		40		ns
Data to $\overline{WR}$ Rise Setup Time	t_{DS}		50		ns
Data to $\overline{WR}$ Rise Hold Time	t_{DH}		0		ns
$\overline{WR}$ Rise to $\overline{UPDATE}$ Fall Setup Time	t_{WRS}		0		ns
$\overline{UPDATE}$ Pulse Width Low	t_{UP}		40		ns
$\overline{UPDATE}$ Rise to $\overline{WR}$ Fall Setup Time	t_{UPS}		25		ns
SERIAL-MODE TIMING (see Figure 6)					
SCLK to $\overline{CS}$ Fall	t_{CSO}		0		ns
$\overline{CS}$ Fall to SCLK Rise	t_{CSS}		35		ns
SCLK Pulse Width High	t_{CH}		50		ns
SCLK Pulse Width Low	t_{CL}		30		ns
DIN to SCLK Rise Setup Time	t_{DS}		50		ns
DIN to SCLK Rise Hold Time	t_{DH}		0		ns
SCLK Fall to DOUT	t_{DO}			200	ns
SCLK Rise to $\overline{CS}$ Rise	t_{CSH}		30		ns
$\overline{CS}$ Rise to SCLK Rise	t_{CS1}		20		ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100		ns

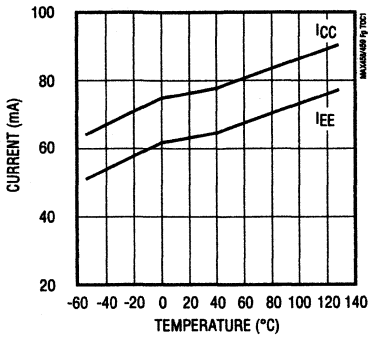
Note 12: Timing Characteristics are guaranteed by design.

8x4 Video Crosspoint Switches with Buffers

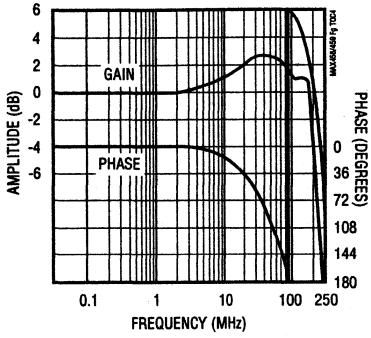
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

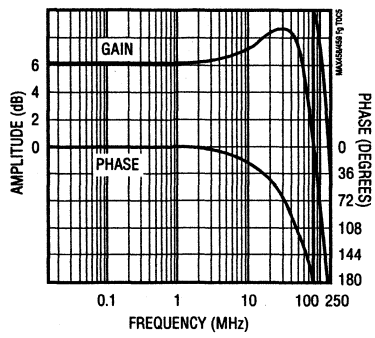
POWER SUPPLY CURRENT vs. TEMPERATURE



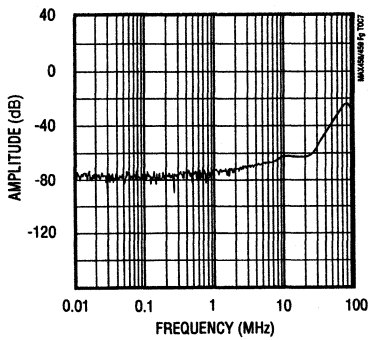
MAX458 GAIN vs. FREQUENCY



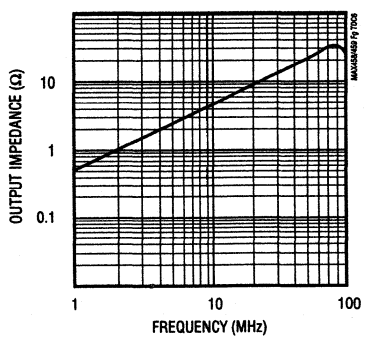
MAX459 GAIN vs. FREQUENCY



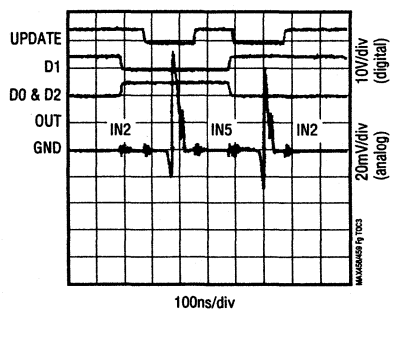
CROSSTALK vs. FREQUENCY



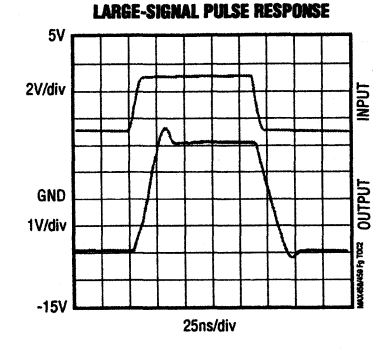
OUTPUT IMPEDANCE vs. FREQUENCY



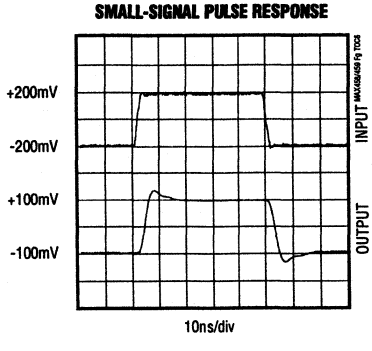
CHANNEL SWITCH TRANSIENT



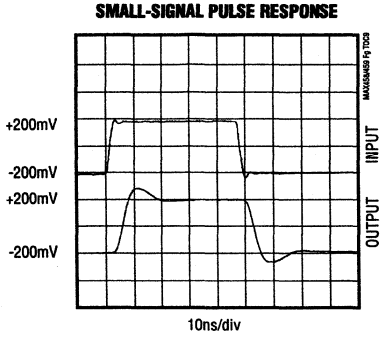
MAX458 LARGE-SIGNAL PULSE RESPONSE



MAX458 SMALL-SIGNAL PULSE RESPONSE



MAX459 SMALL-SIGNAL PULSE RESPONSE



8

8x4 Video Crosspoint Switches with Buffers

Pin Description

PIN		NAME	FUNCTION
DIP	PLCC		
1	1	DIN	Serial Data Input
2, 4, 6, 8, 14, 16, 18, 27, 33, 35	3, 5, 8, 10, 16, 18, 20, 30, 37, 39	GND	Ground
3	4	IN0	Analog Input Channel 0
5	7	IN1	Analog Input Channel 1
7	9	IN2	Analog Input Channel 2
9	11	IN3	Analog Input Channel 3
10, 31	12, 35	V_{CC}	Positive Power Supply (+5V). Connect both V_{CC} pins to the positive supply.
11	13	IN4	Analog Input Channel 4
12, 29	14, 33	V_{EE}	Negative Power Supply (-5V). Connect both V_{EE} pins to the negative supply.
13	15	IN5	Analog Input Channel 5
15	17	IN6	Analog Input Channel 6
17	19	IN7	Analog Input Channel 7
19	21	SHDN	Shutdown, active high. Connect to GND if not used.
20	22	DOUT	Serial Data Output used for daisy-chaining devices.
21	23	D3	Parallel Digital Channel Input Address Bit 3
22	25	D2	Parallel Digital Channel Input Address Bit 2
23	26	D1	Parallel Digital Channel Input Address Bit 1
24	27	D0	Parallel Digital Channel Input Address Bit 0
25	28	A1	Parallel Digital Amplifier Output Address Bit 1
26	29	A0	Parallel Digital Amplifier Output Address Bit 0
28	31	OUT3	Amplifier 3 Analog Output
30	34	OUT2	Amplifier 2 Analog Output
32	36	OUT1	Amplifier 1 Analog Output
34	38	OUT0	Amplifier 0 Analog Output
36	40	$\overline{CE}$	Chip Enable, used in parallel mode. Keep high for serial operation.
37	41	$\overline{WR}$	Write Low, latches input registers in parallel mode. Hold high for serial operation.
38	42	$\overline{UPDATE}$	Update Low, latches amplifier registers in parallel mode. Hold high for serial operation.
39	43	SCLK	Serial Clock
40	44	$\overline{CS}$	Chip Select, used in serial operation. Hold high for parallel mode of operation.
—	2, 6, 24, 32	N.C.	Not Internally Connected

Note: All GND pins must be grounded for optimum crosstalk performance.

8x4 Video Crosspoint Switches with Buffers

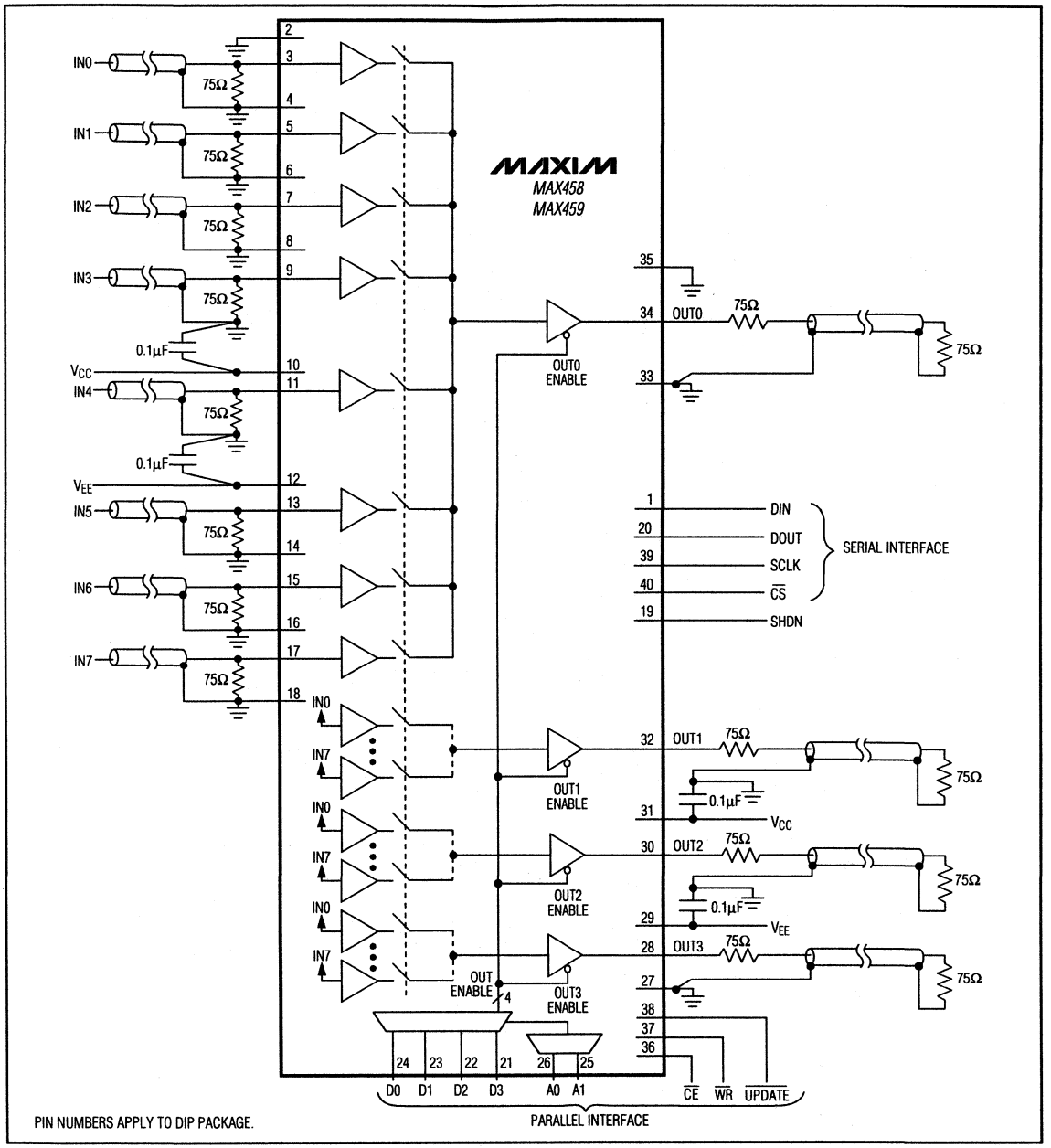


Figure 1. Block Diagram and Typical Operating Circuit

8x4 Video Crosspoint Switches with Buffers

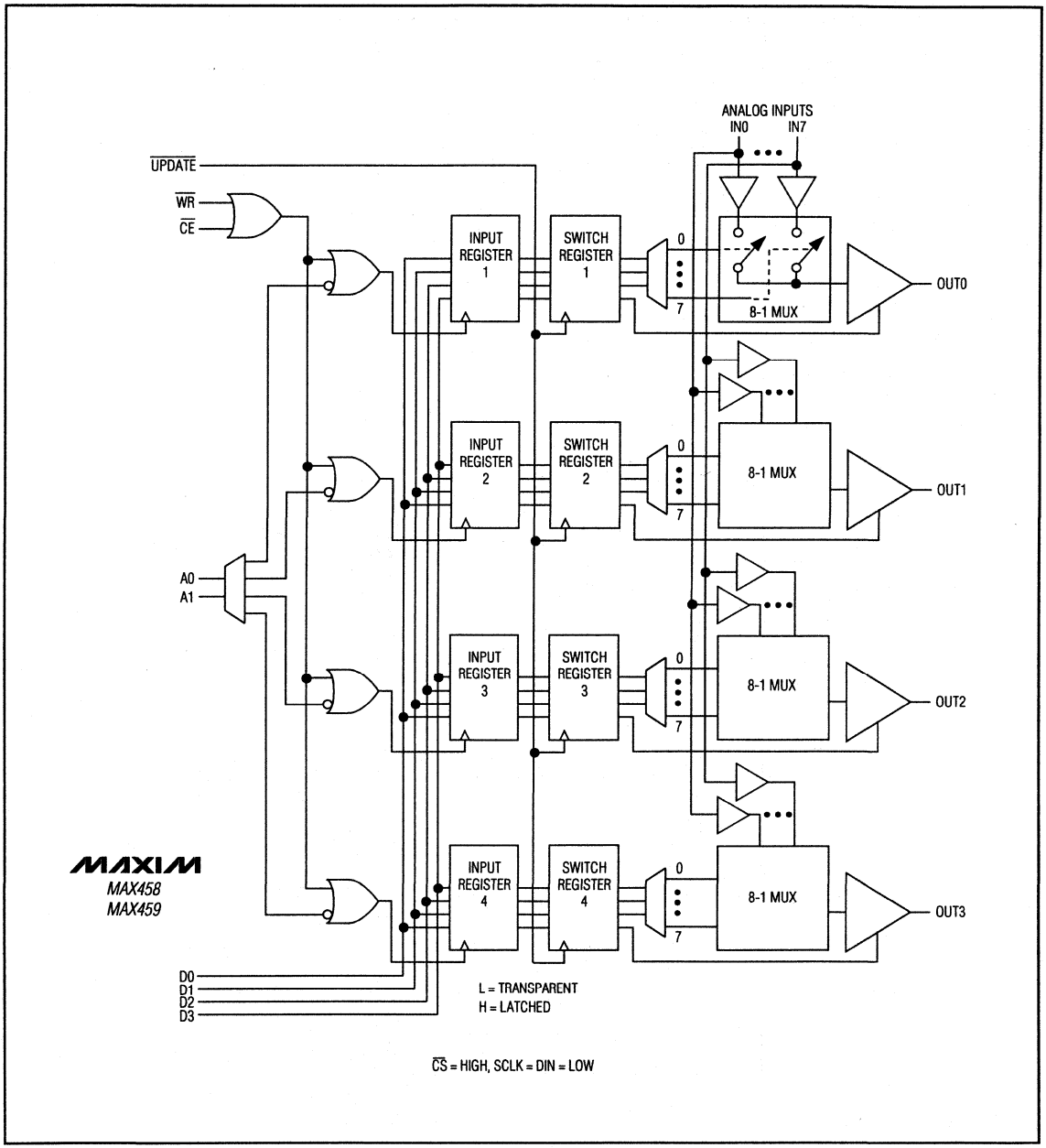


Figure 2. Parallel-Logic Block Diagram

8x4 Video Crosspoint Switches with Buffers

Detailed Description

Analog Section

The MAX458/MAX459 video crosspoint switches consist of a high-speed 32 (8x4) switch array with wide-bandwidth line drivers (Figure 1). This design allows make-before-break switching to reduce output noise and glitches, but the inputs will not short together. It also provides high input impedance and low input capacitance, so no input buffer amplifier is needed. However, because different transistors provide gain depending on the input selection, the DC offset voltage shifts slightly when a new input is switched in. The change in offset voltage is typically 3mV.

All output buffers will drive back-terminated 50Ω, 75Ω, or higher impedance lines with up to 100pF capacitance. The amplifier outputs can be disabled, which is useful for creating large arrays. When disabled, the MAX458 presents an output impedance of approximately 1MΩ. The MAX459 disabled output impedance is 1kΩ (to ground), due to the internal feedback resistors used to achieve the gain of two.

During power-on, if $\overline{CS}$ and $\overline{UPDATE}$ are held high, all output amplifiers are disabled. In a large array, this feature prevents two ON paralleled amplifiers from distorting each other's signals. The amplifiers can be programmed to come up in any state simultaneously at any time after power-on. See the *Creating Large Arrays* section.

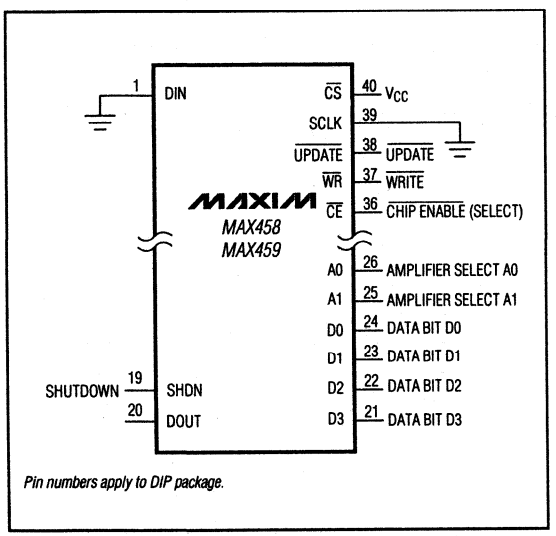


Figure 3. Parallel Connection (only logic pins shown)

Digital Section—Parallel Mode

The MAX458/MAX459 have two register banks—an input register and a switch register (Figure 2). Each of these registers is either latched (when the control input is high) or transparent (when the control input is low). The input register is controlled by $\overline{WR}$ and $\overline{CE}$ and is selected by the decode of A0 and A1. If both $\overline{WR}$ and $\overline{CE}$ are low, the input register selected by A0 and A1 is transparent, and the state of D0–D3 is presented to the switch register. The other three input registers remain latched. If D0–D3 change before $\overline{UPDATE}$ is asserted (goes low), the new data (the changed D0–D3) will then be latched in the switch register. If $\overline{WR}$ or $\overline{CE}$ is high, all input registers are latched and their data is presented

Table 1. Amplifier Selection

A1	A0	Output Amplifier Selected
L	L	0
L	H	1
H	L	2
H	H	3

Table 2. Input Selection

D3	D2	D1	D0	Input Channel Selected
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	X	X	X	Disable output amplifier selected by A0, A1.

Table 3. Writing Data

$\overline{CE}$	$\overline{WR}$	$\overline{UPDATE}$	FUNCTION
H X	X H	H H	Device not selected or is operating in serial mode. Both registers are latched.
H X	X H	L L	Data in input registers passes through switch registers. Output reflects data in input registers.
L	L	H	Input register of selected amplifier is transparent. Switch registers are latched. Other input registers are latched.
L	L	L	All switch registers and selected input register are transparent. Selected amplifier (chosen by state of A0, A1) reflects input data. Other amplifiers reflect data that had been latched into the input registers previously.

8x4 Video Crosspoint Switches with Buffers

to their switch registers. As long as either $\overline{WR}$ or $\overline{CE}$ is high, the input register will not change. The switch register will pass any new data on the falling transition of $\overline{UPDATE}$.

Each register of the switch-register bank controls the inputs to one amplifier. With $\overline{UPDATE}$ low, the switch registers are transparent and switch connection is controlled by the input register. However, if $\overline{UPDATE}$ is high, the switch register is latched and any change in data by the input register will not affect the amplifier output state. Two register banks are used so that data can be loaded into input registers without affecting the switch/amplifier selection. This allows amplifiers to be programmed and then changed simultaneously. When the registers are not latched, they are made transparent.

Use data bit D3 to disable the amplifier selected by A0–A1 and place its output in high-impedance mode. As an example, the code to disable OUT0 is as follows:

Pin Name:	D3	D2	D1	D0	A1	A0
Input Code:	1	X	X	X	0	0

When operating in parallel mode, $\overline{CS}$ must be wired high and SCLK and DIN should be grounded, as shown in Figure 3. Refer to Figure 4 for the correct timing relationships.

Digital Section—Serial Mode

The MAX458/MAX459 use a three-wire serial interface that is compatible with SPI, QPSI and Microwire interfaces. Serial mode, shown in Figure 5, is enabled when $\overline{WR}$, $\overline{UPDATE}$, and $\overline{CE}$ are held high and $\overline{CS}$ goes low. Figures 6 and 7 show serial-mode timing. Figure 8 shows the MAX458/MAX459 configured for serial operation. Figure 9 shows the Microwire connection, and Figure 10 shows the SPI/QSPI connection.

In parallel mode, inputs A0 and A1 determine which of the output amplifiers is controlled by data bits D0–D3. In serial mode, however, this function is performed when $\overline{CS}$ goes high. If $\overline{CS}$ is held low for only the first four clock pulses, the controlled amplifier will be OUT0. After eight clock pulses, it will be OUT0 and OUT1. After 12 clock pulses, it will be OUT0, OUT1, and OUT2. Holding $\overline{CS}$ low for 16 clock pulses will input data for all four amplifiers OUT0–OUT3. If the high transition of $\overline{CS}$ occurs before four clock positive edges, the connection to OUT0 will be arbitrary.

The serial output, DOUT, allows cascading of two or more crosspoint switches to create larger arrays. The data at DOUT is delayed by 16 cycles plus one clock pulse width at DIN. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

The MAX458/MAX459 input data in 16-bit blocks. SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data. The QSPI interface allows variable word lengths from 8 to 16 bits and can be loaded into the crosspoint in one write cycle. SPI and Microwire limit clock rates to 2MHz, while the QSPI maximum clock rate is 4MHz.

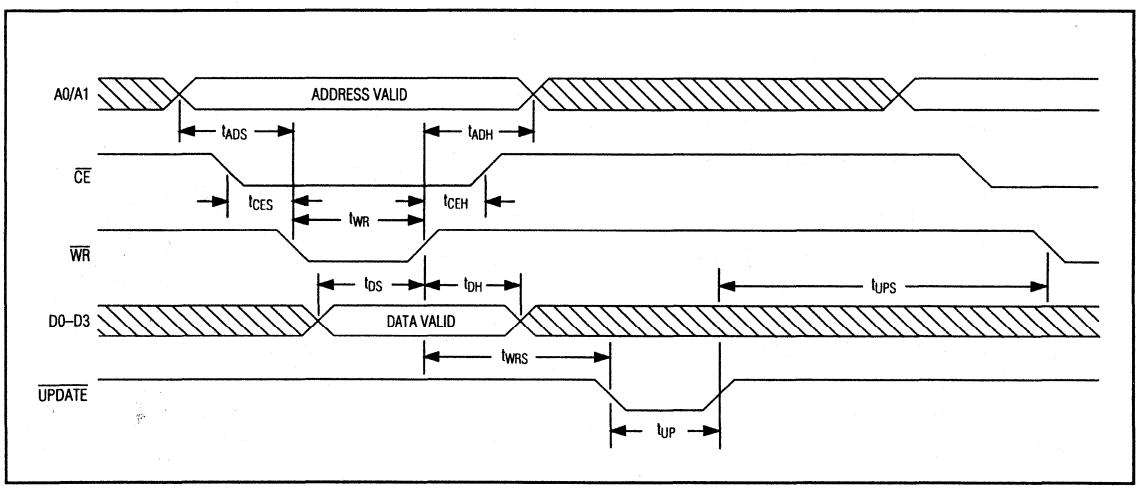


Figure 4. Parallel-Mode Timing

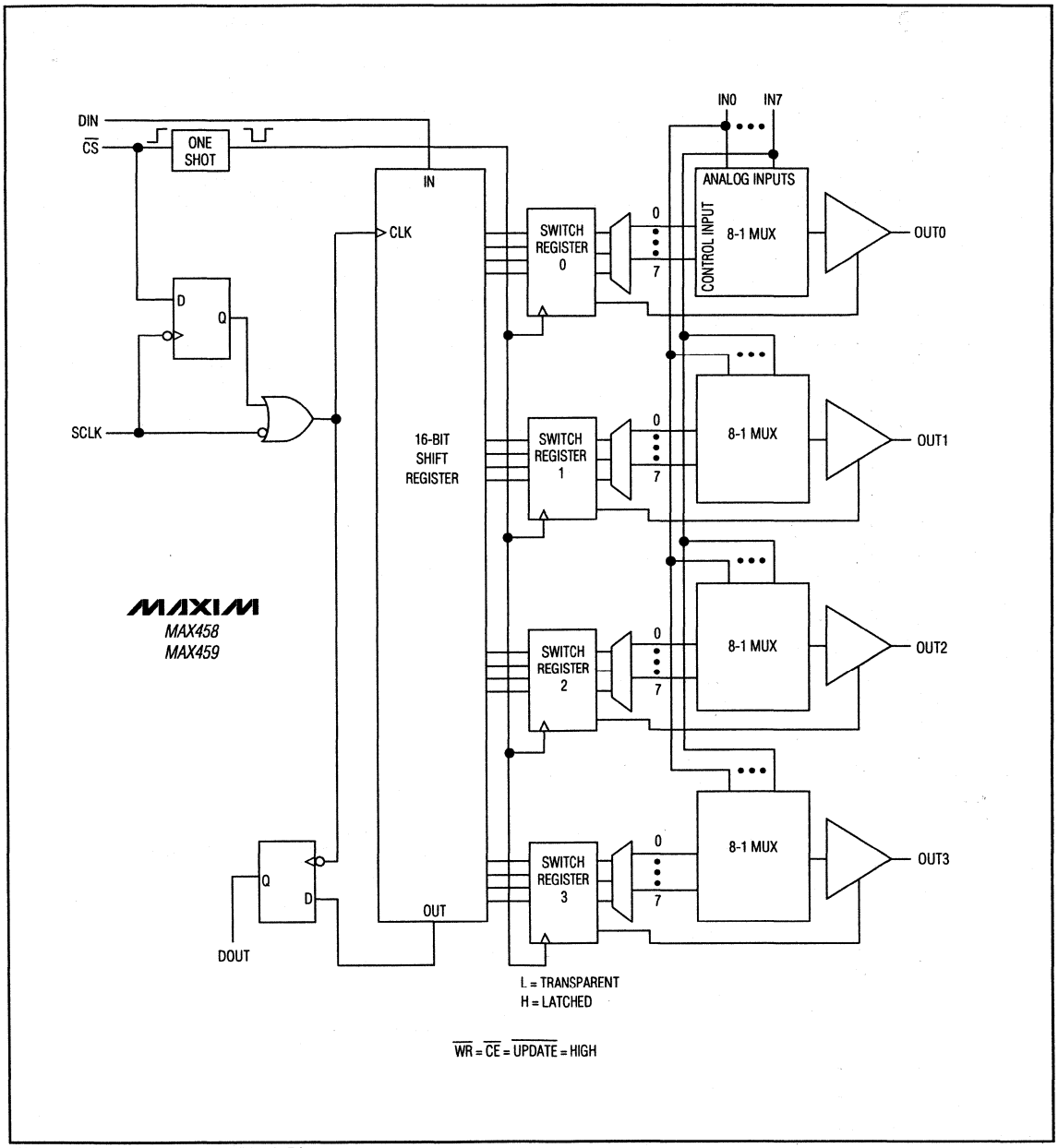


Figure 5. Serial-Mode Logic Block Diagram

8x4 Video Crosspoint Switches with Buffers

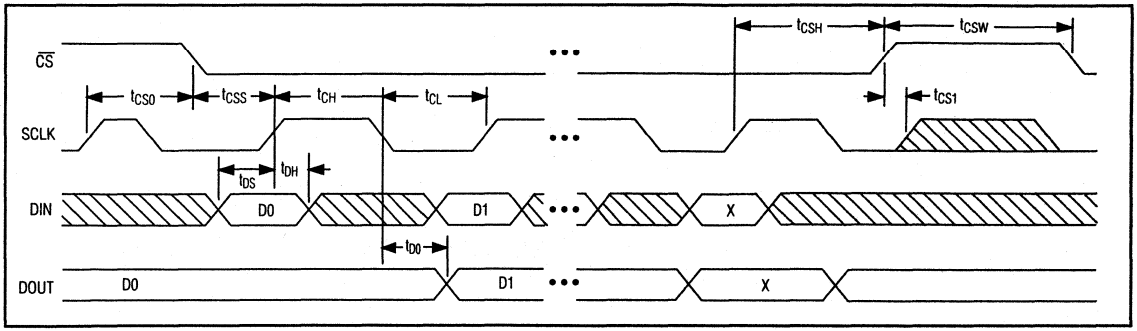


Figure 6. Serial-Mode Timing

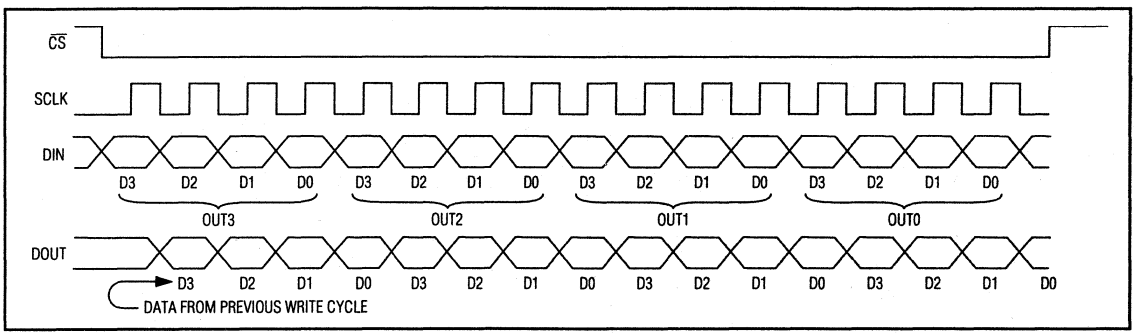


Figure 7. Serial-Mode Data Sequence

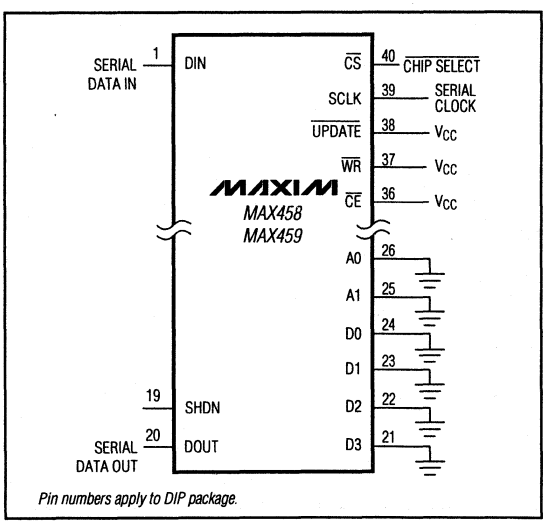
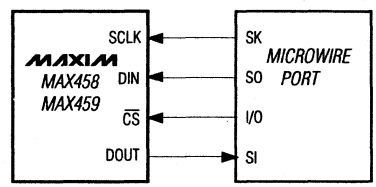


Figure 8. Serial Connection (only logic pins shown)



THE DOUT-SI CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX458/MAX459, BUT MAY BE USED FOR DATA-ECHO PURPOSES.

Figure 9. Microwire Connection

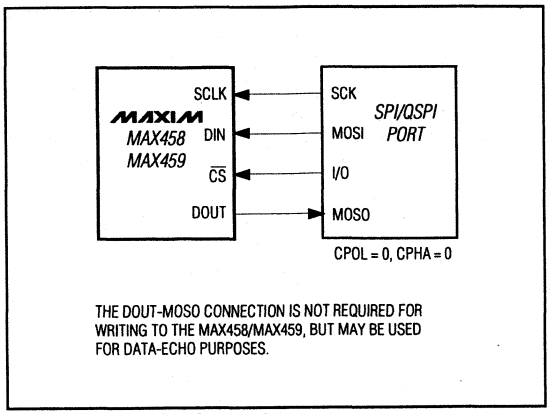


Figure 10. SPI/QSPI Connection

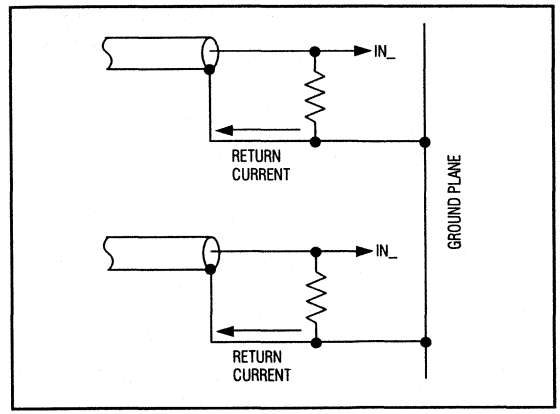


Figure 11. Low-Crosstalk Layout. Return current from termination resistor does not flow through the ground plane.

Applications Information

Grounding and Bypassing, PC Board Layout

As with all analog circuits, good PC board layout, proper grounding, and careful component selection are crucial for realizing the full AC performance of high-speed amplifiers such as the MAX458/MAX459. For optimal performance:

1) Use a large, low-impedance analog ground plane. With multilayer boards, the ground plane(s) should be located on the layer that does not contain signal traces. Connect all GND pins to the analog ground plane.
2) Minimize trace area at the circuit's critical high-impedance nodes to prevent unwanted signal coupling. Surround analog inputs with an AC ground trace (bypassed DC power supply, etc.). The analog input pins of the MAX458/MAX459 have been separated with AC ground pins (GND, V_{CC}, V_{EE}) to minimize parasitic coupling, which can degrade crosstalk.
3) Connect the coaxial-cable shield to the ground side of the 75Ω terminating resistor at the ground plane to further reduce crosstalk (Figure 11).
4) Bypass all power-supply pins directly to the ground plane with 0.1µF ceramic capacitors placed as close to the supply pins as possible. For high-current loads, you may need 10µF tantalum or aluminum-electrolytic capacitors in parallel with the 0.1µF ceramics. Keep capacitor lead lengths as short as possible to minimize series inductance; surface-mount chip capacitors are ideal.

Creating Larger Arrays

The MAX458/MAX459 assume a high-impedance state on power-up if the inputs are not being programmed to any particular state during that time. They also are in a high-impedance state when disabled. This feature makes it possible to create larger arrays than 8x4 without special programming, other than ensuring that your program doesn't turn on two paralleled outputs simultaneously. Testing has shown no degradation of differential gain or phase when the outputs are connected in parallel.

The MAX458/MAX459's input registers remain active during shutdown, which allows the crosspoint to be programmed while the devices are shut down. As a result, all outputs may be simultaneously brought to any state, including disabled. Just program all of the MAX458/MAX459s into shutdown, and enter the program of your choice by selecting the desired inputs and outputs. Taking SHDN low takes the device(s) out of shutdown.

A power-on reset circuit causes the output amplifiers to power up in the disabled mode, whether or not SHDN is applied, if $\overline{UPDATE}$ and $\overline{CS}$ are high.

The number of MAX458s that can be paralleled is limited by capacitive loading on each output, which must not exceed 100pF. Each input presents approximately 7pF of load, and each output presents approximately 12pF. Therefore, the MAX458/MAX459 will drive a maximum of 14 inputs, or 7 outputs and 2 inputs, or any other combination resulting in less than a 100pF load. Adding isolation resistors enables more MAX458s to be paralleled (see the *Driving Capacitive Loads* section).

8x4 Video Crosspoint Switches with Buffers

Driving Capacitive Loads

When driving loads greater than 100pF, you may need a capacitance compensating resistor in series with the output of each affected amplifier. The required resistor will depend on load as well as capacitance. For 150Ω or higher load resistances and capacitance up to 1000pF, use a 2.4Ω resistor. For 100Ω loads, use a 4.7Ω resistor.

If an output amplifier is loaded with a pure capacitance or with the inputs of other MAX458/MAX459s, the resistors will cause no degradation of gain or other performance because of the high impedance of the crosspoints. However, resistive loads may cause a reduction in gain.

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more crosspoint switches to create larger arrays. The data at DOUT is the DIN data delayed by 16 cycles plus one clock width. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX458/MAX459 crosspoint switches can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain, as shown in Figure 12. For proper timing, ensure that both t_{CSS} ($\overline{CS}$ low to SCLK high) and t_{CL} are greater than $t_{DO} + t_{DS}$.

DOUT is a TTL-compatible output with an active pull-up. It does not become high impedance when $\overline{CS}$ is high.

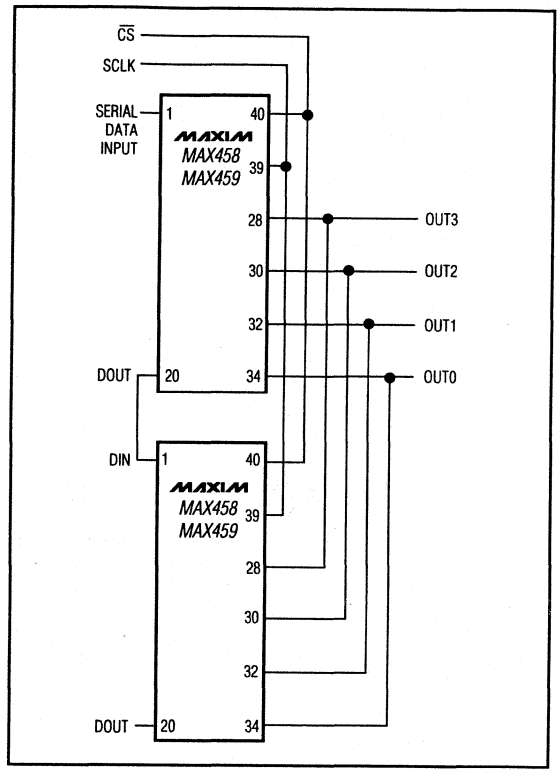
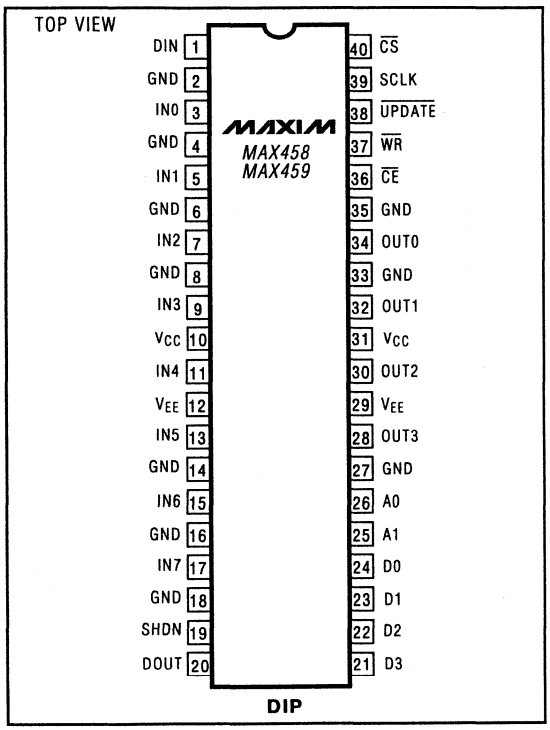


Figure 12. 16x4 Crosspoint Switch Using Serial "Daisy Chain" Connection

8x4 Video Crosspoint Switches with Buffers

Pin Configurations (continued)



19-0219; Rev 1; 3/94

EVALUATION KIT AVAILABLE

Two-Channel, Triple/Quad RGB Video Switches and Buffers

General Description

The MAX463–MAX470 series of two-channel, triple/quad buffered video switches and video buffers combines high-accuracy, unity-gain-stable amplifiers with high-performance video switches. Fast switching time and low differential gain and phase error make this series of switches and buffers ideal for all video applications. The devices are all specified for ±5V supply operation with inputs and outputs as high as ±2.5V when driving 150Ω loads (75Ω back-terminated cable).

Input capacitance is typically only 5pF, and channel-to-channel crosstalk is better than 60dB, accomplished by surrounding all inputs with AC ground pins. The on-board amplifiers feature a 200V/µs slew rate (300V/µs for A_V = 2V/V amplifiers), and a bandwidth of 100MHz (90MHz for A_V = 2V/V buffers). Channel selection is controlled by a single TTL-compatible input pin or by a microprocessor interface, and channel switch time is only 20ns.

For design flexibility, devices are offered with buffer-amplifier gains of 1V/V or 2V/V for 75Ω back-terminated applications. Output amplifiers have a guaranteed output swing of ±2V into 75Ω.

Devices offered in this series are as follows:

PART	DESCRIPTION	VOLTAGE GAIN (V/V)
MAX463	Triple RGB Switch & Buffer	1
MAX464	Quad RGB Switch & Buffer	1
MAX465	Triple RGB Switch & Buffer	2
MAX466	Quad RGB Switch & Buffer	2
MAX467	Triple Video Buffer	1
MAX468	Quad Video Buffer	1
MAX469	Triple Video Buffer	2
MAX470	Quad Video Buffer	2

Applications

Broadcast-Quality Color-Signal Multiplexing
RGB Multiplexing
RGB Color Video Overlay Editors
RGB Color Video Security Systems
RGB Medical Imaging
Coaxial-Cable Line Drivers

Typical Operating Circuit appears at end of data sheet.

Features

- ♦ **100MHz Unity-Gain Bandwidth**
- ♦ **90MHz Bandwidth with 2V/V Gain**
- ♦ **0.01%/0.03° Differential Gain/Phase Error**
- ♦ **Drives 50Ω and 75Ω Back-Terminated Cable Directly**
- ♦ **Wide Output Swing:**
  ±2V into 75Ω
  ±2.5V into 150Ω
- ♦ **300V/µs Slew Rate (2V/V gain)**
- ♦ **20ns Channel Switching Time**
- ♦ **Logic Disable Mode:**
  High-Z Outputs
  Reduced Power Consumption
- ♦ **Outputs May Be Paralleled for Larger Networks**
- ♦ **5pF Input Capacitance (channel on or off)**

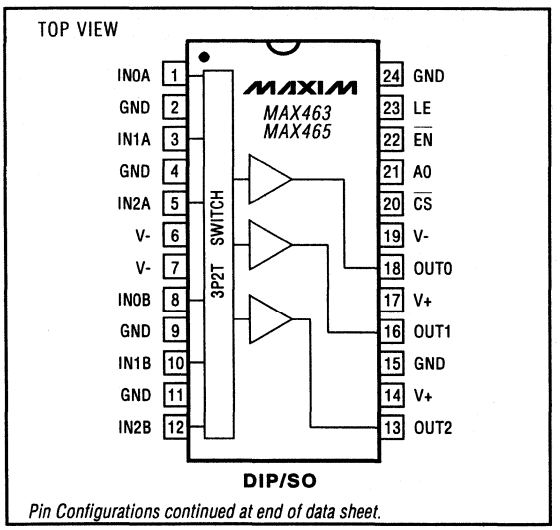
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX463CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX463CWG	0°C to +70°C	24 Wide SO
MAX463C/D	0°C to +70°C	Dice*
MAX463ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX463EWG	-40°C to +85°C	24 Wide SO

Ordering Information continued on last page.

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations



Pin Configurations continued at end of data sheet.

8

Two-Channel, Triple/Quad RGB Video Switches and Buffers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Ranges
V+ to V- 12V
Analog Input Voltage ..... (V- - 0.3V) to (V+ + 0.3V)
Digital Input Voltage ..... -0.3V to (V+ + 0.3V)
Output Short-Circuit Duration (to GND) ..... 1 Minute
Input Current into Any Pin, Power On or Off ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 22.22mW/°C above +70°C) 1778mW
16-Pin Wide SO (derate 20.00mW/°C above +70°C) 1600mW
24-Pin Narrow Plastic DIP
(derate 20.2mW/°C above +70°C) 1620mW
24-Pin Wide SO (derate 19.3mW/°C above +70°C) 1590mW
28-Pin Narrow Plastic DIP
(derate 20.2mW/°C above +70°C) 1620mW
28-Pin Wide SO (derate 18.1mW/°C above +70°C) 1440mW
Operating Temperature Ranges
MAX4_ _C_ _ ..... 0°C to +70°C
MAX4_ _E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, -2V ≤ V_{IN} ≤ +2V, R_{LOAD} = 75Ω, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C MIN	TYP	MAX	T_A = T_{MIN} to T_{MAX} MIN	MAX	UNITS
Operating Supply Voltage	V_S		±4.75	±5	±5.25	±4.75	±5.25	V
Input Voltage Range	V_{IN}		-2		2	-2	2	V
Offset Voltage	V_{OS}			±3	±10		±15	mV
Power-Supply Rejection Ratio	PSRR		50	60		50		dB
On Input Bias Current	I_{BIAS}			±1	±3		±5	µA
On Input Resistance	R_{IN}		300	700		150		kΩ
Input Capacitance	C_{IN}	Channel off or on		5				pF
Voltage-Gain Accuracy		MAX463/MAX464, MAX467/MAX468 (Note 1)		0.2	0.5		1.0	%
		MAX465/MAX466, MAX469/MAX470, R_{LOAD} = 150Ω, (Note 2)		0.3	1.0		2.0	
Output Voltage Swing	V_{OUT}	R_{LOAD} = 150Ω	±2.5	±2.8		±2.5		V
		R_{LOAD} = 75Ω	±2.0	±2.4		-1.5/+2		
Output Impedance	R_{OUT}	f_{IN} = 10MHz		5				Ω
		f_{IN} = DC, MAX463/MAX464, MAX467/MAX468		0.05				
		f_{IN} = DC, MAX465/MAX466, MAX469/MAX470		0.1				
Output Resistance, Disabled Mode	R_{OUTD}	MAX463/MAX464	150	250		100		kΩ
		MAX465/MAX466	0.7	1		0.7		kΩ
Output Capacitance, Disabled Mode	C_{OUTD}	MAX463–MAX466		10				pF
Positive Supply Current	I+	MAX463/MAX465/MAX467/MAX469, V_{IN} = 0V		65	80		100	mA
		MAX464/MAX466/MAX468/MAX470, V_{IN} = 0V		85	100		120	
		MAX463/MAX465, disabled mode		35	45		50	
		MAX464/MAX466, disabled mode		40	50		55	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, -2V ≤ V_{IN} ≤ +2V, R_{LOAD} = 75Ω, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C MIN	TYP	MAX	T_A = T_{MIN} to T_{MAX} MIN	MAX	UNITS
Negative Supply Current	I-	MAX463/MAX465/MAX467/MAX469, V_{IN} = 0V		50	65		75	mA
		MAX464/MAX466/MAX468/MAX470, V_{IN} = 0V		65	80		95	
		MAX463/MAX465, disabled mode		20	30		35	
		MAX464/MAX466, disabled mode		25	35		40	
Input Noise Density	en	f_{IN} = 10kHz		20				nV/√Hz
Slew Rate	SR	MAX463/MAX464, MAX467/MAX468		200				V/µs
		MAX465/MAX466, MAX469/MAX470		300				
-3dB Bandwidth	BW	MAX463/MAX464, MAX467/MAX468		100				MHz
		MAX465/MAX466, MAX469/MAX470		90				
Differential Gain Error (Note 3)	DG	MAX463/MAX464, MAX467/MAX468		0.01				%
		MAX465/MAX466, MAX469/MAX470		0.12				
Differential Phase Error (Note 3)	DP	MAX463/MAX464, MAX467/MAX468		0.03				deg.
		MAX465/MAX466, MAX469/MAX470		0.14				
Settling Time to 0.1%	t_S	V_{IN} = 2V-to-0V step		50				ns
Adjacent Channel Crosstalk (Note 4)	XTALK	f_{IN} = 10MHz		60				dB
All-Hostile Crosstalk (Note 5)	XTALK	f_{IN} = 10MHz		50				dB
All-Hostile Off Isolation (Note 6)	ISO	f_{IN} = 10MHz, MAX463–MAX466		70				dB
Channel Switching Propagation Delay (Note 7)	t_{PD}	MAX463–MAX466		15				ns
Channel Switching Time (Note 8)	t_{SW}	MAX463–MAX466		20				ns
Switching Transient		V_{INA} = V_{INB} = 0V, MAX463–MAX466		300				mV_{P-P}
Amplifier Switching Off-Time (Note 9)	t_{OFF}	MAX463–MAX466		80				ns
Amplifier Switching On-Time (Note 10)	t_{ON}	MAX463–MAX466		100				ns
Logic Input High Threshold	V_{IH}	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466			2		2	V
Logic Input Low Threshold	V_{IL}	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466	0.8			0.8		V
Logic Input Current High	I_{INHI}	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466			200		200	µA
Logic Input Current Low	I_{INLO}	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466			200		200	µA

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Two-Channel, Triple/Quad RGB Video Switches and Buffers

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, -2V ≤ V_{IN} ≤ +2V, R_{LOAD} = 75Ω, unless otherwise noted.)

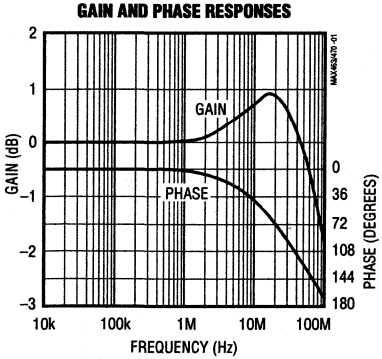
PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C MIN	TYP	MAX	T_A = T_{MIN} to T_{MAX} MIN	MAX	UNITS
Address Setup Time (Note 11)	t_{SU}	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466	30			30		ns
Address Hold Time (Note 11)	t_H	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466			0		0	ns
$\overline{CS}$ Pulse Width Low (Note 11)	t_{CS}	$\overline{EN}$, A0, $\overline{CS}$, LE; MAX463–MAX466	15			15		ns

Note 1: Voltage gain accuracy for the unity-gain devices is defined as [(V_{OUT} - V_{IN}) at V_{IN} = 1V - (V_{OUT} - V_{IN}) at V_{IN} = -1V]/2.
Note 2: Voltage gain accuracy for the gain-of-two devices is defined as [(V_{OUT}/2 - V_{IN}) at V_{IN} = 1V - (V_{OUT}/2 - V_{IN}) at V_{IN} = -1V]/2.
Note 3: Tested with a 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0IRE to 100IRE), R_L = 150Ω to ground.
Note 4: Tested with the selected input connected to ground through a 75Ω resistor, and a $4V_{P-P}$ sine wave at 10MHz driving adjacent input.
Note 5: Tested in the same manner as described in Note 4, but with all other inputs driven.
Note 6: Tested with LE = 0V, $\overline{EN}$ = V+, and all inputs driven with a $4V_{P-P}$, 10MHz sine wave.
Note 7: Measured from a channel switch command to measurable activity at the output.
Note 8: Measured from where the output begins to move to the point where it is well defined.
Note 9: Measured from a disable command to amplifier in a non-driving state.
Note 10: Measured from an enable command to the point where the output reaches 90% current out.
Note 11: Guaranteed by design.

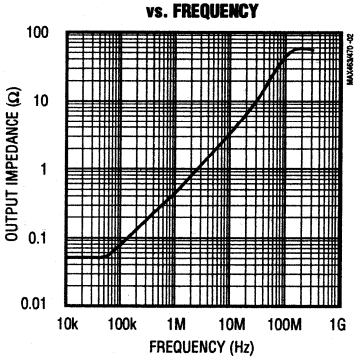
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

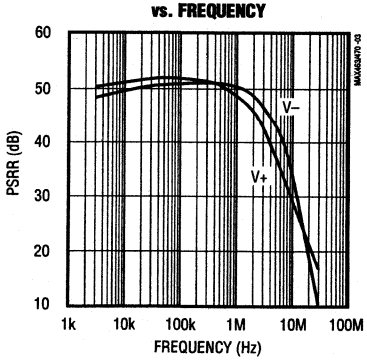
MAX468
GAIN AND PHASE RESPONSES



MAX464
OUTPUT IMPEDANCE vs. FREQUENCY



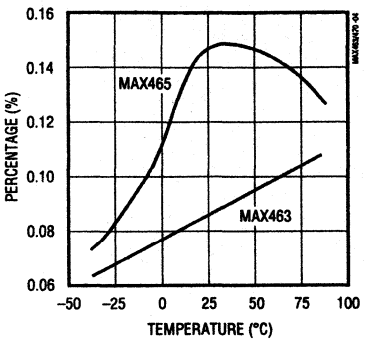
MAX468
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



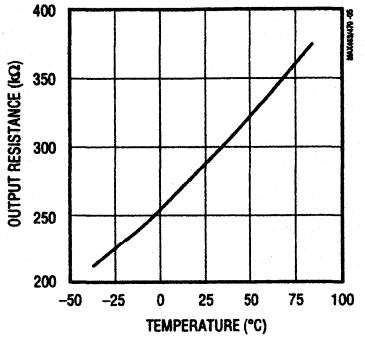
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

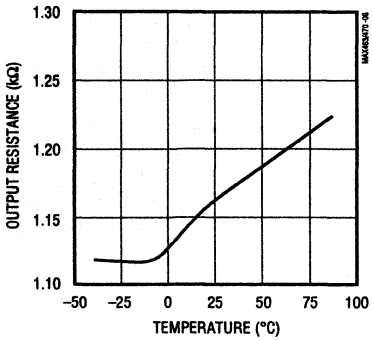
VOLTAGE GAIN ACCURACY vs. TEMPERATURE



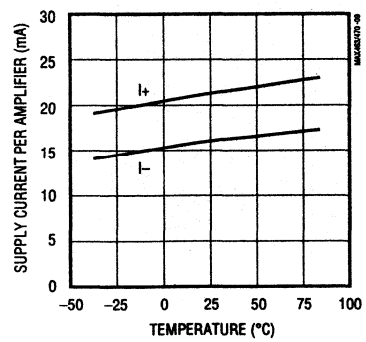
MAX463 DISABLED OUTPUT RESISTANCE vs. TEMPERATURE



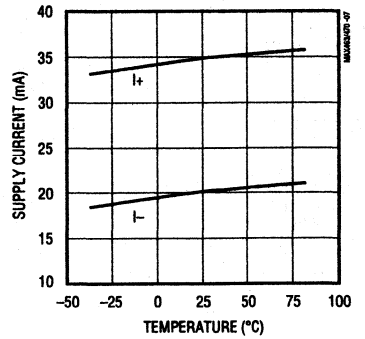
MAX465 DISABLED OUTPUT RESISTANCE vs. TEMPERATURE



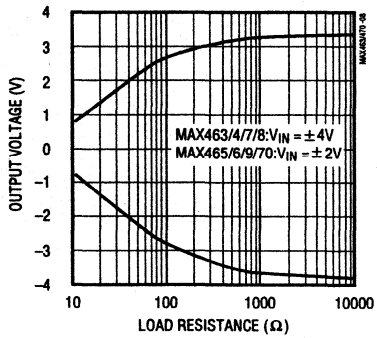
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



DISABLED SUPPLY CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



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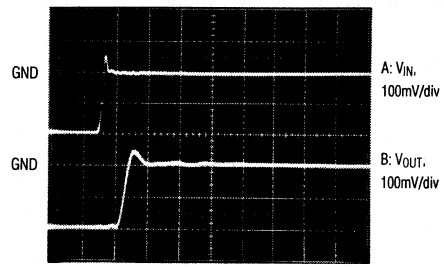
Two-Channel, Triple/Quad RGB Video Switches and Buffers

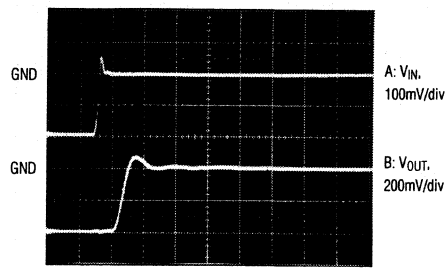
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

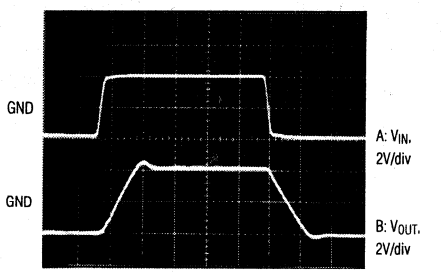
MAX464
SMALL-SIGNAL STEP RESPONSE



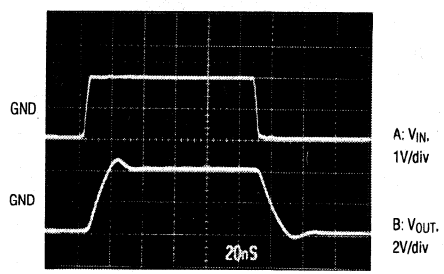
MAX466
SMALL-SIGNAL STEP RESPONSE



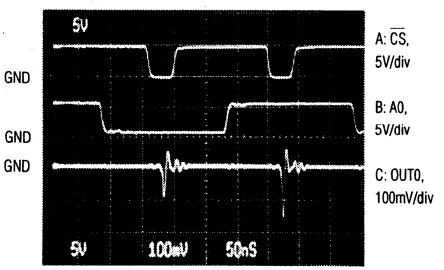
MAX464
LARGE-SIGNAL STEP RESPONSE



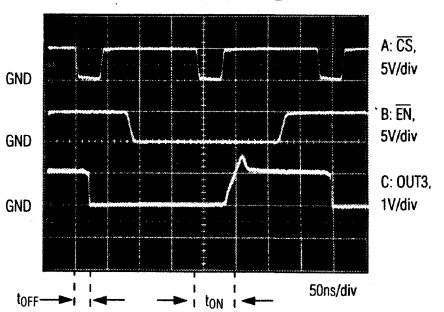
MAX466
LARGE-SIGNAL STEP RESPONSE



MAX464
OUTPUT TRANSIENT WHEN SWITCHING BETWEEN TWO GROUNDED INPUTS



MAX464
EN RESPONSE TIME



Pin Descriptions

PIN		NAME	FUNCTION
MAX463/MAX465	MAX464/MAX466		
1	28	IN0A	Channel A, Analog Input 0
2, 4, 9, 11, 15, 24	1, 3, 5, 11, 13, 19	GND	Analog Ground
3	2	IN1A	Channel A, Analog Input 1
5	4	IN2A	Channel A, Analog Input 2
–	6	IN3A	Channel A, Analog Input 3
6, 7, 19	7, 9, 21, 23	V-	Negative Power-Supply Input. Connect to -5V. Thermal path.
8	8	IN0B	Channel B, Analog Input 0
10	10	IN1B	Channel B, Analog Input 1
12	12	IN2B	Channel B, Analog Input 2
–	14	IN3B	Channel B, Analog Input 3
–	15	OUT3	Buffered Analog Output 3
13	17	OUT2	Buffered Analog Output 2
14, 17	16, 18	V+	Positive Power-Supply Input. Connect to +5V.
16	20	OUT1	Buffered Analog Output 1
18	22	OUT0	Buffered Analog Output 0
20	24	$\overline{CS}$	Chip-Select—latch control for the digital inputs. When $\overline{CS}$ is low, A0 and $\overline{EN}$ input registers are transparent. When $\overline{CS}$ goes high, the A0 input register latches. If LE is high, the $\overline{EN}$ input register also latches when $\overline{CS}$ goes high (see LE).
21	25	A0	Channel-Select Input. When $\overline{CS}$ is low, driving A0 low selects channel A and driving A0 high selects channel B.
22	26	$\overline{EN}$	Buffer-Enable Input. When $\overline{CS}$ is low or LE is low, driving $\overline{EN}$ low enables all output buffers and driving $\overline{EN}$ high disables all output buffers.
23	27	LE	Digital Latch-Enable Input. When LE is low, the $\overline{EN}$ register is transparent; when LE is high, the $\overline{EN}$ register is transparent only when $\overline{CS}$ is low. Hard-wire to V+ or GND for best crosstalk performance.

PIN		NAME	FUNCTION
MAX467/MAX469	MAX468/MAX470		
1	1	IN0	Analog Input 0
2, 7, 8, 9, 15	2, 7, 15	GND	Analog Ground
3	3	IN1	Analog Input 1
4, 5, 12, 13	4, 5, 12, 13	V-	Negative Power-Supply Input. Connect to -5V. Thermal path.
6	6	IN2	Analog Input 2
–	8	IN3	Analog Input 3
–	9	OUT3	Buffered Analog Output 3
10	10	V+	Positive Power-Supply Input. Connect to +5V.
11	11	OUT2	Buffered Analog Output 2
14	14	OUT1	Buffered Analog Output 1
16	16	OUT0	Buffered Analog Output 0

Two-Channel, Triple/Quad RGB Video Switches and Buffers

Detailed Description

The MAX463–MAX470 have a bipolar construction, which results in a typical channel input capacitance of only 5pF, whether the channel is on or off. This low input capacitance allows the amplifiers to realize full AC performance, even with source impedances as great as 250Ω. It also minimizes switching transients because the driving source sees the same load whether the channel is on or off. Low input capacitance is critical, because it forms a single-pole RC low-pass filter with the output impedance of the signal source, and this filter can limit the system's signal bandwidth if the RC product becomes too large.

The MAX465/MAX466/MAX469/MAX470's amplifiers are internally configured for a gain of two, resulting in an overall gain of one at the cable output when driving back-terminated coaxial cable (see the section *Driving Coaxial Cable*). The MAX463/MAX464/MAX467/MAX468 are internally configured for unity gain.

Power-Supply Bypassing and Board Layout

To realize the full AC performance of high-speed amplifiers, pay careful attention to power-supply bypassing and board layout, and use a large, low-impedance ground plane. With multi-layer boards, the ground plane should be located on the layer that is not dedicated to a specific signal trace.

To prevent unwanted signal coupling, minimize the trace area at the circuit's critical high-impedance nodes, and surround the analog inputs with an AC ground trace (analog ground, bypassed DC power supply, etc). The analog input pins to the MAX463–MAX470 have been separated with AC ground pins (GND, V+, V-, or a hard-wired logic input) to minimize parasitic coupling, which can degrade crosstalk and/or stability of the amplifier. Keep signal paths as short as possible to minimize inductance, and ensure that all input channel traces are of equal length to maintain the phase relationship between the R, G, and B signals. Connect the coaxial-cable shield to the ground side of the 75Ω terminating resistor at the ground plane to further reduce crosstalk (see Figure 1).

Bypass all power-supply pins directly to the ground plane with 0.1µF ceramic capacitors, placed as close to the supply pins as possible. For high-current loads, it may be necessary to include 10µF tantalum or aluminum-electrolytic capacitors in parallel with the 0.1µF ceramics. Keep capacitor lead lengths as short as possible to minimize series inductance; surface-mount (chip) capacitors are ideal.

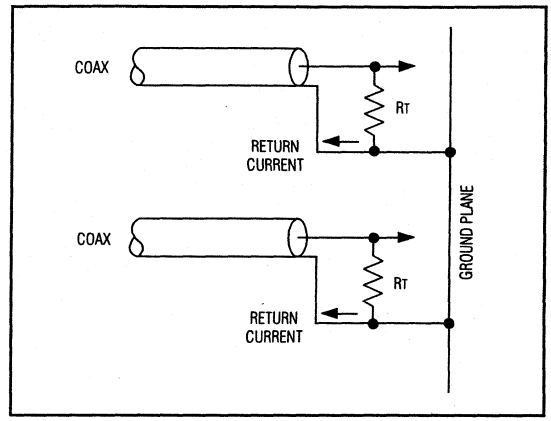


Figure 1. Low-Crosstalk Layout. Return current from the termination resistor does not flow through the ground plane.

Connect all V- pins to a large power plane. The V- pins conduct heat away from the internal die, aiding thermal dissipation.

Differential Gain and Phase Errors

Differential gain and phase errors are critical specifications for an amplifier/buffer in color video applications, because these errors correspond directly to changes in the color of the displayed picture in composite video systems. The MAX467–MAX470 have low differential gain and phase errors, making them ideal in broadcast-quality composite color applications, as well as in RGB video systems where these errors are less significant.

The MAX467–MAX470 differential gain and phase errors are measured with the Tektronix VM700 Video Measurement Set, with the input test signal provided by the Tektronix 1910 Digital Generator as shown in Figure 2.

Measuring the differential gain and phase of the MAX469/MAX470 (Figure 2a) is straightforward because the output amplifiers are configured for a gain of two, allowing connection to the VM700 through a back-terminated coaxial cable. Since the MAX467/MAX468 are unity-gain devices, driving a back-terminated coax would result in a gain of 1/2 at the VM700.

Figure 2b shows a test method to measure the differential gain and phase for the MAX467/MAX468. First, measure and store the video signal with the device under test (DUT) removed and replaced with a short circuit, and the 150Ω load resistor omitted. Then do another measurement with the DUT and load resistor in the circuit, and calculate the differential gain and phase errors by subtracting the results.

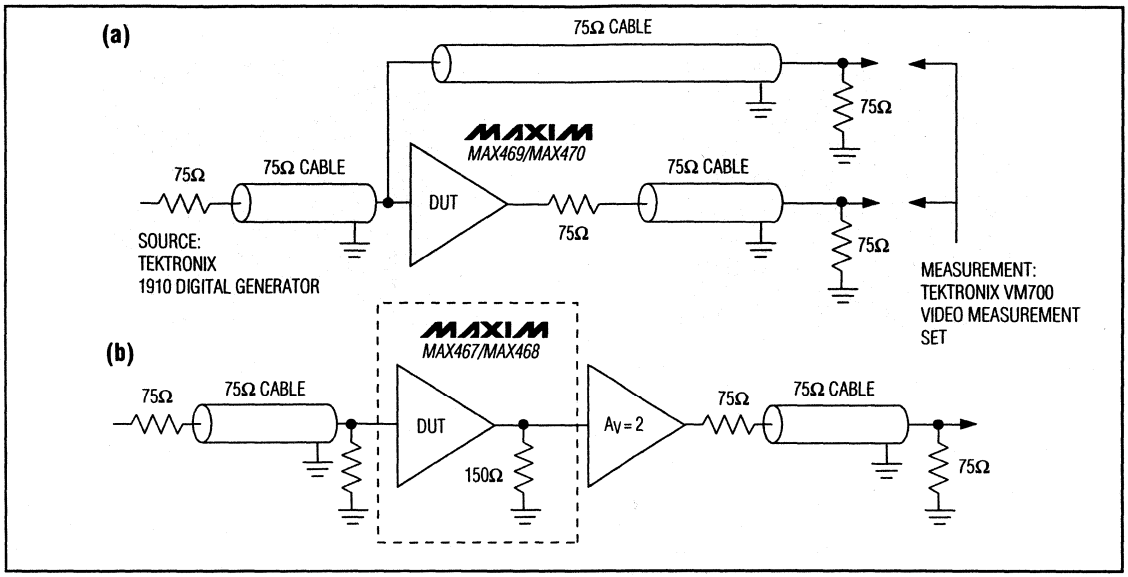


Figure 2. Differential Phase and Gain Error Test Circuits (a) for the MAX469/MAX470 Gain-of-Two Amplifiers, (b) for the MAX467/MAX468 Unity-Gain Amplifiers

Driving Coaxial Cable

High-speed performance, excellent output current capability, and an internally fixed gain of two make the MAX465/MAX466/MAX469/MAX470 ideal for driving 50Ω or 75Ω back-terminated coaxial cables. The MAX465/MAX466/MAX469/MAX470 will drive a 150Ω load (75Ω back-terminated cable) to ±2.5V.

The *Typical Operating Circuit* shows the MAX465/MAX466 driving four back-terminated 75Ω video cables. The back-termination resistor (at each amplifier output) provides impedance matching at the driven end of the cable to eliminate signal reflections. It forms a voltage divider with the load impedance, which attenuates the signal at the cable output by one-half. The amplifier operates with an internal 2V/V closed-loop gain to provide unity gain at the cable's output.

Driving Capacitive Loads

Driving large capacitive loads increases the likelihood of oscillation in most amplifier circuits. This is especially true for circuits with high loop-gains, like voltage followers. The amplifier's output impedance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded and oscillation may occur.

The MAX463–MAX470 phase margin and capacitive-load driving performance are optimized by internal compensation. When driving capacitive loads greater than 50pF, connect an isolation resistor between the amplifier output and the capacitive load, as shown in Figure 3.

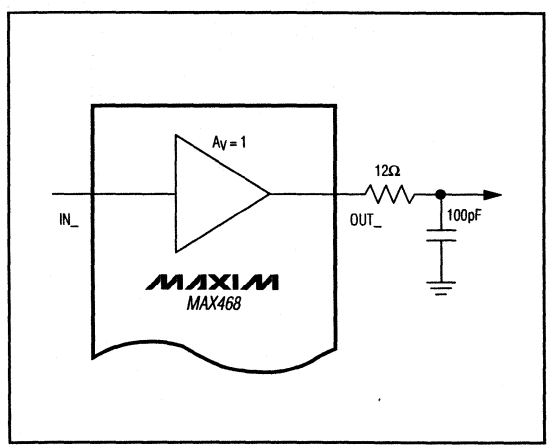


Figure 3a. Using an Isolation Resistor with a Capacitive Load

Two-Channel, Triple/Quad RGB Video Switches and Buffers

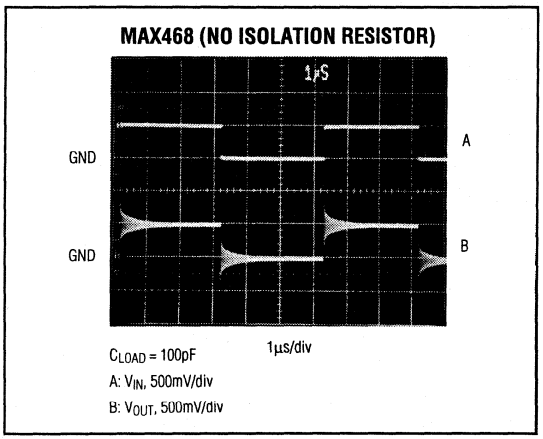


Figure 3b. Step Response without an Isolation Resistor

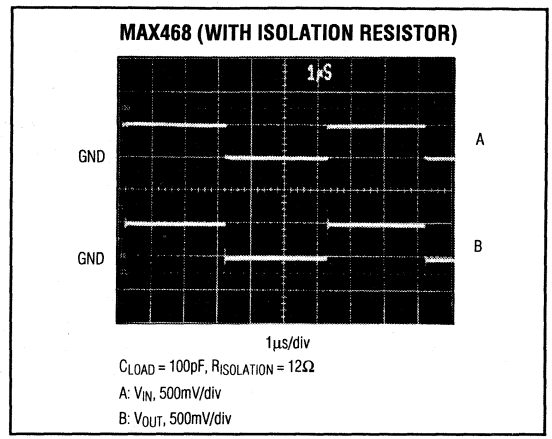


Figure 3c. Step Response with an Isolation Resistor

Digital Interface

The MAX463–MAX466 multiplexer architecture provides an input transistor buffer, ensuring that no input channels are ever connected together. Select a channel by changing A0's state (A0 = 0 for channel A, and A0 = 1 for channel B) and pulsing $\overline{CS}$ low (see Tables 1a, 1b). Figure 4 shows the logic timing diagram.

Output Disable (MAX463–MAX466)

When the enable input ($\overline{EN}$) is driven to a TTL low state, it enables the MAX463–MAX466 amplifier outputs. When $\overline{EN}$ is driven high, it disables the amplifier outputs. The disabled MAX463/MAX464 outputs exhibit a 250kΩ typical resistance. Because their internal feedback resistors are required to produce a gain of two, the MAX465/MAX466 exhibit a 1kΩ disabled output resistance.

LE determines whether $\overline{EN}$ is latched by $\overline{CS}$ or operates independently. When the latch-enable input (LE) is connected to V+, $\overline{CS}$ becomes the latch control for the $\overline{EN}$ input register. If $\overline{CS}$ is low, both the $\overline{EN}$ and A0 registers are transparent; once $\overline{CS}$ returns high, both registers are latched.

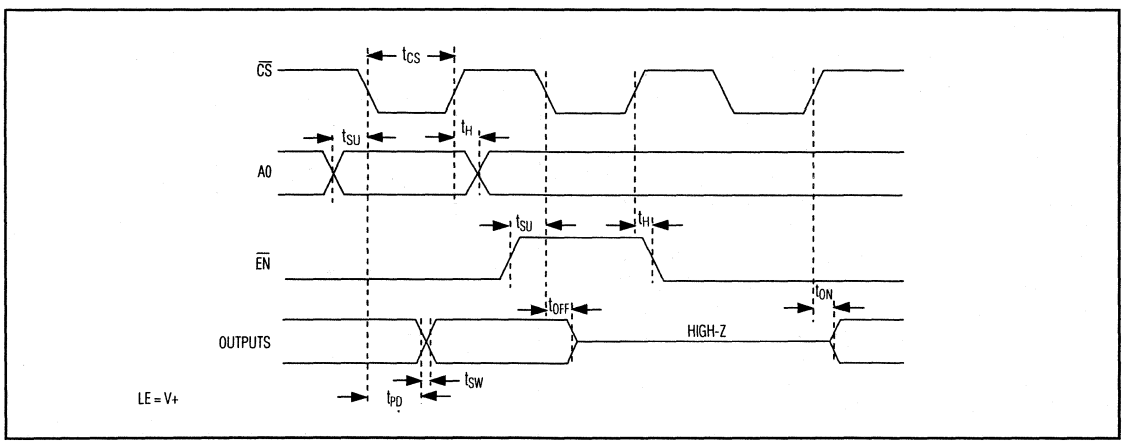


Figure 4. Logic Timing Diagram

Table 1a. Amplifier and Channel Selection with LE = V+

$\overline{CS}$	$\overline{EN}$	A0	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
0	0	1	Enables amplifier outputs. Selects channel B.
0	1	X	Disables amplifiers. Outputs high-Z.
1	X	X	Latches all input registers. Changes nothing.

Table 1b. Amplifier and Channel Selection with LE = GND

$\overline{CS}$	$\overline{EN}$	A0	FUNCTION
0	0	0	Enables amplifier outputs. Selects channel A.
0	0	1	Enables amplifier outputs. Selects channel B.
0	1	0	Disables amplifiers. Outputs high-Z. A0 register = channel A
0	1	1	Disables amplifiers. Outputs high-Z. A0 register = channel B
1	0	X	Enables amplifier outputs, latches A0 register, programs outputs to output A or B, according to the setting of A0 at $\overline{CS}$'s last edge.
1	1	X	Disables amplifiers. Outputs high-Z.

When LE is connected to ground, the $\overline{EN}$ register is transparent and independent of $\overline{CS}$ activity. This allows all MAX463–MAX466 devices to be simultaneously shut down, regardless of the $\overline{CS}$ input state. Simply connect LE to ground and connect all $\overline{EN}$ inputs together (Figure 5a). For the MAX464 and MAX466, LE must be hard-wired to either V+ or ground (rather than driving LE with a gate) to prevent crosstalk from the digital inputs to IN0A.

Another option for output disable is to connect LE to V+, parallel the outputs of several MAX463-MAX466s, and use $\overline{EN}$ to individually disable all devices but the one in use (Figure 5b).

When the outputs are disabled, the off isolation from the analog inputs to the amplifier outputs is typically 70dB at 10MHz, all inputs driven with a 4V$_{P-P}$ sine wave and a 150Ω load impedance. Figure 6 shows the test circuits used to measure isolation and crosstalk.

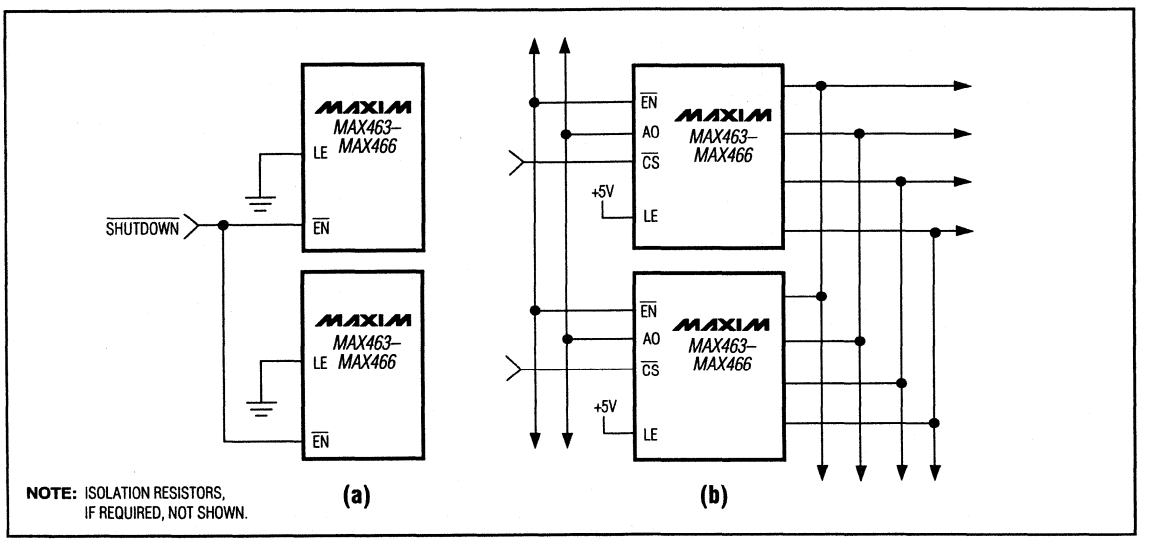


Figure 5. (a) Simultaneous Shutdown of all MAX463–MAX466, (b) Enable ($\overline{EN}$) Register Latched by $\overline{CS}$

Two-Channel, Triple/Quad RGB Video Switches and Buffers

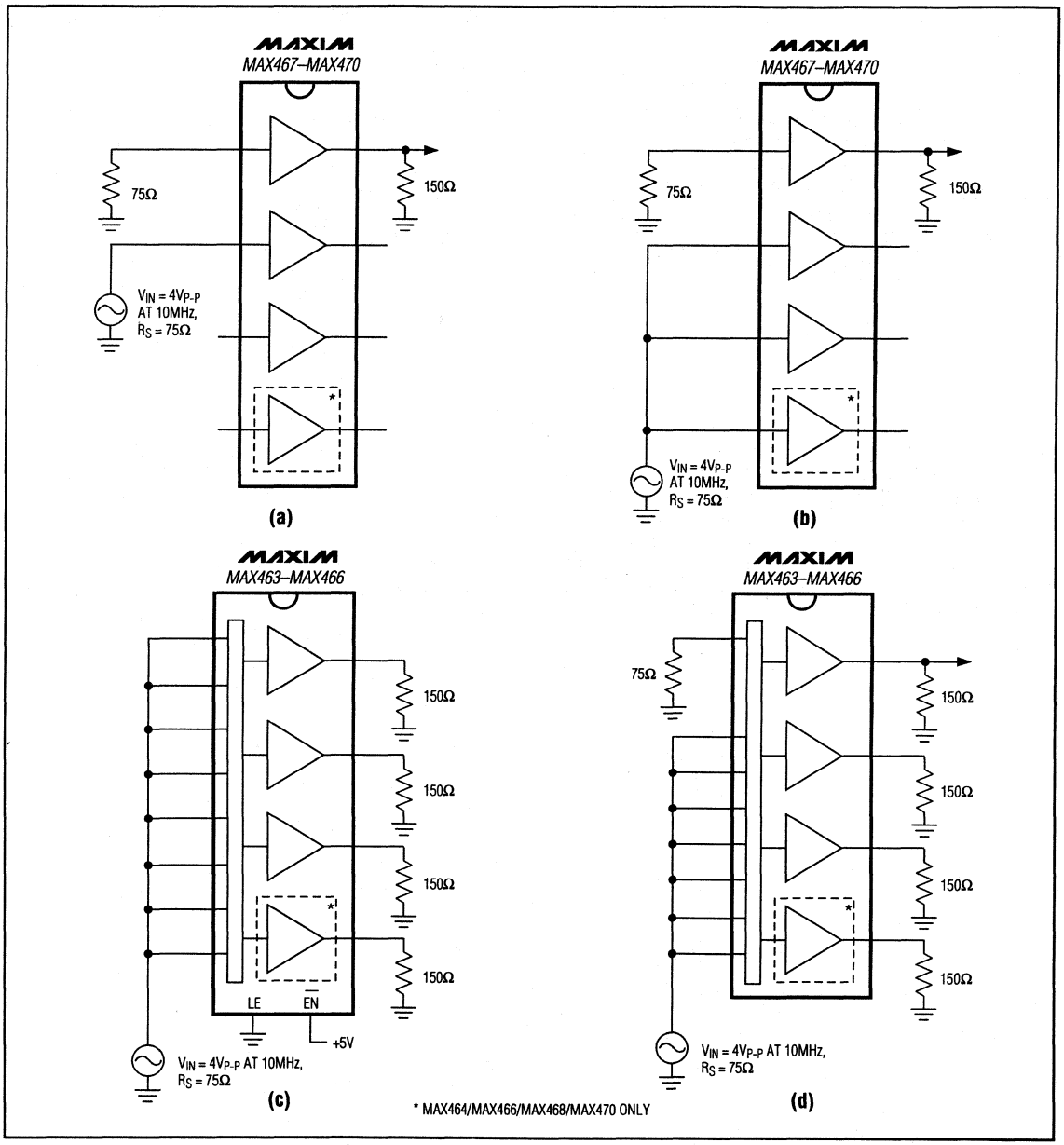


Figure 6. (a) MAX467–MAX470 Adjacent Channel Crosstalk, (b) MAX467–MAX470 All-Hostile Crosstalk, (c) MAX463–MAX466 All-Hostile Off Isolation, (d) MAX463–MAX466 All-Hostile Crosstalk

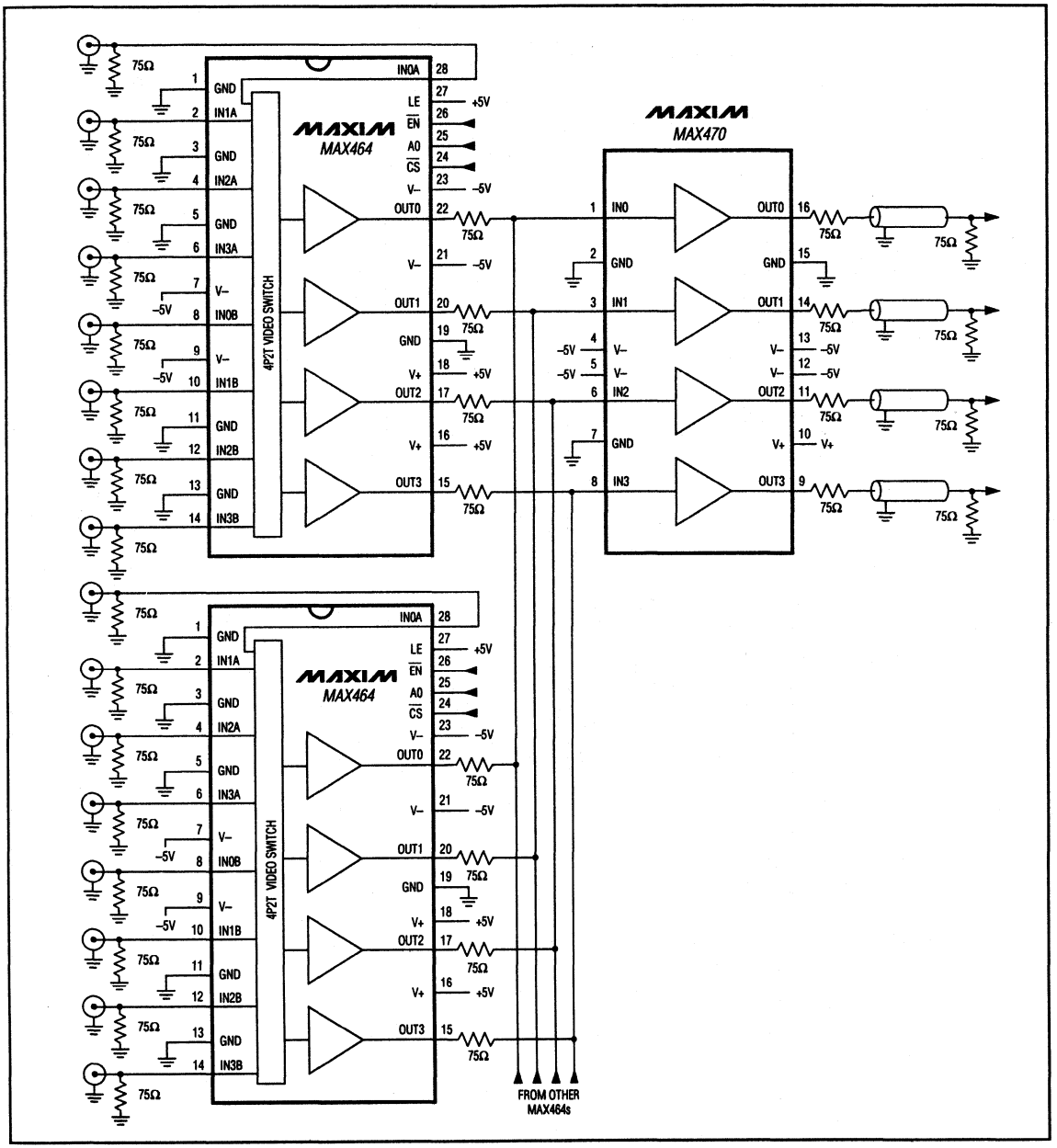


Figure 7. Higher-Order RGB + Sync Video Multiplexer

Two-Channel, Triple/Quad RGB Video Switches and Buffers

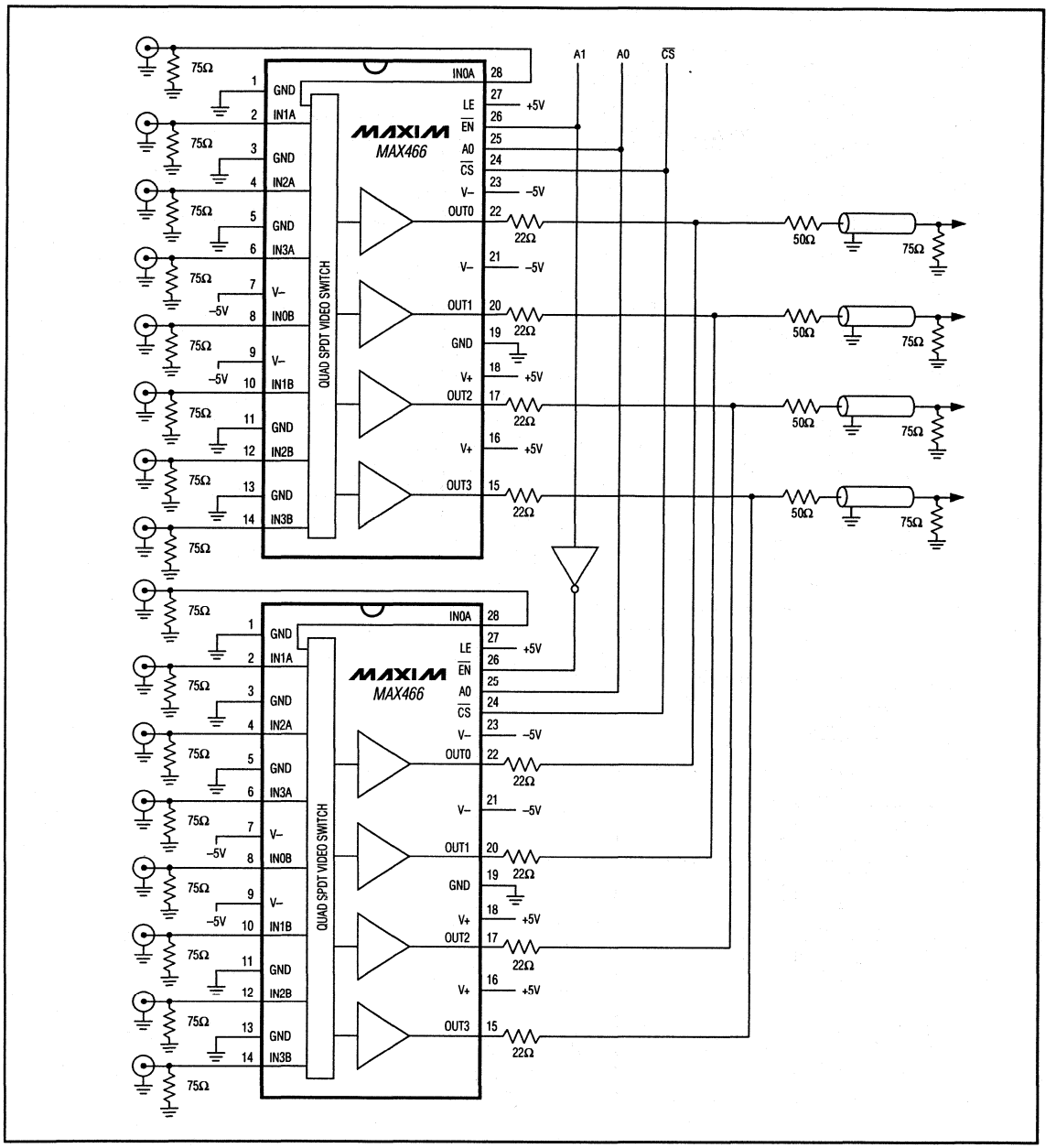


Figure 8. 1-of-4 RGB + Sync Video Multiplexer

Two-Channel, Triple/Quad RGB Video Switches and Buffers

Applications Information

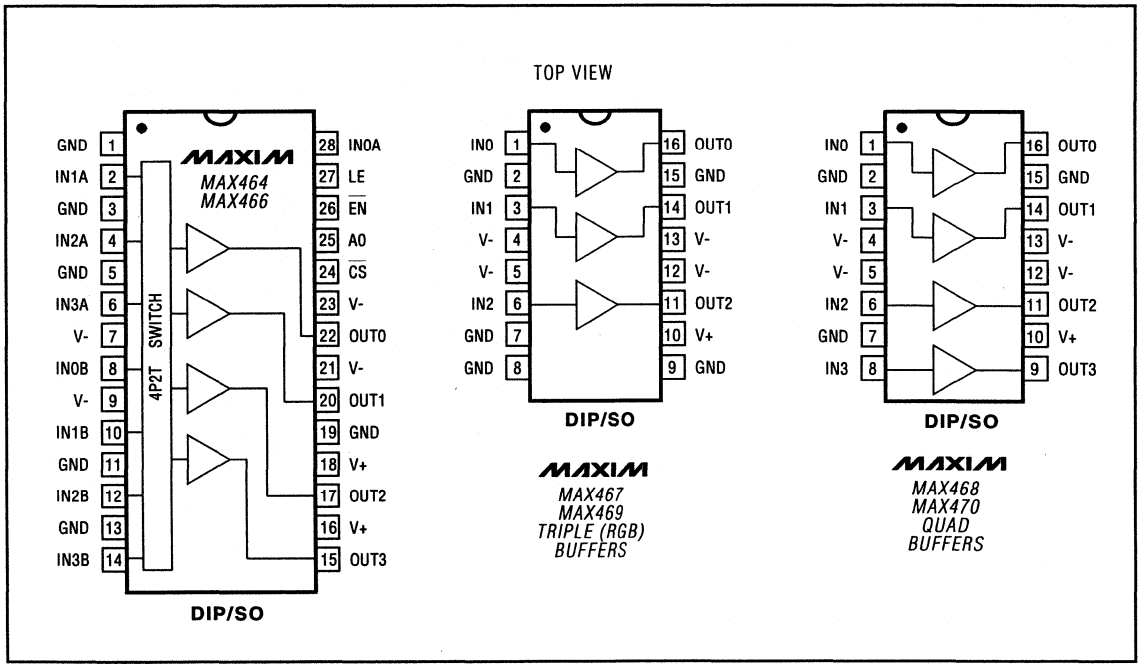
Higher-Order RGB + Sync Video Multiplexing

Higher-order RGB video multiplexers can be realized by paralleling several MAX463/MAX464s. Connect LE to V+ and use $\overline{CS}$ and $\overline{EN}$ to disable all devices but the one in use. Since the disabled output resistance of the MAX463/MAX464 is 250kΩ, several devices may be paralleled to form larger RGB video multiplexer arrays without signal degradation. Connect series resistors at each amplifier's output to isolate the disabled output capacitance of each paralleled device, and use a MAX469 or MAX470 to drive the output coaxial cables (see Figure 7).

Paralleling MAX466s to Switch 1-of-4 RGB + Sync Signal Inputs

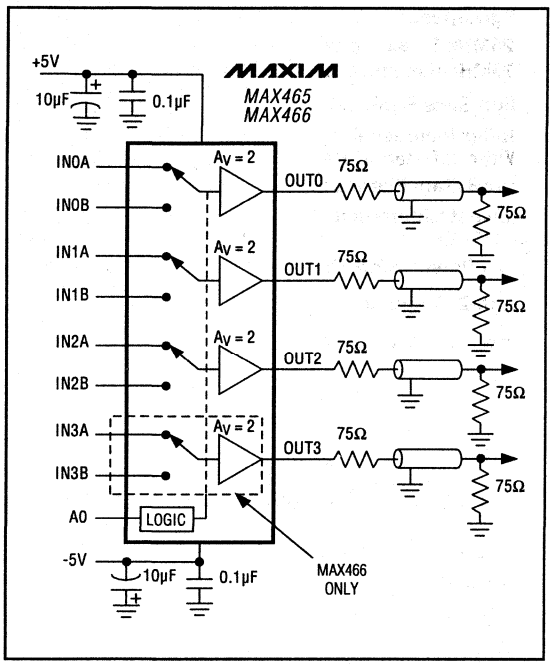
Figure 8 shows a 1-of-4 RGB + sync video mux/amp circuit. The 1kΩ disabled output resistance limits the number of paralleled MAX465/MAX466s to no more than two. The amplifier outputs are connected after a 22Ω isolation resistor and ahead of a 50Ω back-termination resistor, which isolates the active amplifier output from the capacitive load (5pF typ) presented by the inactive output of the second MAX466. Impedance mismatching is minimal, and the signal gain at the cable end is near 1. This minimizes ringing in the output signals. For multiplexing more than two devices, see the section *Higher Order RGB + Sync Video Multiplexing*, above.

Pin Configurations (continued)



Two-Channel, Triple/Quad RGB Video Switches and Buffers

Typical Operating Circuit



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX464CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX464CWI	0°C to +70°C	28 Wide SO
MAX464C/D	0°C to +70°C	Dice*
MAX464ENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX464EWI	-40°C to +85°C	28 Wide SO
MAX465CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX465CWG	0°C to +70°C	24 Wide SO
MAX465C/D	0°C to +70°C	Dice*
MAX465ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX465EWG	-40°C to +85°C	24 Wide SO
MAX466CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX466CWI	0°C to +70°C	28 Wide SO
MAX466C/D	0°C to +70°C	Dice*
MAX466ENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX466EWI	-40°C to +85°C	28 Wide SO
MAX467CPE	0°C to +70°C	16 Plastic DIP
MAX467CWE	0°C to +70°C	16 Wide SO
MAX467C/D	0°C to +70°C	Dice*
MAX467EPE	-40°C to +85°C	16 Plastic DIP
MAX467EWE	-40°C to +85°C	16 Wide SO
MAX468CPE	0°C to +70°C	16 Plastic DIP
MAX468CWE	0°C to +70°C	16 Wide SO
MAX468C/D	0°C to +70°C	Dice*
MAX468EPE	-40°C to +85°C	16 Plastic DIP
MAX468EWE	-40°C to +85°C	16 Wide SO
MAX469CPE	0°C to +70°C	16 Plastic DIP
MAX469CWE	0°C to +70°C	16 Wide SO
MAX469C/D	0°C to +70°C	Dice*
MAX469EPE	-40°C to +85°C	16 Plastic DIP
MAX469EWE	-40°C to +85°C	16 Wide SO
MAX470CPE	0°C to +70°C	16 Plastic DIP
MAX470CWE	0°C to +70°C	16 Wide SO
MAX470C/D	0°C to +70°C	Dice*
MAX470EPE	-40°C to +85°C	16 Plastic DIP
MAX470EWE	-40°C to +85°C	16 Wide SO

** Dice are specified at T_A = +25°C, DC parameters only.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

425MHz High-Speed Amplifier and Buffer

General Description

The MAX476/MAX477 are wide-bandwidth, fast-settling unity-gain-stable devices featuring low differential gain and phase error, high slew rate, high precision, and high output current capability. The MAX476 is an open-loop operational amplifier that is user-configurable to any gain setting possible, as with general-purpose amplifiers (unlike current-mode amplifiers). The MAX477 is a buffer whose programmable gain (+1/+2/-1) is set by pin selection, without external resistors.

The MAX476/MAX477 feature the high slew rate and low power of current-feedback amplifiers. However, unlike a conventional current-feedback design, the MAX476/MAX477 have a unique input structure that combines the benefits of voltage-feedback design (flexibility in choice of feedback resistor, two high-impedance inputs) with the benefits of current-feedback design. They also have the precision of voltage-feedback amplifiers, boasting low offset voltage, low bias currents, and high common-mode and power-supply rejection.

These devices incorporate a high-speed shutdown mode that can be used to disable the output in multiplexer applications and to conserve power. The MAX476/MAX477 are available in 8-pin DIP and SO packages.

Applications

Broadcast and High-Definition TV Systems

Video Switching and Routing

Communications

Medical Imaging

Precision DAC/ADC Buffer

Features

- **High-Speed:**
  425MHz Small-Signal Bandwidth (A_V = +1)
  175MHz Full-Power Bandwidth (A_V = +1, V_O = $4V_{p-p}$)
- **High Slew Rate: 2200V/µs**
- **Buffer Includes Programmable Gain: +1, -1, +2 Without External Resistors**
- **0.1dB Gain Flatness to 30MHz**
- **Lowest Differential Phase/Gain Error: 0.01° DP, 0.01% DG.**
- **Low Power: 9mA Quiescent, 300µA Shutdown**
- **High-Z Output in Shutdown Mode**
- **Low Input Bias Current: 2µA (both inputs)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX476CPA	0°C to +70°C	8 Plastic DIP
MAX476CSA	0°C to +70°C	8 SO
MAX476C/D	0°C to +70°C	Dice*
MAX476EPA	-40°C to +85°C	8 Plastic DIP
MAX476ESA	-40°C to +85°C	8 SO
MAX476MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on next page.

** Dice are tested at T_A = +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

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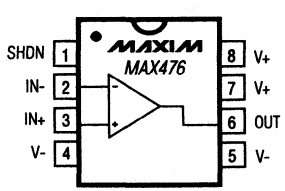
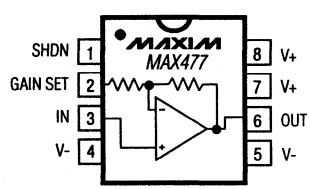
Pin Configurations

TOP VIEW



DIP/SO



DIP/SO

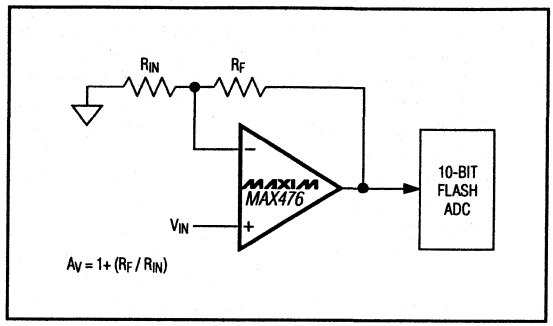
425MHz High-Speed Amplifier and Buffer

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX477CPA	0°C to +70°C	8 Plastic DIP
MAX477CSA	0°C to +70°C	8 SO
MAX477C/D	0°C to +70°C	Dice*
MAX477EPA	-40°C to +85°C	8 Plastic DIP
MAX477ESA	-40°C to +85°C	8 SO
MAX477MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

_____Typical Operating Circuit



D/A Converters

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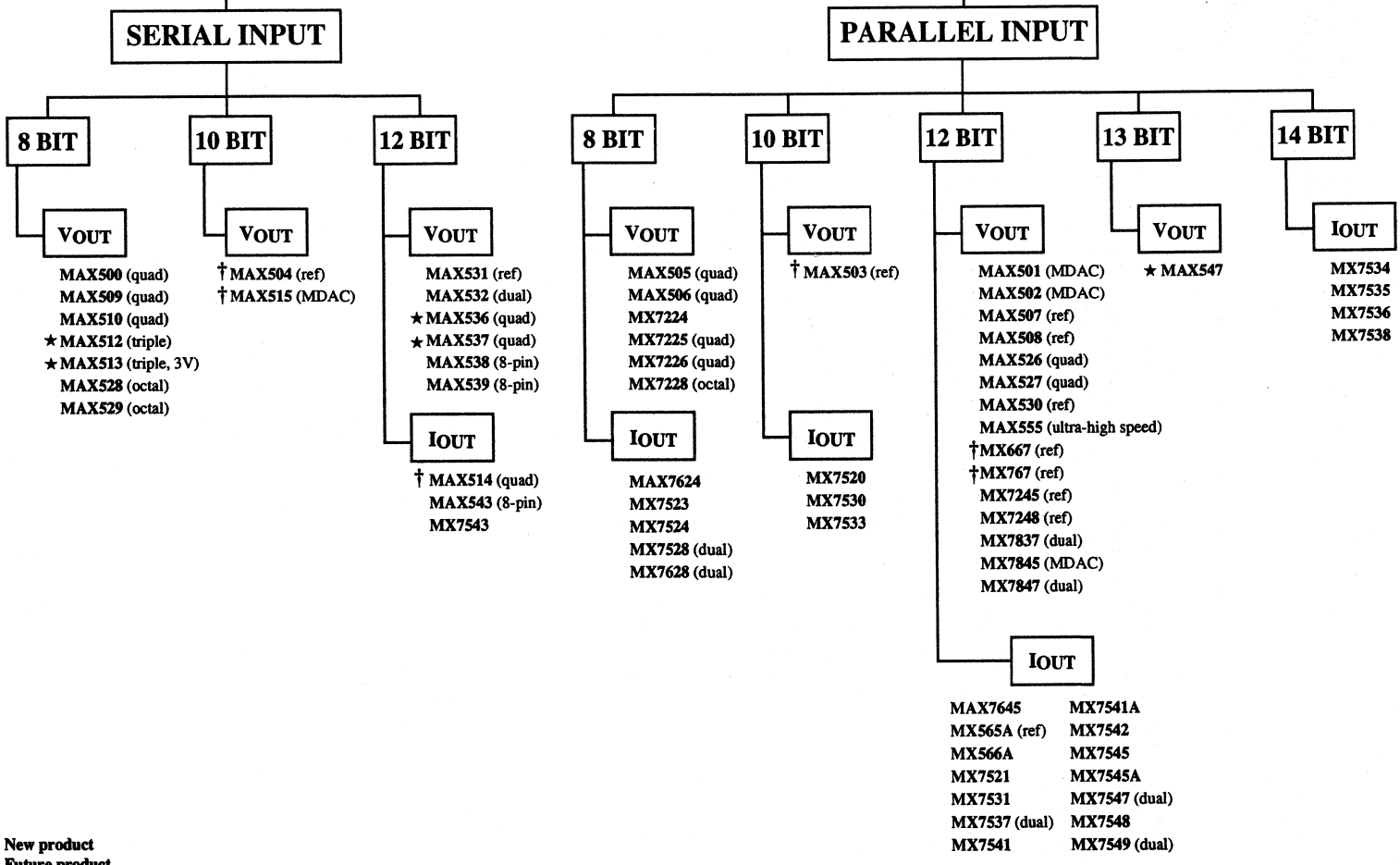
*Advance Information–first page of data sheet in preparation.

D/A CONVERTERS



★ New product
† Future product

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MX7224	8	V	5.0	Ext	µP/8	+12 to +15 & -5	Single or dual supplies	3.16
MX7523	8	I	0.15	MDAC	Logic	+15	Low-cost 8-bit DAC	2.60
MAX7624	8	I	0.25	MDAC	µP/8	+12 to +15	Improved MX7524	2.26
MX7524	8	I	0.4	MDAC	µP/8	+5 to +15	Low-cost 8-bit DAC	2.52
MAX503	10	V	25.0	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, complete DAC	††
MAX504	10	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX503	††
MAX515	10	V	25.0	Ext	Serial	+5	Ultra-low power, 8-pin SO/DIP	††
MX7520	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	0.6	MDAC	Logic	+15	Low-cost 10-bit DAC	2.84
MAX555	12	V	0.5ns	Ext/MDAC	Parallel	-5.2	250Msps update rate, 72dB SFDR	††
MX667	12	V	3.0	Int	µP/4 or 8	±12 to ±15	Compatible with 4- or 8-bit bus	††
MX767	12	V	3.0	Int	µP/12	±12 to ±15	12-bit bus, fast logic interface	††
MAX501	12	V	5.0	MDAC	µP/8	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	5.0	MDAC	µP/12	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	5.0	Int	µP/12	±12 to ±15	Complete 12-bit DAC with reference	7.65
MAX508	12	V	5.0	Int	µP/8	±12 to ±15	Complete 12-bit DAC with reference	7.65
MX7845	12	V	5.0	MDAC	µP/12	±15	4-range 4-quadrant multiplying DAC	6.26
MX7245	12	V	10.0	Int	µP/12	±15 or +12 to +15	Single or dual supplies with reference	8.33
MX7248	12	V	10.0	Int	µP/8	±15 or +12 to +15	8-bit interface MX7245	8.33
MAX530	12	V	25.0	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX531	12	V	25.0	Int/MDAC	Serial	+5 or ±5	Serial version of MAX530	5.45
MAX538	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	25.0	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MX565A	12	I	0.25	Int	Logic	±15	Has +10V buried-zener reference	9.68
MX566A	12	I	0.35	Ext	Logic	-15	No built-in reference	9.04
MX7521	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541A	12	I	0.6	MDAC	Logic	+15	12-bit data bus	5.72
MAX543	12	I	1.0	MDAC	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	5.45
MX7541	12	I	1.0	MDAC	Logic	+15	12-bit data bus	5.07
MX7545A	12	I	1.0	MDAC	µP/12	+5 to +15	Improved MX7545	6.03
MX7548	12	I	1.0	MDAC	µP/8	+5 to +15	8-bit data bus with latches	6.06
MAX7645	12	I	1.0	MDAC	µP/12	+15	Improved MX7545	5.60
MX7542	12	I	2.0	MDAC	µP/4	+5	4-bit data bus with latches	7.52
MX7543	12	I	2.0	MDAC	Serial	+5	12-bit multiplying DAC	7.52
MX7545	12	I	2.0	MDAC	µP/12	+5 to +15	12-bit data bus with latches	5.00
MX7534	14	I	1.5	MDAC	µP/8	+12 to +15	Double-buffered inputs	13.37
MX7535	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	Double-buffered inputs	15.00
MX7536	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	No external resistors needed	14.66
MX7538	14	I	1.5	MDAC	µP/14	+12 to +15	Low-cost 14-bit DAC	8.88

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Multiple D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
DUAL								
MX7528	8	I	0.18	MDAC	µP/8	+5 to +15	Data latches for both DACs	3.79
MX7628	8	I	0.35	MDAC	µP/8	+12 to +15	Data latches for both DACs	3.80
MAX532	12	V	4.0	MDAC	Serial	±12 to ±15	16-pin DIP/SO	8.45
MX7837	12	V	4.0	Ext	µP/8	±12 to ±15	Dual V_{OUT} DAC with 8-bit data bus	12.18
MX7847	12	V	4.0	Ext	µP/12	±12 to ±15	Dual V_{OUT} DAC with 12-bit data bus	12.18
MX7537	12	I	1.5	MDAC	µP/8	+12 to +15	Dual DAC with 8-bit data bus	11.23
MX7547	12	I	1.5	MDAC	µP/12	+12 to +15	Dual DAC with 12-bit data bus	11.40
MX7549	12	I	1.5	MDAC	µP/4	+15	Dual DAC with 4-bit data bus	12.97
TRIPLE								
MAX512	8	V	60.0	MDAC	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.58
MAX513	8	V	70.0	MDAC	Serial	+2.7 to ±3.6	MAX512 for 3V systems	2.58
QUAD								
MAX500	8	V	4.0	Ext	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MX7225	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Double buffered, separate reference inputs	14.14
MX7226	8	V	4.0	Ext	µP/8	+12 to +15 & -5	Single buffered, single reference input	11.80
MAX505	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to rail outputs, separate reference inputs	5.95
MAX506	8	V	6.0	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, single reference input	6.10
MAX509	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	6.0	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX526	12	V	3.0	Ext	µP/8	+12 to +15 & -5	Quad voltage-output DACs, available in DIP/SO	19.44
MAX527	12	V	3.0	Ext	µP/8	±5	±5V version of MAX526	16.56
MAX536	12	V	3.0	Ext	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	3.0	Ext	Serial	±5	Serial version of MAX527	15.95
MAX514	12	I	1.0	MDAC	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25
OCTAL								
MAX528	8	V	5.0	Ext	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	5.0	Ext	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MX7228	8	V	5.0	Ext	µP/8	+5 to +15 & -5 or +15	Single or dual supplies	24.57
MAX547	13	V	5.0	Ext	µP/13	±5	Unipolar or bipolar	29.60

* V = voltage, I = current

** MDAC= 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX500	8	V	4	Ext	4.0	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MAX509	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	4	MDAC	6.0	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX512	8	V	3	MDAC	60.0	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.58
MAX513	8	V	3	MDAC	70.0	Serial	+2.7 to ± 3.6	MAX512 for 3V systems	2.58
MAX528	8	V	8	Ext	5.0	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5.0	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MAX504	10	V	1	Int/MDAC	25.0	Serial	+5 or ±5	Ultra-low power, rail-to-rail	††
MAX515	10	V	1	Ext	25.0	Serial	+5	Ultra-low power, 8-pin SO/DIP	††
MAX531	12	V	1	Int/MDAC	25.0	Serial	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX538	12	V	1	Ext	25.0	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	1	Ext	25.0	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MAX532	12	V	2	MDAC	4.0	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX536	12	V	4	Ext	3.0	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	4	Ext	3.0	Serial	±5	Serial version of MAX527	15.95
MAX543	12	I	1	MDAC	1.0	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	5.45
MX7543	12	I	1	MDAC	2.0	Serial	+5	12-bit multiplying DAC	7.52
MAX514	12	I	4	MDAC	1.0	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

19-0252; Rev 0; 4/94

MAXIM

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX512/MAX513 contain three 8-bit, voltage-output digital-to-analog converters (DAC A, DAC B, and DAC C). Output buffer amplifiers for DACs A and B provide voltage outputs while reducing external component count. The output buffer for DAC A can source or sink 5mA to within 0.5V of V_{DD} or V_{SS}. The buffer for DAC B can source or sink 0.5mA to within 0.5V of V_{DD} or V_{SS}. DAC C is unbuffered, providing a third voltage output with increased accuracy. The MAX512 operates with a single +5V ±10% supply, and the MAX513 operates with a +2.7V to +3.6V supply. Both devices can also operate with split supplies.

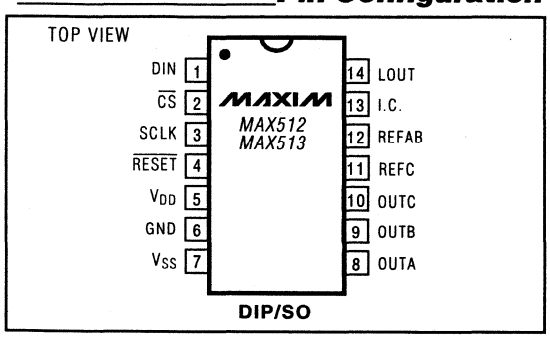
The 3-wire serial interface has a maximum operating frequency of 5MHz and is compatible with SPI™, QSPI™, and Microwire™. The serial input shift register is 16 bits long and consists of 8 bits of DAC input data and 8 bits for DAC selection and shutdown. DAC registers can be loaded independently or in parallel at the positive edge of $\overline{CS}$. A latched logic output is also available for auxiliary control.

Ultra-low power consumption and small packages (14-pin DIP/SO) make the MAX512/MAX513 ideal for portable and battery-powered applications. Supply current is only 1mA, dropping to less than 1µA in shutdown. Any of the three DACs can be independently shut down. In shutdown mode, the DAC's R-2R ladder network is disconnected from the reference input, minimizing system power consumption.

Applications

Digital Gain and Offset Adjustment
Programmable Attenuators
Programmable Current Sources
Programmable Voltage Sources
RF Digitally Adjustable Bias Circuits
VCO Tuning

Pin Configuration



Features

- ♦ **Operate from a Single +5V (MAX512) or +3V (MAX513) Supply, or from Bipolar Supplies**
- ♦ **Low Power Consumption**
  1mA Operating Current
  <1µA Shutdown Current
- ♦ **Unipolar or Bipolar Outputs**
- ♦ **5MHz, 3-Wire Serial Interface**
- ♦ **SPI, QSPI, and Microwire Compatible**
- ♦ **Two Buffered, Bipolar-Output DACs (DACs A/B)**
- ♦ **Independently Programmable Shutdown Mode**
- ♦ **Space-Saving 14-Pin SO/DIP Packages**
- ♦ **Pin and Software Reset**

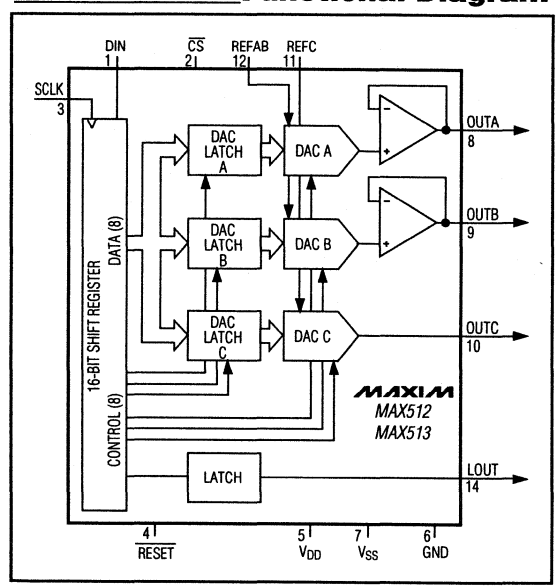
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX512CPD	0°C to +70°C	14 Plastic DIP
MAX512CSD	0°C to +70°C	14 SO
MAX512C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

* *Contact factory for dice specifications.*

Functional Diagram



™ *Microwire is a trademark of National Semiconductor Corp. SPI and QSPI are trademarks of Motorola Inc.*

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +6V
V_{SS} to GND ..... -6V, +0.3V
V_{DD} to V_{SS} ..... -0.3V, +12V
Digital Inputs and Outputs to GND ..... -0.3V, (V_{DD} + 0.3V)
REFAB ..... (V_{SS} - 0.3V), (V_{DD} + 0.3V)
OUTA, OUTB (Note 1) ..... V_{SS}, V_{DD}
OUTC ..... -0.3V, (V_{DD} + 0.3V)
REFC ..... -0.3V, (V_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.33mW/°C above +70°C) 667mW
CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges
MAX51_C_ _ ..... 0°C to +70°C
MAX51_E_ _ ..... -40°C to +85°C
MAX51_MJD ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The outputs may be shorted to V_{DD}, V_{SS}, or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Integral Nonlinearity	INL	DAC A/B (Note 2)			±1.5	LSB
		DAC C			±1	
Total Unadjusted Error	TUE	(Note 2)		±1		LSB
Zero-Code Temperature Coefficient		DAC A/B		100		µV/°C
		DAC C		5		
Power-Supply Rejection Ratio	PSRR	MAX512, 4.5V ≤ V_{DD} ≤ 5.5V, REFAB = REFC = 4.096V		0.01		%/%
		MAX513, 2.7V ≤ V_{DD} ≤ 3.6V, REFAB = REFC = 2.4V		0.015		
REFERENCE INPUTS						
Reference Input Voltage Range		REFAB	V_{SS}		V_{DD}	V
		REFC	GND		V_{DD}	
Reference Input Capacitance				25		pF
Reference Input Resistance	R_{REF}	REFAB (Note 3)	8			kΩ
		REFC (Note 3)	12			
Reference Input Resistance (shutdown mode)		REFAB, REFC		2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, REFAB = REFC = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC OUTPUTS							
Output Voltage Range				0		REF_	V
Capacitive Load		DAC A		0.05			µF
		DAC B		0.01			
		DAC C		0			
Output Resistance		DAC A			0.050		kΩ
		DAC B			0.500		
		DAC C			24		
DIGITAL INPUTS							
Input High Voltage	V_{IH}			(0.7)(V_{DD})			V
Input Low Voltage	V_{IL}					(0.3)(V_{DD})	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			0.1	±10	µA
Input Capacitance	C_{IN}	(Notes 4, 5)				10	pF
DIGITAL OUTPUT							
Output High Voltage	V_{OH}	I_{SOURCE} ≤ 1.6mA		V_{DD} - 0.4			V
Output Low Voltage	V_{OL}	I_{SINK} ≤ 1.6mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	C_L = 0.1µF (DAC A), C_L = 0.01µF (DAC B)			0.1		V/µs
Voltage-Output Settling Time		To ±½LSB	C_L = 0.1µF (DAC A)		70		µs
			C_L = 0.01µF (DAC B)		70		
			C_L = 0.1nF (DAC C)		35		
Digital Feedthrough and Crosstalk		All 0s to all 1s			10		nV-s
POWER SUPPLIES							
Positive Supply Voltage Range	V_{DD}	MAX512		4.5		5.5	V
		MAX513		2.7		3.6	
Negative Supply Voltage Range (Note 6)	V_{SS}	MAX512		-5.5		-4.5	V
		MAX513		-3.6		-2.7	
Positive Supply Current	I_{DD}	All inputs = 0V	MAX512 (V_{DD} = 5.5V)		1.3	2.8	mA
			MAX513 (V_{DD} = 3.6V)		0.9	2.5	
Negative Supply Current	I_{SS}	All inputs = 0V, V_{SS} = -5.5V			-1.3		mA
Shutdown Supply Current					0.1		µA

Note 2: Digital code from 24 through 232 are due to swing limitations of output amplifiers on DAC A and DAC B. See *Typical Operating Characteristics.*

Note 3: Reference input resistance is code dependent. The lowest input resistance occurs at code 55hex. Refer to the reference input section in the *Detailed Description.*

Note 4: Guaranteed by design. Not production tested.

Note 5: Input capacitance is code dependent. The highest capacitance occurs at code 00hex.

Note 6: For single-supply mode, tie V_{SS} to GND.

Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

TIMING CHARACTERISTICS (Note 4)

(V_{DD} = +4.5V to +5.5V for MAX512, V_{DD} = +2.7V to +3.6V for MAX513, V_{SS} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

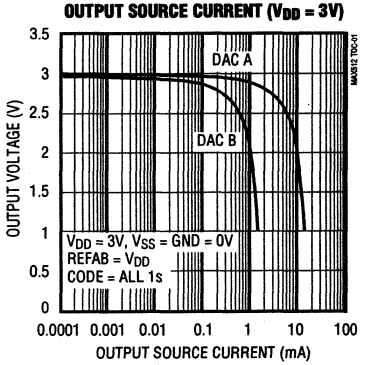
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING						
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		150			ns
SCLK Rise to $\overline{CS}$ Rise Setup Time	t_{CSH}		150			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		50			ns
SCLK Pulse Width High	t_{CH}		100			ns
SCLK Pulse Width Low	t_{CL}		100			ns
Output Delay LOUT	t_{OD}	C_L = 100pF			150	ns
$\overline{CS}$ Pulse Width High	t_{CSPWH}		200			ns

Note 4: Guaranteed by design. Not production tested.

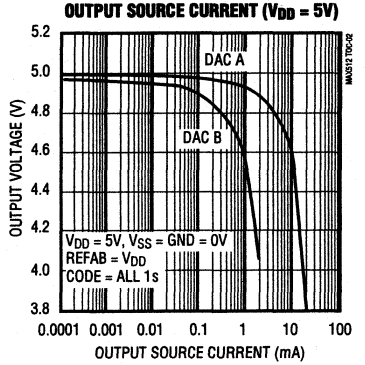
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

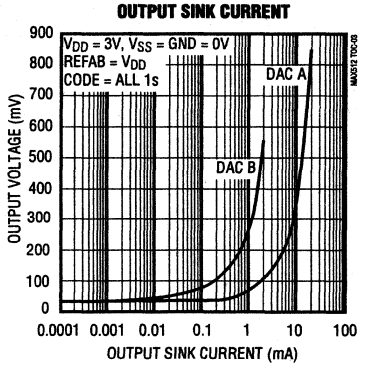
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 3V)



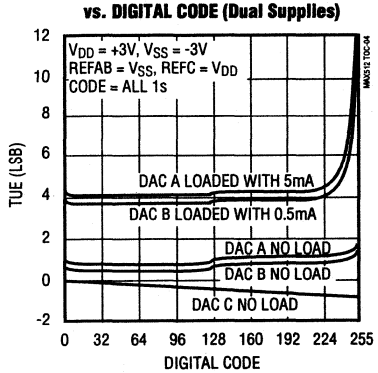
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 5V)



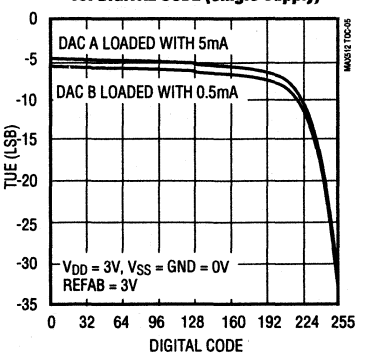
OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



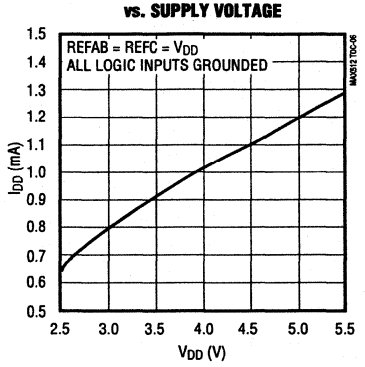
TOTAL UNADJUSTED ERROR vs. DIGITAL CODE (Dual Supplies)



TOTAL UNADJUSTED ERROR vs. DIGITAL CODE (Single Supply)



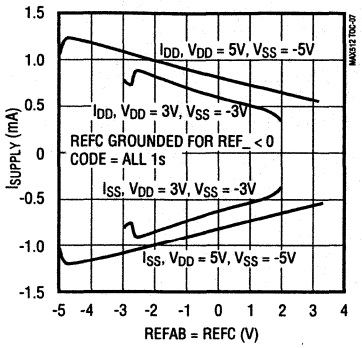
POSITIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



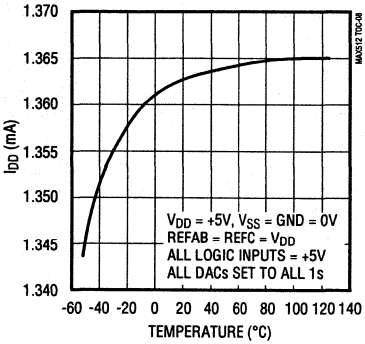
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

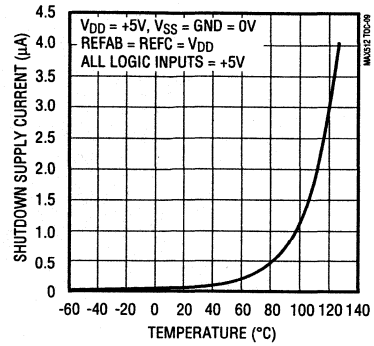
SUPPLY CURRENT vs. REFERENCE VOLTAGE



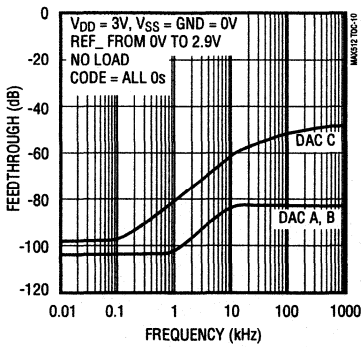
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



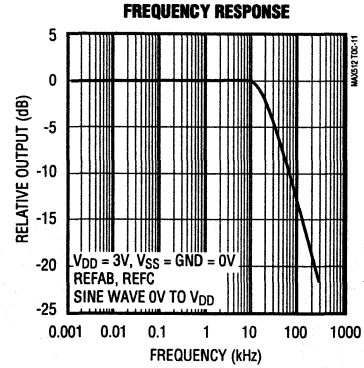
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



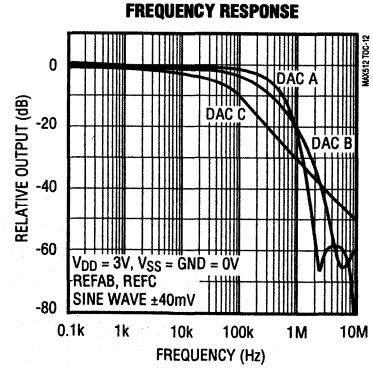
REFERENCE FEEDTHROUGH vs. FREQUENCY



REFERENCE LARGE-SIGNAL FREQUENCY RESPONSE



REFERENCE SMALL-SIGNAL FREQUENCY RESPONSE



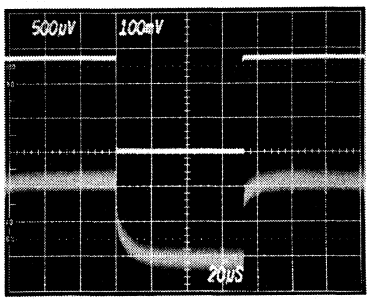
9

Low-Cost, Triple, 8-Bit Voltage Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

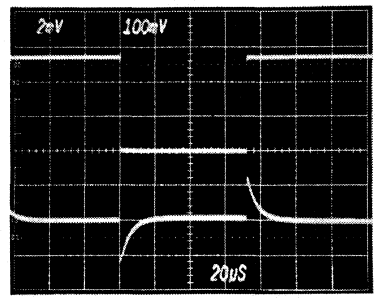
LINE-TRANSIENT RESPONSE (OUTA)



20µs/div

REFAB = 2.56V, NO LOAD, CODE = ALL 1s
A : V_{DD}, 100mV/div
B : OUTA, 500µV/div

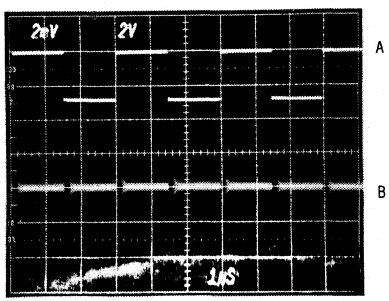
LINE-TRANSIENT RESPONSE (OUTC)



20µs/div

REFC = 2.56V, NO LOAD, CODE = ALL 1s
A : V_{DD}, 100mV/div
B : OUTC, 2mV/div

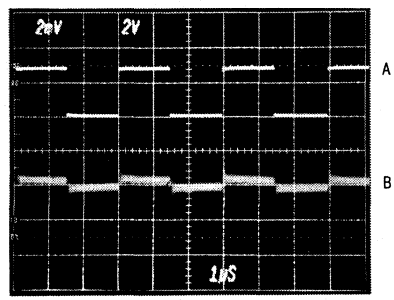
CLOCK FEEDTHROUGH (OUTA)



1µs/div

V_{SS} = 0V, $\overline{CS}$ = HIGH
A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
B: OUTA, 2mV/div

CLOCK FEEDTHROUGH (OUTC)



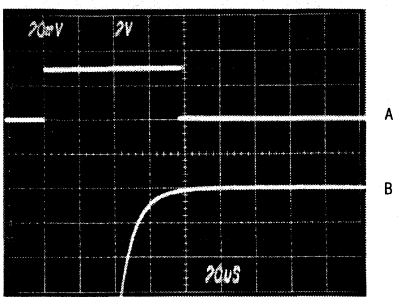
1µs/div

V_{SS} = 0V, $\overline{CS}$ = HIGH
A: SCLK, 333kHz, 0V TO 2.9V, 2V/div
B: OUTC, 2mV/div

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

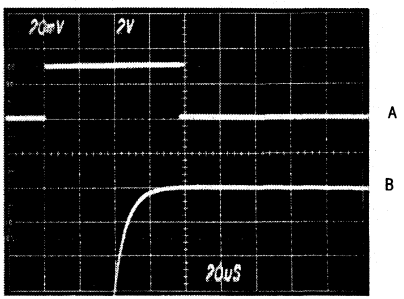
POSITIVE SETTLING TIME (DAC A)



20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1kΩ, C_L = 0.1µF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 2V/div
B: OUTA, 20mV/div

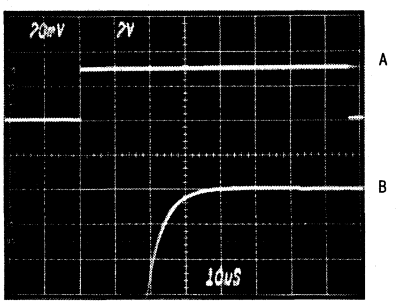
POSITIVE SETTLING TIME (DAC B)



20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 10kΩ, C_L = 0.01µF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 2V/div
B: OUTB, 20mV/div

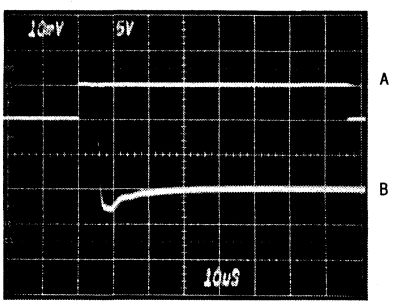
POSITIVE SETTLING TIME (DAC C)



10µs/div

V_{DD} = 3V, V_{SS} = 0V, REFC = V_{DD}, R_L = ∞, C_L = 122pF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 2V/div
B: OUTC, 20mV/div

POSITIVE SETTLING TIME WITH DUAL SUPPLIES



10µs/div

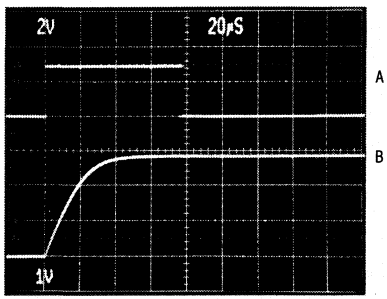
V_{DD} = 5V, V_{SS} = -5V, REFAB = 2.56V, R_L = 1kΩ, C_L = 0.1µF
ALL BITS OFF TO ALL BITS ON
A: $\overline{CS}$, 5V/div
B: OUTA, 10mV/div

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

TIME EXITING SHUTDOWN MODE

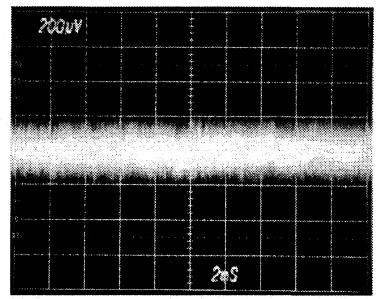


20µs/div

V_{DD} = 3V, V_{SS} = 0V, REFAB = V_{DD}, R_L = 1kΩ, C_L = 0.1µF
DAC LOADED WITH ALL 1s

A: $\overline{CS}$, 2V/div
B: OUTA, 1V/div

OUTPUT VOLTAGE NOISE DC TO 1MHz



OUTA, 200µV/div

2ms/div

DIGITAL CODE = 80, REFAB = V_{DD}, NO LOAD

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial Data Input of the 16-bit shift register. Data is clocked into the register on the rising edge of SCLK.
2	$\overline{CS}$	Chip Select (active low). Enables data to be shifted into the 16-bit shift register. Programming commands are executed at the rising edge of $\overline{CS}$.
3	SCLK	Serial Clock Input. Data is clocked in on the rising edge of SCLK.
4	$\overline{RESET}$	Asynchronous reset input (active low). Clears all registers to their default state (FFhex for DAC A and DAC B registers); all other registers are reset to 0 (including the input shift register).
5	V_{DD}	Positive Power Supply (2.7V to 5.5V). Bypass with 0.22µF to GND.
6	GND	Ground
7	V_{SS}	Negative Power Supply 0V or (-1.5V to -5.5V). Tie to GND for single supply operation. If a negative supply is applied, bypass with 0.22µF to GND.
8	OUTA	DAC A Output Voltage (Buffered). Resets to full scale. **Connect 0.05µF capacitor or greater to GND.**
9	OUTB	DAC B Output Voltage (Buffered). Resets to full scale. **Connect 0.01µF capacitor or greater to GND.**
10	OUTC	DAC C Output Voltage (Unbuffered). Resets to zero.
11	REFC	DAC C Reference Voltage
12	REFAB	DAC A/B Reference Voltage
13	I.C.	Internally connected. Do not make connections to this pin.
14	LOUT	Logic Output (latched)

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Detailed Description

Analog Section

The MAX512/MAX513 contain three 8-bit, voltage-output, digital-to-analog converters (DACs). The DACs are "inverted" R-2R ladder networks using complementary switches that convert 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltages.

The MAX512/MAX513 have two reference inputs: one is shared by DAC A and DAC B and the other is used by DAC C. These inputs allow different full-scale output voltages and different output voltage polarities for the DAC pair A/B and DAC C.

The MAX512/MAX513 include output buffer amplifiers for DACs A and B and input logic for simple microprocessor (µP) and CMOS interfaces.

The MAX512/MAX513 operate in either single-supply or dual-supply mode, as determined by V_{SS}. If V_{SS} is within approximately -0.5V of GND, single-supply mode is assumed. If V_{SS} is below -1.5V, the devices are in dual-supply mode.

Reference Inputs and DAC Output Range

The voltage at REF_ sets the full-scale output of the DACs. The input impedance of the REF_ inputs is code dependent. The lowest value, approximately 12kΩ for REFC (8kΩ for REFAB), occurs when the input code is 01010101 (55hex). The maximum value of infinity occurs when the input code is zero.

In shutdown mode, the selected DAC output is set to zero while the value stored in the DAC register remains unchanged. This removes the load from the reference input to save power. Bringing the MAX512/MAX513 out of shutdown mode restores the DAC output voltage. Because the input resistance at REF_ is code dependent, the DAC's reference sources should have an output impedance of no more than 5Ω. The input capacitance at the REF_ pins is also code dependent and typically does not exceed 25pF.

The reference voltage on REFAB can range anywhere between the supply rails. In dual-supply mode, a positive reference input voltage on REFAB should be less than (V_{DD} - 1.5V) to avoid saturating the buffer amplifiers. The reference voltage includes the negative supply rail. See the *Output Buffer Amplifier* section for more information. The REFC input accepts positive voltages up to V_{DD} and should not be forced below ground.

The absolute difference between any reference voltage and GND should not exceed 6V.

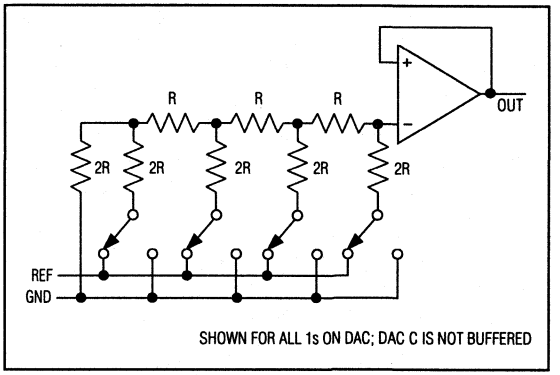


Figure 1. DAC Simplified Circuit Diagram

Output Buffer Amplifiers (DAC A / DAC B)

DAC A and DAC B voltage outputs are internally buffered. The buffer amplifiers have a rail-to-rail (V_{SS} to V_{DD}) output voltage range.

In single-supply mode, the DAC outputs A and B are internally divided by two and the buffer is set to a gain of two, eliminating the need for a buffer input voltage range to the positive supply rail.

In dual-supply mode, the DAC outputs are not attenuated and the buffer is set to unity gain.

Although only necessary for negative output voltages, the dual-supply mode may be used even if the desired DAC output voltage is positive. Possible errors associated with the divide-by-two attenuator and gain-of-two buffers in single-supply mode are eliminated in dual-supply mode. In this case, do not use reference voltages higher than (V_{DD} - 1.5V).

DAC A's output amplifier can source and sink up to 5mA of current (0.5mA for DAC B buffer). See the Total Unadjusted Error vs. Digital Code graph in the *Typical Operating Characteristics* for dual and single supplies. The amplifier is unity-gain stable with a capacitive load of 0.05µF (0.01µF for DAC B buffer) or greater. The slew rate is limited by the load capacitor and is typically 0.1V/µs with a 0.1µF load (0.01µF for DAC B buffer).

Unbuffered Output (DAC C)

The output of DAC C is unbuffered and has a typical output impedance of 24kΩ. It can be used to drive a high-impedance load, such as an op amp or comparator, and has 35µs typical settling time to 1/2LSB with a single 3V supply. Use DAC C if a quick dynamic response is required.

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Shutdown Mode

When programmed to shutdown mode, the outputs of DAC A and B go into a high-impedance state. Virtually no current flows into or out of the buffer amplifiers in that state. The output of DAC C goes to 0V when shut down. In shutdown mode, the REF_ inputs are high impedance (2MΩ typ) to conserve current drain from the system reference; therefore, the system reference does not have to be powered down. The logic output LOUT remains active in shutdown.

Coming out of shutdown, the DAC outputs return to the values kept in the registers. The recovery time is equivalent to the DAC settling time.

Reset

The $\overline{\text{RESET}}$ input is active low. When asserted ($\overline{\text{RESET}}$ = 0), DACs A and B are set to full scale (FFhex) and active, while DAC C is set to zero code (00hex) and active. The 16-bit serial register is cleared to 0000hex. LOUT is reset to zero.

Serial Interface

An active-low chip select ($\overline{\text{CS}}$) enables the shift register to receive data from the serial data input. Data is clocked into the shift register on every rising edge of the serial clock signal (SCLK). The clock frequency can be as high as 5MHz.

Data is sent MSB first and can be transmitted in one 16-bit word. The write cycle can be interrupted at any time when $\overline{\text{CS}}$ is kept active (low) to allow, for example, two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, the rising edge of CS updates the DAC outputs, the shutdown status, and the status of the logic output. Because of their single buffered structure, DACs cannot be simultaneously updated to different digital values.

Table 1. Input Shift Register

DATA BITS	B0*	DAC Data Bit 0 (LSB)
	B1	DAC Data Bit 1
	B2	DAC Data Bit 2
	B3	DAC Data Bit 3
	B4	DAC Data Bit 4
	B5	DAC Data Bit 5
	B6	DAC Data Bit 6
	B7	DAC Data Bit 7 (MSB)
CONTROL BITS	LA	Load Reg DAC A, Active High
	LB	Load Reg DAC B, Active High
	LC	Load Reg DAC C, Active High
	SA	Shut Down DAC A, Active High
	SB	Shut Down DAC B, Active High
	SC	Shut Down DAC C, Active High
	Q1	Logic Output
	Q2**	Uncommitted Bit

* Clocked in last.
**Clocked in first.

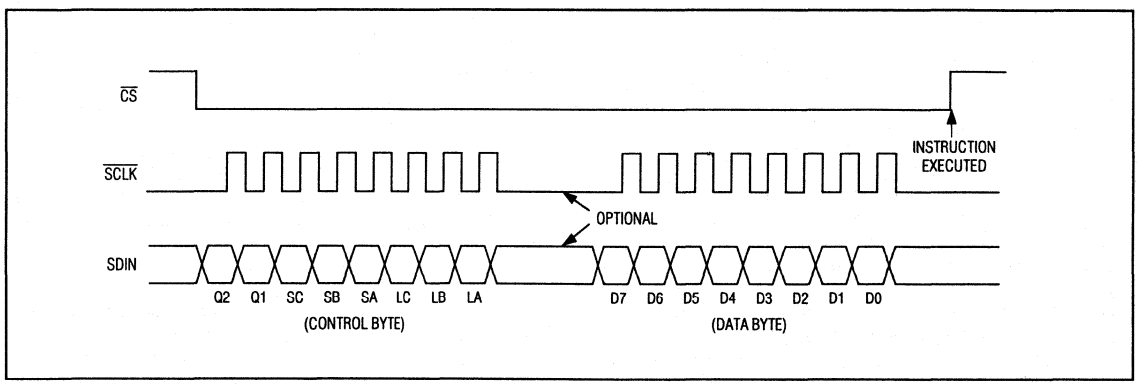


Figure 2. MAX512/MAX513 3-Wire Serial-Interface Timing Diagram

Table 2. Serial-Interface Programming Commands

CONTROL								DATA								FUNCTION
								MSB							LSB	
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0	
*	*	*	*	*	0	0	0	X	X	X	X	X	X	X	X	No Operation to DAC Registers
*	*	*	*	*	1	0	0	8-Bit DAC Data								Load Register to DAC C
*	*	*	*	*	0	1	0	8-Bit DAC Data								Load Register to DAC B
*	*	*	*	*	0	0	1	8-Bit DAC Data								Load Register to DAC A
*	*	*	*	*	1	1	1	8-Bit DAC Data								Load All DAC Registers
*	*	0	0	0	*	*	*	X	X	X	X	X	X	X	X	All DACs Active
*	*	1	0	0	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC C
*	*	0	1	0	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC B
*	*	0	0	1	*	*	*	X	X	X	X	X	X	X	X	Shut Down DAC A
*	*	1	1	1	*	*	*	X	X	X	X	X	X	X	X	Shut Down All DACs
X	0	*	*	*	*	*	*	X	X	X	X	X	X	X	X	Reset LOUT
X	1	*	*	*	*	*	*	X	X	X	X	X	X	X	X	Set LOUT

X *Don't care.*

* *Not shown for clarity. The functions of loading and shutting down the DACs and programming the logic can be combined in a single command.*

Serial-Input Data Format and Control Codes

Table 2 lists the serial-input data format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally. Every control bit performs one function. Data is clocked in starting with Q2 (uncommitted bit), followed by the remaining control bits and the data byte. The LSB of the data byte (B0) is the last bit clocked into the shift register (Figure 2).

Example of a 16-bit input word:

Loaded in First															Loaded in Last
Q2	Q1	SC	SB	SA	LC	LB	LA	B7	B6	B5	B4	B3	B2	B1	B0
X	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

The example above performs the following functions:

- 80hex (128 decimal) loaded into DAC registers A and B.
- Content of the DAC C register remains unchanged.
- DAC A and DAC B are active.
- DAC C is shut down.
- LOUT is reset to 0.

Digital Inputs

The digital inputs are compatible with CMOS logic. Supply current increases slightly when toggling the logic inputs through the transition zone between $(0.3)(V_{DD})$ and $(0.7)(V_{DD})$.

Digital Output

The latched digital output (LOUT) has a 1.6mA source capability while maintaining a (V_{DD} - 0.4V) output level. With a 1.6mA sink current, the output voltage is guaranteed to be no more than 0.4V. The output can be used for digital auxiliary control. Please note that the digital output remains fully active during shutdown mode.

Microprocessor Interfacing

The MAX512/MAX513 serial interface is compatible with Microwire, SPI, and QSPI. For SPI and QSPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the inactive state of clock to zero and CPHA = 0 changes data at the falling edge of SCLK. This setting allows both SPI and QSPI to run at full clock speeds (0.5MHz and 4MHz, respectively). If a serial port is not available on your µP, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the voltage outputs by operating the serial clock only when necessary.

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

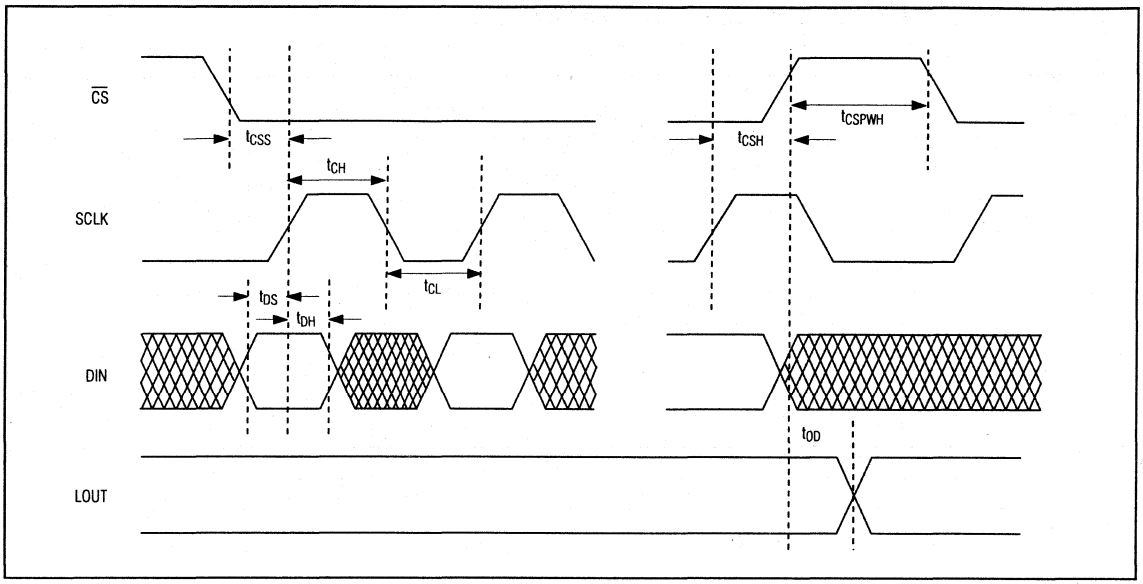


Figure 3. MAX512/MAX513 Detailed Serial-Interface Timing Diagram

Applications Information

Power-Supply and Reference Operating Ranges

The MAX512 is fully specified to operate with V_{DD} = 5V ±10% and V_{SS} = GND = 0V. The MAX513 is specified for single-supply operation with V_{DD} ranging from 2.7V to 3.6V, covering all commonly used supply voltages in 3V systems. The MAX512/MAX513 can also be used with a negative supply ranging from -1.5V to -5.5V. Using a negative supply typically improves zero-code error and settling time (as shown in the *Typical Operating Characteristics* graphs).

The two seperate reference inputs for the DAC pair A/B and the unbuffered output C allow different full-scale output voltages and, if a negative supply is used, also allow different polarity. In dual-supply mode, REFAB can vary from V_{SS} to (V_{DD} - 1.5V). In single-supply mode, the specified range for REFAB is 0V to V_{DD}. REFC can range from GND to V_{DD}. Do not force REFC below ground.

Power-supply sequencing is not critical. If a negative supply is used, make sure V_{SS} is never more than 0.3V above ground. Do not apply signals to the digital inputs until the device is powered-up. If this is not possible, add current-limiting resistors to the digital inputs.

Power-Supply Bypassing and Ground Management

In single-supply operation (V_{SS} = GND), GND and V_{SS} should be connected to the highest quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. For dual-supply operation, bypass V_{SS} with a 0.1µF to 0.22µF capacitor to GND. Reference inputs can be used without bypassing. For optimum line/load-transient response and noise performance, bypass the reference inputs with 0.1µF to 4.7µF to GND. Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Separate analog lines with ground traces between them. Make sure that high-frequency digital lines are not routed in parallel to analog lines.

Unipolar Output

With unipolar output, the output voltage and the reference voltage are the same polarity. The MAX512/MAX513 can be used with a single supply if the reference voltages are positive. With a negative supply, the REFAB voltage can vary from V_{SS} to approximately (V_{DD} - 1.5V), allowing two-quadrant multiplication.

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

Table 3. Unipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+REF\_ \times \left(\frac{128}{256}\right) = +\frac{REF\_}{2}$
0	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note:

$$1LSB = REF\_ \times 2^{-8} = REF\_ \times \left(\frac{1}{256}\right)$$

$$ANALOG\ OUTPUT = REF\_ \times \left(\frac{D}{256}\right)$$

Table 4. Bipolar Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF\_ \times \left(\frac{127}{128}\right)$
1	0	0	0	0	0	0	1	$+REF\_ \times \left(\frac{1}{128}\right)$
0	0	0	0	0	0	0	1	0V
1	1	1	1	1	1	1	0	$-REF\_ \times \left(\frac{1}{128}\right)$
1	0	0	0	0	0	0	0	$-REF\_ \times \left(\frac{127}{128}\right)$
0	0	0	0	0	0	0	0	$-REF\_ \times \left(\frac{128}{128}\right) = -REF\_$

Note:

$$1LSB = REF\_ \times 2^{-(8-1)} = REF\_ \times \left(\frac{1}{128}\right)$$

$$ANALOG\ OUTPUT = REF\_ \times \left(\frac{D}{128} - 1\right)$$

Bipolar Output

Using Figure 4's circuit, the MAX512/MAX13 can be configured for bipolar outputs. Table 4 lists the bipolar codes and corresponding output voltages. There are two ways to achieve rail-to-rail outputs: 1) Operate the MAX512/MAX513 with a single supply and positive reference voltages or 2) Use dual supplies with a positive or negative voltage at REFAB and a positive voltage at REFC. In either case, the op amps need dual supplies. When using the dual-supply mode, possible errors associated with the divide-by-two attenuator and gain-of-two buffer are eliminated (see the *Output Buffer Amplifier* section). For maximum output swing of all outputs in dual-supply mode, connect REFAB to V_{SS} and REFC to V_{DD}. In single-supply mode, connect REFAB, REFC, and V_{DD} together.

With dual supplies, DACs A and B can perform four-quadrant multiplication. Please note that in dual-supply mode, the REFAB input ranges from V_{SS} to (V_{DD} - 1.5V). Because REFC accepts only positive inputs, DAC C performs two-quadrant multiplication.

Figure 4 shows Maxim's ICL7612A with rail-to-rail input common-mode range and rail-to-rail output voltage swing—ideal for a high output voltage swing from low supply voltages.

RF Applications

Both the MAX512 and MAX513 can bias GaAs FETs, where the gate of the FETs must be negatively biased to ensure that there is no drain current. In a typical application, power to the RF amplifiers should not be turned on until the bias voltages provided by DAC A and DAC B are fully established; likewise, the supply should be turned off before the bias voltage is switched off. Figure 5 shows how DAC B supplies the negative bias V_{GG1} for the driver stage and DAC A provides the negative bias V_{GG2} for the output stage [1].

The DAC A and DAC B outputs are also ideal for controlling VCOs in mobile radios or cellular phones. Other applications include varactor and PIN diode circuits.

The unbuffered DAC C provides a span within GND and V_{DD} and is individually set at REF C. DAC C typically adjusts offset and gain in the system.

1 [John Wachsmann. "A High-Efficiency GaAs MMIC Power Amplifier for 1.9GHz PCS Applications," Proceedings of the First Annual Wireless Symposium, pp. 375, Penton Publishing, Jan. 1993.]

Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

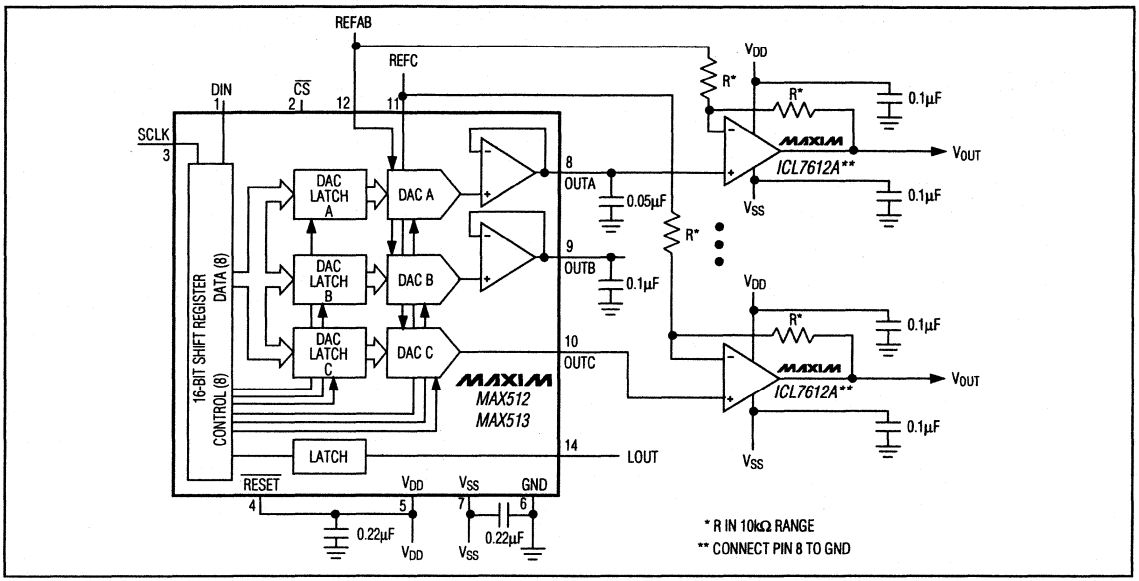


Figure 4. Bipolar Output Circuit

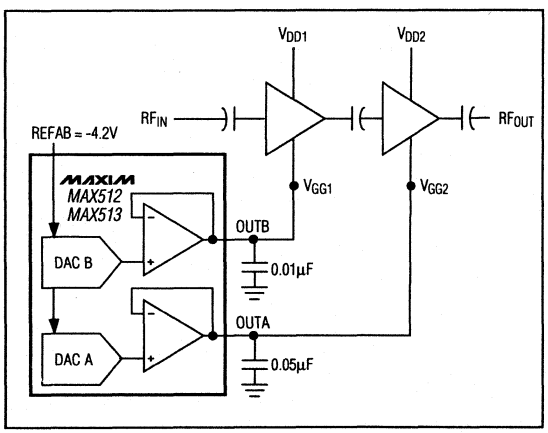


Figure 5. RF Bias Circuit

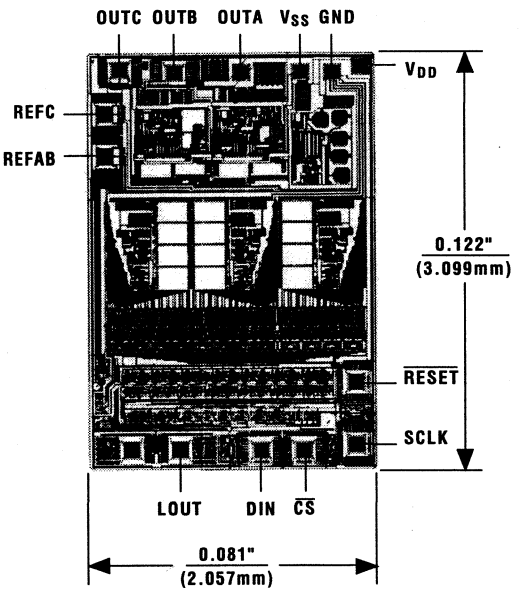
Low-Cost, Triple, 8-Bit Voltage-Output DACs with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX512EPD	-40°C to +85°C	14 Plastic DIP
MAX512ESD	-40°C to +85°C	14 SO
MAX512MJD	-55°C to +125°C	14 CERDIP
MAX513CPD	0°C to +70°C	14 Plastic DIP
MAX513CSD	0°C to +70°C	14 SO
MAX513C/D	0°C to +70°C	Dice*
MAX513EPD	-40°C to +85°C	14 Plastic DIP
MAX513ESD	-40°C to +85°C	14 SO
MAX513MJD	-55°C to +125°C	14 CERDIP

** Contact factory for dice specifications.*

_Chip Topography



TRANSISTOR COUNT: 1910

SUBSTRATE CONNECTED TO V_{DD}

9

19-0168; Rev 1; 11/93

MAXIM

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

General Description

The MAX530 is a low-power, 12-bit, voltage-output digital-to-analog converter (DAC) that uses single +5V or dual ±5V supplies. This device has an on-chip voltage reference plus an output buffer amplifier. Operating current is only 250µA from a single +5V supply, making it ideal for portable and battery-powered applications. In addition, the SSOP (Shrink-Small-Outline-Package) measures only 0.1 square inches, using less board area than an 8-pin DIP. 12-bit resolution is achieved through laser trimming of the DAC, op amp, and reference. No further adjustments are necessary.

Internal gain-setting resistors can be used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V, or ±2.048V. Four-quadrant multiplication is possible without the use of external resistors or op amps. The parallel logic inputs are double buffered and are compatible with 4-bit, 8-bit, and 16-bit microprocessors. For DACs with similar features but with a serial data interface, refer to the MAX531/MAX538/MAX539 data sheet.

Applications

Battery-Powered Data-Conversion Products
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor-Controlled Calibration

Features

- ♦ **Buffered Voltage Output**
- ♦ **Internal 2.048V Voltage Reference**
- ♦ **Operates from Single +5V or Dual ±5V Supplies**
- ♦ **Low Power Consumption:**
  250µA Operating Current
  40µA Shutdown-Mode Current
- ♦ **SSOP Package Saves Space**
- ♦ **Relative Accuracy: ±1/2 LSB Max Over Temperature**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **4-Quadrant Multiplication with No External Components**
- ♦ **Power-On Reset**
- ♦ **Double-Buffered Parallel Logic Inputs**

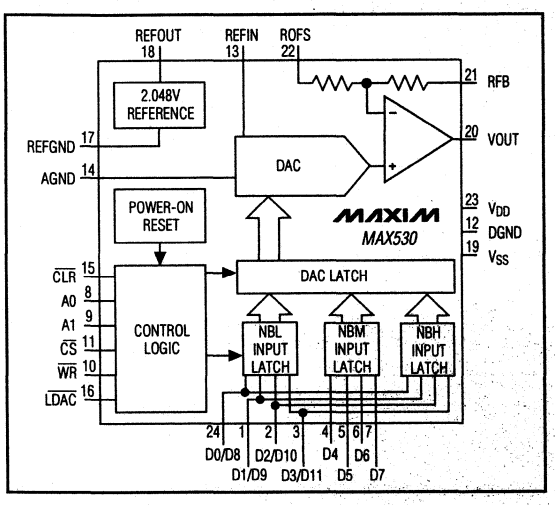
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX530ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX530BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX530ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX530BCWG	0°C to +70°C	24 Wide SO	±1
MAX530ACAG	0°C to +70°C	24 SSOP	±1/2
MAX530BCAG	0°C to +70°C	24 SSOP	±1
MAX530BC/D	0°C to +70°C	Dice*	±1

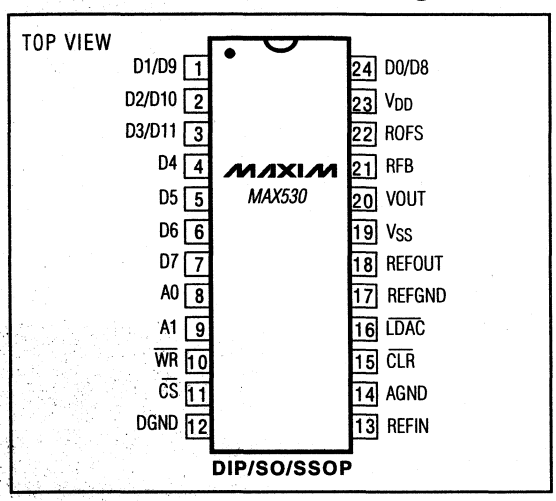
Ordering Information continued on last page.

** Dice are tested at T_A = +25°C, DC parameters only.*

Functional Diagram



Pin Configuration



+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND and V_{DD} to AGND .....-0.3V, +6V
V_{SS} to DGND and V_{SS} to AGND .....-6V, +0.3V
V_{DD} to V_{SS} ..... -0.3V, +12V
AGND to DGND.....-0.3V, +0.3V
REFGND to AGND.....-0.3V, (V_{DD} + 0.3V)
Digital Input Voltage to DGND ..... -0.3V, (V_{DD} + 0.3V)
REFIN.....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
REFOUT .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
REFOUT to REFGND..... -0.3V, (V_{DD} + 0.3V)
RFB .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
ROFS .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
VOUT to AGND (Note 1) ..... V_{SS}, V_{DD}

Continuous Current, Any Input .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C).....1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Narrow CERDIP (derate 12.50mW/°C above +70°C).....1000mW
Operating Temperature Ranges:
MAX530_C_ _ .....0°C to +70°C
MAX530_E_ _ .....-40°C to +85°C
MAX530_MRG .....-55°C to +125°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, DGND, or AGND if the continuous package power dissipation and current ratings are not exceeded. Typical short-circuit currents are 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V ±10%, V_{SS} = 0V, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	V_{DD} = 5V (Note 2)	MAX530AC/AE			±0.5	LSB
			MAX530BC/BE			±1	
			MAX530AM			±1	
			MAX530BM			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	V_{DD} = 5V		0	1	4	LSB
Zero-Code Temperature Coefficient	ZCTC				3		ppm/°C
Zero-Code-Error Supply Rejection	ZCPSRR	4.5V ≤ V_{DD} ≤ 5.5V (Note 3)			200	500	µV/V
Gain Error (Note 2)	GE	DAC latch = all 1s, VOUT < V_{DD} - 0.4V (Note 2)	MAX530_C/E			±1	LSB
			MAX530_M			±2	
Gain-Error Temperature Coefficient	GETC				1		ppm/°C
Gain-Error Power-Supply Rejection	GEPSRR	4.5V ≤ V_{DD} ≤ 5.5V (Note 3)			200	500	µV/V
DAC VOLTAGE OUTPUT (VOUT)							
Output Voltage Range				0		V_{DD} - 0.4	V
Resistive Load		VOUT = 2V, load regulation ≤ ±1LSB		2			kΩ
DC Output Impedance					0.2		Ω
Short-Circuit Current	ISC				20		mA
REFERENCE INPUT (REFIN)							
Reference Input Range				0		V_{DD} - 2	V
Reference Input Resistance		Code dependent, minimum at code 555hex		40			kΩ
Reference Input Capacitance		Code dependent (Note 4)		10		50	pF
AC Feedthrough		(Note 5)			-80		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V_{DD} = 5V ±10%, V_{SS} = 0V, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT)							
Reference Tolerance	V_{REFOUT}	V_{DD} = 5.0V (Note 6)	T_A = +25°C	2.024	2.048	2.072	V
			MAX530BC	2.017		2.079	
			MAX530BE	2.013		2.083	
Reference Output Resistance	R_{REFOUT}	(Note 9)				2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V				300	µV/V
Noise Voltage	e_n	0.1Hz to 10kHz			400		µVp-p
Temperature Coefficient		MAX530AC/AE/AM/BM			30	50	ppm/°C
		MAX530BC/BE			30		
Minimum Required External Capacitor	C_{MIN}			3.3			µF
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		T_A = +25°C		0.15	0.25		V/µs
Voltage Output Settling Time		To ±0.5LSB, VOUT = 2V			25		µs
Digital Feedthrough		$\overline{WR}$ = V_{DD}, digital inputs all 1s to all 0s			5		nV-s
Signal-to-Noise Plus Distortion Ratio	SINAD	Unity gain (Note 5)			68		dB
		Gain = 2 (Note 5)			68		
DIGITAL INPUTS (D0-D7, $\overline{LDAC}$, $\overline{CLR}$, $\overline{CS}$, $\overline{WR}$, A0, A1)							
Logic High Input	V_{IH}			2.4			V
Logic Low Input	V_{IL}					0.8	V
Digital Leakage Current		V_{IN} = 0V or V_{DD}				±1	µA
Digital Input Capacitance					8		pF
POWER SUPPLIES							
Positive Supply-Voltage Range	V_{DD}	(Note 7)		4.5		5.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}			250	400	µA
SWITCHING CHARACTERISTICS							
Address to $\overline{WR}$ Setup	t_{AWS}			5			ns
Address to $\overline{WR}$ Hold	t_{AWH}			5			ns
$\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS}			0			ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{CWH}			0			ns
Data to $\overline{WR}$ Setup	t_{DS}			45			ns
Data to $\overline{WR}$ Hold	t_{DH}			0			ns
$\overline{WR}$ Pulse Width	t_{WR}			45			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}			45			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			45			ns
Internal Power-On Reset Pulse Width	t_{POR}	(Note 4)			1.3	10	µs

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies

(V_{DD} = 5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	V_{DD} = 5V, V_{SS} = -5V	MAX530AC/AE			±0.5	LSB
			MAX530BC/BE			±1.5	
			MAX530AM			±1.5	
			MAX530BM			±2.5	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Bipolar Zero Code Error	BZCE	V_{DD} = 5V, V_{SS} = -5V			0	±4	LSB
Bipolar Zero Code Temperature Coefficient	ZCTC				3		ppm/°C
Bipolar Zero Code Error Power-Supply Rejection	ZCPSRR	4.5V ≤ V_{DD} ≤ 5.5V, -5.5V ≤ V_{SS} ≤ -4.5V (Note 3)			200	500	µV/V
Gain Error	GE	MAX530_C/E				±1	LSB
		MAX530_M				±2	
Gain-Error Temperature Coefficient	GETC				1		ppm/°C
Gain-Error Power-Supply Rejection	GEPSRR	4.5V ≤ V_{DD} ≤ 5.5V, -5.5V ≤ V_{SS} ≤ -4.5V (Note 3)			200	500	µV/V
DAC VOLTAGE OUTPUT (VOUT)							
Output Voltage Range				V_{SS} + 0.4		V_{DD} - 0.4	V
Resistive Load		VOUT = 2V, load regulation ≤ ±1LSB		2			kΩ
DC Output Impedance					0.2		Ω
Short-Circuit Current	ISC				20		mA
REFERENCE INPUT (REFIN)							
Reference Input Range				V_{SS} + 2		V_{DD} - 2	V
Reference Input Resistance		Code dependent, minimum at code 555hex		40			kΩ
Reference Input Capacitance		Code dependent (Note 4)		10		50	pF
AC Feedthrough		(Note 5)			-80		dB
REFERENCE OUTPUT (REFOUT)—Specifications are identical to those under Single +5V Supply							
DYNAMIC PERFORMANCE—Specifications are identical to those under Single +5V Supply							
DIGITAL INPUTS (D0-D7, $\overline{LDAC}$, $\overline{CLR}$, $\overline{CS}$, $\overline{WR}$, A0, A1)—Specifications are identical to those under Single +5V Supply							
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	(Note 7)		4.5		5.5	V
Negative Supply Voltage	V_{SS}	(Note 8)		-5.5		-4.5	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}			250	400	µA
Negative Supply Current	I_{SS}	Outputs unloaded, all digital inputs = 0V or V_{DD}			150	200	µA
SWITCHING CHARACTERISTICS—Specifications are identical to those under Single +5V Supply							

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (continued)

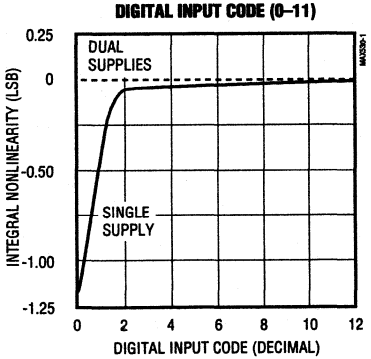
(V_{DD} = 5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = REFGND = 0V, REFIN = 2.048V (external), RFB = ROFS = VOUT, C_{REFOUT} = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Note 2: In single supply, INL and GE are calculated from code 11 to code 4095.
Note 3: Zero Code, Bipolar and Gain Error PSRR are input referred specifications. In Unity Gain, the specification is 500µV. In Gain = 2 and Bipolar modes, the specification is 1mV.
Note 4: Guaranteed by design.
Note 5: REFIN = 1kHz, 2.0Vp-p.
Note 6: MAX530AC/AE/AM reference tolerance over temperature is guaranteed at 50ppm/°C max temperature coefficient.
Note 7: For specified performance, V_{DD} = 5V ±10% is guaranteed by PSRR tests.
Note 8: For specified performance, V_{SS} = -5V ±10% is guaranteed by PSRR tests.
Note 9: Tested at I_{OUT} = 100µA. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).

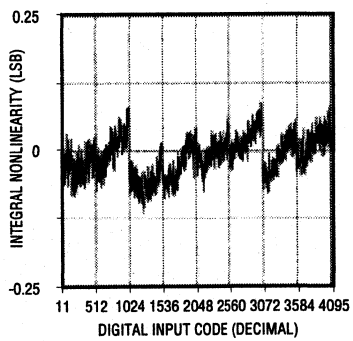
Typical Operating Characteristics

(T_A = +25°C, single supply (+5V), unity gain, code = all 1s, unless otherwise noted).

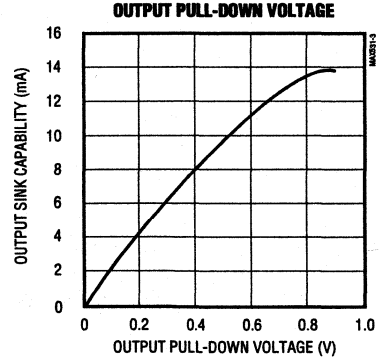
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (0–11)



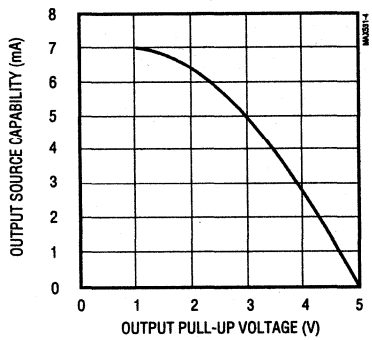
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (11–4095)



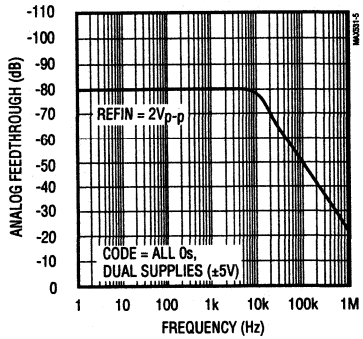
OUTPUT SINK CAPABILITY vs. OUTPUT PULL-DOWN VOLTAGE



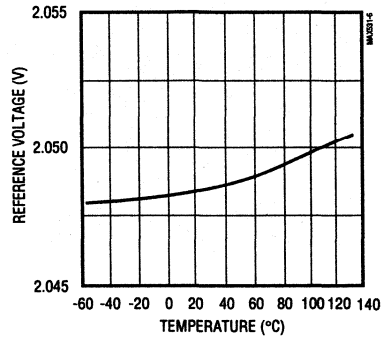
OUTPUT SOURCE CAPABILITY vs. OUTPUT PULL-UP VOLTAGE



ANALOG FEEDTHROUGH vs. FREQUENCY



REFERENCE VOLTAGE vs. TEMPERATURE

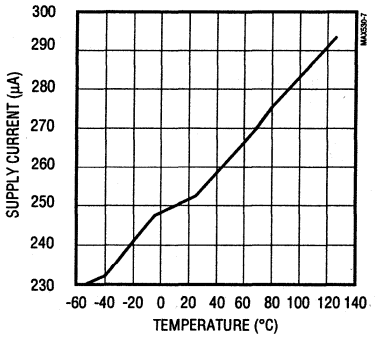


+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

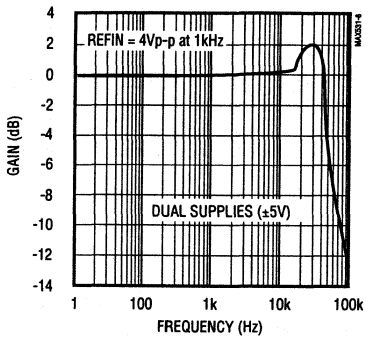
Typical Operating Characteristics (continued)

(T_A = +25°C, single supply (+5V), unity gain, code = all 1s, unless otherwise noted).

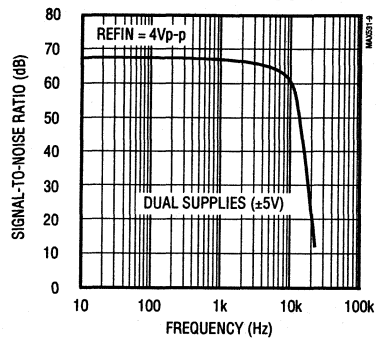
SUPPLY CURRENT vs. TEMPERATURE



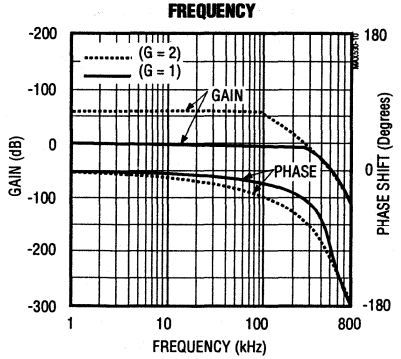
GAIN vs. FREQUENCY



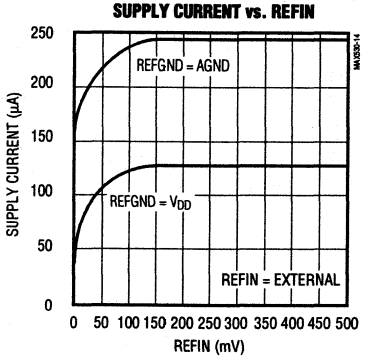
AMPLIFIER SIGNAL-TO- NOISE RATIO



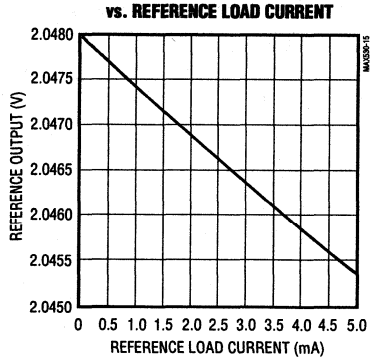
GAIN AND PHASE vs. FREQUENCY



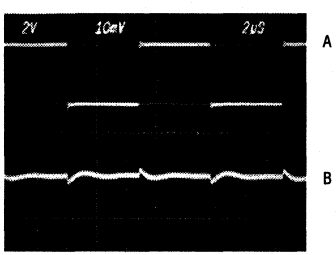
SUPPLY CURRENT vs. REFIN



REFERENCE OUTPUT VOLTAGE vs. REFERENCE LOAD CURRENT



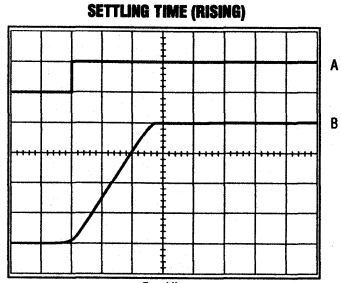
DIGITAL FEEDTHROUGH



2µs/div

A: D0...D7 = 100kHz, 4Vp-p
B: VOUT, 10mV/div
$\overline{LDAC}$ = $\overline{CS}$ = HIGH

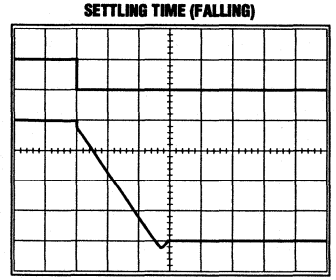
SETTLING TIME (RISING)



5µs/div

A: DIGITAL INPUTS RISING EDGE,
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY (±5V)
$\overline{LDAC}$ = LOW

SETTLING TIME (FALLING)



5µs/div

A: DIGITAL INPUTS FALLING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
DUAL SUPPLY (±5V)
$\overline{LDAC}$ = LOW

Pin Description

PIN	NAME	FUNCTION
1	D1/D9	Input Data D1 if A0 = 0 and A1 = 1, or D9 if A0 = A1 = 1
2	D2/D10	Input Data D2 if A0 = 0 and A1 = 1, or D10 if A0 = A1 = 1
3	D3/D11	Input Data D3 if A0 = 0 and A1 = 1, or D11 (MSB) if A0 = A1 =1
4	D4	Input Data D4, or tie to D0 and multiplex if A0 = 1 and A1 = 0
5	D5	Input Data D5, or tie to D1 and multiplex if A0 = 1 and A1 = 0
6	D6	Input Data D6, or tie to D2 and multiplex if A0 = 1 and A1 = 0
7	D7	Input Data D7, or tie to D3 and multiplex if A0 = 1 and A1 = 0
8	A0	Address Line A0. With A1, used to multiplex 4 of 12 data lines to load low (NBL), middle (NBM), and high (NBH) 4-bit nibbles. (12 bits can also be loaded as 8+4.)
9	A1	Address Line A1. Set A0 = 1 and A1 = 1 for NBL, A0 = 1 and A1 = 0 for NBM, or A0 = A1 = 1 for NBH. See Table 2 for complete input latch addressing.
10	$\overline{WR}$	Write Input (active low). Used with $\overline{CS}$ to load data into the input latch selected by A0 and A1.
11	$\overline{CS}$	Chip Select (active low). Enables addressing and writing to this chip from common bus lines.
12	DGND	Digital Ground
13	REFIN	Reference Input. Input for the R-2R DAC. Connect an external reference to this pin or a jumper to REFOUT (pin 18) to use the internal 2.048V reference.
14	AGND	Analog Ground
15	$\overline{CLR}$	Clear (active low). A low on $\overline{CLR}$ resets the DAC latches to all 0s.
16	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of the input latch to the DAC latch and updates VOUT.
17	REFGND	Reference Ground must be connected to AGND when using the internal reference. Connect to V_{DD} to disable the internal reference and save power.
18	REFOUT	Reference Output. Output of the internal 2.048V reference. Tie to REFIN to drive the R-2R DAC.
19	V_{SS}	Negative Power Supply. Usually ground for single-supply or -5V for dual-supply operation.
20	VOUT	Voltage Output. Op-amp buffered DAC output.
21	RFB	Feedback Pin. Op-amp feedback resistor. Always connect to VOUT.
22	ROFS	Offset Resistor Pin. Connect to VOUT for G = 1, to AGND for G = 2, or to REFIN for bipolar output.
23	V_{DD}	Positive Power Supply (+5V)
24	D0/D8	Input Data D0 (LSB) if A0 = 0 and A1 = 1, or D8 if A0 = A1= 1

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

Detailed Description

The MAX530 consists of a parallel-input logic interface, a 12-bit R-2R ladder, a reference, and an op amp. The *Functional Diagram* shows the control lines and signal flow through the input data latch to the DAC latch, as well as the 2.048V reference and output op amp. Total supply current is typically 250µA with a single +5V supply. This circuit is ideal for battery-powered, microprocessor-controlled applications where high accuracy, no adjustments, and minimum component count are key requirements.

R-2R Ladder

The MAX530 uses an "inverted" R-2R ladder network with a BiCMOS op amp to convert 12-bit digital data to analog voltage levels. Figure 1 shows a simplified diagram of the R-2R DAC and op amp. Unlike a standard DAC, the MAX530 uses an "inverted" ladder network. Normally, the REFIN pin is the current output of a standard DAC and would be connected to the summing junction, or virtual ground, of an op amp. In a standard DAC configuration, the output voltage would be the inverse of the reference voltage. The MAX530's topology makes the ladder output voltage the same polarity as the reference input, which makes the device suitable for single-supply operation. The BiCMOS op amp is then used to buffer, invert, or amplify the ladder signal.

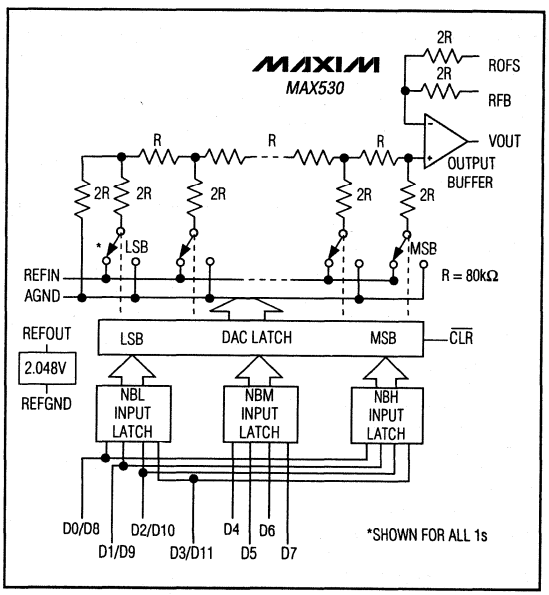


Figure 1. Simplified MAX530 DAC Circuit

Ladder resistors are nominally 80kΩ to conserve power and are laser trimmed for gain and linearity. The input impedance at REFIN is code dependent. When the DAC register is all 0s, all legs of the ladder are grounded and REFIN is open or no load. Maximum loading (minimum REFIN impedance) occurs at code 010101... or 555hex. Minimum reference input impedance at this code is guaranteed to be not less than 40kΩ.

The REFIN and REFOUT pins allow the user to choose between driving the R-2R ladder with the on-chip reference or an external reference. REFIN may be below analog ground when using dual supplies. See the *External Reference* and *Four-Quadrant Multiplication* sections for more information.

Internal Reference

The on-chip reference is laser trimmed to generate 2.048V at REFOUT. The output stage can source and sink current so REFOUT can settle to the correct voltage quickly in response to code-dependent loading changes. Typical source current is 5mA with a sink current of 100µA.

REFOUT connects the internal reference to the R-2R DAC ladder at REFIN. The R-2R ladder draws 50µA maximum load current. If any other connection is made to REFOUT, ensure that the total load current is less than 100µA to avoid gain errors.

A separate REFGND pin is provided to isolate reference currents from other analog and digital ground currents. To achieve specified noise performance, connect a 33µF capacitor from REFOUT to REFGND (see Figure 2). Using smaller capacitance values increases noise, and values less than 3.3µF may compromise the reference's stability. For applications requiring the lowest noise, insert a buffered RC filter between REFOUT and REFIN. When using the internal reference, REFGND must be connected to AGND. In applications not requiring the internal reference, connect REFGND to V_{DD}, which shuts down the reference and saves typically 100µA of V_{DD} supply current.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

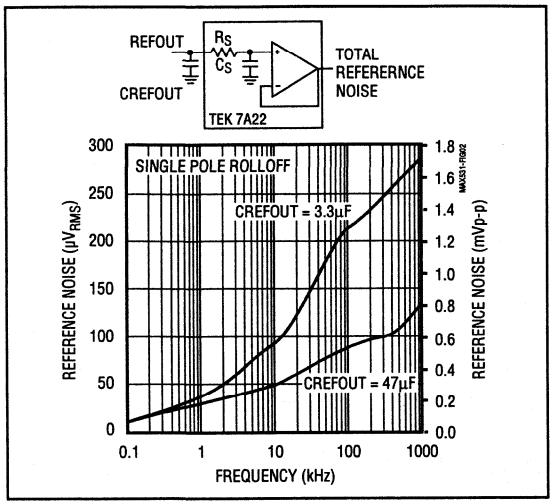


Figure 2. Reference Noise vs. Frequency

Output Buffer

The output amplifier uses a folded cascode input stage and a type AB output stage. Large-output devices with low series resistance allow the output to swing to ground in single-supply operation. The output buffer is unity-gain stable. Input offset voltage and supply current are laser trimmed. Settling time is 25µs to 0.01% of full scale. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF of load capacitance. The op amp may be placed in unity-gain (G = 1), in a gain of two (G = 2), or in a bipolar-output mode by using the ROFS and RFB pins. These pins are used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V or ±2.048V, by connecting ROFS to VOUT, GND, or REFIN. RFB is always connected to VOUT. Table 1 summarizes ROFS usage.

Table 1. ROFS Usage

ROFS CONNECTED TO:	DAC OUTPUT RANGE	OP-AMP GAIN
VOUT	0V to 2.048V	G = 1
AGND	0V to 4.096V	G = 2
REFIN	-2.048V to +2.048V	Bipolar

Note: Assumes RFB = VOUT and REFIN = REFOUT = 2.048V

External Reference

An external reference in the range (V_{SS} + 2V) to (V_{DD} - 2V) may be used with the MAX530 in dual-supply, unity-gain operation. In single-supply, unity-gain operation, the reference must be positive and may not exceed (V_{DD} - 2V). The reference voltage determines the DAC's full-scale output. Because of the code-dependent nature of reference input impedances, a high-quality, low-output-impedance amplifier (such as the MAX480 low-power, precision op amp) should be used to drive REFIN.

If an upgrade to the internal reference is required, the 2.5V MAX873A is ideal: ±15mV initial accuracy, 7ppm/°C (max) temperature coefficient.

Power-On Reset

An internal power-on reset (POR) circuit forces the DAC register to reset to all 0s when V_{DD} is first applied. The POR pulse is typically 1.3µs; however, it may take 2ms for the internal reference to charge its large filter capacitor and settle to its trimmed value.

In addition to POR , a clear ($\overline{CLR}$) pin, when held low, sets the DAC register to all 0s. $\overline{CLR}$ operates asynchronously and independently from chip select ($\overline{CS}$). With the DAC input at all 0s, the op-amp output is at zero for unity-gain and G = 2 configurations.

Shutdown Mode

The MAX530 is designed for low power consumption. Understanding the circuit allows power consumption management for maximum efficiency. In single-supply mode (V_{DD} = +5V, V_{SS} = GND) the initial supply current is typically only 160µA, including the reference, op amp, and DAC. This low current occurs when the power-on reset circuit clears the DAC to all 0s and forces the op-amp output to zero. (See the Supply Current vs. REFIN graph in the *Typical Operating Characteristics*.) Under this condition, there is no internal load on the reference (DAC = 000hex, REFIN = ∞ Ω) and the op amp operates at its minimum quiescent current. The $\overline{CLR}$ signal resets the MAX530 to these same conditions and can be used to control a power-saving mode when the DAC is not being used by the system.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

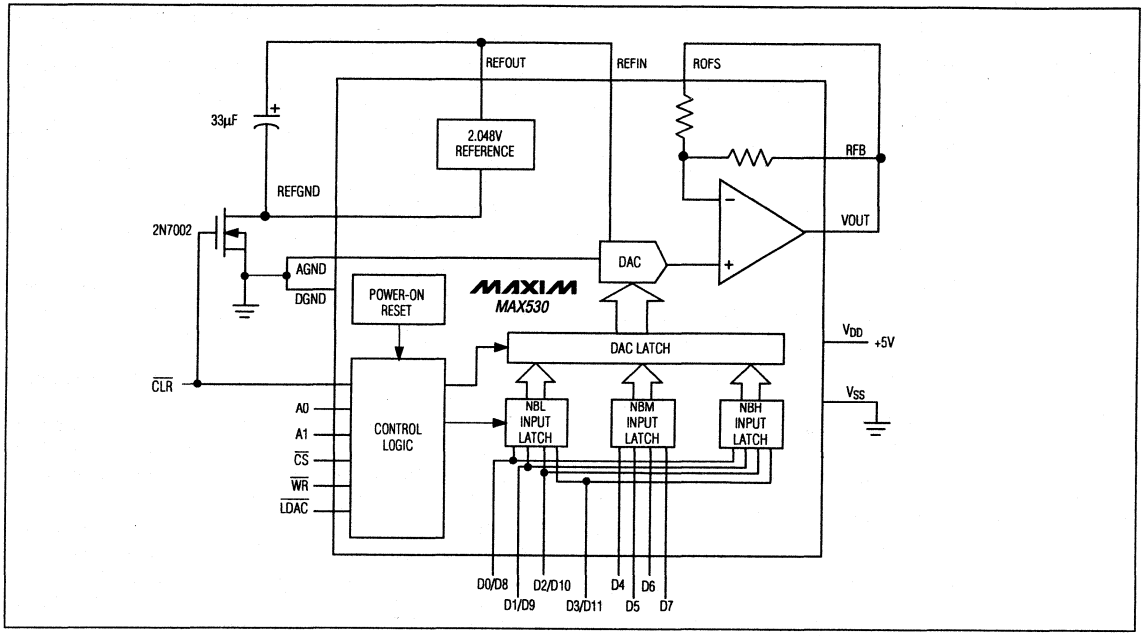


Figure 3. Low-Current Shutdown Mode

An additional 110µA of supply current can be saved when the internal reference is not used by connecting REFGND to V_{DD}. A low on resistance N-channel FET, such as the 2N7002, can be used to turn off the internal reference to create a shutdown mode with minimum current drain (Figure 3). When $\overline{CLR}$ is high, the transistor pulls REFGND to AGND and the reference and DAC operate normally. When $\overline{CLR}$ goes low, REFGND is pulled up to V_{DD} and the reference is shut down. At the same time, $\overline{CLR}$ resets the DAC register to all 0s, and the op-amp output goes to 0V for unity-gain and G = 2 modes. This reduces the total single-supply operating current from 250µA (400µA max) to typically 40µA in shutdown mode.

A small error voltage is added to the reference output by the reference current flowing through the N-channel pull-down transistor. The switch's on resistance should be less than 5Ω. A typical reference current of 100µA would add 0.5mV to REFOUT. Since the reference current and on resistance increase with temperature, the overall temperature coefficient will degrade slightly.

As data is loaded into the DAC and the output moves above GND, the op-amp quiescent current increases to its nominal value and the total operating current averages 250µA. Using dual supplies (±5V), the op amp is fully biased continuously, and the V_{DD} supply current is more constant at 250µA. The V_{SS} current is typically 150µA.

The MAX530 logic inputs are compatible with TTL and CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Table 2. Input Latch Addressing

$\overline{CLR}$	$\overline{CS}$	$\overline{WR}$	$\overline{LDAC}$	A0	A1	DATA UPDATED
L	X	X	X	X	X	Reset DAC Latches
H	H	X	H	X	X	No Operation
H	X	H	H	X	X	No Operation
H	L	L	H	H	H	NBH (D8-D11)
H	L	L	H	H	L	NBM (D4-D7)
H	L	L	H	L	H	NBL (D0-D3)
H	H	H	L	X	X	Update DAC Only
H	L	L	X	L	L	NBL and NBM (D0-D7)
H	L	L	L	H	H	NBH and Update DAC

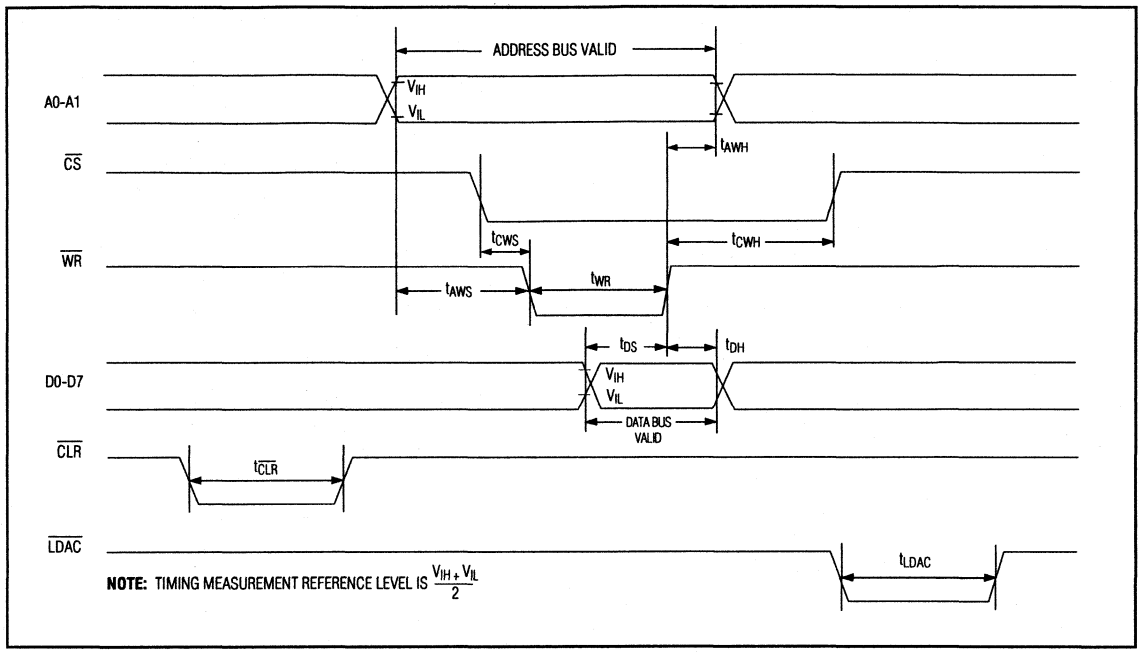


Figure 4. MAX530 Write-Cycle Timing Diagram

Parallel Logic Interface

Designed to interface with 4-bit, 8-bit, and 16-bit microprocessors (µPs), the MAX530 uses 8 data pins and double-buffered logic inputs to load data as 4 + 4 + 4 or 8 + 4. The 12-bit DAC latch is updated simultaneously through the control signal $\overline{LDAC}$. Signals A0, A1, $\overline{WR}$, and $\overline{CS}$ select which input latches to update. The 12-bit data is broken down into nibbles (NB); NBL is the enable signal for the lowest 4 bits, NBM is the enable for the middle 4 bits, and NBH is the enable for the highest and most significant 4 bits. Table 2 lists the address decoding scheme.

Refer to Figure 4 for the MAX530 write-cycle timing diagram.

Figure 5 shows the circuit configuration for a 4-bit µP application. Figure 6 shows the corresponding timing sequence. The 4 low bits (D0-D3) are connected in parallel to the other 4 bits (D4-D7) and then to the µP bus. Address lines A0 and A1 enable the input data latches for the high, middle, or low data nibbles. The µP sends chip select ($\overline{CS}$) and write ($\overline{WR}$) signals to latch in each of three nibbles in three cycles when the data is valid.

Figure 7 shows a typical interface to an 8-bit or a 16-bit µP. Connect 8 data bits from the data bus to pins D0-D7 on the MAX530. With $\overline{LDAC}$ held high, the user can load NBH or NBL + NBM in any order. Figure 8a shows the corresponding timing sequence. For fastest throughput, use Figure 8b's sequence. Address lines A0 and A1 are tied together and the DAC is loaded in 2 cycles as 8 + 4. In this scheme, with $\overline{LDAC}$ held low, the DAC latch is transparent. Always load NBL and NBM first, followed by NBH.

$\overline{LDAC}$ is asynchronous with respect to $\overline{WR}$. If $\overline{LDAC}$ is brought low before or at the same time $\overline{WR}$ goes high, $\overline{LDAC}$ must remain low for at least 50ns to ensure the correct data is latched. Data is latched into DAC registers on $\overline{LDAC}$'s rising edge.

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

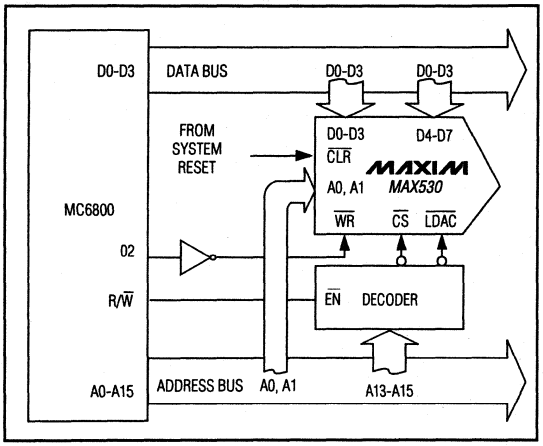


Figure 5. 4-Bit µP Interface

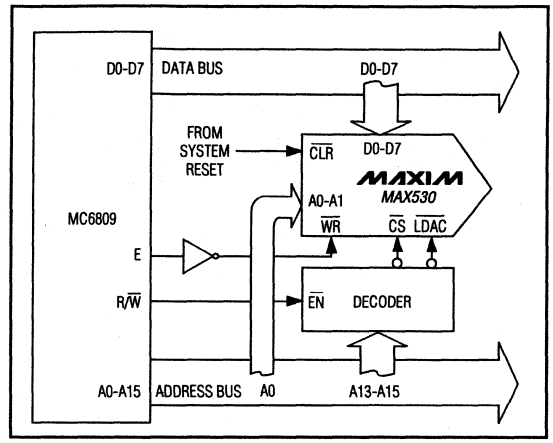


Figure 7. 8-Bit and 16-Bit µP Interface

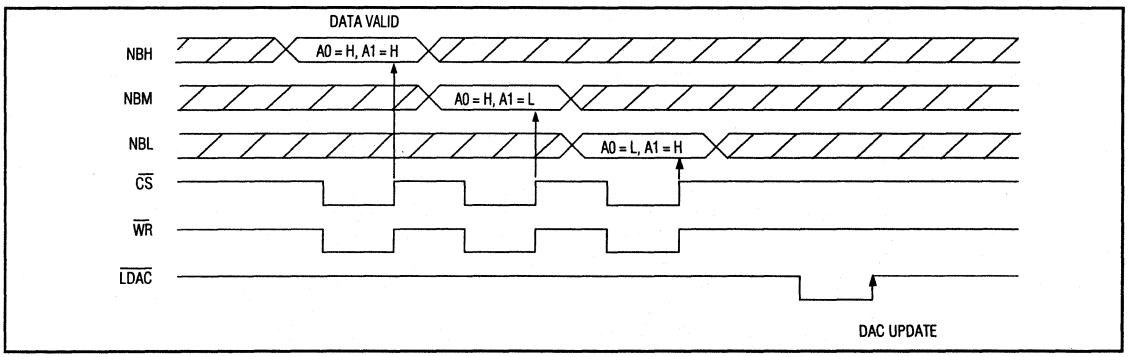


Figure 6. 4-Bit µP Timing Sequence

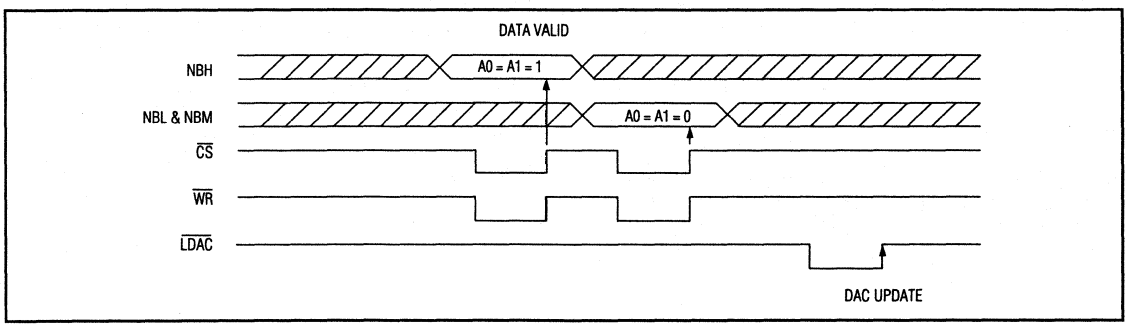


Figure 8a. 8-Bit and 16-Bit µP Timing Sequence Using $\overline{LDAC}$

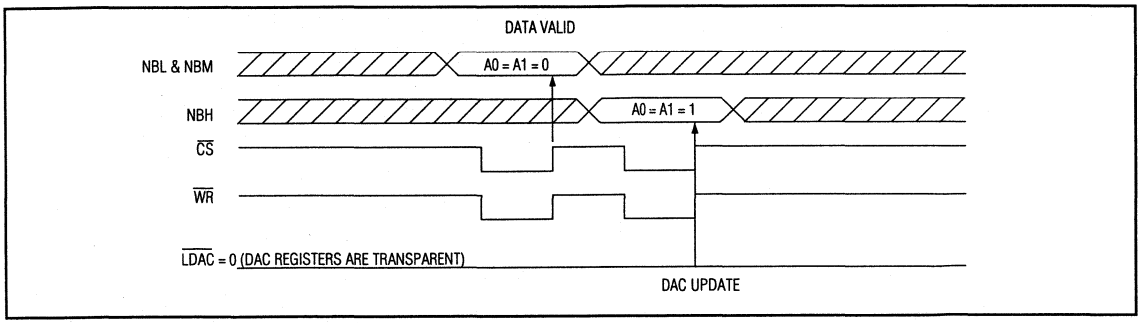


Figure 8b. 8-Bit and 16-Bit µP Timing Sequence with $\overline{LDAC}$ = 0

Unipolar Configuration

The MAX530 is configured for a 0V to +2.048V unipolar output range by connecting ROFS and RFB to VOUT (Figure 9). The converter operates from either single or dual supplies in this configuration. See Table 3 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, 1LSB = REFIN (2^{-12}).

A 0V to 4.096V unipolar output range is set up by connecting ROFS to AGND and RFB to VOUT (Figure 10). Table 4 shows the DAC-latch contents vs. VOUT. The MAX530 operates from either single or dual supplies in this mode. In this range, 1LSB = (2)(REFIN)(2^{-12}) = (REFIN)(2^{-11}).

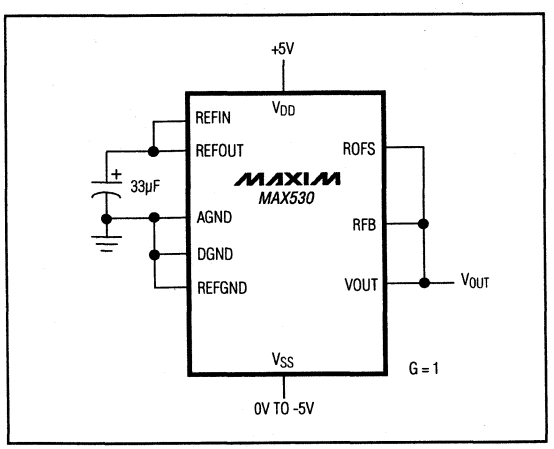


Figure 9. Unipolar Configuration (0V to +2.048V Output)

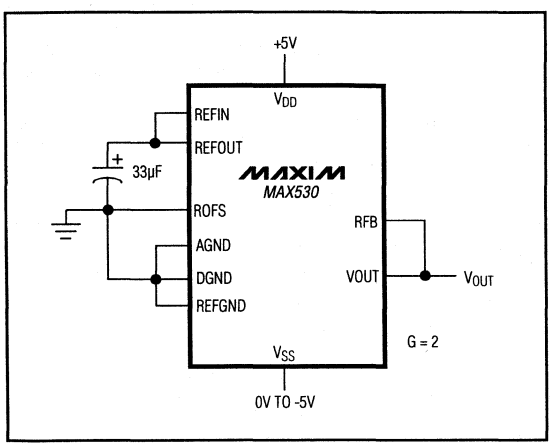


Figure 10. Unipolar Configuration (0V to +4.096V Output)

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

Table 3. Unipolar Code Table (0V to +2.048V Output)

INPUT	OUTPUT
1111 1111 1111	$(VREF)\frac{4095}{4096}$
1000 0000 0001	$(VREF)\frac{2049}{4096}$
1000 0000 0000	$(VREF)\frac{2048}{4096} = +VREF/2$
0111 1111 1111	$(VREF)\frac{2047}{4096}$
0000 0000 0001	$(VREF)\frac{1}{4096}$
0000 0000 0000	0V

Table 4. Unipolar Code Table (0V to +4.096V Output)

INPUT	OUTPUT
1111 1111 1111	$+2\,(VREF)\frac{4095}{4096}$
1000 0000 0001	$+2\,(VREF)\frac{2049}{4096}$
1000 0000 0000	$+2\,(VREF)\frac{2048}{4096} = +VREF$
0111 1111 1111	$+2\,(VREF)\frac{2047}{4096}$
0000 0000 0001	$+2\,(VREF)\frac{1}{4096}$
0000 0000 0000	0V

Bipolar Configuration

A -2.048V to +2.048V bipolar range is set up by connecting ROFS to REFIN and RFB to VOUT, and operating from dual (±5V) supplies (Figure 11). Table 5 shows the DAC-latch contents (input) vs. VOUT (output). In this range, 1 LSB = REFIN (2^{-11}).

Four-Quadrant Multiplication

The MAX530 can be used as a four-quadrant multiplier by connecting ROFS to REFIN, using (1) an offset dual or twos-complement digital code, (2) bipolar power supplies, and (3) a bipolar analog input at REFIN within the range V_{SS} + 2V to V_{DD} - 2V, as shown in Figure 12.

In general, a 12-bit DAC's output is $(D)(V_{REFIN})(G)$, where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{12} or 4,096. This formula is precise for unipolar operation. However, for bipolar, twos-complement operation, the MSB is really a polarity bit. No resolution is lost, because there are the same number of steps. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V (G = 2) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. The negative full scale is $-V_{REFIN}$, while the positive full scale is $+V_{REFIN}$ - 1LSB.

Table 5. Bipolar Code Table (-2.048V to +2.048V Output)

INPUT	OUTPUT
1111 1111 1111	$(+VREF)\frac{2047}{2048}$
1000 0000 0001	$(+VREF)\frac{1}{2048}$
1000 0000 0000	0V
0111 1111 1111	$(-VREF)\frac{1}{2048}$
0000 0000 0001	$(-VREF)\frac{2047}{2048}$
0000 0000 0000	$(-VREF)\frac{2048}{2048} = -VREF$

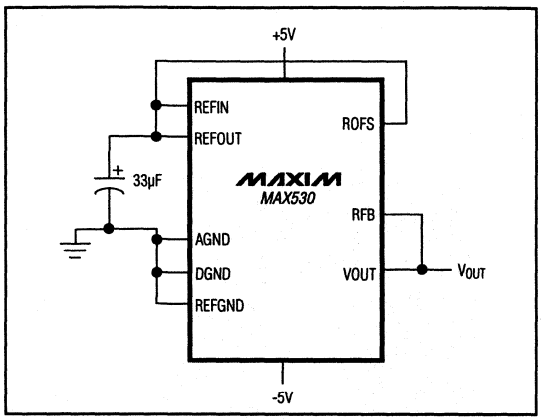


Figure 11. Bipolar Configuration (-2.048V to +2.048V Output)

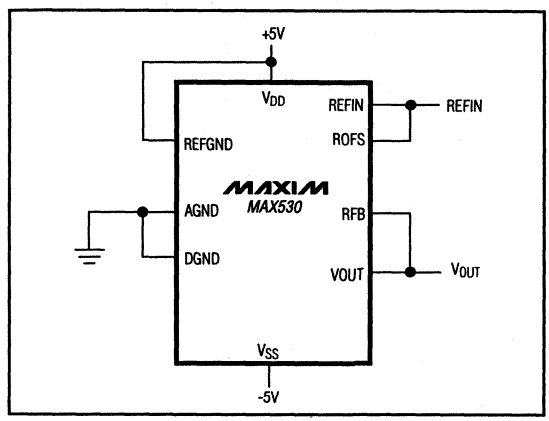


Figure 12. Four-Quadrant Multiplying Circuit

Applications Information

Single-Supply Linearity

As with any amplifier, the MAX530's output op amp offset can be positive or negative. When the offset is positive, it is easily accounted for. However, when the offset is negative, the output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive. The resulting transfer function is shown in Figure 13.

Normally, linearity is measured after allowing for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. In the MAX530, linearity and gain error are measured from code 11 to code 4095 (see Note 2 under *Electrical Characteristics*). The output amplifier offset does not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 4095.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

AGND and REFGND should be connected together, and then to DGND at the chip. For single-supply applications, connect V_{SS} to AGND at the chip. The best ground connection may be achieved by connecting the AGND, REFGND, and DGND pins together and connecting that point to the system analog ground plane. If DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

Bypass V_{DD} (and V_{SS} in dual-supply mode) with a 1.0µF ceramic capacitor connected between V_{DD} and AGND (and between V_{SS} and AGND). The ceramic capacitor(s) should be mounted with short leads as close to the device as possible. Power-supply bypass with a capacitor ensures a low impedance over a wide frequency range. All capacitors should have low equivalent series resistance (ESR).

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC package and cause internal stray capacitance to appear as noise at the DAC output, even though $\overline{LDAC}$ and $\overline{CS}$ are held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding $\overline{LDAC}$ and $\overline{CS}$ high and toggling the data inputs from all 1s to all 0s.

Analog Feedthrough

Because of internal stray capacitance, higher-frequency analog input signals at REFIN may couple to the output, even when the input digital code is all 0s, as shown in the *Typical Operating Characteristics* graph Analog Feedthrough vs. Frequency. It is tested by sweeping REFIN and setting $\overline{CLR}$ to low (which sets the DAC latches to 000hex).

+5V, Low-Power, Parallel-Input, Voltage-Output, 12-Bit DAC

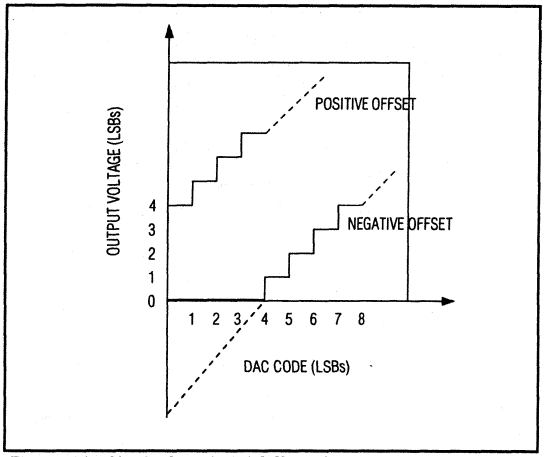


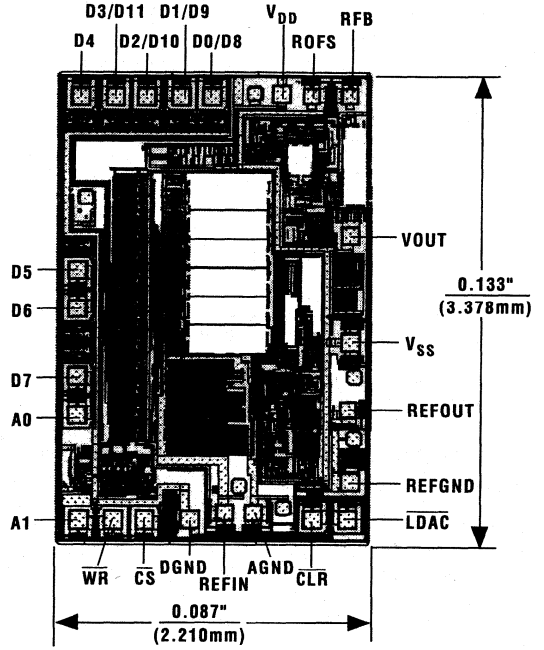
Figure 13. Single-Supply DAC Transfer Function

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX530AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX530BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX530AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX530BEWG	-40°C to +85°C	24 Wide SO	±1
MAX530AEAG	-40°C to +85°C	24 SSOP	±1/2
MAX530BEAG	-40°C to +85°C	24 SSOP	±1
MAX530AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX530BMRG	-55°C to +125°C	24 Narrow CERDIP**	±2

*** Contact factory for availability and processing to MIL-STD-883.*

_Chip Topography



TRANSISTOR COUNT: 913;
SUBSTRATE CONNECTED TO V_{DD}.

19-0172; Rev 3; 11/93

MAXIM

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

General Description

The MAX531/MAX538/MAX539 are low-power, voltage-output, 12-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. In addition, the MAX531 can be operated with ±5V supplies. The MAX538/MAX539 draw only 140µA, and the MAX531, with internal reference, draws only 260µA. The MAX538/MAX539 come in 8-pin DIP and SO packages, while the MAX531 comes in 14-pin DIP and SO packages. All parts have been trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary.

The MAX538's buffer is fixed at a gain of 1 and the MAX539's buffer at a gain of 2. The MAX531's internal op amp may be configured for a gain of 1 or 2, as well as for unipolar or bipolar output voltages. The MAX531 can also be used as a four-quadrant multiplier without external resistors or op amps.

For parallel data inputs, see the MAX530 data sheet.

Applications

Battery-Powered Test Instruments

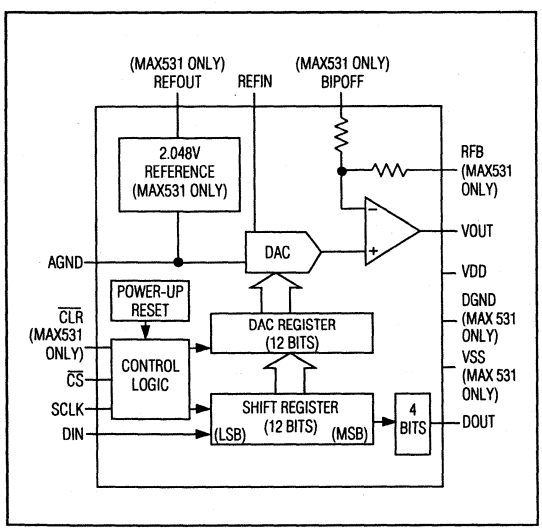
Digital Offset and Gain Adjustment

Battery-Operated/Remote Industrial Controls

Machine and Motion Control Devices

Cellular Telephones

Functional Diagram



Features

- ♦ **Operate from Single +5V Supply**
- ♦ **Buffered Voltage Output**
- ♦ **Internal 2.048V Reference (MAX531)**
- ♦ **140µA Supply Current (MAX538/MAX539)**
- ♦ **INL = ±1/2LSB (max)**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Flexible Output Ranges:**
  0V to V_{DD} (MAX531/MAX539)
  ±4.5V (MAX531)
  0V to 2.6V (MAX531/MAX538)
- ♦ **8-Pin SO/DIP (MAX538/MAX539)**
- ♦ **Power-On Reset**
- ♦ **Serial Data Output for Daisy-Chaining**

Ordering Information

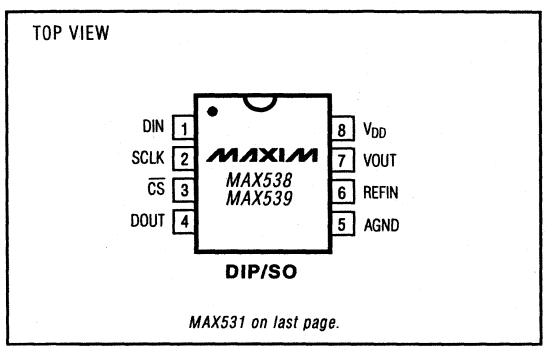
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX531ACPD	0°C to +70°C	14 Plastic DIP	±1/2
MAX531BCPD	0°C to +70°C	14 Plastic DIP	±1
MAX531ACSD	0°C to +70°C	14 SO	±1/2
MAX531BCSD	0°C to +70°C	14 SO	±1
MAX531BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

* *Dice are tested at T_A = +25°C only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



MAX531 on last page.

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5V, Low-Power, Voltage-Output Serial 12-Bit DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND and V_{DD} to AGND .....-0.3V, +6V
V_{SS} to DGND and V_{SS} to AGND .....-6V, +0.3V
V_{DD} to V_{SS} .....-0.3V, +12V
AGND to DGND .....-0.3V, +0.3V
Digital Input Voltage to DGND .....-0.3V, (V_{DD} + 0.3V)
REFIN .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
REFOUT to AGND .....-0.3V, (V_{DD} + 0.3V)
RFB .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
BIPOFF .....(V_{SS} - 0.3V), (V_{DD} + 0.3V)
V_{OUT} (Note 1) .....V_{SS}, V_{DD}
Continuous Current, Any Pin .....-20mA, +20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX53_ _C_ _ .....0°C to +70°C
MAX53_ _E_ _ .....-40°C to +85°C
MAX53_ _MJ_ .....-55°C to +125°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The output may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation limit is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V_{DD} = 5V ±10%, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT (MAX531), CREFOUT = 33µF (MAX531), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Relative Accuracy (Note 2)	INL	MAX53_AC/E			±0.5	LSB
		MAX53_AM			±1	
		MAX53_BC/E			±1	
		MAX53_BM			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Unipolar Offset Error (Note 3)	V_{OS}		0		4	LSB
Unipolar Offset Tempco	TCV_{OS}			3		ppm/°C
Gain Error (Note 2)	GE	MAX53_ _C/E			±1	LSB
		MAX53_ _M			±2	
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio, Unipolar Offset Error and Gain Error	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		200	500	µV/V
VOLTAGE OUTPUT (V_{OUT})						
Output Voltage Range		MAX531(G = 1), MAX538	0		V_{DD} -2	V
		MAX531(G = 2), MAX539	0		V_{DD} - 0.4	
Output Load Regulation		VOUT = 2V, R_L = 2kΩ			-1	LSB
Short-Circuit Current	I_{SC}			12		mA
REFERENCE INPUT (REFIN)						
Voltage Range			0		V_{DD} -2	V
Input Resistance		Code dependent, minimum at code 555hex	40			kΩ
Input Capacitance		Code dependent (Note 4)	10		50	pF
AC Feedthrough		REFIN = 1kHz, 2Vp-p		-80		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V_{DD} = 5V ±10%, V_{SS} = 0V, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT (MAX531), CREFOUT = 33µF (MAX531), R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE OUTPUT (REFOUT—MAX531 only)							
Reference Output Voltage		V_{DD} = 5.0V (Note 6)	T_A = +25°C	2.024	2.048	2.072	V
			MAX531BC	2.017		2.079	
			MAX531BE	2.013		2.083	
Temperature Coefficient	TC_{REFOUT}	MAX531AC/AE/AM/BM			15	50	ppm/°C
		MAX531BC/BE			15		
Resistance	R_{REFOUT}	(Note 5)			0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V				300	µV/V
Noise Voltage	e_n	0.1Hz to 10kHz			400		µVp-p
Minimum Required External Capacitor	C_{MIN}			3.3			µF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{CLR}$)							
Input High	V_{IH}			2.4			V
Input Low	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance	C_{IN}				8		pF
DIGITAL OUTPUT (DOUT)							
Output High	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 1			V
Output Low	V_{OL}	I_{SINK} = 2mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	T_A = +25°C		0.15	0.25		V/µs
Voltage-Output Settling Time		To ±1/2LSB, VOUT = 2V			25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz			5		nV-s
Signal-to-Noise plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p (G = 1 or 2), Code = FFhex			68		dB
POWER SUPPLY							
Positive Supply Voltage	V_{DD}			4.5		5.5	V
Power-Supply Current	I_{DD}	All inputs = 0V or V_{DD}, output = no load	MAX531		260	400	µA
			MAX538, MAX539		140	300	
SWITCHING CHARACTERISTICS							
$\overline{CS}$ Setup Time	t_{CSS}			20			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}			15			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}			0			ns
SCLK High Width	t_{CH}			35			ns
SCLK Low Width	t_{CL}			35			ns
DIN Setup Time	t_{DS}			45			ns
DIN Hold Time	t_{DH}			0			ns
DOUT Valid Propagation Delay	t_{DO}	C_L = 50pF				80	ns
$\overline{CS}$ High Pulse Width	t_{CSW}			20			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			25			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}			50			ns

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only)

(V_{DD} = 5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT, CREFOUT = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution	N			12			Bits
Relative Accuracy	INL	Tested at V_{DD} = 5V, V_{SS} = -5V	MAX531AC/E			±0.5	LSB
			MAX531AM			±1	
			MAX531BC/E			±1	
			MAX531BM			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Bipolar Offset Error	V_{OS}	BIPOFF = REFIN				±4	LSB
Bipolar Offset Tempco	TCV_{OS}	BIPOFF = REFIN			3		ppm/°C
Gain Error (Unipolar or Bipolar)	GEU	MAX53_ _C/E				±1	LSB
		MAX53_ _M				±2	
Gain-Error Tempco					1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V, -5.5V ≤ V_{SS} ≤-4.5V				200	µV/V
REFERENCE INPUT (REFIN)							
Voltage Range				V_{SS} +2		V_{DD} -2	V
Input Resistance		Code dependent, minimum at code 555 hex		40			kΩ
Input Capacitance		Code dependent (Note 4)		10		50	pF
AC Feedthrough		REFIN = 1kHz, 2.0Vp-p			-80		dB
REFERENCE OUTPUT (REFOUT—MAX531 only)							
Reference Output Voltage		V_{DD} = 5.0V (Note 6)	T_A = +25°C	2.024	2.048	2.072	V
			MAX531BC	2.017		2.079	
			MAX531BE	2.013		2.083	
Temperature Coefficient	TC_{REFOUT}	MAX531AC/AE/AM/BM			15	50	ppm/°C
		MAX531BC/BE			15		
Resistance	R_{REFOUT}	(Note 5)			0.5	2	Ω
Power-Supply Rejection Ratio	PSRR	4.5 ≤ V_{DD} ≤ 5.5V				300	µV/V
Noise Voltage	e_n	0.1Hz to 10kHz			400		µVp-p
Minimum Required External Capacitor	C_{MIN}			3.3			µF
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)							
Input High	V_{IH}			2.4			V
Input Low	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance	C_{IN}				8		pF
DIGITAL OUTPUT (DOUT)							
Output High	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 1			V
Output Low	V_{OL}	I_{SINK} = 2mA				0.4	V

ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX531 Only) (continued)

(V_{DD} = 5V ±10%, V_{SS} = -5V ±10%, AGND = DGND = 0V, REFIN = 2.048V (external), RFB = BIPOFF = VOUT, CREFOUT = 33µF, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE OUTPUT (VOUT)						
Output Voltage Range		MAX531(G = 1)	V_{SS} + 2		V_{DD} - 2	V
		MAX531(G = 2)	V_{SS} + 0.4		V_{DD} - 0.4	
Output Load Regulation		VOUT = 2V, R_L = 2kΩ			-1	LSB
Short-Circuit Current	I_{SC}			12		mA
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR		0.15	0.25		V/µs
Voltage-Output Settling Time		To ±1/2LSB, VOUT = 2V		25		µs
Digital Feedthrough		Step 000hex to FFFhex		5		nV-s
Signal-to-Noise plus Distortion	SINAD	REFIN = 1kHz, 2Vp-p, (G = 1)		68		dB
		REFIN = 1kHz, 2Vp-p, (G = 2)		68		
POWER SUPPLY						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Negative Supply Voltage	V_{SS}		-5.5		0	V
Positive Supply Current	I_{DD}	All inputs = 0V or V_{DD}, no load		260	400	µA
Negative Supply Current	I_{SS}	All inputs = 0V or V_{DD}, no load		-120	-200	µA
SWITCHING CHARACTERISTICS						
$\overline{CS}$ Setup Time	t_{CSS}		20			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		15			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
SCLK High Width	t_{CH}		35			ns
SCLK Low Width	t_{CL}		35			ns
DIN Setup Time	t_{DS}		45			ns
DIN Hold Time	t_{DH}		0			ns
DOUT Valid Propagation Delay	t_{DO}	C_L = 50pF			80	ns
$\overline{CS}$ High Pulse Width	t_{CSW}		20			ns
$\overline{CLR}$ Pulse Width	t_{CLR}		25			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CS1}		50			ns

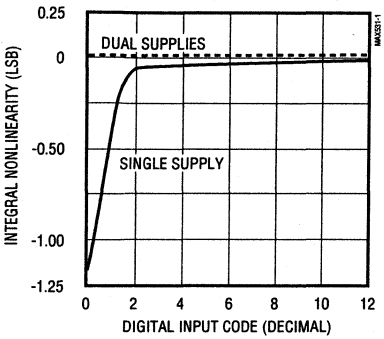
Note 2: In single-supply operation, INL and GE calculated from Code 11 to Code 4095. Tested at V_{DD} = 5V.
Note 3: Unipolar Offset Error is an input referred error. For a gain of 1, the output error is 500µV, while for a gain of 2 the output error is 1mV.
Note 4: Guaranteed by design.
Note 5: Tested at I_{OUT} = 100µA. The reference can typically source up to 5mA (see *Typical Operating Characteristics*).
Note 6: MAX531AC/AE/AM/BM reference tolerance over temp is guaranteed by 50ppm/°C max temperature coefficient.

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

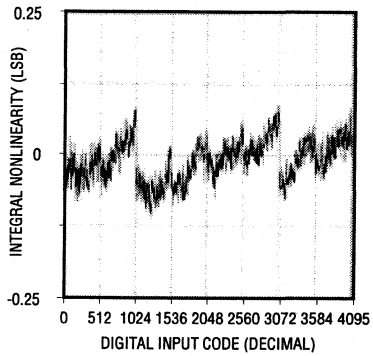
Typical Operating Characteristics

(V_{DD} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted.)

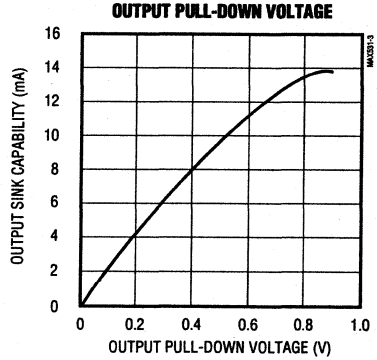
INTEGRAL NONLINEARITY vs.DIGITAL INPUT CODE (FIRST 12 CODES)



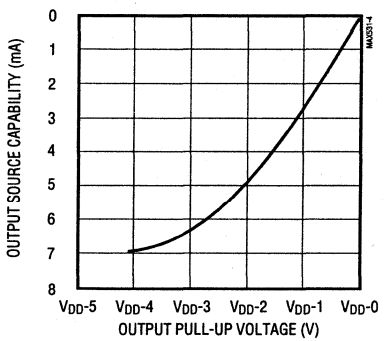
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (ALL CODES)



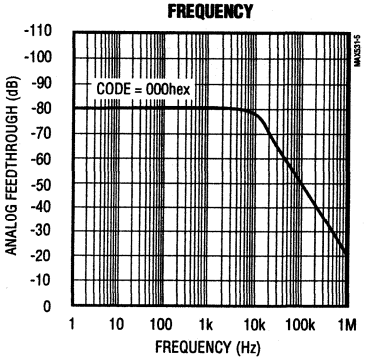
OUTPUT SINK CAPABILITY vs. OUTPUT PULL-DOWN VOLTAGE



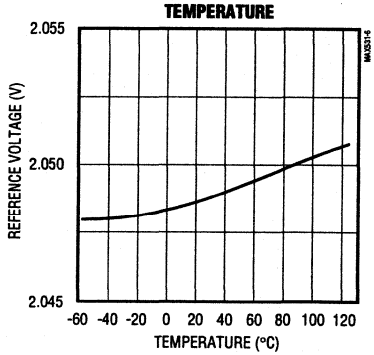
OUTPUT SOURCE CAPABILITY vs. OUTPUT PULL-UP VOLTAGE



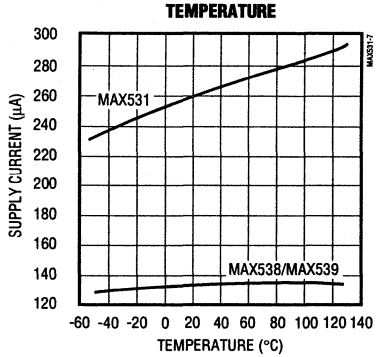
ANALOG FEEDTHROUGH vs. FREQUENCY



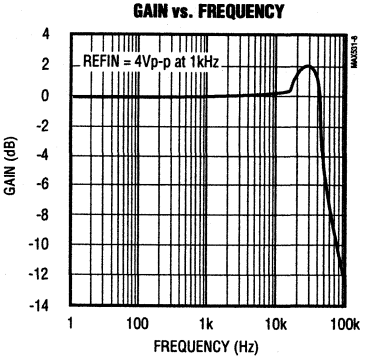
MAX531 REFERENCE VOLTAGE vs. TEMPERATURE



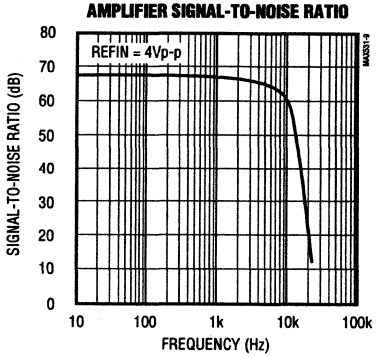
SUPPLY CURRENT vs. TEMPERATURE



MAX531 GAIN vs. FREQUENCY



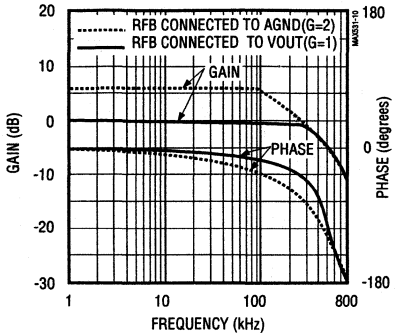
MAX531 AMPLIFIER SIGNAL-TO-NOISE RATIO



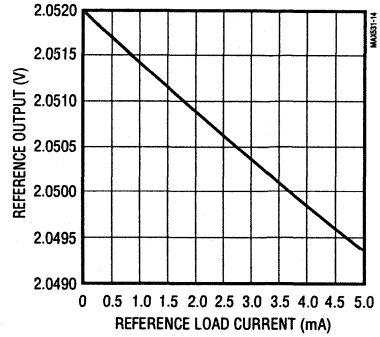
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{REFIN} = 2.048V, T_A = +25°C, unless otherwise noted.)

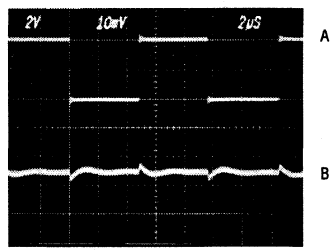
MAX531
GAIN AND PHASE vs. FREQUENCY



MAX531 REFERENCE OUTPUT VOLTAGE vs. REFERENCE LOAD CURRENT

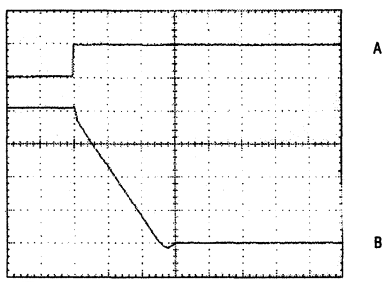


DIGITAL FEEDTHROUGH



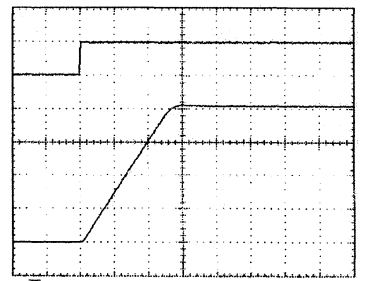
$\overline{CS}$ = HIGH
A: DIN = 4Vp-p, 100kHz
B: VOUT, 10mV/div
HORIZONTAL: 2µs/div

NEGATIVE SETTLING TIME (MAX531)



A: $\overline{CS}$ RISING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
HORIZONTAL: 5µs/div
DUAL SUPPLY ±5V

POSITIVE SETTLING TIME (MAX531)



A: $\overline{CS}$ RISING EDGE, 5V/div
B: VOUT, NO LOAD, 1V/div
HORIZONTAL: 5µs/div
DUAL SUPPLY ±5V

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5V, Low-Power, Voltage-Output Serial 12-Bit DACs

Pin Description

PIN		NAME	FUNCTION
MAX531	MAX538/ MAX539		
1	—	BIPOFF	Bipolar offset/gain resistor
2	1	DIN	Serial data input
3	—	$\overline{CLR}$	Clear. Asynchronously sets DAC register to 000hex.
4	2	SCLK	Serial clock input
5	3	$\overline{CS}$	Chip select, active low
6	4	DOUT	Serial data output for daisy-chaining
7	—	DGND	Digital ground
8	5	AGND	Analog ground
9	6	REFIN	Reference input
10	—	REFOUT	Reference output, 2.048V
11	—	V_{SS}	Negative power supply
12	7	VOUT	DAC output
13	8	V_{DD}	Positive power supply
14	—	RFB	Feedback resistor

Detailed Description

General DAC Discussion

The MAX531/MAX538/MAX539 use an "inverted" R-2R ladder network with a single-supply CMOS op amp to convert 12-bit digital data to analog voltage levels (see *Functional Diagram).* The term "inverted" describes the ladder network because the REFIN pin in current-output DACs is the summing junction, or virtual ground, of an op amp. However, such use would result in the output voltage being the inverse of the reference voltage. The MAX531/MAX538/MAX539's topology makes the output the same polarity as the reference input.

An internal reset circuit forces the DAC register to reset to 000hex on power-up. Additionally, a clear ($\overline{CLR}$) pin, when held low, sets the DAC register to 000hex. $\overline{CLR}$ operates asynchronously and independently from the chip select ($\overline{CS}$) pin.

Buffer Amplifier

The output buffer is a unity-gain stable, rail-to-rail output, BiCMOS op amp. Input offset voltage and CMRR are trimmed to achieve better than 12-bit performance. Settling time is 25µs to 0.01% of full scale. The output is short-circuit protected and can drive a 2kΩ load with more than 100pF load capacitance.

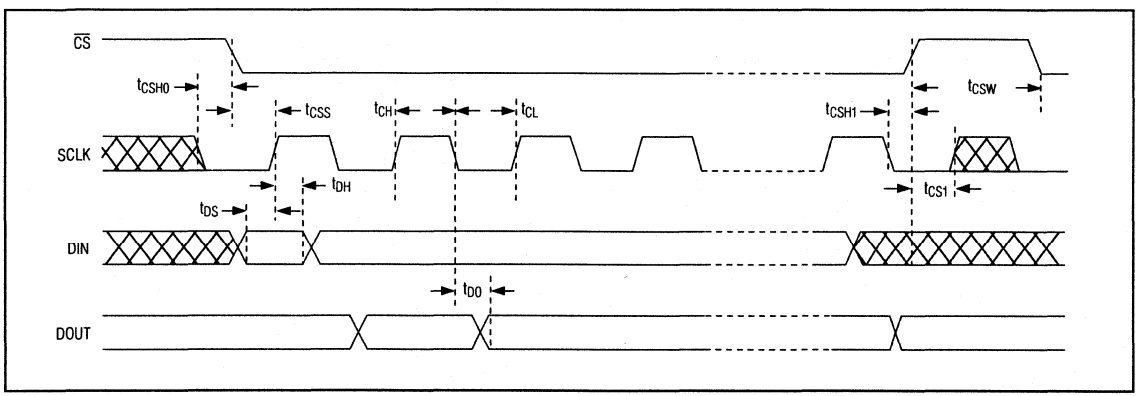

Figure 1. Timing Diagram

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

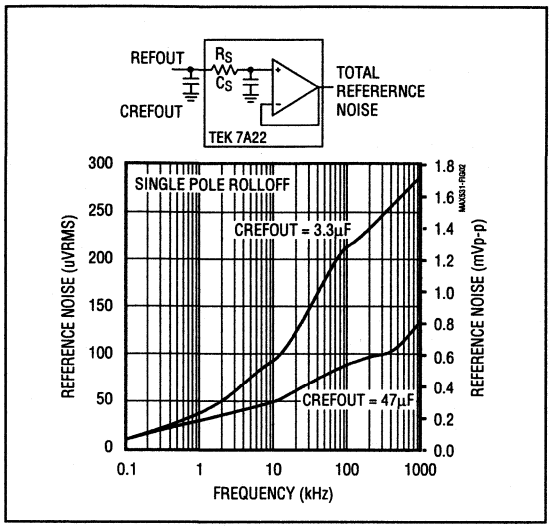

Figure 2. Reference Noise vs. Frequency

Internal Reference (MAX531 only)

To achieve the lowest-power design possible, the DAC ladder resistance has been set to approximately 80kΩ, which allows the internal reference circuit to be biased at about 100µA. The reference voltage is trimmed to 2.048V. In the MAX531, this reference is brought to an external pin and may be gained up or down, inverted, or connected to V_{DD} for a multiplying application. The reference output can source up to 5mA of external load current, and has an output resistance typically less than 1 ohm (2 ohms max).

For applications requiring very low-noise performance, connect a 33µF capacitor from REFOUT to AGND. If noise is not a concern, a lower value (3.3µF min) capacitor may be used. To reduce noise further, insert a buffered RC filter between REFOUT and REFIN (Figure 2). The reference bypass capacitor C_{REFOUT} is still required for reference stability. In applications not requiring the reference, connect REFOUT to V_{DD} or use the MAX538 or MAX539 (no internal reference).

External Reference

An external reference in the range (V_{SS} + 2V) to (V_{DD} - 2V) may be used with the MAX531 in dual-supply operation. With the MAX538/MAX539 or the MAX531 in single-supply use, the reference must be positive and may not exceed V_{DD} - 2V. The reference voltage determines the DAC's full-scale output. The DAC input resistance is code dependent and is minimum (40kΩ) at code 555hex and virtually infinite at code 000hex. REFIN's input capacitance is also code dependent and has a 50pF maximum value at several codes. Because of the code-dependent nature of reference input impedances, a high-quality, low output impedance amplifier (such as the MAX480 low-power, precision op amp) should be used.

If an upgrade to the internal reference is required, the 2.5V MAX873A is suitable: ±15mV initial accuracy, TCV_{OUT} = 7ppm/°C (max).

Logic Interface

The MAX531/MAX538/MAX539 logic inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, drive the digital inputs with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately 2.

Serial Clock and Update Rate

Figure 1 shows the MAX531/MAX538/MAX539 timing. The maximum serial clock rate is given by $1/(t_{CH}+t_{CL})$, approximately 14MHz. The digital update rate is limited by the chip-select period, which is 16 x SCLK periods plus the $\overline{CS}$ high pulse width t_{CSW}. This equals a 1.14µs, or 877kHz, update rate. However, the DAC settling time to 12 bits is 25µs, which may limit the update rate to 40kHz for full-scale step transitions.

Applications Information

Refer to Figures 3a and 3b for typical operating connections.

Serial Interface

The MAX531/MAX538/MAX539 use a three-wire serial interface that is compatible with SPI™, QSPI™ (CPOL = CPHA = 0), and Microwire™ standards as shown in Figures 4 and 5. The DAC is programmed by writing two 8-bit words (see Figure 1 and the *Functional Diagram*). 16 bits of serial data are clocked into the DAC MSB first with the MSB preceded by 4 fill (dummy) bits. The 4 dummy bits are not normally needed. They are required **only** when DACs are daisy-chained. Data is clocked in on SCLK's rising edge while $\overline{CS}$ is low. The serial input data is held in a 16-bit serial shift register. On $\overline{CS}$'s rising edge, the 12 least significant bits are transferred to the DAC register and update the DAC. With $\overline{CS}$ high, data cannot be clocked into the MAX531/MAX538/MAX539.

The MAX531/MAX538/MAX539 inputs data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks, thereby requiring two write cycles to input data to the DAC. The QSPI interface allows variable data input from 8 to 16 bits, and can be loaded into the DAC in one write cycle.

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

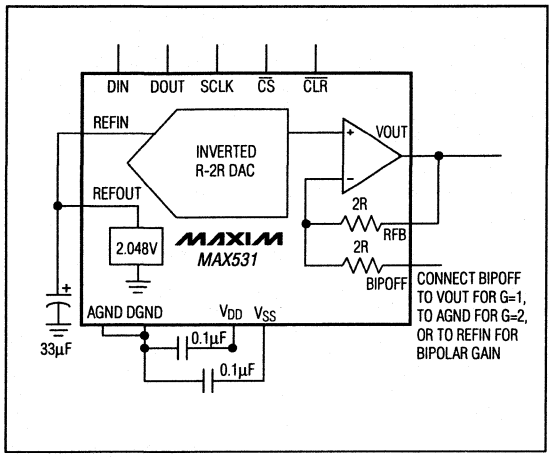

Figure 3a. MAX531 Typical Operating Circuit

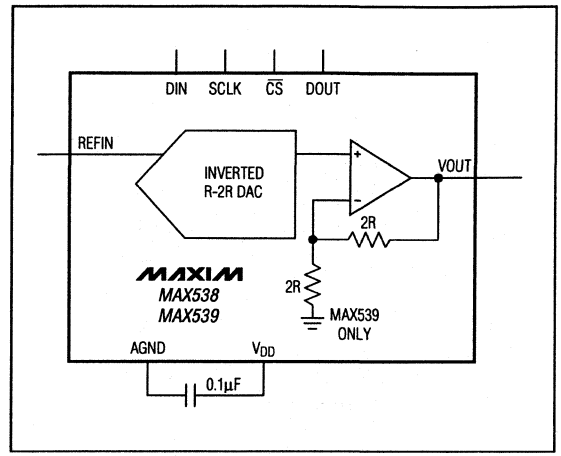

Figure 3b. MAX538/MAX539 Typical Operating Circuit

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT is a CMOS output that does not require an external pull-up resistor. DOUT does **not** go into a high-impedance state when $\overline{CS}$ is high. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of MAX531/MAX538/MAX539 DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain. For proper timing, ensure that t_{CSS0} ($\overline{CS}$ low to SCLK high) is greater than $t_{DV} + t_{DS}$.

Unipolar Configuration

The MAX531 is configured for a Gain = 1, 0V to +2.048V unipolar output range by connecting BIPOFF and RFB to VOUT (Figure 6). The converter operates from either single or dual supplies in this configuration. See Table 1 for the DAC-latch contents (input) vs. the analog VOUT (output). In this range, 1LSB = REFIN (2^{-12}). The MAX538 is internally configured for unipolar Gain = 1 operation.

A Gain = 2, 0V to 4.096V unipolar output range is set up by connecting BIPOFF to AGND and RFB to VOUT (Figure 7). Table 2 shows the DAC-latch contents vs. VOUT. The MAX531 operates from either single or dual supplies in this mode. In this range, 1LSB = $(2)(REFIN)(2^{-12}) = (REFIN)(2^{-11})$. The MAX539 is internally configured for unipolar Gain = 2 operation.

Bipolar Configuration

A bipolar range is set up by connecting BIPOFF to REFIN and RFB to VOUT, and operating from dual (±5V) supplies (Figure 8). Table 3 shows the DAC-latch contents (input) vs. VOUT (output). In this range, 1 LSB = REFIN (2^{-11}).

Four-Quadrant Multiplication

The MAX531 can be used as a four-quadrant multiplier by connecting BIPOFF to REFIN, using an offset binary or twos-complement digital code, and using dual power supplies and a bipolar analog input at REFIN within the range V_{SS} + 2V to V_{DD} - 2V, as shown in Figure 9.

In general, a 12-bit DAC's output is (D) (V_{REFIN}) (G), where "G" is the gain (1 or 2) and "D" is the binary representation of the digital input divided by 2^{12} or 4,096. This formula is precise for unipolar operation. However, for bipolar, twos-complement operation, the MSB is really a polarity bit. No resolution is lost, as there are the same number of steps. The output voltage, however, has been shifted from a range of, for example, 0V to 4.096V (G = 2) to a range of -2.048V to +2.048V.

Keep in mind that when using the DAC as a four-quadrant multiplier, the scale is skewed. Negative full scale is $-V_{REFIN}$, while positive full scale is $+V_{REFIN}$ - 1LSB.

™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

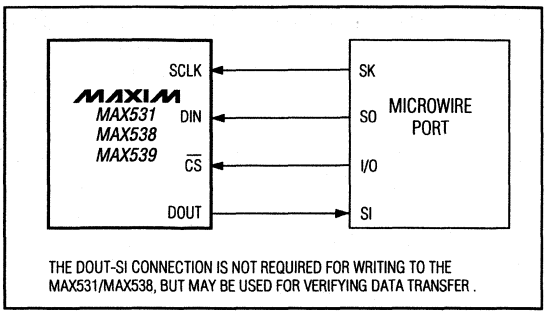

Figure 4. Microwire Connection

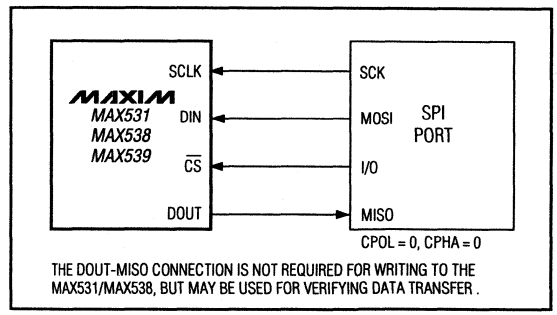

Figure 5. SPI/QSPI Connection

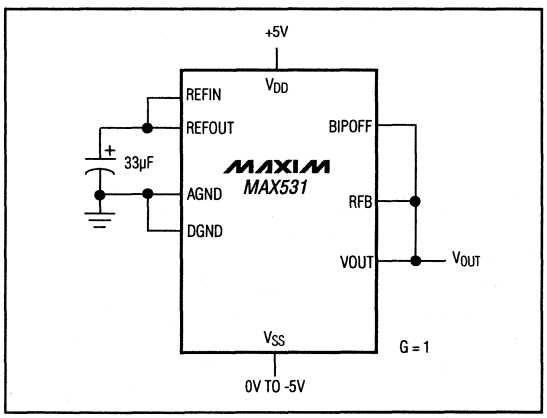

Figure 6. Unipolar Configuration (0V to +2.048V Output)

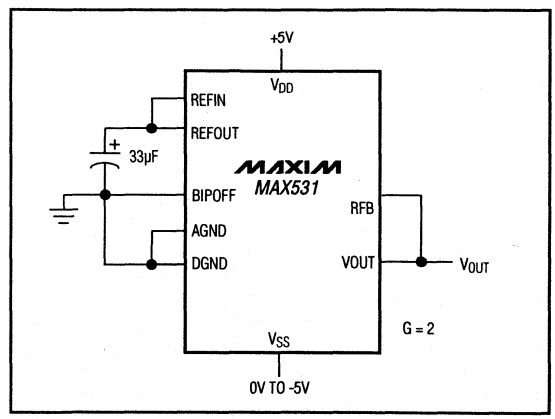

Figure 7. Unipolar Configuration (0V to +4.096V Output)

Table 1. Unipolar Code Table (0V to V_{REF} Output)
Gain = 1

INPUT	OUTPUT
1111 1111 1111	$(V_{REF})\frac{4095}{4096}$
1000 0000 0001	$(V_{REF})\frac{2049}{4096}$
1000 0000 0000	$(V_{REF})\frac{2048}{4096} = +V_{REF}/2$
0111 1111 1111	$(V_{REF})\frac{2047}{4096}$
0000 0000 0001	$(V_{REF})\frac{1}{4096}$
0000 0000 0000	0V

Table 2. Unipolar Code Table (0V to $2V_{REF}$ Output)
Gain = 2

INPUT	OUTPUT
1111 1111 1111	$+2\,(V_{REF})\frac{4095}{4096}$
1000 0000 0001	$+2\,(V_{REF})\frac{2049}{4096}$
1000 0000 0000	$+2\,(V_{REF})\frac{2048}{4096} = +V_{REF}$
0111 1111 1111	$+2\,(V_{REF})\frac{2047}{4096}$
0000 0000 0001	$+2\,(V_{REF})\frac{1}{4096}$
0000 0000 0000	0V

5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

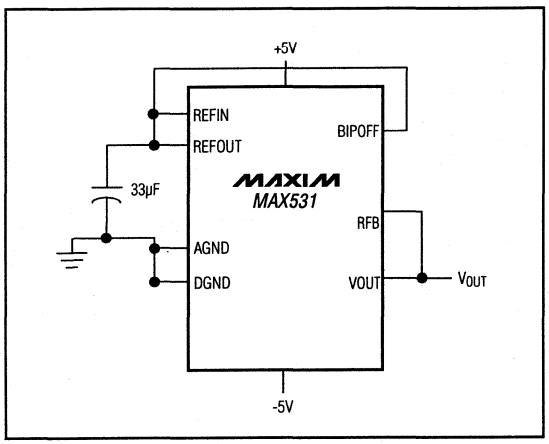

Figure 8. Bipolar Configuration (-2.048V to +2.048V Output)

Table 3. Bipolar Code Table (-VREF to +VREF Output)

INPUT	OUTPUT
1111 1111 1111	$(+V_{REF})\frac{2047}{2048}$
1000 0000 0001	$(+V_{REF})\frac{1}{2048}$
1000 0000 0000	0V
0111 1111 1111	$(-V_{REF})\frac{1}{2048}$
0000 0000 0001	$(-V_{REF})\frac{2047}{2048}$
0000 0000 0000	$(-V_{REF})\frac{2048}{2048} = -V_{REF}$

Single-Supply Linearity

As with any amplifier, the MAX531/MAX538/MAX539's output buffer can be positive or negative. When the offset is positive, it is easily accounted for (Figure 10). However, when the offset is negative, the buffer output cannot follow linearly when there is no negative supply. In that case, the amplifier output (VOUT) remains at ground until the DAC voltage is sufficient to overcome the offset and the output becomes positive. Normally, linearity is measured after accounting for zero error and gain error. Since, in single-supply operation, the actual value of a negative offset is unknown, it cannot be accounted for during test. Additionally, the output buffer amplifier exhibits a nonlinearity near-zero output when operating with a single supply. To account for this nonlinearity in the MAX531/MAX538/MAX539, linearity and gain error are measured from code 11 to code 4095. The output buffer's offset and nonlinear behavior do not affect monotonicity, and these DACs are guaranteed monotonic starting with code zero. In dual-supply operation, linearity and gain error are measured from code 0 to 4095.

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source.

DGND and AGND should be connected together at the chip. For the MAX531 in single-supply applications, connect VSS to AGND at the chip. The best ground connection may be achieved by connecting the DAC's DGND and AGND pins together and connecting that point to the system analog ground plane. If the DAC's DGND is connected to the system digital ground, digital noise may get through to the DAC's analog portion.

The power supply itself must be properly bypassed to prevent digital noise from creeping back into the analog circuitry. Figures 11a and 11b illustrate the grounding and bypassing scheme described. Power-supply bypass is shown with two capacitors to ensure a low impedance at a wide frequency range. All capacitors should have low equivalent series resistance (ESR). Ferrite beads may also be placed at the analog power-supply leads to further isolate the digital power lines. The ceramic capacitors should be mounted with short leads as close to the device as possible.

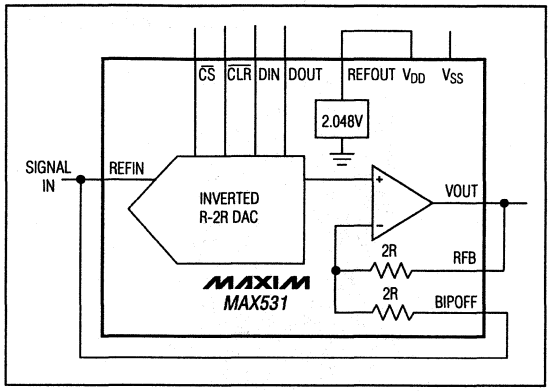

Figure 9. MAX531 Connected as Four-Quadrant Multiplier. The unused REFOUT is connected to V_{DD}.

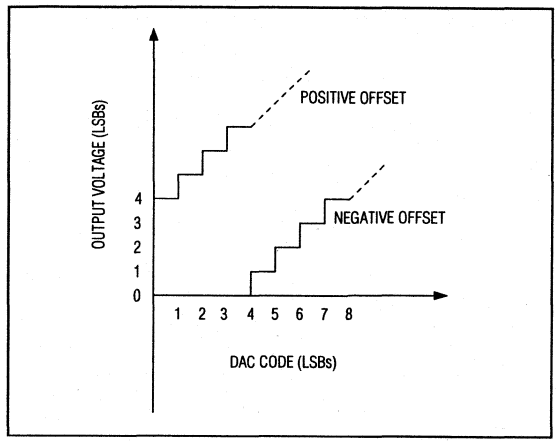

Figure 10. Single-Supply Offset

AC Considerations

Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package and cause internal stray capacitance to appear at the DAC output as noise, even though $\overline{CS}$ is held high (see *Typical Operating Characteristics*). This digital feedthrough is tested by holding $\overline{CS}$ high transmitting 555hex from DIN to DOUT.

Analog Feedthrough

Because of internal stray capacitance, higher frequency analog input may couple to the output as shown in the Analog Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. It is tested by sweeping an analog input with $\overline{CS}$ not asserted and DIN set to 000hex.

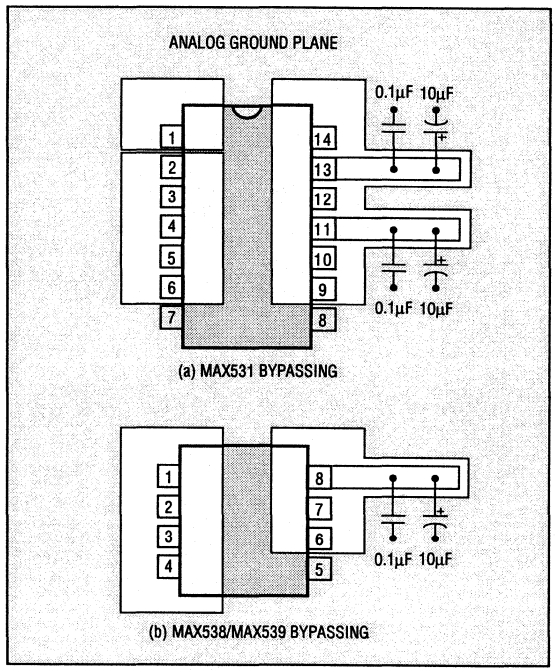

Figure 11. Power-Supply Bypassing

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5V, Low-Power, Voltage-Output, Serial 12-Bit DACs

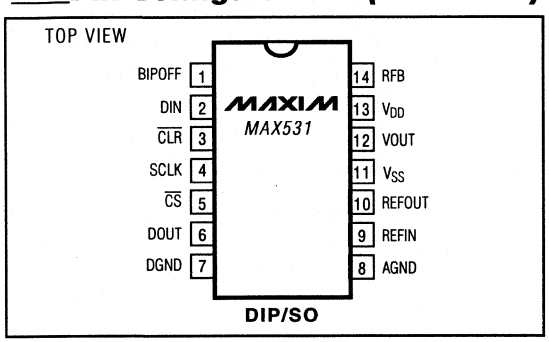
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX531AEPD	-40°C to +85°C	14 Plastic DIP	±1/2
MAX531BEPD	-40°C to +85°C	14 Plastic DIP	±1
MAX531AESD	-40°C to +85°C	14 SO	±1/2
MAX531BESD	-40°C to +85°C	14 SO	±1
MAX531AMJD	-55°C to +125°C	14 CERDIP**	±1
MAX531BMJD	-55°C to +125°C	14 CERDIP**	±2
MAX538ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX538BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX538ACSA	0°C to +70°C	8 SO	±1/2
MAX538BCSA	0°C to +70°C	8 SO	±1
MAX538BC/D	0°C to +70°C	Dice*	±1
MAX538AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX538BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX538AESA	-40°C to +85°C	8 SO	±1/2
MAX538BESA	-40°C to +85°C	8 SO	±1
MAX538AMJA	-55°C to +125°C	8 CERDIP**	±1
MAX538BMJA	-55°C to +125°C	8 CERDIP**	±2
MAX539ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX539BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX539ACSA	0°C to +70°C	8 SO	±1/2
MAX539BCSA	0°C to +70°C	8 SO	±1
MAX539BC/D	0°C to +70°C	Dice*	±1
MAX539AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX539BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX539AESA	-40°C to +85°C	8 SO	±1/2
MAX539BESA	-40°C to +85°C	8 SO	±1
MAX539AMJA	-55°C to +125°C	8 CERDIP**	±1
MAX539BMJA	-55°C to +125°C	8 CERDIP**	±2

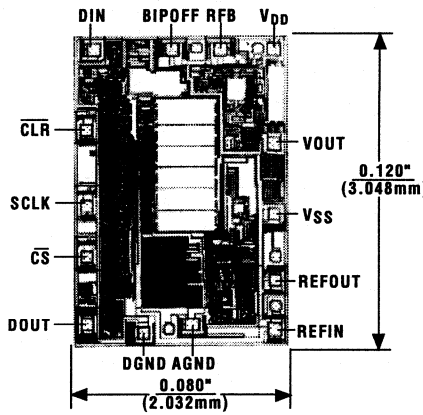
* *Dice are tested at T_A = +25°C only.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



Chip Topography



TRANSISTOR COUNT: 922;
SUBSTRATE CONNECTED TO V_{DD}.

19-0046; Rev. 1; 3/94

MAXIM

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

General Description

The MAX532 is a complete, dual, serial-input, 12-bit multiplying digital-to-analog converter (MDAC) with output amplifiers. No external user trims are required to achieve full specified performance. The MAX532's 3-wire serial interface minimizes the number of package pins, so it uses less board space than parallel-interface parts. The interface is SPI™, QSPI™ and Microwire™ compatible. A serial output, DOUT, allows cascading of two or more MAX532s and read-back of the data written to the device.

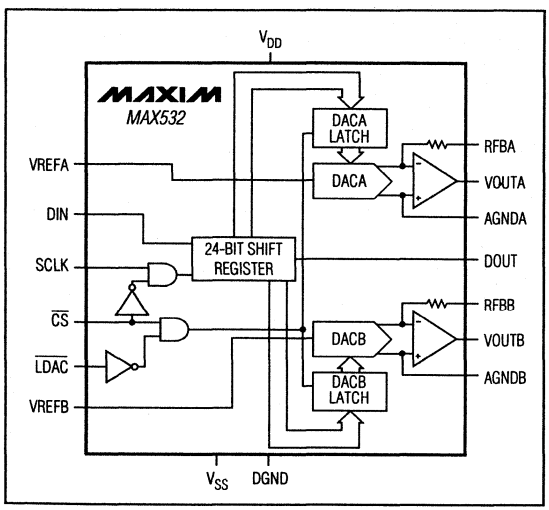
The device's serial interface minimizes digital-noise feedthrough from its logic pins to its analog outputs. Serial interfacing also simplifies opto-coupler-isolated or transformer-isolated applications.

The MAX532 is specified with ±12V to ±15V power supplies. All logic inputs are TTL and CMOS compatible. It comes in space-saving 16-pin DIP and wide SO packages.

Applications

Automatic Test Equipment
Arbitrary Waveform Generators
Programmable-Gain Amplifiers
Motion Control Systems
Servo Controls

Functional Diagram



Features

- ♦ **Two 12-Bit MDACs with Output Amplifiers**
- ♦ **Fast, 6MHz 3-Wire Interface**
- ♦ **SPI, QSPI, and Microwire Compatible**
- ♦ **±12V Output Swing**
- ♦ **±10mA Output Current**
- ♦ **2.5µs Settling Time to ±1/2LSB**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Low Integral Nonlinearity: ±1/2LSB Max**
- ♦ **Low Gain Tempco: 2ppm/°C**
- ♦ **Operates from ±12V to ±15V Supplies**
- ♦ **Power-On Reset**
- ♦ **Available in 16-Pin DIP and Wide SO Packages**

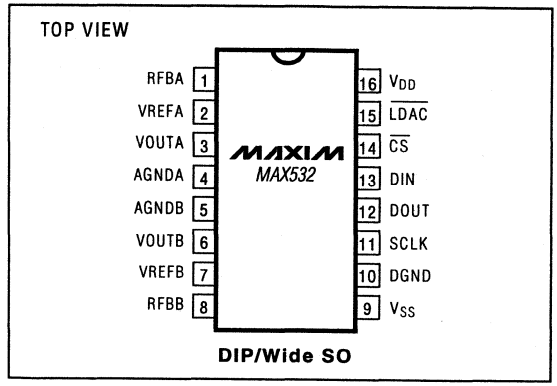
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX532ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX532BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX532ACWE	0°C to +70°C	16 Wide SO	±1/2
MAX532BCWE	0°C to +70°C	16 Wide SO	±1
MAX532BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Pin Configuration



DIP/Wide SO

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Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V_{DD} to DGND, AGNDA, AGNDB ..... -0.3V to +17V
- V_{SS} to DGND, AGNDA, AGNDB (Note 1) ..... +0.3V to -17V
- VREFA, VREFB ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- AGNDA, AGNDB ..... (DGND - 0.3V) to (V_{DD} + 0.3V)
- VOUTA, VOUTB ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- RFBA, RFBB ..... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
- SCLK, DIN, DOUT, $\overline{LDAC}$, $\overline{CS}$ .. (DGND - 0.3V) to (V_{DD} + 0.3V)

DOUT Sink Current 20mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Wide SO (derate 9.52mW/°C above +70°C) 762mW
- CERDIP (derate 10.00mW/°C above +70°C) 800mW

Operating Temperature Ranges:
- MAX532_C__ ..... 0°C to +70°C
- MAX532_E__ ..... -40°C to +85°C
- MAX532_MJE ..... -55°C to +125°C

Junction Temperatures:
- MAX532_C__, E__ ..... +150°C
- MAX532_MJE ..... +175°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: If V_{SS} is open-circuited with V_{DD} and either AGND applied, the V_{SS} pin will float positive, exceeding the Absolute Maximum Ratings. A Schottky diode connected between V_{SS} and GND ensures the maximum ratings will not be exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)							
Resolution				12			Bits
Relative Accuracy	INL		MAX532A			±1/2	LSB
			MAX532B			±1	
Differential Nonlinearity		Guaranteed monotonic				±1	LSB
Zero-Code Offset Error		DAC latch loaded with all 0s	T_A = +25°C, MAX532_			±2	mV
			T_A = T_{MIN} to T_{MAX}, MAX532A			±3	
			T_A = T_{MIN} to T_{MAX}, MAX532B			±4	
Zero-Code Offset Temperature Coefficient		DAC latch loaded with all 0s			±5		µV/°C
Gain Error		T_A = +25°C, DAC latch loaded with all 1s	MAX532A			±2	LSB
			MAX532B			±5	
		T_A = T_{MIN} to T_{MAX}, DAC latch loaded with all 1s	MAX532A			±4	
			MAX532B			±7	
Gain-Error Temperature Coefficient					±2		ppm/°C of FSR
REFERENCE INPUTS (VREFA, VREFB)							
VREFA, VREFB Input Resistance				8	10	13	kΩ
VREFA, VREFB Input Resistance Matching					±0.5	±3.0	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{LDAC}$, $\overline{CS}$)						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}				0.8	V
Input Current		Digital inputs at 0V or V_{DD}			±1	µA
Input Capacitance (Note 2)					8	pF
DIGITAL OUTPUT (DOUT) (Note 3)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA		0.08	0.4	V
		I_{SINK} = 16mA		0.2		
Output High Leakage	I_{LKG}	V_{DOUT} = 0V to V_{DD}			±10	µA
Output High Capacitance (Note 2)	C_{OUT}				15	pF
ANALOG OUTPUTS (VOUTA, VOUTB)						
DC Output Impedance				0.2		Ω
Short-Circuit Current		VOUTA, VOUTB connected to AGNDA, AGNDB		20		mA
Output Voltage Swing			(V_{DD} - 2.5) to (V_{SS} + 2.5)			V
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		11.4		16.5	V
Negative Supply Voltage	V_{SS}		-11.4		-16.5	V
Power-Supply Rejection	PSR	ΔFull scale/ΔV_{DD}, V_{DD} = 11.4V to 16.5V, VREF = -8.9V, DAC latches loaded with all 1s			±0.035	LSB/%
		ΔFull scale/ΔV_{SS}, V_{SS} = -11.4V to -16.5V, VREF = 8.9V, DAC latches loaded with all 1s			±0.035	
Positive Supply Current	I_{DD}	Output unloaded		5	10	mA
Negative Supply Current	I_{SS}	Output unloaded		4	6	mA
AC CHARACTERISTICS						
Voltage-Output Settling Time		Settling time to within 1/2 LSB of final DAC value; DAC latch alternately loaded with all 0s and all 1s		2.5		µs
Slew Rate				8		V/µs
Digital-to-Analog Glitch Impulse		DAC latch alternately loaded with 011...11 and 100...00		60		nV-s
Channel-to-Channel Isolation		VREFA to VOUTB; VREFA = $20V_{p-p}$ 10kHz sine wave; DAC latches loaded with all 0s		-100		dB
		VREFB to VOUTA; VREFB = $20V_{p-p}$ 10kHz sine wave; DAC latches loaded with all 0s		-100		

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V, VREFA and VREFB = +10V, R_L = 2kΩ, C_L = 100pF, VOUT_ connected to RFB_, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Multiplying Feedthrough Error		VREF = $20V_{p-p}$ 10kHz sine wave; DAC latch loaded with all 0s		-77		dB
Unity-Gain Small-Signal Bandwidth		VREF = $100mV_{p-p}$ sine wave; DAC latch loaded with all 1s		1.0		MHz
Full-Power Bandwidth		VREF = $20V_{p-p}$ sine wave; DAC latch loaded with all 1s		125		kHz
Total Harmonic Distortion	THD	VREF = $6V_{RMS}$, 1kHz sine wave; DAC latch loaded with all 1s		-90		dB
Digital Feedthrough		$\overline{CS}$ = 1; transitions on SCLK, $\overline{LDAC}$, DIN		1.1		nV-s
Digital Crosstalk		DACA code all 1s, DACB code transition from all 0s to all 1s		10		nV-s
Output Noise Voltage		0.1Hz to 10Hz		2		μV_{RMS}

Note 1: Static performance tested at V_{DD} = +15V, V_{SS} = -15V. Performance over supplies guaranteed by PSR test.
Note 2: Guaranteed by design. Not subject to production testing.
Note 3: Open-drain output.

TIMING CHARACTERISTICS

(V_{DD} = 11.4V to 16.5V, V_{SS} = -11.4V to -16.5V, AGNDA = AGNDB = DGND = 0V) (Notes 4, 5)

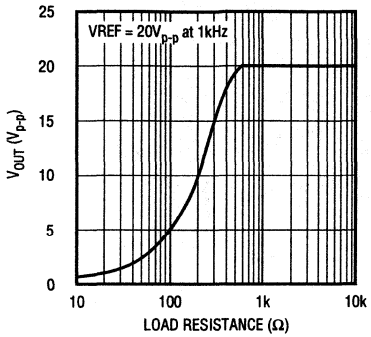
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Frequency	f_{CLK}				6.25	MHz
SCLK Pulse Width High	t_{CH}		80			ns
SCLK Pulse Width Low	t_{CL}		80			ns
DIN to SCLK Rise Setup Time	t_{DS}		50			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS0}		50			ns
$\overline{CS}$ Rise to SCLK Rise Setup Time	t_{CSS1}		50			ns
SCLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		5			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH1}		80			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		120			ns
SCLK Fall to DOUT Valid (Note 6)	t_{DO}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V	0		200	ns
$\overline{CS}$ Fall to DOUT Enable (Note 7)	t_{DV}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V			100	ns
$\overline{CS}$ Rise to DOUT Disable (Note 7)	t_{TR}	C_L = 20pF, $R_{PULL-UP}$ = 1kΩ to 5V			60	ns
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}		60			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Fall Setup Time	t_{LDACS}		100			ns

Note 4: All input signals are specified with t_R = t_F ≤ 5ns. Logic input swing is 0V to 5V.
Note 5: See Figure 1.
Note 6: Timing is for SCLK fall to DOUT fall to 0.8V, or for SCLK fall to DOUT rise to 2.4V. Additional time must be added for any larger passive RC pull-up delay.
Note 7: DOUT enable: DOUT falls to 4.5V from 5.0V. DOUT disable: DOUT rises to 0.5V from 0V.

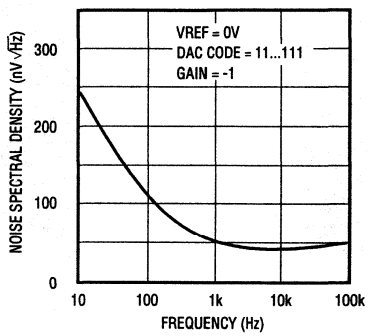
Typical Operating Characteristics

(V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

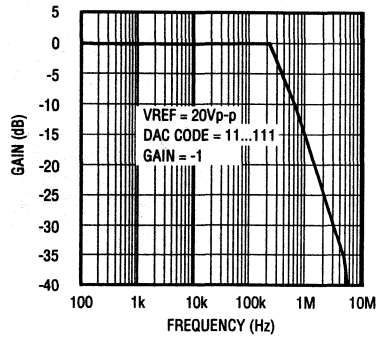
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



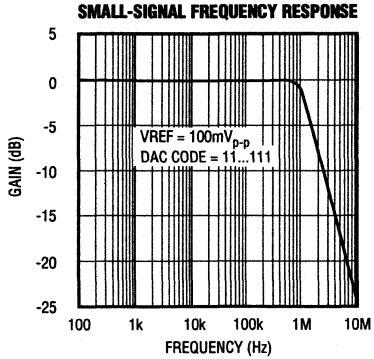
NOISE SPECTRAL DENSITY



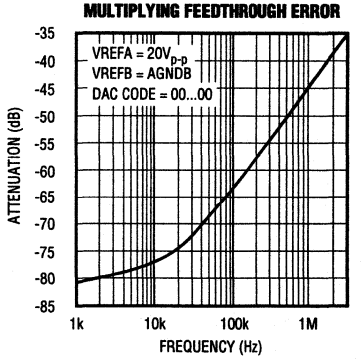
LARGE-SIGNAL FREQUENCY RESPONSE



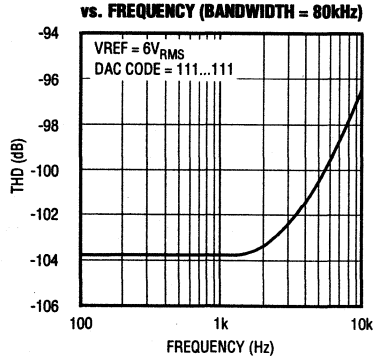
SMALL-SIGNAL FREQUENCY RESPONSE



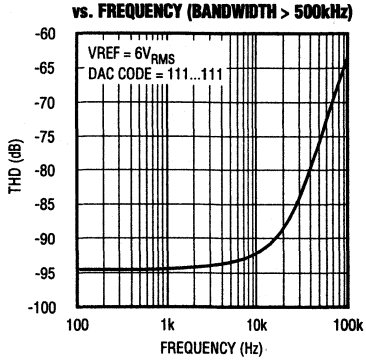
MULTIPLYING FEEDTHROUGH ERROR



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH = 80kHz)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (BANDWIDTH > 500kHz)



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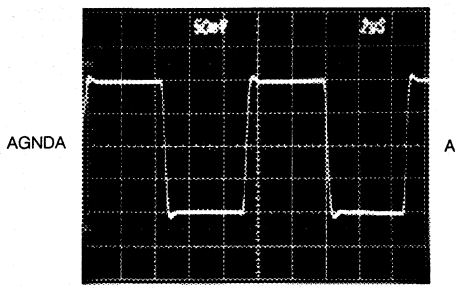
Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Typical Operating Characteristics (continued)

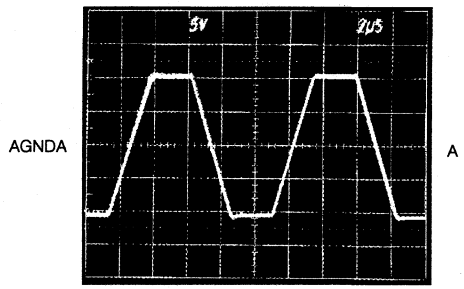
(V_{DD} = 15V, V_{SS} = -15V, R_L = 2kΩ, C_L = 100pF, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE



A = V_{OUTA}, 50mV/div
TIMEBASE = 2µs/div
V_{REFA} = ±100mV SQUARE WAVE

LARGE-SIGNAL PULSE RESPONSE



A = VOUTA, 5V/div
TIMEBASE = 2µs/div
VREFA = ±10V SQUARE WAVE

Pin Description

PIN	NAME	FUNCTION
1	RFBA	Feedback Resistor for DACA
2	VREFA	Reference Input for DACA
3	VOUTA	Voltage Output for DACA
4	AGNDA	Analog Ground for DACA
5	AGNDB	Analog Ground for DACB
6	VOUTB	Voltage Output for DACB
7	VREFB	Reference Input for DACB
8	RFBB	Feedback Resistor for DACB
9	V_{SS}	Negative Supply Voltage
10	DGND	Digital Ground
11	SCLK	Serial Clock Input
12	DOUT	Serial Data Output. Open-drain N-channel MOSFET output: requires external pull-up resistor. Data on DOUT changes on the falling edge of SCLK. Serial output data is delayed 24 clock cycles from DIN.
13	DIN	Serial Data Input. CMOS- and TTL-compatible input. Data is clocked into DIN on the rising edge of SCLK. $\overline{CS}$ must be low for data to be clocked in.
14	$\overline{CS}$	Chip-Select Input, active low. Data is shifted in and out when $\overline{CS}$ is low. DAC latches are updated when $\overline{CS}$ is high and $\overline{LDAC}$ is low.
15	$\overline{LDAC}$	Asynchronous Load DAC Input, active low. DAC latches are updated when $\overline{CS}$ is high and $\overline{LDAC}$ is low.
16	V_{DD}	Positive Supply Voltage

Timing Diagrams

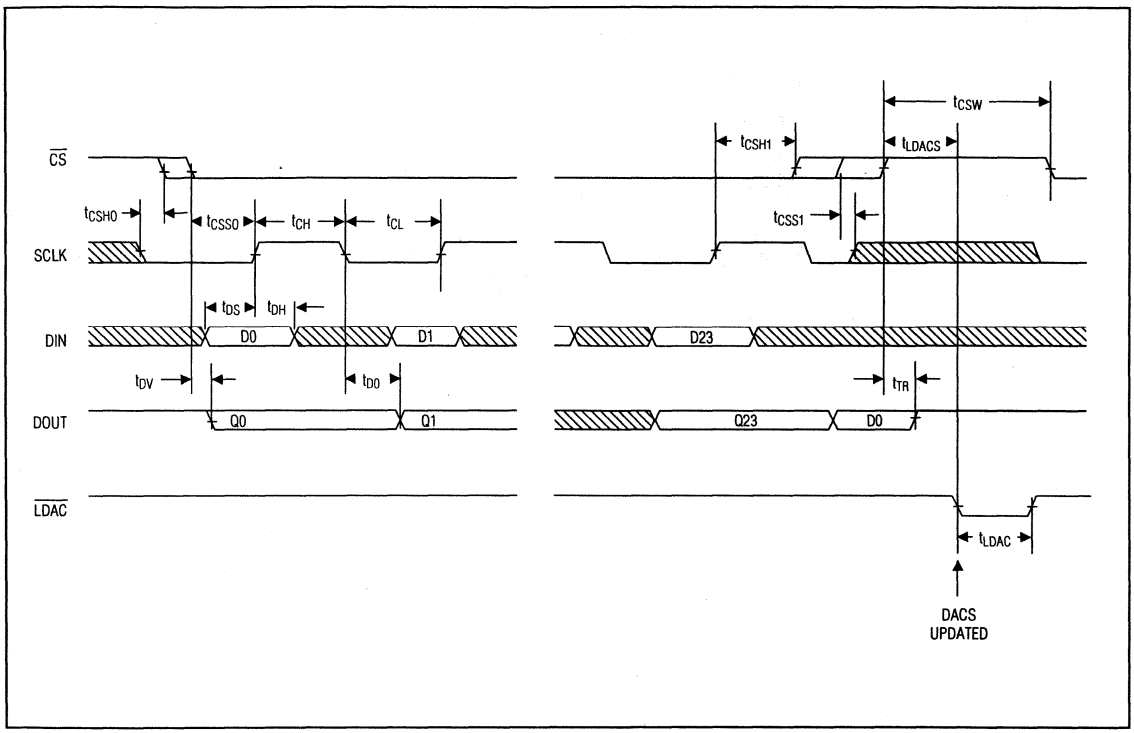


Figure 1. Timing Diagram

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Timing Diagrams (continued)

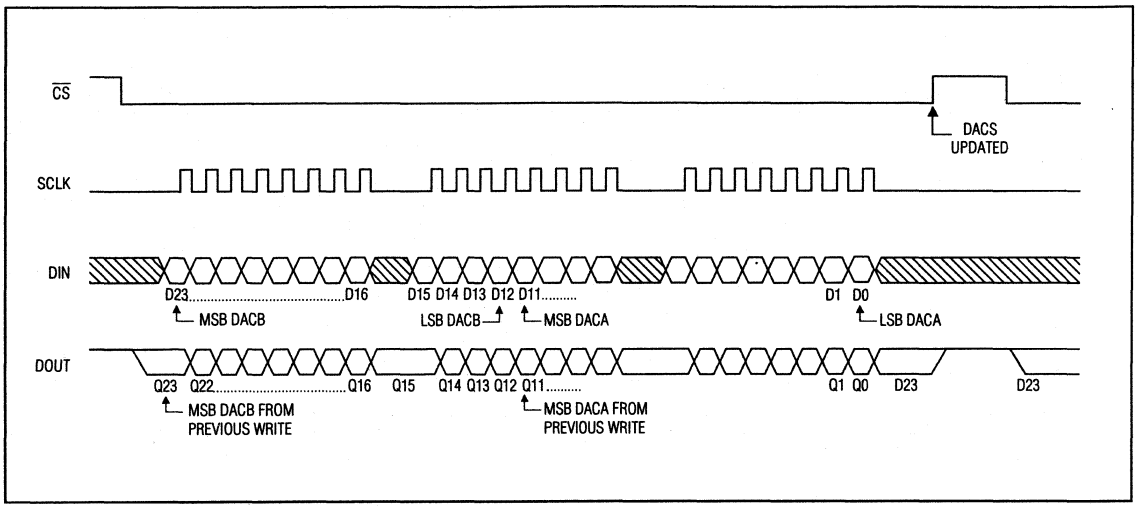


Figure 2. 3-Wire Interface Timing Diagram ($\overline{LDAC}$ = DGND)

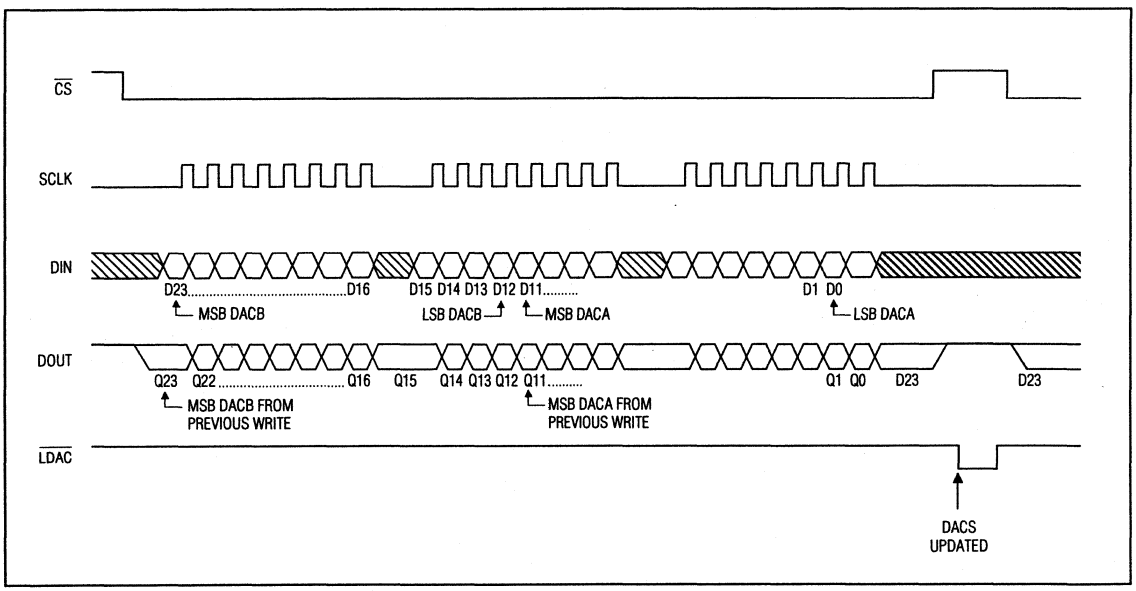


Figure 3. 4-Wire Inferface Timing Diagam

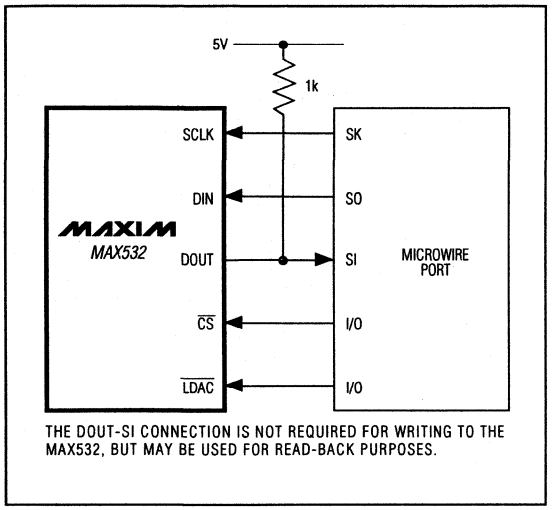


Figure 4. Connections for Microwire

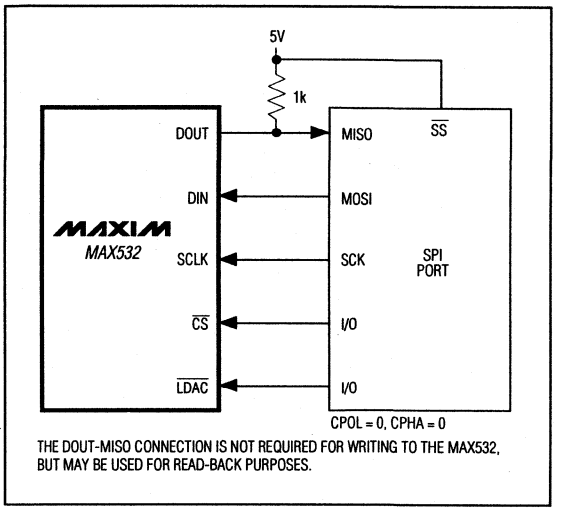


Figure 5. Connections for SPI

Detailed Description

Digital Interface

The MAX532 is Microwire and SPI compatible (Figures 4 and 5). Both DACs are programmed by writing three 8-bit words (see Figures 2 and 3, and the *Functional Diagram*). Serial data is clocked into the data registers MSB first, with DACB information preceding DACA information. Data is clocked in on the rising edge of SCLK while $\overline{CS}$ is low. With $\overline{CS}$ high, data can not be clocked into DIN, and DOUT is high impedance. SCLK can be driven at rates up to 6.25MHz.

The MAX532 uses either a 3-wire or a 4-wire serial interface. Three wires may be used ($\overline{CS}$, DIN, SCLK) by tying $\overline{LDAC}$ low. With $\overline{LDAC}$ low, the DACs are updated simultaneously when $\overline{CS}$ goes high (see Figure 2 and the *Functional Diagram*). The 3-wire interface may be used if the MAX532 is used alone, or if two or more MAX532s are cascaded (DOUT of one device tied to DIN of the other) (Figure 6).

The 4-wire interface ($\overline{LDAC}$, $\overline{CS}$, DIN, SCLK) is required if several serial devices are tied to the same data line, and it is desirable to update them simultaneously (Figure 7). With the 4-wire interface, the DACs are updated when $\overline{LDAC}$ goes low (see Figure 3 and the *Functional Diagram*).

A serial output, DOUT, allows cascading of two or more MAX532s and allows read-back of the data written to the device's 24-bit shift register. The data at DOUT is delayed 24 clock cycles from the data at DIN (see Figures 2 and 3, and the *Functional Diagram*). DOUT is an open-drain N-channel MOSFET that requires an external pull-up resistor (typically 1kΩ if pulled up to +5V, and 3kΩ if pulled up to +12V or +15V). Logic levels are guaranteed with sink currents up to 5mA (see *Electrical Characteristics*). Output data changes on the falling edge of SCLK when $\overline{CS}$ is low. If $\overline{CS}$ is high, DOUT is three-state (high-impedance).

Daisy-Chaining Devices

Any number of MAX532s can be daisy-chained by connecting the DOUT pin of one device (with a pull-up resistor) to the DIN pin of the following device in the chain (Figure 6).

When daisy-chaining devices, t_{CSS0} ($\overline{CS}$ low to SCLK high), must be the greater of $t_{DV} + t_{DS}$ or $t_{DS} + (t_{RC} + t_{TR} - t_{CS})$, where t_{CSW} is the $\overline{CS}$ pulse width used in the system and the term $(t_{RC} + t_{TR} - t_{CSW})$ accounts for the time spent charging the DOUT capacitance with the external pull-up resistor. So, for $t_{RC} < 250ns$, t_{CSS0} is simply $t_{DV} + t_{DS}$. Calculate t_{RC} using the following equation:

$$t_{RC} = R_P \times C \times \ln (V_{PULL\text{-}UP}/(V_{PULL\text{-}UP} - 2.4V))$$

where $V_{PULL\text{-}UP}$ is the voltage that the pull-up resistor is connected to, R_P is the value of the pull-up resistor, and C is the capacitance at DOUT. Values of t_{RC} are given in Table 1.

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

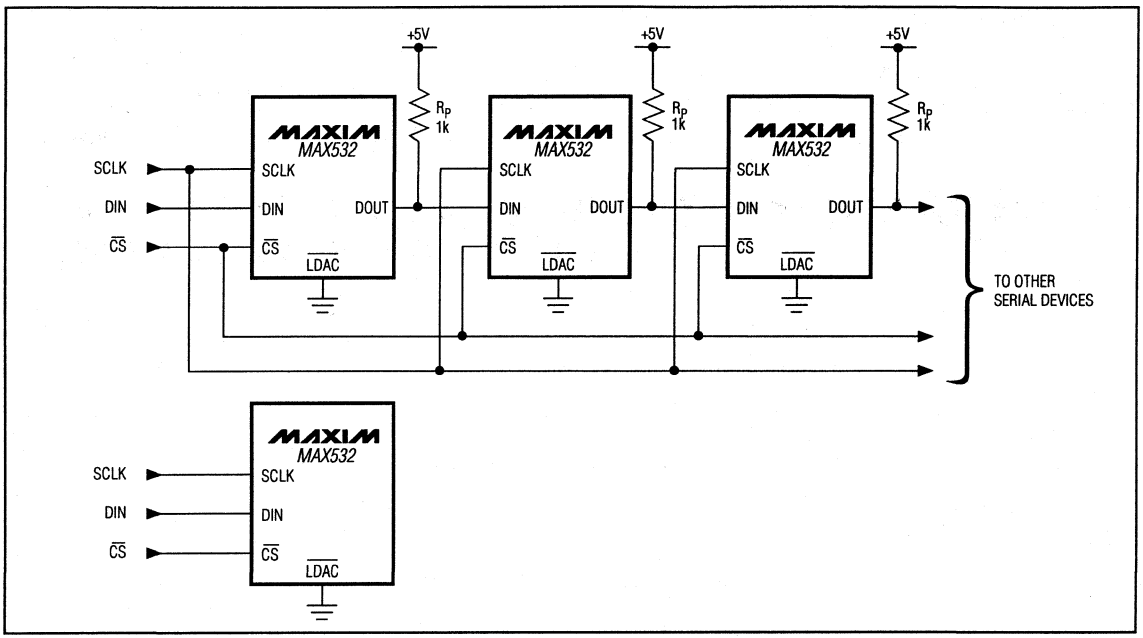


Figure 6. Daisy-chained or individual MAX532s are simultaneously updated by bringing $\overline{CS}$ high when using the 3-wire interface ($\overline{LDAC}$ = DGND).

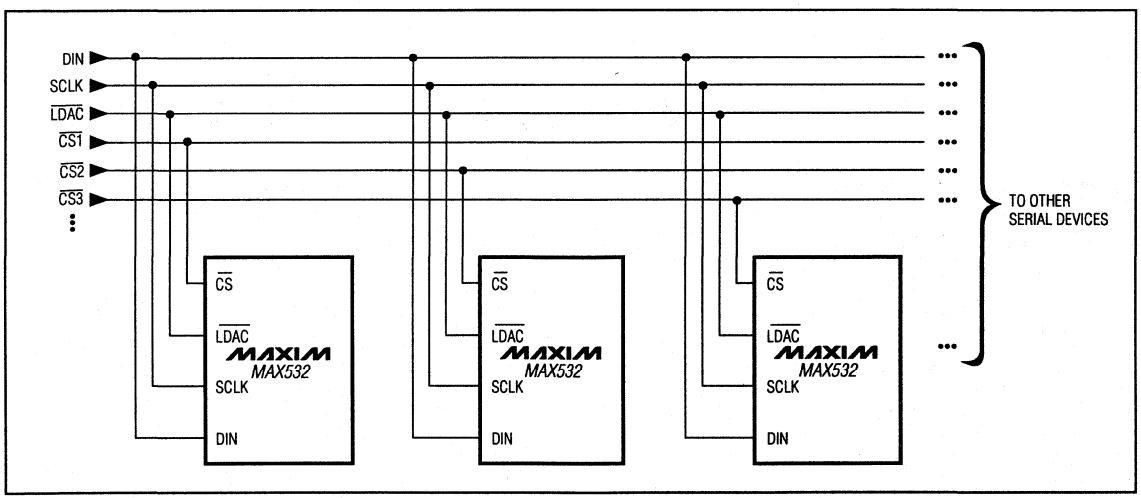


Figure 7. Multiple devices sharing a common DIN line may be simultaneously updated by bringing $\overline{LDAC}$ low. CS1, CS2, CS3, . . ., are driven separately, thus controlling which data are written to devices 1, 2, 3, ...

Table 1. t_{RC} Delay Times

$V_{PULL-UP}$ (V)	C (pF)	Rp (kΩ)	t_{RC} (ns)
4.5	20	1	15
4.5	35	1	27
4.5	50	1	38
4.5	100	1	76
4.5	150	1	114
11.4	20	3	14
11.4	35	3	25
11.4	50	3	35
11.4	100	3	71
11.4	150	3	106
13.5	20	3	12
13.5	35	3	21
13.5	50	3	29
13.5	100	3	59
13.5	150	3	88

With the values of t_{RC} given in Table 1, t_{CSS0} is always given by $t_{DV} + t_{DS}$. For different values of R or C, t_{RC} must be calculated to determine t_{CSS0}.

Additionally, the maximum clock frequency is limited to

$$f_{CLK}(max) = \frac{1}{2 \times (t_{DO} + t_{RC} - 15ns + t_{DS})}.$$

For example, with t_{RC} = 15ns (5V ±10% supply with 1kΩ pull-up), the maximum clock frequency is 2MHz.

Digital-to-Analog Section

Figure 8 shows a simplified circuit diagram for one of the DACs and the output amplifier.

A segmented scheme is used to improve linearity, whereby the two MSBs of the 12-bit data word are decoded to drive the three switches, SA, SB, and SC. The remaining ten bits drive the switches S0 through S9 in a standard R-2R ladder configuration.

Each of the switches, SA, SB, and SC, steers 1/4 of the total reference current with the remaining 1/4 passing through the R-2R section.

The output amplifier and feedback resistor perform the current-to-voltage conversion, giving the following:

$$VOUT\_ = -D \times VREF\_,$$

where _ denotes A or B, and D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

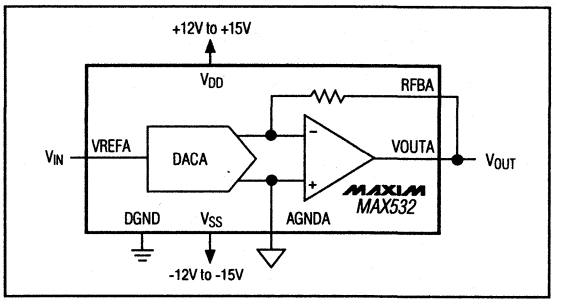


Figure 9. Unipolar Binary Operation

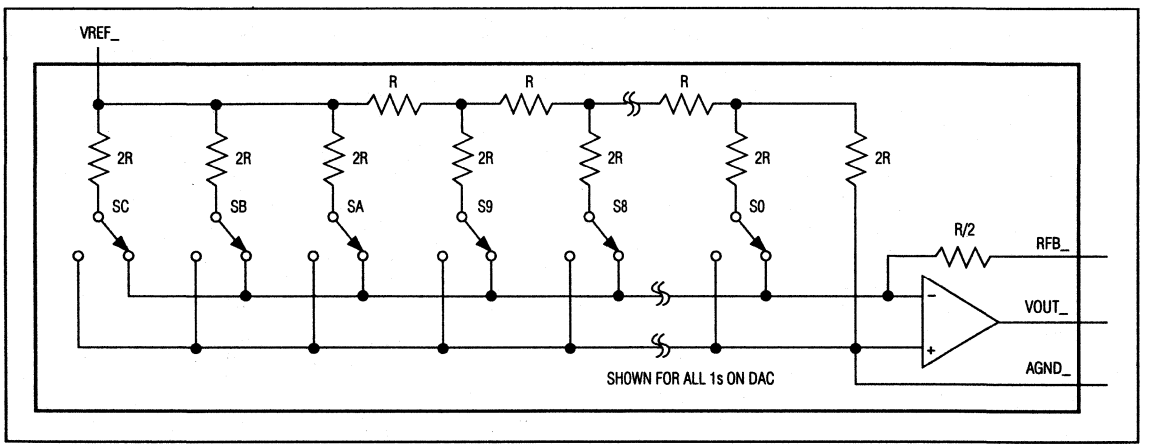


Figure 8. Simplified D/A Circuit Diagram

Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Output Amplifiers

The output amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 100pF. They are internally compensated, and settle to ±0.01% FSR (1/2LSB) in 2.5µs.

Unipolar Configuration

Figure 9 shows DACA connected for unipolar binary operation. Similar connections apply for DACB. When V_{IN} is an AC signal, the circuit performs two-quadrant multiplication. Table 2 shows the codes for this circuit.

Bipolar Operation

Figure 10 shows the MAX532 connected for bipolar operation. The coding is offset binary, as shown in Table 3. When V_{IN} is an AC signal, the circuit performs four-quadrant multiplication. To maintain gain error specifications, resistors R1, R2, and R3 should be ratio-matched to 0.01%.

Applications Information

Layout, Grounding, and Bypassing

For best system performance, use printed circuit boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be tied together at the low-impedance power-supply source, as shown in Figure 11.

The board layout should ensure that digital and analog signal lines are kept separate from each other as much as possible. Do not run analog and digital lines parallel to one another.

The output amplifiers are sensitive to high-frequency noise in the V_{DD} and V_{SS} power supplies. Bypass these supplies to the analog ground plane with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best noise rejection.

Table 2. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN}$ x (4095/4096)
1000 0000 0000	$-V_{IN}$ x (2048/4096) = $-1/2V_{IN}$
0000 0000 0001	$-V_{IN}$ x (1/4096)
0000 0000 0000	0V

1LSB = V_{IN}/4096

Table 3. Bipolar Code Table

DAC Latch Contents MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}$ x (2047/2048)
1000 0000 0001	$+V_{IN}$ x (1/2048)
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}$ x (1/2048)
0000 0000 0000	$-V_{IN}$ + (2048/2048) = $-V_{IN}$

1LSB = V_{IN}/2048

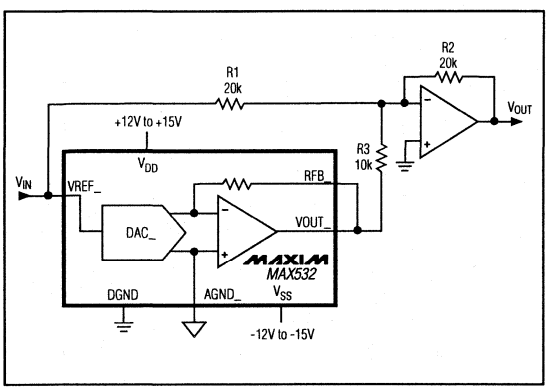


Figure 10. Bipolar Operation

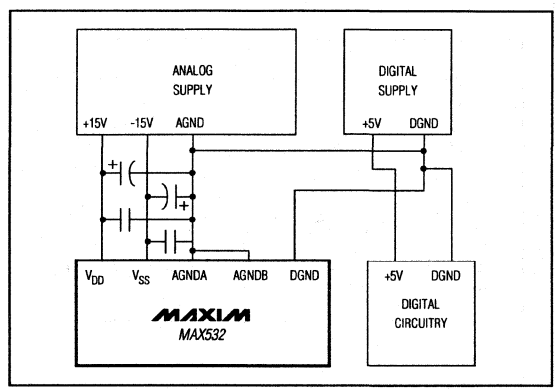


Figure 11. Power-Supply Grounding

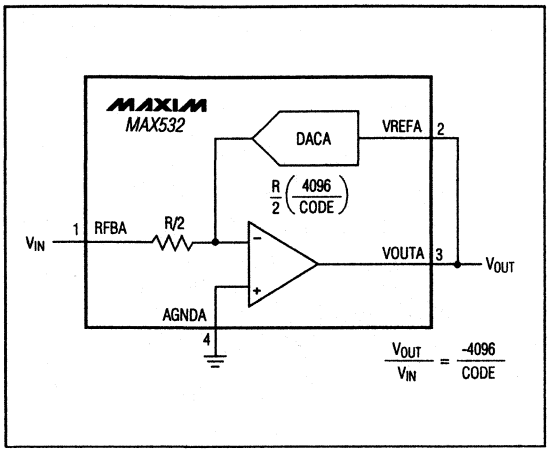


Figure 12. Programmable-Gain Amplifer

Programmable-Gain Amplifier (PGA)

The DAC/amplifier combination, along with access to the feedback resistors, makes the MAX532 ideal as a programmable-gain amplifier. In this application, the DAC functions as a programmable resistor in the feedback loop. This type of configuration is shown in Figure 12, and is suitable for AC gain control. The DAC code controls the gain for the PGA. As the code decreases, the effective DAC resistance increases, and so the gain also increases. The transfer function is given by:

$$V_{OUT}/V_{IN} = -REQA/RFBA,$$

where RFBA is the value of the feedback resistor (R/2), and REQA is the effective DAC resistance controlled by the digital input code:

$$REQA = \frac{R}{2}\left(\frac{4096}{CODE}\right),$$

where CODE is the DAC code in decimal.

The transfer function is thus:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-4096}{CODE}$$

The code may be programmed between 1 and (2^{12} -1). The zero code is not allowed, as it results in an open-loop amplifier response.

Power-On Reset

On power-up, the internal DAC latches are set to 00 . . . . .00.

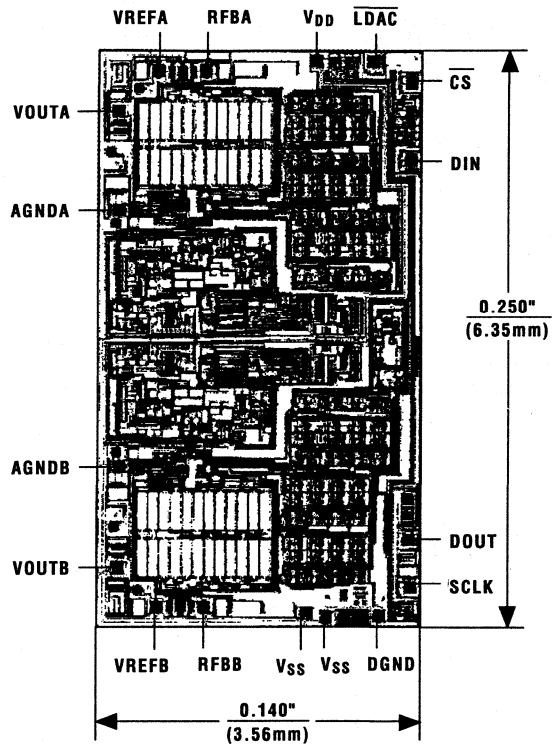
Dual, Serial-Input, Voltage-Output, 12-Bit MDAC

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX532AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX532BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX532AEWE	-40°C to +85°C	16 Wide SO	±1/2
MAX532BEWE	-40°C to +85°C	16 Wide SO	±1
MAX532AMJE	-55°C to +125°C	16 CERDIP**	±1/2
MAX532BMJE	-55°C to +125°C	16 CERDIP**	±1

***Contact factory for availability and processing to MIL-STD-883B.*

Chip Topography



TRANSISTOR COUNT: 1324;
SUBSTRATE CONNECTED TO V_{DD}.

19-0230; Rev 0; 2/94

MAXIM

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX536/MAX537 combine four 12-bit, voltage-output digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving 16-pin package. Offset, gain, and linearity are factory calibrated to provide the MAX536's ±1LSB total unadjusted error. The MAX537 operates with ±5V supplies, while the MAX536 uses -5V and +12V to +15V supplies.

Each DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word is used to load data into each input/DAC register. The serial interface is compatible with either SPI/QSPI™ or Microwire™, and allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated with a hardware $\overline{LDAC}$ pin. All logic inputs are TTL/CMOS compatible.

Applications

Industrial Process Controls

Automatic Test Equipment

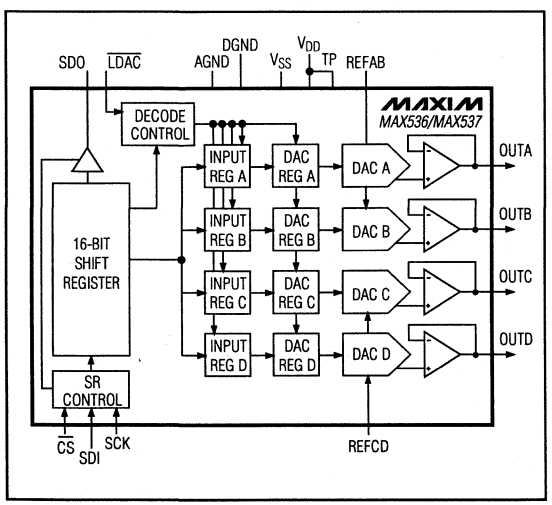
Digital Offset and Gain Adjustment

Motion Control Devices

Remote Industrial Controls

Microprocessor Controlled Systems

Functional Diagram



Features

- ♦ **4 12-Bit DACs with Output Buffers**
- ♦ **Simultaneous or Independent Control of 4 DACs via a 3-Wire Serial Interface**
- ♦ **Power-On Reset**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **±1LSB Total Unadjusted Error (MAX536)**
- ♦ **Full 12-Bit Performance without Adjustments**
- ♦ **±5V Supply Operation (MAX537)**
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Buffered Voltage Output**
- ♦ **16-Pin DIP/SO Packages**

Ordering Information

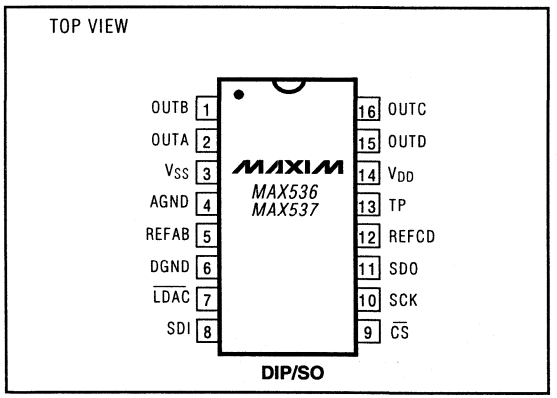
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX536ACPE	0°C to +70°C	16 Plastic DIP	±½
MAX536BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX536ACWE	0°C to +70°C	16 Wide SO	±½
MAX536BCWE	0°C to +70°C	16 Wide SO	±1
MAX536BC/D	0°C to +70°C	Dice*	±1
MAX536AEPE	-40°C to +85°C	16 Plastic DIP	±½
MAX536BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX536AEWE	-40°C to +85°C	16 Wide SO	±½
MAX536BEWE	-40°C to +85°C	16 Wide SO	±1
MAX536AMDE	-55°C to +125°C	16 Ceramic SB**	±½
MAX536BMDE	-55°C to +125°C	16 Ceramic SB**	±1

Ordering Information continued on last page.

** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



™ SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND or DGND
- MAX536 ..... -0.3V, +17V
- MAX537 ..... -0.3V, +7V

V_{SS} to AGND or DGND ..... -7V, +0.3V
SDI, SCK, $\overline{CS}$, $\overline{LDAC}$, TP, SDO to AGND or DGND ..... -0.3V, (V_{DD} + 0.3V)
REFAB, REFCD to AGND or DGND ..... -0.3V, (V_{DD} + 0.3V)
OUT_ to AGND or DGND ..... V_{DD}, V_{SS}
Maximum Current into Any Pin 50mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
- Wide SO (derate 9.52W/°C above +70°C) 762mW
- Ceramic SB (derate 10.53mW/°C above +70°C) 842mW

Operating Temperature Ranges
- MAX53_AC_E/BC_E ..... 0°C to +70°C
- MAX53_AE_E/BE_E ..... -40°C to +85°C
- MAX53_AMDE/BMDE ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX536

(V_{DD} = +15V, V_{SS} = -5V, REFAB/REFCD = 10V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION							
Resolution	N			12			Bits
Total Unadjusted Error (Note 1)	TUE	T_A = +25°C	MAX536A			±1.0	LSB
			MAX536B			±2.0	
		T_A = T_{MIN} to T_{MAX}	MAX536AC			±2.0	
			MAX536BC			±3.0	
			MAX536AE			±2.5	
			MAX536BE			±3.5	
			MAX536AM			±3.0	
			MAX536BM			±4.0	
Integral Nonlinearity	INL		MAX536A		±0.15	±0.50	LSB
			MAX536B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		T_A = +25°C	MAX536A			±2.5	mV
			MAX536B			±5.0	
			MAX536AC			±5.0	
			MAX536BC			±7.5	
			MAX536AE			±6.1	
			MAX536BE			±8.5	
			MAX536AM			±7.5	
			MAX536BM			±10.0	
Gain Error		R_L = ∞			-0.1	±1.0	LSB
		R_L = 5kΩ	MAX536_C/E		-0.6	±1.5	
			MAX536_M			±2.0	
V_{DD} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, 10.8V < V_{DD} < 16.5V			±0.02	±0.125	LSB/V
V_{SS} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, -5.5V < V_{SS} < -4.5V			±0.03	±0.30	LSB/V

ELECTRICAL CHARACTERISTICS—MAX536 (continued)

(V_{DD} = +15V, V_{SS} = -5V, REFAB/REFCD = 10V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MATCHING PERFORMANCE (T_A = +25°C)							
Total Unadjusted Error	TUE	MAX536A				±1.0	LSB
		MAX536B				±2.0	
Gain Error					±0.1	±1.0	LSB
Offset Error		MAX536A			±1.2	±2.5	mV
		MAX536B			±1.2	±5.0	
Integral Nonlinearity	INL				±0.2	±1.0	LSB
REFERENCE INPUT							
Reference Input Range	REF			0.0		V_{DD} – 4	V
Reference Input Resistance	RREF	Code dependent, minimum at code 555hex		5			kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		V_{REF} = $2V_{p-p}$			700		kHz
Reference Feedthrough		Input code = all 0s	V_{REF} = $10V_{p-p}$ at 400Hz		-100		dB
			V_{REF} = $10V_{p-p}$ at 4kHz		-82		
Total Harmonic Distortion Plus Noise	THD + N		V_{REF} = $2.0V_{p-p}$ at 50kHz		0.012		%
DIGITAL INPUTS (SDI, SCK, $\overline{CS}$, $\overline{LDAC}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage Current		V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance (Note 2)						10	pF
DIGITAL OUTPUT (SDO)							
Output Low Voltage	V_{OL}	SDO sinking 5mA			0.18	0.40	V
Output Leakage Current		SDO = 0V to V_{DD}				±10	µA
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					5		V/µs
Output Settling Time		To ±½ LSB of full scale			3		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk (Note 3)		V_{REF} = 5V			8		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			10.8		16.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current (Note 4)	I_{DD}	T_A = +25°C			8	18	mA
		T_A = T_{MIN} to T_{MAX}				25	
Negative Supply Current (Note 4)	I_{SS}	T_A = +25°C			-6	-16	mA
		T_A = T_{MIN} to T_{MAX}				-23	

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX536 (continued)

(V_{DD} = +15V, V_{SS} = -5V, REFAB/REFCD = 10V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Note 5)							
Internal Power-On Reset Pulse Width (Note 2)	t_{POR}					20	µs
SCK Clock Period	t_{CP}			100			ns
SCK Pulse Width High	t_{CH}			30			ns
SCK Pulse Width Low	t_{CL}			30			ns
$\overline{CS}$ Fall to SCK Rise Setup Time	t_{CSS}			20			ns
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			10			ns
SDI Setup Time	t_{DS}			40	26		ns
SDI Hold Time	t_{DH}			0			ns
SCK Rise to SDO Valid Propagation Delay (Note 6)	t_{DO1}	1kΩ pull-up on SDO to V_{DD}, C_{LOAD} = 50pF	SDO high		78	105	ns
			SDO low		50	80	
SCK Fall to SDO Valid Propagation Delay (Note 7)	t_{DO2}	1kΩ pull-up on SDO to V_{DD}, C_{LOAD} = 50pF	SDO high		81	110	ns
			SDO low		53	85	
$\overline{CS}$ Fall to SDO Enable (Note 8)	t_{DV}				27	45	ns
$\overline{CS}$ Rise to SDO Disable (Note 9)	t_{TR}				40	60	ns
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	Continuous SCK, SCK edge ignored		20			ns
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}	SCK edge ignored		20			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDAC}			30			ns
$\overline{CS}$ Pulse Width High	t_{CSW}			40			ns

Note 1: TUE is specified with no resistive load.
Note 2: Guaranteed by design.
Note 3: Crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.
Note 4: Digital inputs at 2.4V; with digital inputs at CMOS levels, I_{DD} decreases slightly.
Note 5: All input signals are specified with $t_R = t_F \leq 5ns$. Logic input swing is 0V to 5V.
Note 6: Serial data clocked out of SDO on SCK's falling edge. (SDO is an open-drain output for the MAX536. The MAX537's SDO pin has an internal active pull-up.)
Note 7: Serial data clocked out of SDO on SCK's rising edge.
Note 8: SDO changes from High-Z state to 90% of final value.
Note 9: SDO rises 10% toward High-Z state.

ELECTRICAL CHARACTERISTICS—MAX537

(V_{DD} = +5V, V_{SS} = -5V, REFAB/REFCD = 2.5V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION							
Resolution	N			12			Bits
Integral Nonlinearity	INL	MAX537A			±0.15	±0.50	LSB
		MAX537B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		T_A = +25°C	MAX537A			±3.0	mV
			MAX537B			±6.0	
		T_A = T_{MIN} to T_{MAX}	MAX537AC			±6.0	
			MAX537BC			±9.0	
			MAX537AE			±7.0	
			MAX537BE			±11.0	
			MAX537AM			±9.0	
			MAX537BM			±15.0	
Gain Error		R_L = ∞			-0.3	±1.5	LSB
		R_L = 5kΩ			-0.8	±3.0	
V_{DD} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, 4.5V ≤ V_{DD} ≤ 5.5V			±0.01	±0.5	LSB/V
V_{SS} Power-Supply Rejection Ratio	PSRR	T_A = +25°C, -5.5V ≤ V_{SS} ≤ -4.5V			±0.02	±0.7	LSB/V
MATCHING PERFORMANCE (T_A = +25°C)							
Gain Error					±0.1	±1.25	LSB
Offset Error		MAX537A			±0.3	±3.0	mV
		MAX537B			±0.3	±6.0	
Integral Nonlinearity	INL				±0.35	±1.0	LSB
REFERENCE INPUT							
Reference Input Range	REF			0.0		V_{DD} - 2.2	V
Reference Input Resistance	RREF	Code dependent, minimum at code 555hex		5			kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		V_{REF} = $2V_{p-p}$			700		kHz
Reference Feedthrough		Input code = all 0s	V_{REF} = $10V_{p-p}$ at 400Hz		-100		dB
			V_{REF} = $10V_{p-p}$ at 4kHz		-82		
Total Harmonic Distortion Plus Noise	THD + N	V_{REF} = $850mV_{p-p}$ at 100kHz			0.024		%
DIGITAL INPUTS (SDI, SCK, $\overline{CS}$, $\overline{LDAC}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Leakage Current		V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance (Note 2)						10	pF

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX537 (continued)

(V_{DD} = +5V, V_{SS} = -5V, REFAB/REFCD = 2.5V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUT (SDO)							
Output High Voltage	V_{OH}	SDO sourcing 2mA		V_{DD} - 0.5	V_{DD} - 0.25		V
Output Low Voltage	V_{OL}	SDO sinking 2mA			0.13	0.40	V
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					5		V/µs
Output Settling Time		To ±½ LSB of full scale			5		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk (Note 3)					5		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			4.5		5.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current (Note 4)	I_{DD}	T_A = +25°C			5.5	12	mA
		T_A = T_{MIN} to T_{MAX}				16	
Negative Supply Current (Note 4)	I_{SS}	T_A = +25°C			-4.7	-10	mA
		T_A = T_{MIN} to T_{MAX}				-14	
TIMING CHARACTERISTICS (Note 5)							
Internal Power-On Reset Pulse Width (Note 2)	t_{POR}					50	µs
SCK Clock Period	t_{CP}			100			ns
SCK Pulse Width High	t_{CH}	MAX537_C/E		35			ns
		MAX537_M		40			
SCK Pulse Width Low	t_{CL}	MAX537_C/E		35			ns
		MAX537_M		40			
$\overline{CS}$ Fall to SCK Rise Setup Time	t_{CSS}	MAX537_C/E		40			ns
		MAX537_M		50			
SCK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}			0			ns
SDI Setup Time	t_{DS}	MAX537_C/E		40	24		ns
		MAX537_M		50			
SDI Hold Time	t_{DH}			0			ns
SCK Rise to SDO Valid Propagation Delay (Note 6)	t_{DO1}	C_{LOAD} = 50pF	MAX537_C/E		116	200	ns
			MAX537_M			230	
SCK Fall to SDO Valid Propagation Delay (Note 7)	t_{DO2}	C_{LOAD} = 50pF	MAX537_C/E		123	210	ns
			MAX537_M			250	

ELECTRICAL CHARACTERISTICS—MAX537 (continued)

(V_{DD} = +5V, V_{SS} = -5V, REFAB/REFCD = 2.5V, AGND = DGND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{CS}$ Fall to SDO Enable	t_{DV}	C_{LOAD} = 50pF	MAX537_C/E		75	140	ns
			MAX537_M			170	
$\overline{CS}$ Rise to SDO Disable (Note 10)	t_{TR}	C_{LOAD} = 50pF	MAX537_C/E		70	130	ns
			MAX537_M			165	
SCK Rise to $\overline{CS}$ Fall Delay	t_{CS0}	Continuous SCK, SCK edge ignored	MAX537_C/E	35			ns
			MAX537_M	40			
$\overline{CS}$ Rise to SCK Rise Hold Time	t_{CS1}	SCK edge ignored	MAX537_C/E	35			ns
			MAX537_M	40			
$\overline{LDAC}$ Pulse Width High	t_{LDAC}	MAX537_C/E		50			ns
		MAX537_M		70			
$\overline{CS}$ Pulse Width High	t_{CSW}	MAX537_C/E		100			ns
		MAX537_M		125			

Note 2: Guaranteed by design.
Note 3: Crosstalk is defined as the glitch energy at any DAC output in response to a full-scale step change on any other DAC.
Note 4: Digital inputs at 2.4V; with digital inputs at CMOS levels, I_{DD} decreases slightly.
Note 5: All input signals are specified with t_R = t_F ≤ 5ns. Logic input swing is 0V to 5V.
Note 6: Serial data clocked out of SDO on SCK's falling edge. (SDO is an open-drain output for the MAX536. The MAX537's SDO pin has an internal active pull-up.)
Note 7: Serial data clocked out of SDO on SCK's rising edge.
Note 10: When disabled, SDO is internally pulled high.

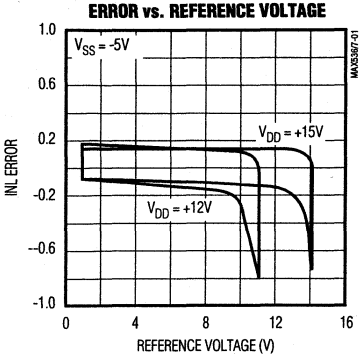
Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

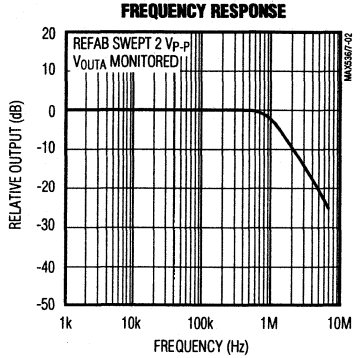
(T_A = +25°C, unless otherwise noted.)

MAX536

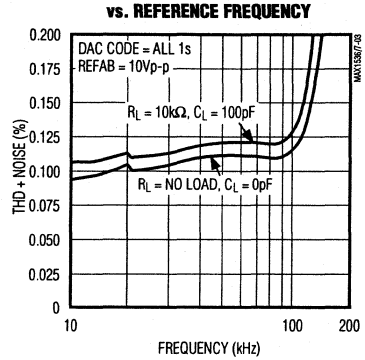
MAX536
INTEGRAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



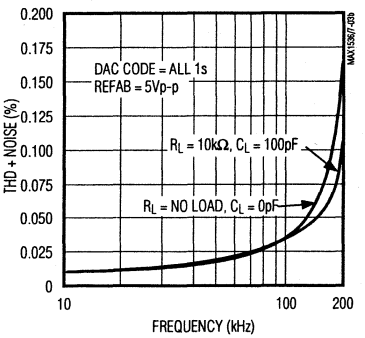
MAX536
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



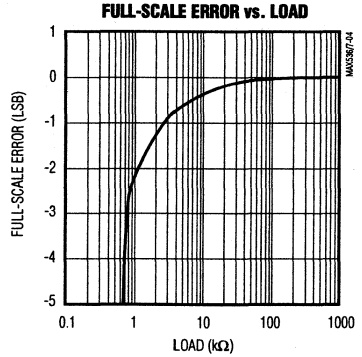
MAX536
TOTAL HARMONIC DISTORTION PLUS NOISE vs. REFERENCE FREQUENCY



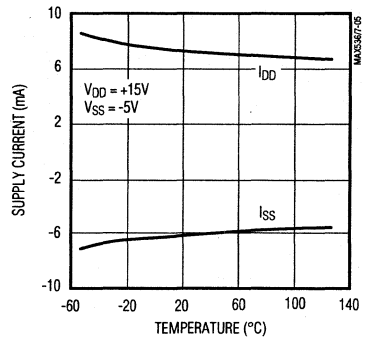
MAX536
TOTAL HARMONIC DISTORTION PLUS NOISE vs. REFERENCE FREQUENCY



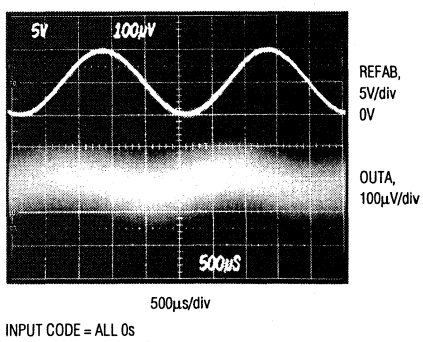
MAX536
FULL-SCALE ERROR vs. LOAD



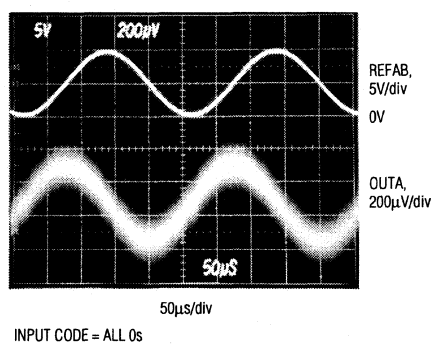
MAX536
SUPPLY CURRENT vs. TEMPERATURE



MAX536
REFERENCE FEEDTHROUGH AT 400Hz



MAX536
REFERENCE FEEDTHROUGH AT 4kHz



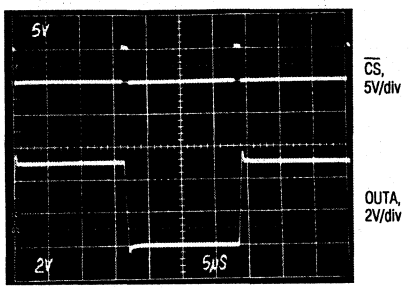
Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

MAX536

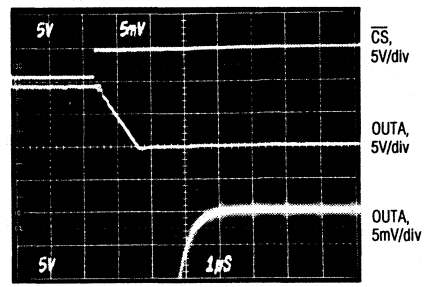
MAX536
DYNAMIC RESPONSE (ALL BITS ON, OFF, ON)



5µs/div

V_{DD} = +15V, V_{SS} = -5V, REFAB = 5V, C_L = 100pF, R_L = 10kΩ

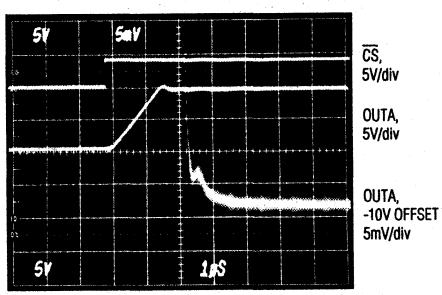
MAX536
NEGATIVE FULL-SCALE SETTLING TIME
(ALL BITS ON TO ALL BITS OFF)



1µs/div

V_{DD} = +15V, V_{SS} = -5V, REFAB = 10V, C_L = 100pF, R_L = 10kΩ

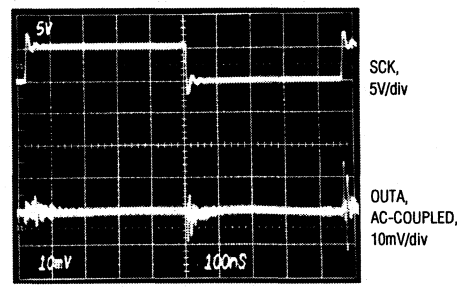
MAX536
POSITIVE FULL-SCALE SETTLING TIME
(ALL BITS OFF TO ALL BITS ON)



1µs/div

V_{DD} = +15V, V_{SS} = -5V, REFAB = 10V, C_L = 100pF, R_L = 10kΩ

MAX536
DIGITAL FEEDTHROUGH



V_{DD} = +15V, V_{SS} = -5V, REFAB = 10V, $\overline{CS}$ = HIGH,
DIN TOGGLING AT ½ THE CLOCK RATE,
OUTA = 5V

9

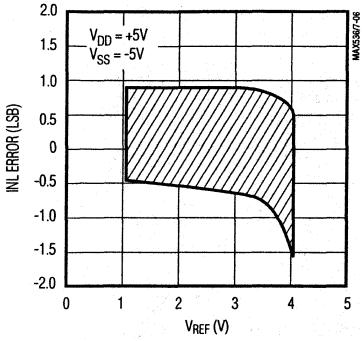
Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

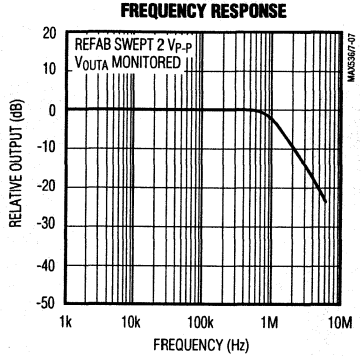
(TA = +25°C, unless otherwise noted.)

MAX537

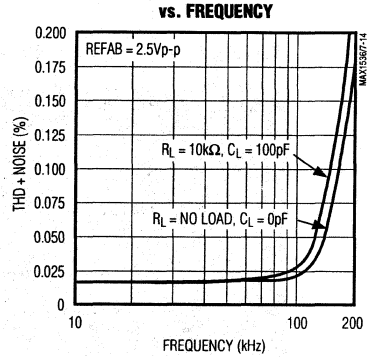
MAX537
INTEGRAL NONLINEARITY ERROR vs. REFERENCE VOLTAGE



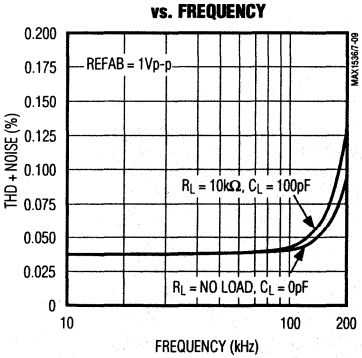
MAX537
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



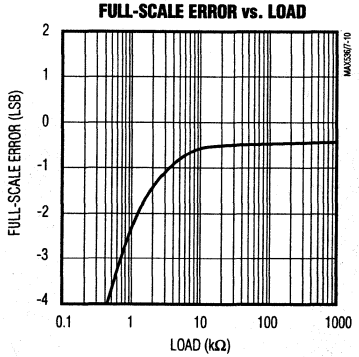
MAX537
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



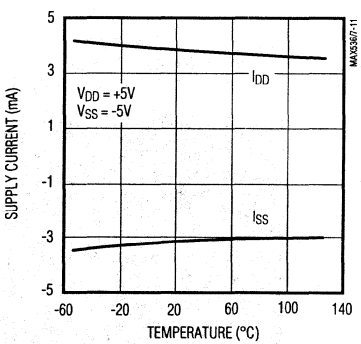
MAX537
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



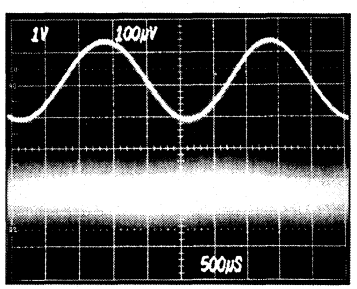
MAX537
FULL-SCALE ERROR vs. LOAD



MAX537
SUPPLY CURRENT vs. TEMPERATURE



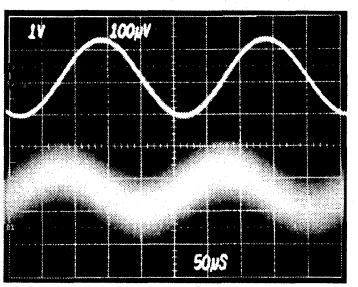
MAX537
REFERENCE FEEDTHROUGH AT 400Hz



500µs/div

INPUT CODE = ALL 0s

MAX537
REFERENCE FEEDTHROUGH AT 4kHz



50µs/div

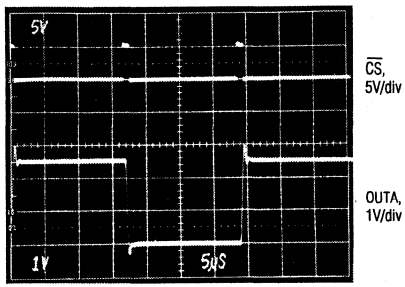
INPUT CODE = ALL 0s

Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

MAX537

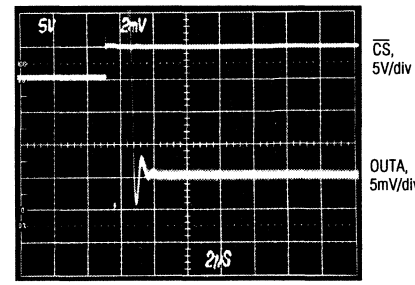
MAX537
DYNAMIC RESPONSE (ALL BITS ON, OFF, ON)



5µs/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, C_L = 100pF, R_L = 10kΩ

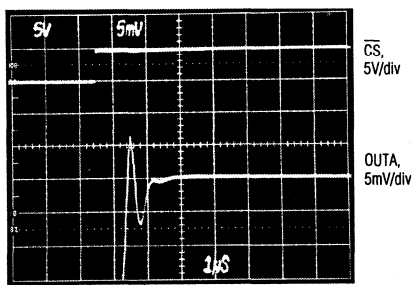
MAX537
NEGATIVE FULL-SCALE SETTLING TIME
(ALL BITS ON TO ALL BITS OFF)



1µs/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, C_L = 100pF, R_L = 10kΩ

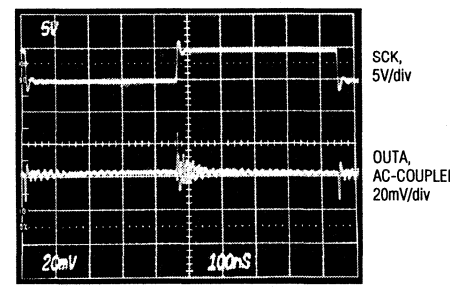
MAX537
POSITIVE FULL-SCALE SETTLING TIME
(ALL BITS OFF TO ALL BITS ON)



1µs/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, C_L = 100pF, R_L = 10kΩ

MAX537
DIGITAL FEEDTHROUGH



100ns/div

V_{DD} = +5V, V_{SS} = -5V, REFAB = 2.5V, $\overline{CS}$ = HIGH,
DIN TOGGLING AT $\frac{1}{2}$ THE CLOCK RATE,
OUTA = 1.25V

9

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	OUTB	DAC B Output Voltage
2	OUTA	DAC A Output Voltage
3	V_{SS}	Negative Power Supply
4	AGND	Analog Ground
5	REFAB	Reference Voltage Input for DAC A and DAC B
6	DGND	Digital Ground
7	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of all input registers to their respective DAC registers.
8	SDI	Serial Data Input. Data is shifted into an internal 16-bit shift register on SCK's rising edge.
9	$\overline{CS}$	Chip-Select Input (active low). A low level on $\overline{CS}$ enables the input shift register and SDO. On $\overline{CS}$'s rising edge, data is latched into the appropriate register(s).
10	SCK	Shift Register Clock Input
11	SDO	Serial Data Output. SDO is the output of the internal shift register. SDO is enabled when $\overline{CS}$ is low. For the MAX536, SDO is an open-drain output. For the MAX537, SDO has an active pull-up to V_{DD}.
12	REFCD	Reference Voltage Input for DAC C and DAC D
13	TP	Test Pin. Connect to V_{DD} for proper operation.
14	V_{DD}	Positive Power Supply
15	OUTD	DAC D Output Voltage
16	OUTC	DAC C Output Voltage

Detailed Description

The MAX536/MAX537 contain four 12-bit voltage-output DACs that are easily addressed using a simple 3-wire serial interface. They include a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see the *Functional Diagram* on the front page).

The DACs are "inverted" R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference-voltage inputs. DAC A and DAC B share the REFAB reference input, while DAC C and DAC D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

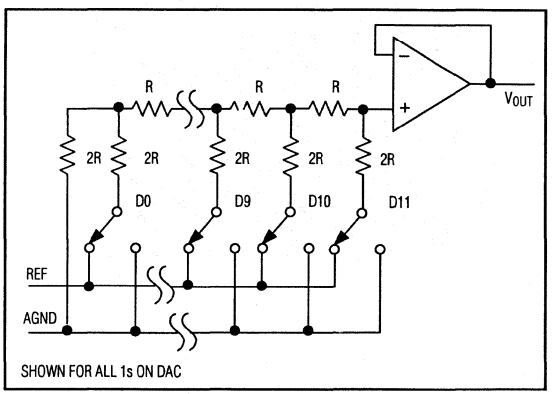


Figure 1. Simplified DAC Circuit Diagram

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The REFAB/REFCD voltage range is 0V to (V_{DD} - 4V) for the MAX536 and 0V to (V_{DD} - 2.2V) for the MAX537. The output voltages $V_{OUT\_}$ are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = N_B\ (V_{REF}) / 4096$$

N_B is the numeric value of the DAC's binary input code (0 to 4095) and V_{REF} is the reference voltage.

The input impedance at each reference input is code dependent, ranging from a low value of typically 6kΩ (with an input code of 0101 0101 0101) to a high value of 60kΩ (with an input code of 0000 0000 0000). Since the input impedance at the reference pins is code dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 5kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance becomes 2.5kΩ. A voltage reference with a load regulation of 0.001%/mA, such as the MAX674, would typically deviate by 0.164LSB (0.328LSB worst case) when simultaneously driving both MAX536 reference inputs at 10V.

An op amp, such as the MAX400 or OP07, can be used to buffer the reference to increase reference accuracy. The op amp's closed-loop output impedance should be kept below 0.05Ω to ensure an error of less than 0.08LSB. Reference accuracy is also improved by driving the REFAB and REFCD pins separately, or by using a reference with excellent accuracy and superior load regulation, such as the MAX676/MAX677/MAX678.

The reference input capacitance is also code dependent and typically ranges from 125pF to 300pF.

Output Buffer Amplifiers

All MAX536/MAX537 voltage outputs are internally buffered by precision unity-gain followers with a typical slew rate of 5V/µs for the MAX536 and 3V/µs for the MAX537.

With a full-scale transition at the MAX536 output (0V to 10V or 10V to 0V), the typical settling time to ±1/2LSB is 3µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance).

With a full-scale transition at the MAX537 output (0V to 2.5V or 2.5V to 0V), the typical settling time to ±1/2LSB is 5µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance).

Output dynamic responses and settling performances of the MAX536/MAX537 output amplifier are shown in the *Typical Operating Characteristics*.

Serial-Interface Configurations

The MAX536/MAX537's 3-wire or 4-wire serial interface is compatible with both Microwire (Figure 2) and SPI/QSPI (Figure 3). In Figures 2 and 3, $\overline{LDAC}$ can be tied either high or low for a 3-wire interface, or used as the fourth input with a 4-wire interface. The connection between SDO and the serial-interface port is not necessary, but may be used for data echo. (Data held in the shift register

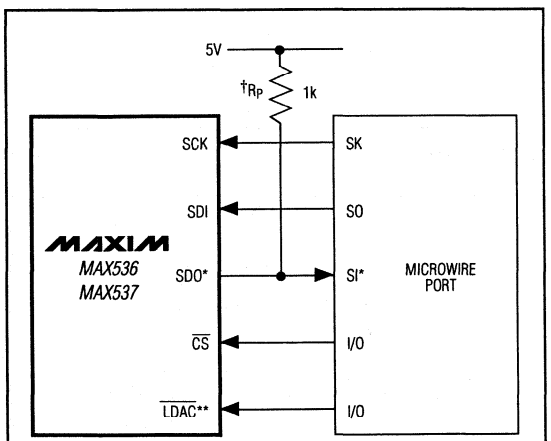


Figure 2. Connections for Microwire

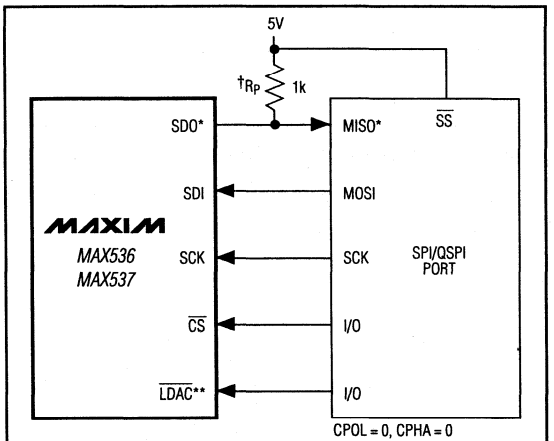


Figure 3. Connections for SPI/QSPI

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

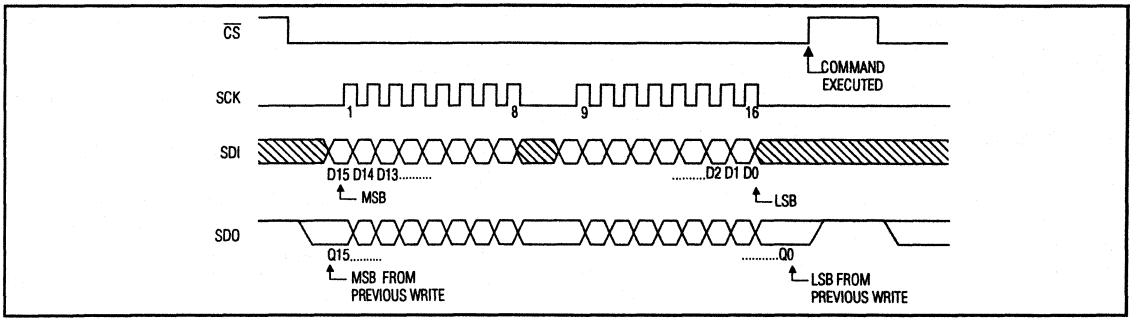


Figure 4. 3-Wire Serial-Interface Timing Diagram ($\overline{LDAC}$ = GND or V_{DD})

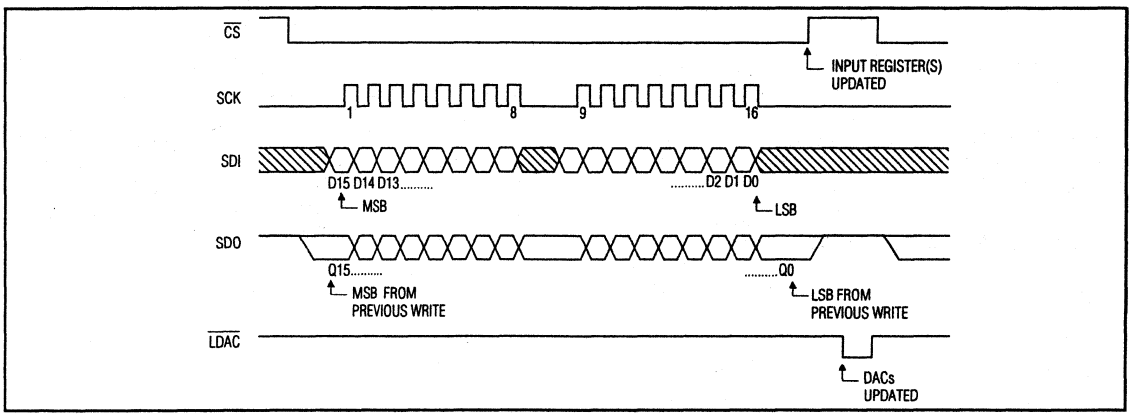


Figure 5. 4-Wire Serial-Interface Timing Diagram for Asynchronous DAC Updating Using $\overline{LDAC}$

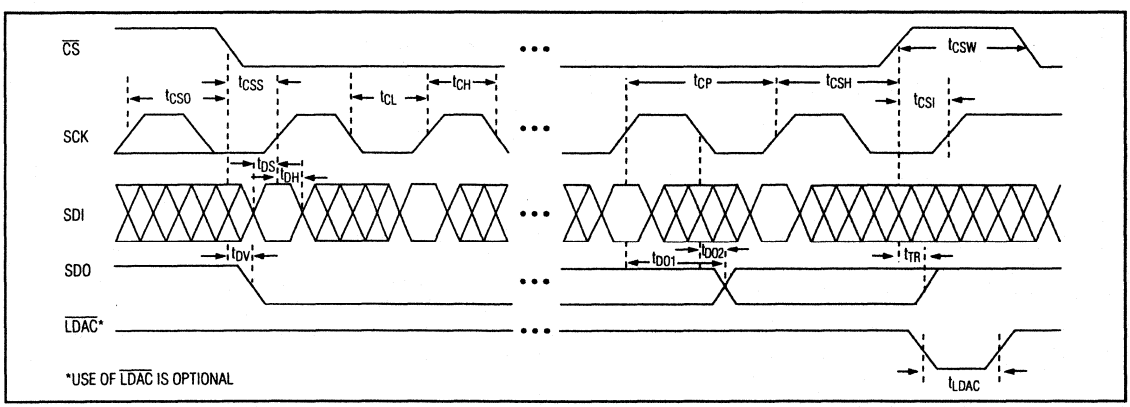


Figure 6. Detailed Serial-Interface Timing Diagram

of the MAX536/MAX537 can be shifted out of SDO and returned to the microprocessor for data verification; data in the MAX536/MAX537 input/DAC registers cannot be read.)

With a 3-wire interface ($\overline{CS}$, SCK, SDI) and $\overline{LDAC}$ tied high, the DACs are double-buffered. In this mode, depending on the command issued through the serial interface, the input register(s) may be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers may be simultaneously updated from the input registers. With a 3-wire interface ($\overline{CS}$, SCK, SDI) and $\overline{LDAC}$ tied low (Figure 4), the DAC registers remain transparent. Any time an input register is updated, the change will appear at the DAC output with the rising edge of $\overline{CS}$.

The 4-wire interface ($\overline{CS}$, SCK, SDI, $\overline{LDAC}$), is similar to the 3-wire interface with $\overline{LDAC}$ tied high, except $\overline{LDAC}$ is a hardware input that simultaneously and asynchronously loads all DAC registers from their respective input registers when driven low (Figure 5).

Serial-Interface Description

The MAX536/MAX537 require 16 bits of serial data. Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0), two control bits (C1, C0), and the 12 data bits D12...D0 (Figure 7). The 4-bit address/control code determines the following: 1) the register(s) to be updated and/or the status of the input and DAC registers (i.e., whether they are in transparent or latch mode), and 2) the edge on which data is clocked out of SDO.

MSB ..... LSB			
← 16 Bits of Serial Data →			
Address Bits		Control Bits	Data Bits MSB ..... LSB
A1	A0	C1 C0	D11 ..... D0
← 4 Address/ Control Bits →			← 12 Data Bits →

Figure 7. Serial-Data Format (MSB Sent First)

Figure 6 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled and the serial data output pin (SDO) is driven high (MAX537) or is a high-impedance open drain (MAX536). $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial data input pin (SDI) on SCK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX536/MAX537 input/DAC registers on $\overline{CS}$'s rising edge.

Interface timing is optimized when serial data is clocked out of the microcontroller/microprocessor on one clock edge and clocked into the MAX536/MAX537 on the other edge. Table 1 lists the Serial-Interface Programming Commands. For certain commands, the 12 data bits are "don't cares".

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The NOP (no operation) command allows the register contents to be unaffected and is useful when the MAX536/MAX537 are configured in a daisy-chain (see the *Daisy-Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of the MAX536/MAX537 SDO pin also loads data from all input registers to their respective DAC registers.

Serial-Data Output

The serial-data output, SDO, is the internal shift register's output. The MAX536/MAX537 can be programmed so that data is clocked out of SDO on SCK's rising (Mode 0) or falling (Mode 1) edge . In Mode 1, output data at SDO lags input data at SDI by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 0, output data lags input data by 16 clock cycles. On power-up, SDO defaults to Mode 0 timing.

For the MAX536, SDO is an open-drain output that should be pulled up to +5V. The data sheet timing specifications for SDO use a 1kΩ pull-up resistor. For the MAX537, SDO is a complementary output and does not require an external pull-up.

Test Pin

The test pin (TP) is used for pre-production analysis of the IC. **Connect TP to V_{DD} for proper MAX536/MAX537 operation. Failure to do so affects DAC operation.**

Daisy-Chaining Devices

Any number of MAX536/MAX537s can be daisy-chained by connecting the SDO pin of one device (with a pull-up resistor, if appropriate) to the SDI pin of the following device in the chain (Figure 8).

Since the MAX537's SDO pin has an internal active pull-up, the SDO sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial data out V_{OH} and V_{OL} specifications in the *Electrical Characteristics.*

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					LDAC	FUNCTION
A1	A0	C1	C0	D11...D0		
0	0	0	1	12-bit DAC data	1	Load DAC A input register; DAC output unchanged.
0	1	0	1	12-bit DAC data	1	Load DAC B input register; DAC output unchanged.
1	0	0	1	12-bit DAC data	1	Load DAC C input register; DAC output unchanged.
1	1	0	1	12-bit DAC data	1	Load DAC D input register; DAC output unchanged.
0	0	1	1	12-bit DAC data	1	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	1	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	1	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	1	Load input register D; all DAC registers updated.
X	0	0	0	12-bit DAC data	X	Load all DACs from shift register.
X	1	0	0	XXXXXXXXXXXX	X	No operation (NOP)
0	X	1	0	XXXXXXXXXXXX	1	Update all DACs from their respective input registers.
1	1	1	0	XXXXXXXXXXXX	X	Mode 1, DOUT clocked out on SCK's rising edge. All DACs updated from their respective input registers.
1	0	1	0	XXXXXXXXXXXX	X	Mode 0, DOUT clocked out on SCK's falling edge. All DACs updated from their respective input registers.
0	0	X	1	12-bit DAC data	0	Load DAC A input register; DAC A is immediately updated.
0	1	X	1	12-bit DAC data	0	Load DAC B input register; DAC B is immediately updated.
1	0	X	1	12-bit DAC data	0	Load DAC C input register; DAC C is immediately updated.
1	1	X	1	12-bit DAC data	0	Load DAC D input register; DAC D is immediately updated.

"X" = Don't Care. $\overline{LDAC}$ provides true latch control: when $\overline{LDAC}$ is low, the DAC registers are transparent; when $\overline{LDAC}$ is high, the DAC registers are latched.

When daisy-chaining MAX536s, the delay from $\overline{CS}$ low to SCK high (t_{CSS}) must be the greater of:

$$t_{DV} + t_{DS}$$

or

$$t_{TR} + t_{RC} + t_{DS} - t_{CSW}$$

where t_{RC} is the time constant of the external pull-up resistor (R_P) and the load capacitance (C) at SDO. For $t_{RC} < 20ns$, t_{CSS} is simply $t_{DV} + t_{DS}$. Calculate t_{RC} from the following equation:

$$t_{RC} = R_P (C) \left[\ln \left(\frac{V_{PULL\text{-}UP}}{V_{PULL\text{-}UP} - 2.4V} \right) \right]$$

where $V_{PULL\text{-}UP}$ is the voltage to which the pull-up resistor is connected.

Additionally, when daisy-chaining devices, the maximum clock frequency is limited to:

$$f_{SCK(max)} = \frac{1}{2\,(t_{DO} + t_{RC} - 38ns + t_{DS})}$$

For example, with t_{RC} = 23ns (5V ±10% supply with R_P = 1kΩ and C = 30pF), the maximum clock frequency is 8.7MHz.

Figure 9 shows an alternate method of connecting several MAX536/MAX537s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy-chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

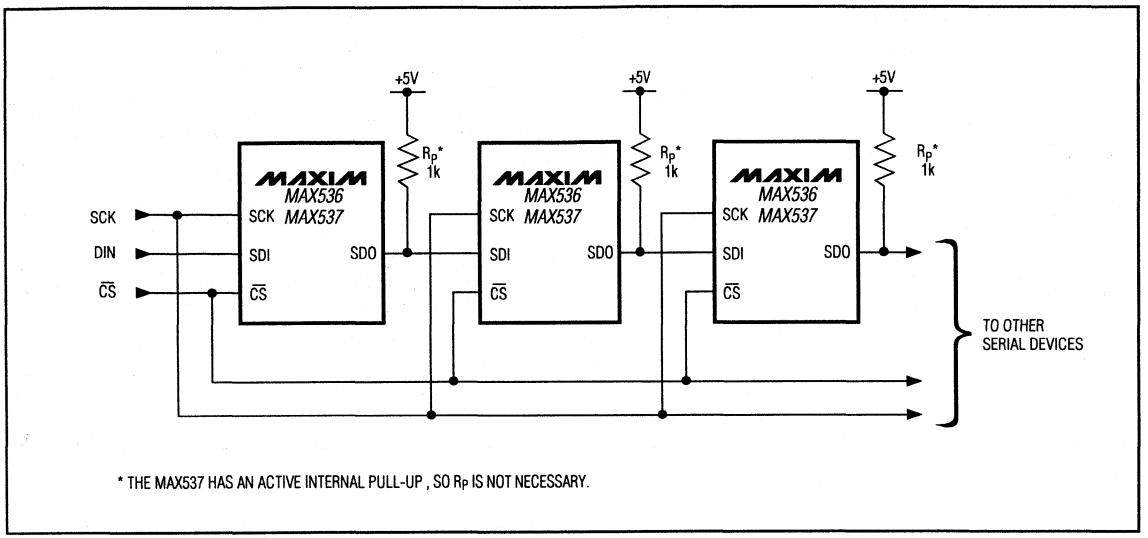


Figure 8. Daisy-Chaining MAX536/MAX537s with a 3-Wire Serial Interface

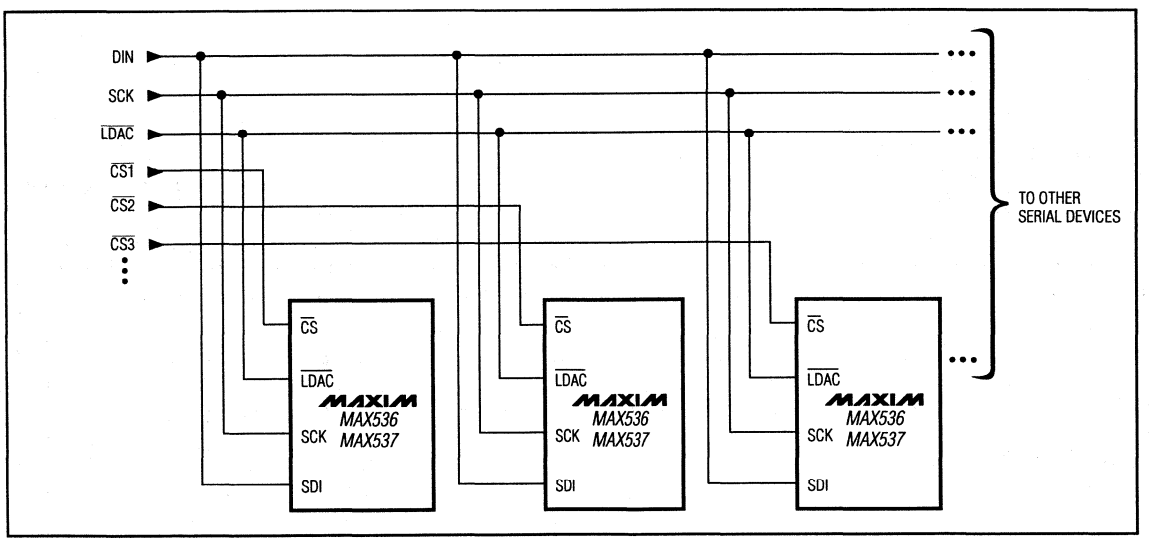


Figure 9. Multiple devices sharing a common DIN line may be simultaneously updated by bringing LDAC low. CS1, CS2, CS3... are driven separately, thus controlling which data are written to devices 1, 2, 3...

Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

Applications Information

Interfacing to the M68HC11*

PORT D of the 68HC11 supports SPI. The four registers used for SPI operation are the Serial Peripheral Control Register, the Serial Peripheral Status Register, the Serial Peripheral Data I/O Register, and PORT D's Data Direction Register. These registers have a default starting location of $1000).

On reset, the PORT D register (memory location $1008) is cleared and bits 5-0 are configured as general-purpose inputs. Setting bit 6 (SPE) of the Serial Peripheral Control Register (SPCR) configures PORT D for SPI as follows:

BIT							
7	6	5	4	3	2	1	0
NAME							
–	–	$\overline{SS}$	SCK	MOSI	MISO	TXD	RXD

Bits 6 and 7 are not used. Writes to these bits are ignored.

The PORT D Data Direction Register (DDRD) determines whether the port bits are inputs or outputs. Its configuration is shown below:

BIT							
7	6	5	4	3	2	1	0
NAME							
–	–	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0

Setting DDD_ = 0 configures the port bit as an input, while setting DDD_ = 1 configures the port bit as an output. Writes to bits 6 and 7 have no effect.

In SPI mode with MSTR = 1, when a PORT D bit is expected to be an input ($\overline{SS}$, MISO, RXD), the corresponding DDRD bit (DDD_) is ignored. If the bit is expected to be an output (SCK, MOSI, TXD), the corresponding DDRD bit must be set for the bit to be an output.

Table 2. Serial Peripheral Control-Register Definitions

NAME	DEFINITION		
SPIE	Serial Peripheral Interrupt Enable. Clearing SPIE disables the SPI hardware-interrupt request; the SPSR is polled to determine when an SPI data transfer is complete. Setting SPIE requests a hardware interrupt when the Serial Peripheral Status Register's SPIF bit or MODF bit is set.		
SPE	Setting SPE (Serial Peripheral System Enable) configures PORT D for SPI. Clearing SPE configures the port as a general-purpose I/O port.		
DWOM	When DWOM is set, the six PORT D outputs are open drain. When DWOM is cleared, the outputs are complementary.		
MSTR	Master/Slave select option		
CPOL	Determines clock polarity. When set, the serial clock idles high while data is not being transferred; when cleared, the clock idles low.		
CPHA	Determines the clock phase.		
SPR1/0	SPI Clock-Rate Select		
	SPR1	SPR0	
	0	0	µP clock divided by 2
	0	1	µP clock divided by 4
	1	0	µP clock divided by 16
	1	1	µP clock divided by 32

*M68HC11 is a Motorola microcontroller. General information about the device was obtained from M68HC11 technical manuals.

Table 3. Serial Peripheral Status Register Definitions

NAME	DEFINITION
SPIF	SPIF is set when an SPI data transfer is complete. It is cleared by reading the SPSR and then accessing the SPDR.
WCOL	Write collision flag that is set when a write to the SPDR occurs while a data transfer is in progress. It is cleared by reading the SPSR and then accessing the SPDR.
MODF	The Mode Fault flag detects master/slave conflicts in a multimaster environment. It is set when the "master" controller has its $\overline{SS}$ line (PORT D) pulled low, and cleared by reading the SPSR followed by a write to the SPCR.

Table 4. M68HC11 Programming Code

```
*****************************************************************************************************
* 68HC11 Programming Code for interfacing to the MAX536/MAX537 DACs.
* Data for the MAX536/MAX537 is stored in memory locations $0100 and $0101.
*
* Release Date February 24, 1994
* Revision 0
* Technical support provided by Motorola
* Additional assistance provided by Diane Scott
*****************************************************************************************************
*
*      68HC11 Code                    Instruction
*
STRT    EQU   $0000         ; Memory location for beginning of program
REGBLK  EQU   $1000         ; Starting address for 68HC11 register block
*
*  The following registers will be addressed relative to the start of the
*  register block (REGBLK) using indexed addressing mode.
*  The effective address = contents of Index Register X + offset.
*
PORTD   EQU   $08           ; PORT D memory location
DDRD    EQU   $09           ; PORT D Data Direction Register memory location
SPCR    EQU   $28           ; SPCR memory location
SPSR    EQU   $29           ; SPSR memory location
SPDR    EQU   $2A           ; SPDR memory location
*
*        Start of main program
*
MAIN    ORG   STRT
        LDAA #$74           ; an arbitrary MAX536/MAX537 DAC code (load input
        STAA $0100          ; register B with 1/4 of full-scale value; all DAC
        LDAA #$00           ; registers updated) is loaded into data memory
        STAA $0101          ; locations $0100 and $0101.
*
        LDX   #REGBLK       ; load Index Register X with starting address of register block
        LDAA  #$38          ; SPI outputs (SCK, MOSI, and /SS configured as an output)
*                           ; configured by setting the Data Direction Register bits
        STAA  DDRD,X        ; load data into the Data Direction Register
        LDAA  #$2F          ; set /SS and MOSI high; set SCK low
        STAA  PORTD,X       ; load data into PORTD to set-up SPI control lines
        LDAA  #$51          ; set data for SPCR
        STAA  SPCR,X        ; load data into the SPCR
        BCLR  PORTD,X $20   ; bring /CS low
        LDAA  $0100         ; load high byte of digital data into Accumulator(A)
        STAA  SPDR,X        ; load high byte of MAX536/MAX537 data into SPDR
WAIT1   LDAA  SPSR,X        ; beginning of loop to poll the SPSR
        BITA  #$80          ; mask all bits except SPIF (transfer complete) flag
        BEQ   WAIT1         ; branch if SPIF is not set to beginning of loop
        LDAA  $0101         ; load low byte of digital data into Accumulator(A)
        STAA  SPDR,X        ; load low byte of MAX536/MAX537 data into SPDR
WAIT2   LDAA  SPSR,X        ; beginning of loop to poll the SPSR
        BITA  #$80          ; mask all bits except SPIF (transfer complete) flag
        BEQ   WAIT2         ; branch if SPIF is not set to beginning of loop
        LDAA  SPDR,X        ; read the SPDR to clear the SPIF bit in the SPSR
        BSET  PORTD,X $20   ; bring /CS high to latch data into the MAX536/MAX537
*
* The MAX536/MAX537 is now configured to have VOUTB = VREF (1024/4096)
*
*****************************************************************************************************
```

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Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

$\overline{SS}$ is an input intended for use in a multimaster environment. However, $\overline{SS}$ or unused PORT D bit RXD, TXD, or possibly MISO (if DAC readback is not used) should be configured as a general-purpose output and used as $\overline{CS}$ by setting the appropriate Data Direction Register bit.

The SPCR configuration (memory location $1028) is shown below:

BIT	7	6	5	4	3	2	1	0
NAME	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
SETTING AFTER RESET	0	0	0	0	0	1	U*	U*
SETTING FOR TYPICAL SPI COMMUNICATION	0	1	0	1	0	0	0**	1**

*U = Unknown
**Depends on µP clock frequency.

Always configure the 68HC11 as the "master" controller and the MAX536/MAX537 as the "slave" device.

When MSTR = 1 in the SPCR, a write to the Serial Peripheral Data I/O Register (SPDR), located at memory location $102A, initiates the transmission/reception of data. The data transfer is monitored and the appropriate flags are set in the Serial Peripheral Status Register.

The SPSR configuration is shown below:

BIT	7	6	5	4	3	2	1	0
NAME	SPIF	WCOL	–	MODF	–	–	–	–
RESET CONDITIONS	0	0	0	0	0	0	0	0

An example of 68HC11 programming code for a two-byte SPI transfer to the MAX536/MAX537 is given in Table 4. $\overline{SS}$ is used for $\overline{CS}$, the high byte of MAX536/MAX537 digital data is stored in memory location $0100 and the low byte is stored in memory location $0101.

Interfacing to Other Controllers

When using Microwire, refer to the section on interfacing to the M68HC11 for guidance, since Microwire can be considered similar to SPI when CPOL = 0 and CPHA = 0. When interfacing to Intel's 80C51/80C31 microcontroller family, use bit-pushing to configure a desired port as the MAX536/MAX537 interface port. Bit-pushing involves arbitrarily assigning I/O port bits as interface control lines, and then writing to the port each time a signal transition is required.

Unipolar Output

For a unipolar output, the output voltages and the reference inputs are the same polarity. Figure 10 shows the MAX536/MAX537 unipolar output circuit, which is also the typical operating circuit. Table 5 lists the unipolar output codes.

Bipolar Output

The MAX536/MAX537 outputs can be configured for bipolar operation using Figure 11's circuit. One op amp and two resistors are required per DAC. With R1 = R2:

$$V_{OUT} = V_{REF}[(2N_B / 4096) - 1]$$

where N_B is the numeric value of the DAC's binary input code. Table 6 shows digital codes and corresponding output voltages for Figure 11's circuit.

Table 5. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}(\frac{4095}{4096})$
1000	0000	0001	$+V_{REF}(\frac{2049}{4096})$
1000	0000	0000	$+V_{REF}(\frac{2048}{4096}) = \frac{+V_{REF}}{2}$
0111	1111	1111	$+V_{REF}(\frac{2047}{4096})$
0000	0000	0001	$+V_{REF}(\frac{1}{4096})$
0000	0000	0000	0V

Table 6. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}(\frac{2047}{2048})$
1000	0000	0001	$+V_{REF}(\frac{1}{2048})$
0000	0000	0000	0V
0111	1111	1111	$-V_{REF}(\frac{1}{2048})$
0000	0000	0001	$-V_{REF}(\frac{2047}{2048})$
1000	0000	0000	$-V_{REF}(\frac{2048}{2048}) = -V_{REF}$

NOTE: $1LSB = (V_{REF})(\frac{1}{4096})$

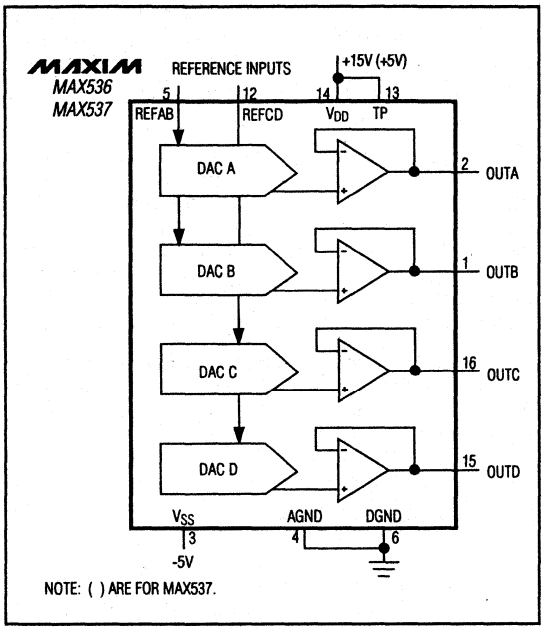

Figure 10. Unipolar Output Circuit

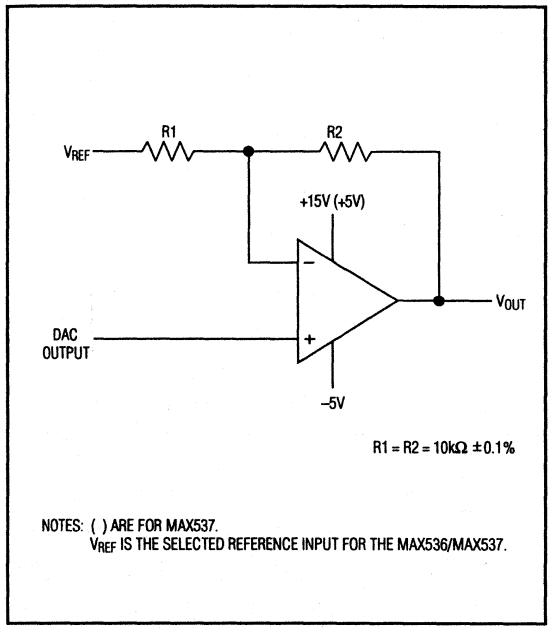

Figure 11. Bipolar Output Circuit

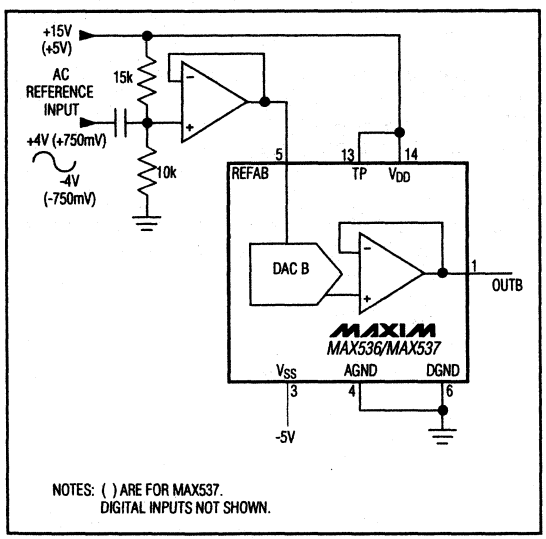

Figure 12. AC Reference Input Circuit

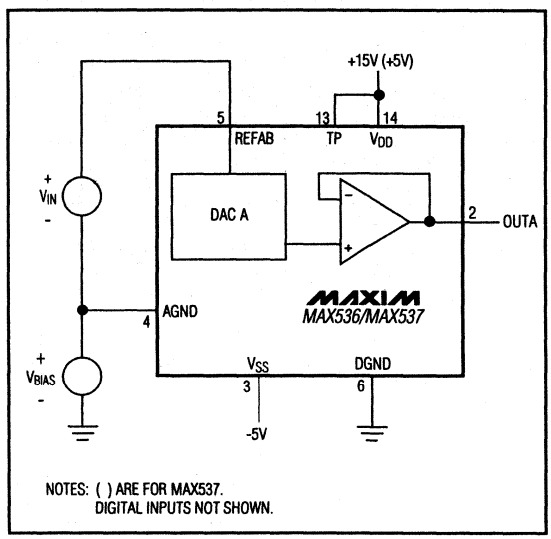

Figure 13. AGND Bias Circuit

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Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

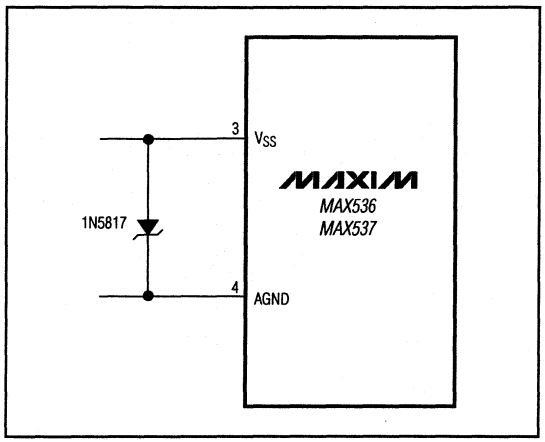


Figure 14. When V_{SS} and V_{DD} cannot be sequenced, tie a Schottky diode between V_{SS} and AGND.

Using an AC Reference

In applications where the reference has AC signal components, the MAX536/MAX537 have multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX536's total harmonic distortion plus noise (THD + N) is typically less than 0.012%, given a $5V_{p-p}$ signal swing and input frequencies up to 35kHz, or given a $2V_{p-p}$ swing and input frequencies up to 50kHz. The typical -3dB frequency is 700kHz as shown in the *Typical Operating Characteristics* graphs.

For the MAX537, with an input signal amplitude of $0.85mV_{p-p}$, THD + N is typically less than 0.024% with a 5kΩ load in parallel with 100pF and input frequencies up to 100kHz, or with a 2kΩ load in parallel with 100pF and input frequencies up to 95kHz.

Offsetting AGND

AGND can be biased from DGND to the reference voltage to provide an arbitrary nonzero output voltage for a zero input code (Figure 13). The output voltage V_{OUTA} is:

$$V_{OUTA} = V_{BIAS} + N_B (V_{IN})$$

where V_{BIAS} is the positive offset voltage (with respect to DGND) applied to AGND, and N_B is the numeric value of the DAC's binary input code. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. As the voltage at AGND increases, the DAC's resolution decreases because its full-scale voltage swing is effectively reduced. AGND should not be biased more negative than DGND.

Power-Supply Considerations

On power-up, V_{SS} should come up first, V_{DD} next, then REFAB or REFCD. If supply sequencing is not possible, tie an external Schottky diode between V_{SS} and AGND as shown in Figure 14. On power-up, all input and DAC registers are cleared (set to zero code) and SDO is in Mode 0 (serial data is shifted out of SDO on the clock's rising edge).

For rated MAX536 performance, V_{DD} should be 4V higher than REFAB/REFCD and should be between 10.8V and 16.5V. When using the MAX537, V_{DD} should be at least 2.2V higher than REFAB/REFCD and should be between 4.75V and 5.5V. Bypass both V_{DD} and V_{SS} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

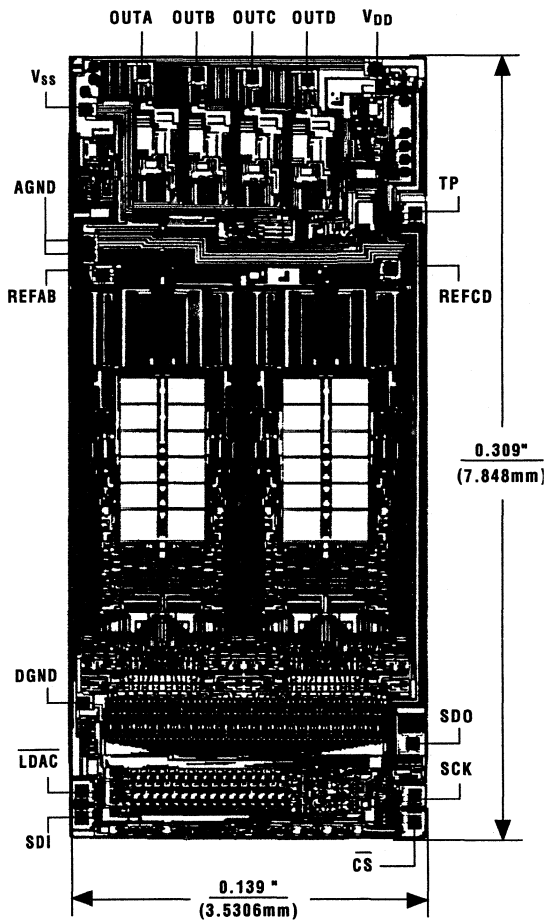
Calibrated, Quad, 12-Bit Voltage-Output DACs with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX537ACPE	0°C to +70°C	16 Plastic DIP	±½
MAX537BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX537ACWE	0°C to +70°C	16 Wide SO	±½
MAX537BCWE	0°C to +70°C	16 Wide SO	±1
MAX537BC/D	0°C to +70°C	Dice*	±1
MAX537AEPE	-40°C to +85°C	16 Plastic DIP	±½
MAX537BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX537AEWE	-40°C to +85°C	16 Wide SO	±½
MAX537BEWE	-40°C to +85°C	16 Wide SO	±1
MAX537AMDE	-55°C to +125°C	16 Ceramic SB**	±½
MAX537BMDE	-55°C to +125°C	16 Ceramic SB**	±1

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 5034;
SUBSTRATE CONNECTED TO V_{DD}.

9

19-0257; Rev 1; 7/94

MAXIM

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

General Description

The MAX547 contains eight 13-bit, voltage-output digital-to-analog converters (DACs). On-chip precision output amplifiers provide the voltage outputs. The MAX547 operates from a ±5V supply. Bipolar output voltages with up to ±4.5V voltage swing can be achieved with no external components. The MAX547 has four separate reference inputs; each is connected to two DACs, providing different full-scale output voltages for every DAC pair.

The MAX547 features double-buffered interface logic with a 13-bit parallel data bus. Each DAC has an input latch and a DAC latch. Data in the DAC latch sets the output voltage. The eight input latches are addressed with three address lines. Data is loaded to the input latch with a single write instruction. An asynchronous load ($\overline{LD\_}$) input transfers data from the input latch to the DAC latch. The four $\overline{LD\_}$ inputs each control two DACs, and all DAC latches can be updated simultaneously by asserting all $\overline{LD\_}$ pins. An asynchronous clear ($\overline{CLR}$) input resets the output of all eight DACs to AGND_. Asserting $\overline{CLR}$ resets both the DAC and the input latch to bipolar zero (1000hex). On power-up, reset circuitry performs the same function as $\overline{CLR}$. All logic inputs are TTL/CMOS compatible.

The MAX547 is available in 44-pin plastic quad flat pack and 44-pin PLCC packages.

Applications

Automatic Test Equipment
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Arbitrary Function Generators
Industrial Process Controls
Avionics Equipment

Features

- ♦ **Full 13-Bit Performance without Adjustments**
- ♦ **8 DACs in One Package**
- ♦ **Buffered Voltage Outputs**
- ♦ **Calibrated Linearity**
- ♦ **Guaranteed Monotonic to 13 Bits**
- ♦ **±5V Supply Operation**
- ♦ **Unipolar or Bipolar Outputs Swing to ±4.5V**
- ♦ **Fast Output Settling (5µs to ±½LSB)**
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Asynchronous Load Inputs Load Pairs of DAC Latches**
- ♦ **Asynchronous $\overline{CLR}$ Input Resets DACs to Analog Ground**
- ♦ **Power-On Reset Circuit Resets DACs to Analog Ground**
- ♦ **Microprocessor and TTL/CMOS Compatible**

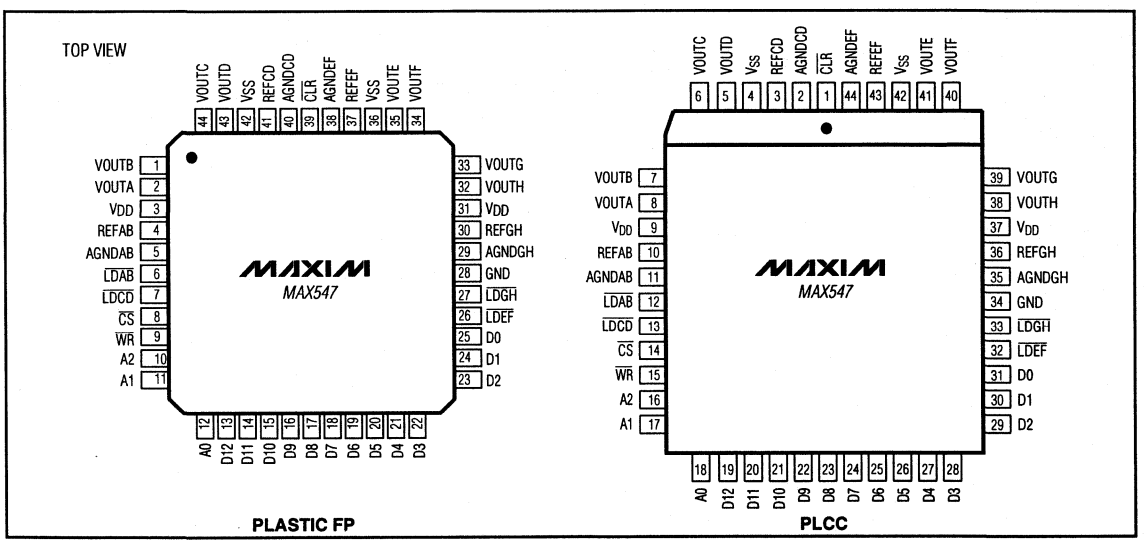
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX547ACQH	0°C to +70°C	44 PLCC	±2
MAX547BCQH	0°C to +70°C	44 PLCC	±4
MAX547ACMH	0°C to +70°C	44 Plastic FP	±2
MAX547BCMH	0°C to +70°C	44 Plastic FP	±4
MAX547BC/D	0°C to +70°C	Dice*	±4

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Pin Configurations



Octal, 13-Bit Voltage-Output DAC with Parallel Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
V_{SS} to GND .....-6V to +0.3V
Digital Input Voltage to GND .....-0.3V to (V_{DD} + 0.3V)
REF_ .....(AGND_ - 0.3V) to (V_{DD} + 0.3V)
AGND_ .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
VOUT_ .....V_{DD} to V_{SS}
Maximum Current into REF_ Pin .....±10mA
Maximum Current into Any Other Signal Pin .....±50mA

Continuous Power Dissipation (T_A = +70°C)
PLCC (derate 13.33mW/°C above +70°C).....1067mW
Plastic FP (derate 11.11mW/°C above +70°C).....889mW
Operating Temperature Ranges
MAX547_C_H.....0°C to +70°C
MAX547_E_H.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		13			Bits
Relative Accuracy	INL	MAX547A		±0.5	±2	LSB
		MAX547B		±0.5	±4	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1	LSB
Bipolar Zero-Code Error				±5	±20	LSB
Gain Error				±1	±8	LSB
Power-Supply Rejection Ratio	PSRR	$\Delta Gain/\Delta V_{DD}$ (Note 1)			±0.0025	%/%
		$\Delta Gain/\Delta V_{SS}$ (Note 1)			±0.0025	
Load Regulation		R_L = ∞ to 10kΩ		0.3		LSB
REFERENCE INPUT (Note 2)						
Reference Input Range	REF	(Notes 2, 3)	AGND_		V_{DD}	V
Reference Input Resistance	RREF	Each REF_ pin (Note 3)	5			kΩ
ANALOG OUTPUT						
Maximum Output Voltage				V_{DD} - 0.5		V
Minimum Output Voltage				V_{SS} + 0.5		V
DYNAMIC PERFORMANCE—ANALOG SECTION						
Voltage-Output Slew Rate				3		V/µs
Output Settling Time		To ±½ LSB of full scale (Note 4)		5		µs
Digital Feedthrough				5		nV-s
Digital Crosstalk				5		nV-s
DIGITAL INPUTS (V_{DD} = 5V ±5%)						
Input Voltage High	V_{IH}		2.4			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}			1.0	µA
Input Capacitance	C_{IN}	(Note 5)			10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, R_L = 10kΩ, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Range	V_{DD}	(Note 6)	4.75		5.25	V
Negative Supply Range	V_{SS}	(Note 6)	-5.25		-4.75	V
Positive Supply Current	I_{DD}	T_A = T_{MIN} to T_{MAX}		14	44	mA
Negative Supply Current	I_{SS}	T_A = T_{MIN} to T_{MAX}		11	40	mA

Note 1: PSRR is tested by changing the respective supply voltage by ±5%.
Note 2: For best performance, REF_ should be greater than AGND_ + 2V and less than V_{DD} - 0.6V. The device operates with reference inputs outside this range, but performance may degrade. For further information on the reference, see the *Reference and Analog-Ground Inputs* section in the *Detailed Description*.
Note 3: Reference input resistance is code dependent. See *Reference and Analog-Ground Inputs* section in the *Detailed Description*.
Note 4: Typical settling time with 1000pF capacitive load is 10µs.
Note 5: Guaranteed by design. Not production tested.
Note 6: Guaranteed by supply-rejection test.

TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

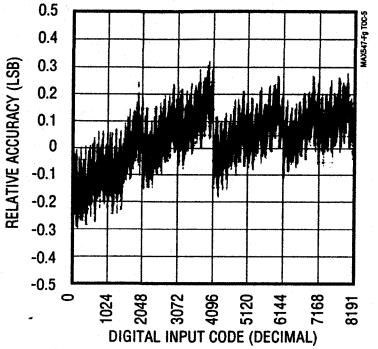
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width Low	t_1		50			ns
$\overline{WR}$ Pulse Width Low	t_2		50			ns
$\overline{LD\_}$ Pulse Width Low	t_3		50			ns
$\overline{CLR}$ Pulse Width Low	t_4		100			ns
$\overline{CS}$ Low to $\overline{WR}$ Low	t_5		0			ns
$\overline{CS}$ High to $\overline{WR}$ High	t_6		0			ns
Data Valid to $\overline{WR}$ Setup	t_7		50			ns
Data Valid to $\overline{WR}$ Hold	t_8		0			ns
Address Valid to $\overline{WR}$ Setup	t_9		50			ns
Address Valid to $\overline{WR}$ Hold	t_{10}		0			ns

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

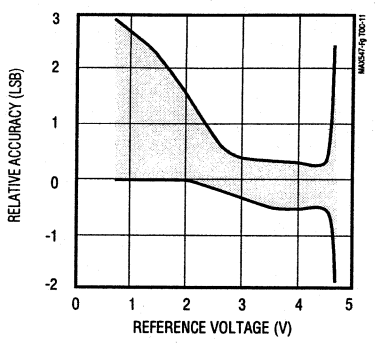
Typical Operating Characteristics

(V_{DD} = 5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = +25°C, unless otherwise noted.)

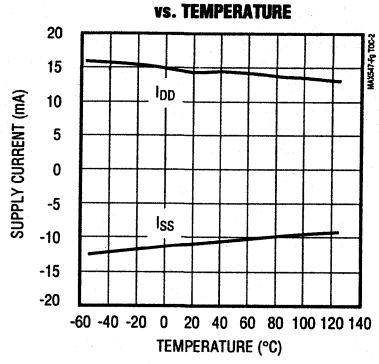
RELATIVE ACCURACY vs. DIGITAL INPUT CODE



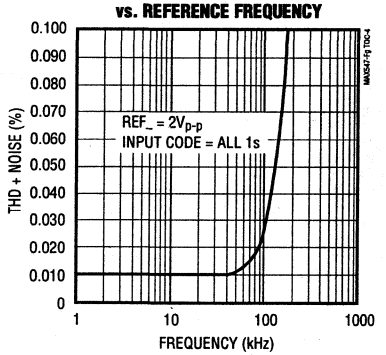
RELATIVE ACCURACY vs. REFERENCE VOLTAGE



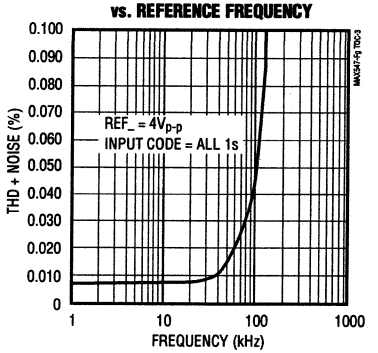
SUPPLY CURRENT vs. TEMPERATURE



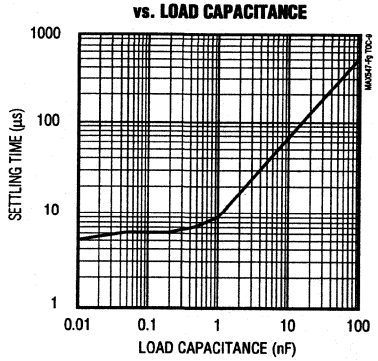
TOTAL HARMONIC DISTORTION + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



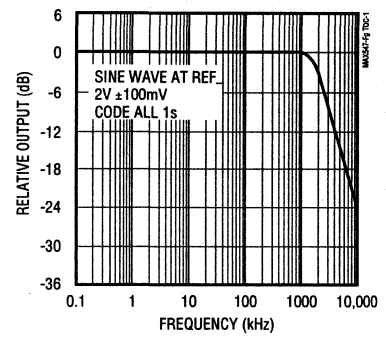
TOTAL HARMONIC DISTORTION + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



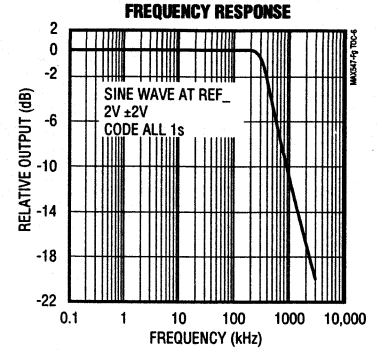
SETTLING TIME vs. LOAD CAPACITANCE



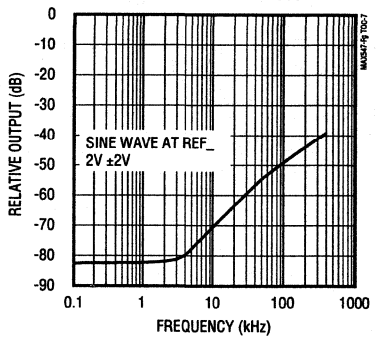
REFERENCE INPUT SMALL-SIGNAL FREQUENCY RESPONSE



REFERENCE INPUT LARGE-SIGNAL FREQUENCY RESPONSE



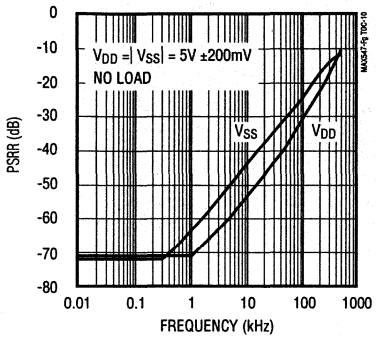
REFERENCE FEEDTHROUGH



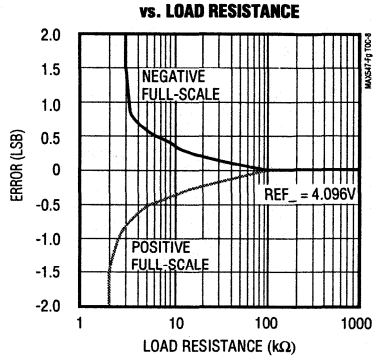
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = +25°C, unless otherwise noted.)

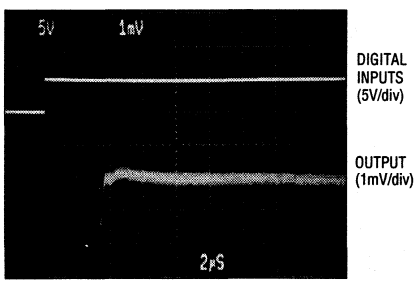
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



FULL-SCALE ERROR vs. LOAD RESISTANCE



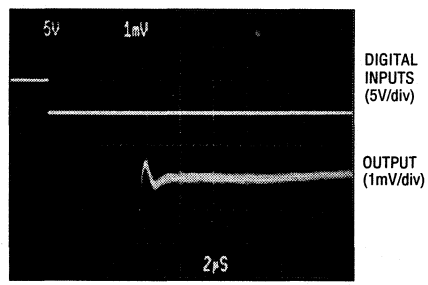
POSITIVE SETTLING TIME TO FULL-SCALE STEP (ALL BITS OFF TO ALL BITS ON)



2µs/div

REF_ = 4.096V, C_L = 100pF, R_L = 5kΩ

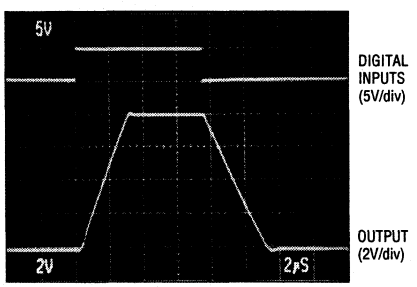
NEGATIVE SETTLING TIME TO FULL-SCALE STEP (ALL BITS ON TO ALL BITS OFF)



2µs/div

REF_ = 4.096V, C_L = 100pF, R_L = 5kΩ

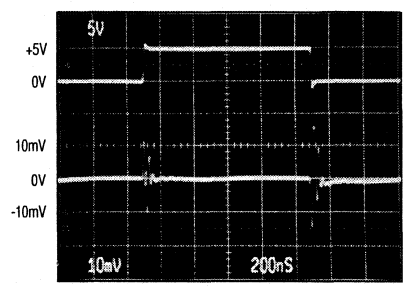
DYNAMIC RESPONSE (ALL BITS OFF, ON, OFF)



2µs/div

REF_ = 4.096V, C_L = 100pF, R_L = 5kΩ

DIGITAL FEEDTHROUGH (GLITCH IMPULSE)



200ns/div

TOP: DIGITAL TRANSITION ON ALL DATA BITS

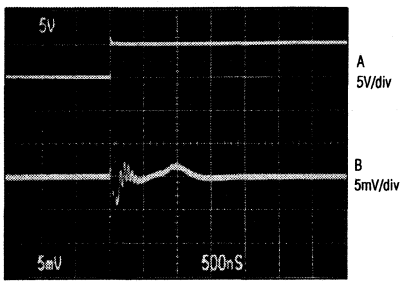
BOTTOM: DAC OUTPUT WITH $\overline{WR}$ HIGH 10mV/div

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Typical Operating Characteristics (continued)

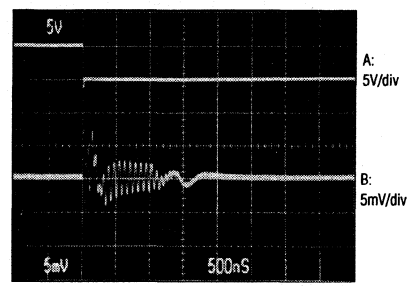
(V_{DD} = 5V, V_{SS} = -5V, REF_ = 4.096V, AGND_ = GND = 0V, T_A = +25°C, unless otherwise noted.)

ADJACENT-CHANNEL CROSSTALK



500ns/div
REF_ = 4.096V, C_L = 50pF, R_L = 10kΩ
A: DIGITAL INPUTS, DAC A, DATA BITS from ALL 0s to 0AAAhex
B: OUTPUT, DAC B

ADJACENT-CHANNEL CROSSTALK



500ns/div
REF_ = 4.096V, C_L = 50pF, R_L = 10kΩ
A: DIGITAL INPUTS, DAC A, DATA BITS from 0AAAhex to ALL 0s
B: OUTPUT, DAC B

Pin Description

PIN		NAME	FUNCTION
PLCC	FLAT PACK		
1	39	$\overline{CLR}$	Clear Input (active low). Driving this asynchronous input low sets the content of all latches to 1000hex. All DAC outputs are reset to AGND_.
2	40	AGNDCD	Analog Ground for DAC C and DAC D
3	41	REFCD	Reference Voltage Input for DAC C and DAC D. Bypass to AGNDCD with a 0.1µF to 1µF capacitor.
4, 42	42, 36	V_{SS}	Negative Power Supply, -5V (2 pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1µF to 1µF capacitor.
5	43	VOUTD	DAC D Output Voltage
6	44	VOUTC	DAC C Output Voltage
7	1	VOUTB	DAC B Output Voltage
8	2	VOUTA	DAC A Output Voltage
9, 37	3, 31	V_{DD}	Positive Power Supply, 5V (2 pins). Connect both pins to the supply voltage. Bypass each pin to the system analog ground with a 0.1µF to 1µF capacitor.
10	4	REFAB	Reference Voltage Input for DAC A and DAC B. Bypass to AGNDAB with a 0.1µF to 1µF capacitor.
11	5	AGNDAB	Analog Ground for DAC A and DAC B
12	6	$\overline{LDAB}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches A and B to the respective DAC latches.
13	7	$\overline{LDCD}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches C and D to the respective DAC latches.
14	8	$\overline{CS}$	Chip Select (active low)
15	9	$\overline{WR}$	Write Input (active low). $\overline{WR}$, along with $\overline{CS}$, loads data into the DAC input latch selected by A0–A2.

Pin Description (continued)

PIN		NAME	FUNCTION
PLCC	FLAT PACK		
16	10	A2	Address Bit 2
17	11	A1	Address Bit 1
18	12	A0	Address Bit 0
19–31	13–25	D12–D0	Data Bits 12–0
32	26	$\overline{LDEF}$	Load Input (active low). Driving this asynchronous input low transfers the content of input latches E and F to the respective DAC latches.
33	27	$\overline{LDGH}$	Load Input (active low). Driving this asynchronous input low transfers the contents of input latches G and H to the respective DAC latches.
34	28	GND	Digital Ground
35	29	AGNDGH	Analog Ground for DAC G and DAC H
36	30	REFGH	Reference Voltage Input for DAC G and DAC H. Bypass to AGNDGH with a 0.1µF to 1µF capacitor.
38	32	VOUTH	DAC H Output Voltage
39	33	VOUTG	DAC G Output Voltage
40	34	VOUTF	DAC F Output Voltage
41	35	VOUTE	DAC E Output Voltage
43	37	REFEF	Reference Voltage Input for DAC E and DAC F. Bypass to AGNDEF with a 0.1µF to 1µF capacitor.
44	38	AGNDEF	Analog Ground for DAC E and DAC F

Detailed Description

Analog Section

The MAX547 contains eight, 13-bit voltage-output DACs. These DACs are "inverted" R-2R ladder networks that convert 13-bit digital inputs into equivalent analog output voltages, in proportion to the applied reference voltages. The MAX547 has one reference input (REF_) and one analog-ground input (AGND_) for each pair of DACs. The four REF_ inputs allow different full-scale output voltages for each DAC pair, and the four AGND_ inputs allow different offset voltages for each DAC pair.

The DAC ladder outputs are buffered with op amps that operate with a gain of two. The inverting node of the amplifier is connected to the respective reference input, resulting in bipolar output voltages from -REF_ to 4095/4096 REF_. Figure 1 shows the simplified DAC circuit.

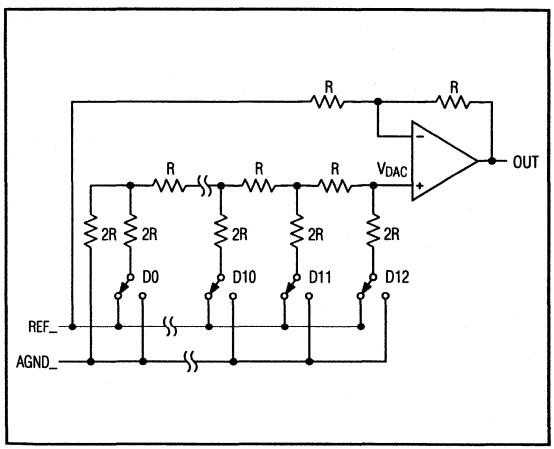


Figure 1. DAC Simplified Circuit Diagram

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Reference and Analog-Ground Inputs

The REF_ inputs can range between AGND_ and V_{DD}. However, the DAC outputs will operate to V_{DD} - 0.6V and V_{SS} + 0.6V, due to the output amplifiers' voltage-swing limitations. The AGND_ inputs can be offset by any voltage within the supply rails. The offset-voltage potential must be lower than the reference-voltage potential. For more information, refer to the *Digital Code* and *Analog Output Voltage* section in the *Applications Information.*

The input impedance of the REF_ inputs is code dependent. It is at its lowest value (5kΩ min) when the input code of the referring DAC pair is 0 1010 1010 1010 (0AAAhex). Its maximum value, typically 50kΩ, occurs when the code is 0000hex. When all reference inputs are driven from the same source, the minimum load impedance is 1.25kΩ. Since the input impedance at REF_ is code dependent, load regulation of the reference used is important. For more information, see *Reference Selection* in the *Applications Information* section.

The input capacitance at REF_ is also code dependent, and typically varies from 125pF to 300pF. Its minimum value occurs when the code of the referring DAC pair is set to all 0s. It is at its maximum value with all 1s on both DACs.

Output Buffer Amplifiers

The MAX547's voltage outputs are internally buffered by precision gain-of-two amplifiers with a typical slew rate of 3V/µs. With a full-scale transition at its output, the typical settling time to ±½LSB is 5µs when loaded with 10kΩ in parallel with 50pF, or 6µs when loaded with 10kΩ in parallel with 100pF.

Digital Inputs and Interface Logic

All digital inputs are compatible with both TTL and CMOS logic. The MAX547 interfaces with microprocessors using a data bus at least 13 bits wide. The interface is double buffered, allowing simultaneous update of all DACs. There are two latches for each DAC (see *Functional Diagram*): an input latch that receives data from the data bus, and a DAC latch that receives data from the input latch. Address lines A0, A1, and A2 select which DAC's input latch receives data from the data bus, as shown in Table 1. Transfer data from the input latches to the DAC latches by asserting the asynchronous $\overline{LD\_}$ signal. Each DAC's analog output reflects the data held in its DAC latch. All control inputs are level triggered.

Data can be latched or transferred directly to the DAC. $\overline{CS}$ and $\overline{WR}$ control the input latch and $\overline{LD\_}$ transfers information from the input latch to the DAC latch. The input latch is transparent when $\overline{CS}$ and $\overline{WR}$ are low, and the DAC latch is transparent when $\overline{LD\_}$ is low. Data is latched within the input latch when either $\overline{CS}$ or $\overline{WR}$ is high. Taking $\overline{LD\_}$ high latches data into the DAC latches.

If $\overline{LD\_}$ is brought low when $\overline{WR}$ and $\overline{CS}$ are low, it must be held low for t_3 or longer after $\overline{WR}$ and $\overline{CS}$ are high (Figure 3).

Pulling the asynchronous $\overline{CLR}$ input low sets all DAC outputs to a nominal 0V, regardless of the state of $\overline{CS}$, $\overline{WR}$, and $\overline{LD\_}$. Taking $\overline{CLR}$ high latches 1000hex into all input latches and DAC latches.

Table 1. MAX547 DAC Addressing

A2	A1	A0	FUNCTION
0	0	0	DAC A input latch
0	0	1	DAC B input latch
0	1	0	DAC C input latch
0	1	1	DAC D input latch
1	0	0	DAC E input latch
1	0	1	DAC F input latch
1	1	0	DAC G input latch
1	1	1	DAC H input latch

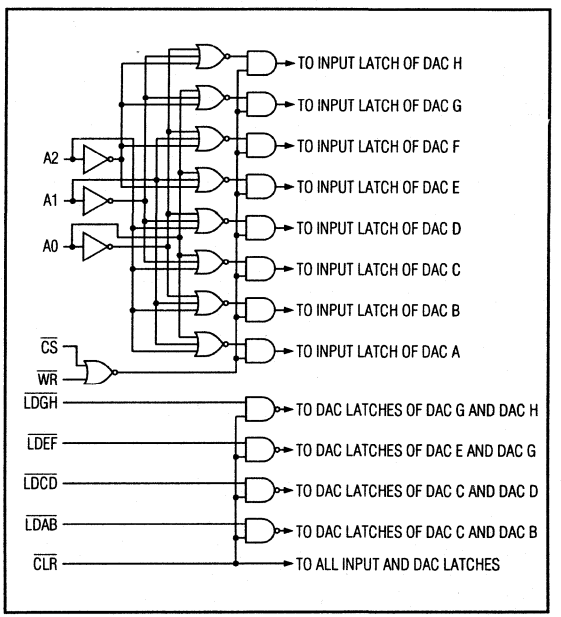
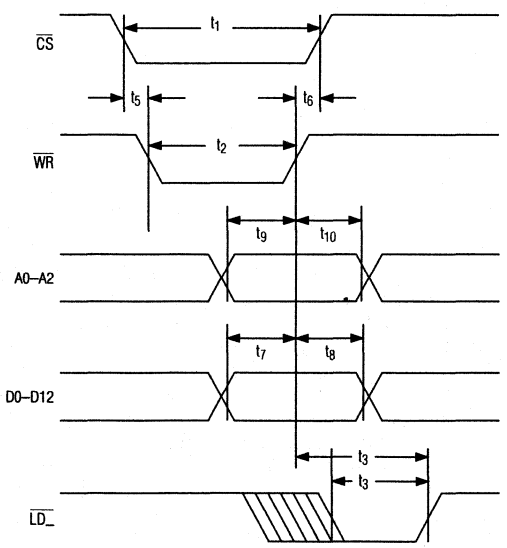


Figure 2. Input Control Logic

Table 2. Interface Truth Table

$\overline{CLR}$	$\overline{LD\_}$	$\overline{WR}$	$\overline{CS}$	FUNCTION
1	0	0	0	Both latches transparent
1	1	1	X	Both latches latched
1	1	X	1	Both latches latched
1	X	0	0	Input latch transparent
1	X	1	X	Input latch latched
1	X	X	1	Input latch latched
1	0	X	X	DAC latch transparent
0	X	X	X	All input and DAC latches at 1000hex, outputs at AGND_



NOTES:

1. ALL INPUT RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 5ns$.
2. MEASUREMENT REFERENCE LEVEL IS $(V_{INH} + V_{INL})/2$.
3. IF $\overline{LD\_}$ IS ACTIVATED WHILE $\overline{WR}$ IS LOW THEN $\overline{LD\_}$ MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 3. Write-Cycle Timing

Applications Information

Multiplying Operation

The MAX547 can be used for multiplying applications. Its reference accepts both DC and AC signals. The voltage at each REF_ input sets the full-scale output voltage for its respective DACs. Since the reference inputs accept only positive voltages, multiplying operation is limited to two quadrants. Do not bypass the reference inputs when applying AC signals to them. Refer to the graphs in the *Typical Operating Characteristics* for dynamic performance of the DACs and output buffers.

Digital Code and Analog Output Voltage

The MAX547 uses offset binary coding. A 13-bit twos-complement code can be converted to a 13-bit offset binary code by adding $2^{12} = 4096$.

Bipolar Output Voltage Range (AGND_ = 0V)

For symmetrical bipolar operation, tie AGND_ to the system ground. Table 3 shows the relationship between digital code and output voltage. The following paragraphs give a detailed explanation of this mode.

The DAC ladder output voltage (V_{DAC}) is multiplied by 2 and level shifted by the reference voltage, which is internally connected to the output amplifiers (Figure 1). Since the feedback resistors are the same size, the amplifier's output voltage is 2 times the voltage at its noninverting input, minus the reference voltage.

$$VOUT = 2(V_{DAC}) - REF\_$$

where VDAC is the voltage at the amplifier's noninverting input (DAC ladder output voltage), and REF_ is the voltage applied to the reference input of the DAC.

With AGND_ connected to the system ground, the DAC ladder output voltage is:

$$V_{DAC} = \frac{D}{2^n}(REF\_) = \frac{D}{2^{13}}(REF\_)$$

where D is the numeric value of the DAC's binary input code and n is the DAC's resolution (13 bits). Replace V_{DAC} in the equation and calculate the output voltage.

$$VOUT\_ = 2\left(\frac{D}{2^{13}}\right)(REF\_) - REF\_$$

$$= REF\_\left(\frac{D}{2^{12}} - 1\right) = REF\_\left(\frac{D}{4096} - 1\right)$$

D ranges from 0 (2^0) to 8191 ($2^{13} - 1$).

$$1LSB = REF\_\left(\frac{1}{4096}\right)$$

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Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Table 3. MAX547 Bipolar Code Table

(AGND_ = 0V)

INPUT	OUTPUT
1 1111 1111 1111	$+REF\_\left(\frac{4095}{4096}\right)$
1 0000 0000 0001	$+REF\_\left(\frac{1}{4096}\right)$
1 0000 0000 0000	0V
0 1111 1111 1111	$-REF\_\left(\frac{1}{4096}\right)$
0 0000 0000 0001	$-REF\_\left(\frac{4095}{4096}\right)$
0 0000 0000 0000	-REF_

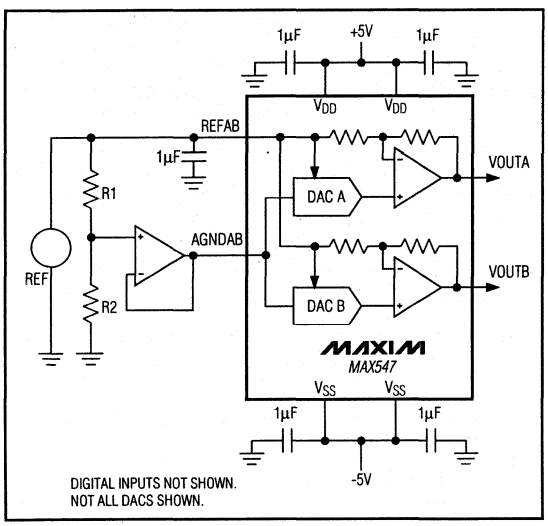


*Figure 4. Offsetting AGND_*

Positive Unipolar Output Voltage Range (AGND_ = REF_/2)

For positive unipolar output operation, set AGND_ to (REF_/2). For example, if you use Figure 4's circuit with, a 4.096V reference and offset AGND_ by 2.048V with matched resistors (R1 = R2) and an op amp, it results in a 0V to 4.0955V (nominal) unipolar output voltage, where 1LSB = 500µV. In general, the maximum current flowing out of any AGND_ pin is given by:

$$I_{AGND\_} = \left(\frac{REF\_ - AGND\_}{5k\Omega}\right)$$

Table 4. MAX547 Positive Unipolar Code Table

(AGND_ = $\frac{REF\_}{2}$)

INPUT	OUTPUT
1 1111 1111 1111	$+REF\_\left(\frac{8191}{8192}\right)$
1 0000 0000 0000	+REF_/2
0 0000 0000 0000	0V

Customizing the Output Voltage Range

The AGND_ inputs can be offset by any voltage within the supply rails if the voltage at the referring REF_ input is higher than the voltage at the AGND_ input. Select the reference voltage and the voltage at AGND_ so the resulting output voltages do not come within ±0.6V of the supply rails. Figure 4's circuit shows one way to add positive offset to AGND_; make sure that the op amp used has sufficient current-sink capability to take up the remaining AGND_ current:

$$I_{AGND\_} = \left(\frac{REF\_ - AGND\_}{5k\Omega}\right)$$

Another way is to digitally offset AGND_ by connecting the output of one DAC to one or more AGND_ inputs. Do not connect a DAC output to its own AGND_ input.

Table 5 summarizes the relationship between the reference and AGND_ potentials and the output voltage in the different modes of operation.

Power-Supply Sequencing

The sequence in which the supply voltages come up is not critical. However, we recommend that on power-up, V_{SS} comes up first, V_{DD} next, followed by the reference voltages. If you use other sequences, limit the current into any reference pin to 10mA. Also, make sure that V_{SS} is never more than 300mV above ground. If there is a risk that this can occur at power-up, connect a Schottky diode between V_{SS} and GND, as shown in Figure 5. We recommend that you not power up the logic input pins before establishing the supply voltages. If this is not possible and the digital lines can drive more than 10mA, you should place current-limiting resistors (e.g., 470Ω) in series with the logic pins.

Reference Selection

If you want a ±2.5V full-scale output voltage swing, you can use the MAX873 reference. It operates from a single 5V supply and is specified to drive up to 10mA. Therefore, it can drive all four reference inputs simultaneously. Because the maximum load impedance can vary from 1.25kΩ to 12.5kΩ (four reference inputs in parallel), the reference load current ranges from 2mA to 0.2mA (1.8mA maximum load step). The MAX873's

Table 5. Reference, AGND_ and Output Relationships

PARAMETER	BIPOLAR OPERATION (AGND_ = 0V)	POSITIVE UNIPOLAR OPERATION (AGND_ = REF_/2)	CUSTOM OPERATION
Bipolar Zero Level, or Unipolar Mid-scale, (Code = 1000000000000)	AGND_ (=0V)	AGND_ $\left(=\frac{REF\_}{2}\right)$	AGND_
Differential Reference Voltage (V_{DR})	REF_	REF_/2	REF_ - AGND_
Negative Full-scale Output (Code = All 0s)	-REF_	0V	AGND_ - V_{DR}
Positive Full-Scale Output (Code = All 1s)	$\left(\frac{4095}{4096}\right)\left(REF\_\right)$	$\left(\frac{8191}{8192}\right)\left(REF\_\right)$	AGND_ + $\left(\frac{4095}{4096}\right)\left(V_{DR}\right)$
LSB Weight	$\frac{REF\_}{4096}$	$\left(\frac{REF\_}{8192}\right)$	$\frac{V_{DR}}{4096}$
VOUT_ as a Function of Digital Code (D, 0 to 8191)	$\left(\frac{D}{4096} - 1\right)\left(REF\_\right)$	$\left(\frac{D}{8192}\right)\left(REF\_\right)$	AGND_ + $\left(\frac{D}{4096} - 1\right)\left(V_{DR}\right)$

load regulation is specified to 20ppm/mA max over temperature, resulting in a maximum error of 36ppm (90µV). This corresponds to a maximum error caused by reference load regulation of only 0.147LSB [0.147LSB = 90µV/(5V/8192)LSB] over temperature.

If you want a ±4.096V full-scale output swing (1LSB = 1mV), you can use the calibrated, low-drift, low-dropout MAX676. Operating from a 5V supply, it is fully specified to drive two REF_ inputs with less than 60.4µV error (0.0604LSB) over temperature, caused by the maximum load step.

Reference Buffering

Another way to obtain high accuracy is to buffer a reference with an op amp. When driving all reference inputs simultaneously, keep the closed-loop output impedance of the op amp below 0.03Ω to ensure an error of less than 0.1LSB. The op amp must also drive the capacitive load (typically 500pF to 1200pF).

Each reference input can also be buffered separately by using the circuit in Figure 6. A reference load step caused by a digital transition only affects the DAC pair where the code transition occurs. It also allows the use of references with little drive capability. Keep the closed-loop output impedance of each op amp below 0.12Ω, to ensure an error of less than 0.1LSB. Figure 6 shows the op amp's inverting input directly connected to the MAX547's reference terminal. This eliminates the influence of board lead resistance by sensing the voltage with a low-current path sense line directly at the reference input.

Adding feedback resistors to individual reference buffer amplifiers enables different reference voltages to be generated from a single reference.

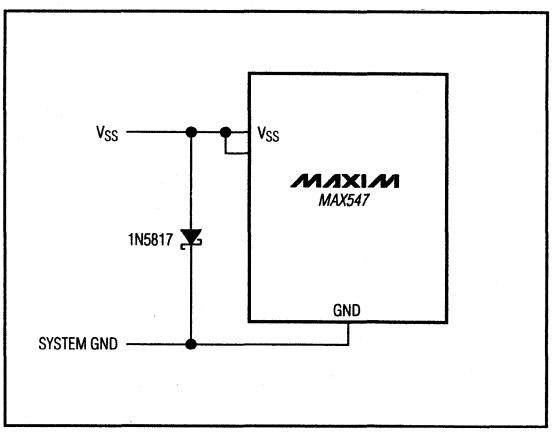


Figure 5. Optional Schottky Diode between V_{SS} and GND

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

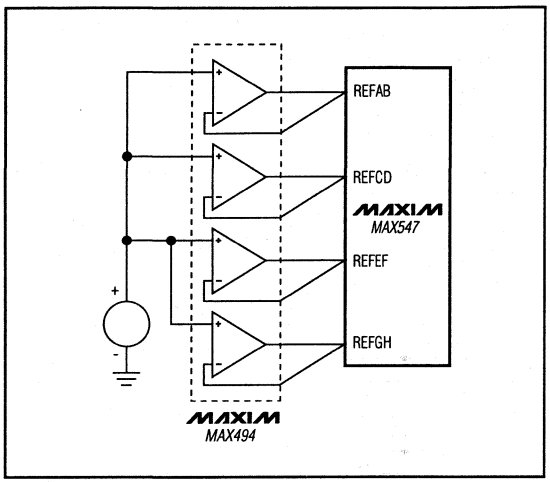


Figure 6. Reference Buffering

Power-Supply Bypassing and Ground Management

For optimum performance, use a multilayer PC board with an unbroken analog ground. For normal operation, when all AGND_ pins are at the same potential, connect the four AGND_ pins directly to the ground plane or connect them together in a "star" configuration. The center of this star point is a good location to connect the digital system ground with the analog ground.

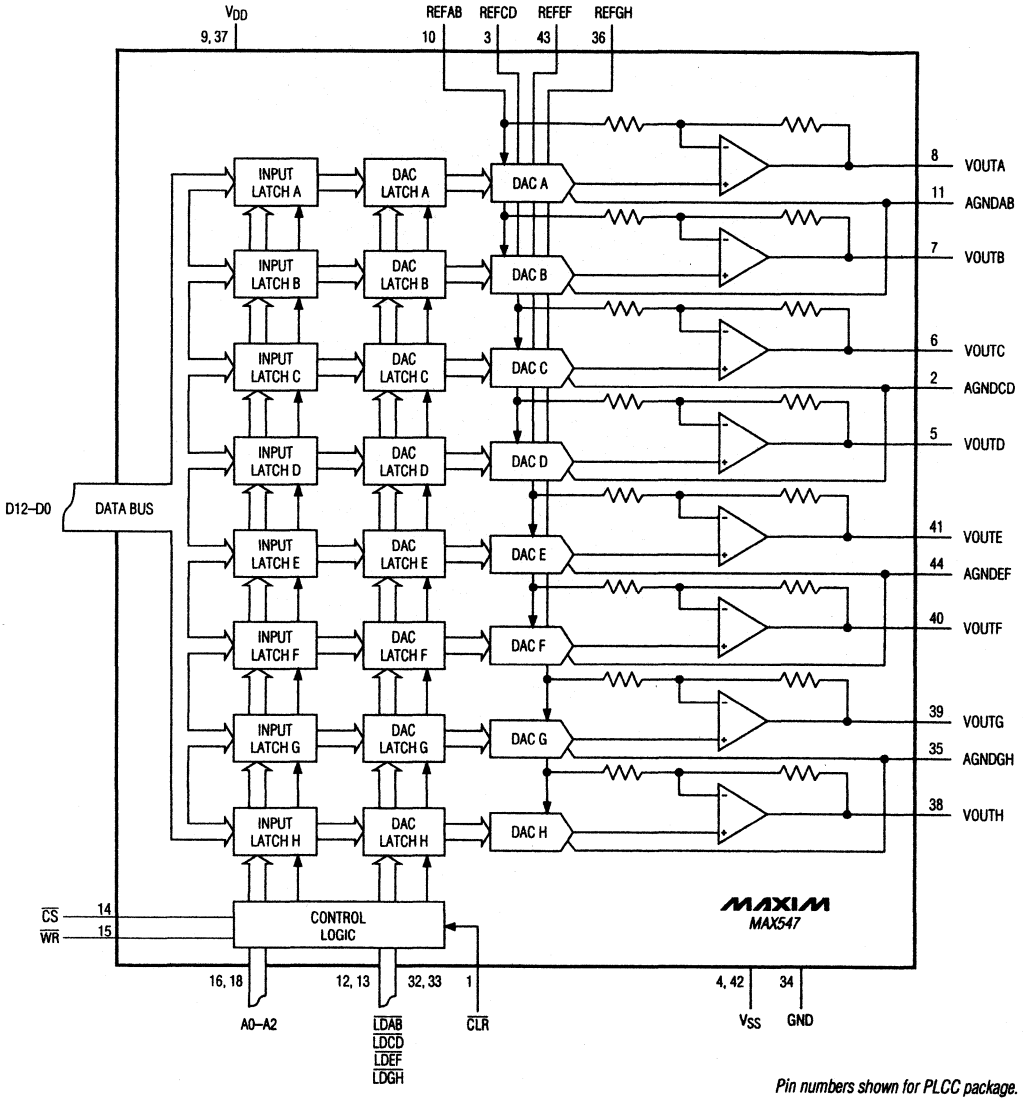
If you are using a single common reference voltage, you can connect the reference inputs together using a "star" configuration. If you are using DC reference voltages, bypass each reference input with a 0.1µF to 1µF capacitor to AGND_.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX547AEQH	-40°C to +85°C	44 PLCC	±2
MAX547BEQH	-40°C to +85°C	44 PLCC	±4
MAX547AEMH	-40°C to +85°C	44 Plastic FP	±2
MAX547BEMH	-40°C to +85°C	44 Plastic FP	±4

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

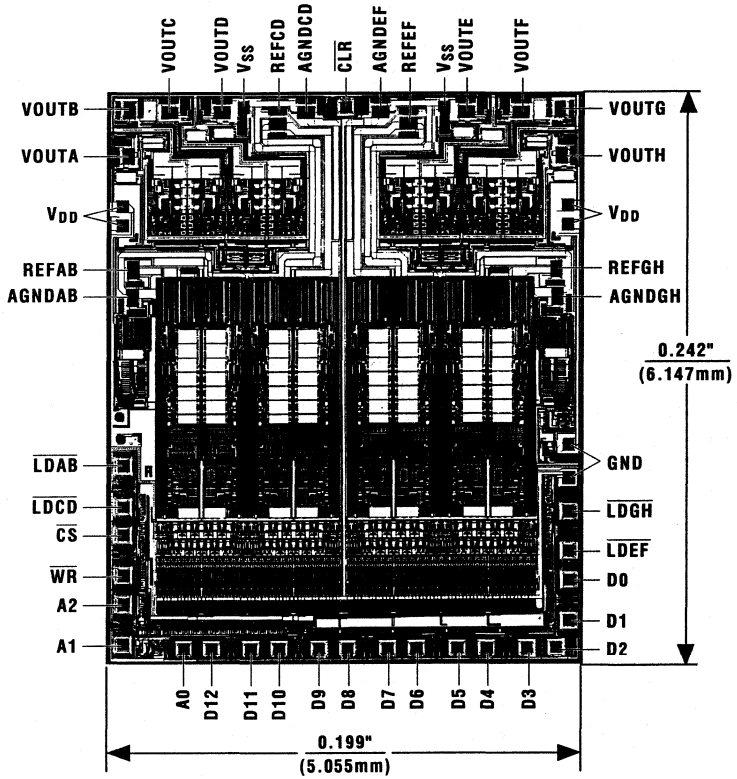
Functional Diagram



Pin numbers shown for PLCC package.

Octal, 13-Bit Voltage-Output DAC with Parallel Interface

Chip Topography



TRANSISTOR COUNT: 8987
SUBSTRATE CONNECTED TO V_{DD}

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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EVALUATION KIT AVAILABLE

MAXIM

250MHz, 12-Bit Multiplying DAC with Complementary Voltage Outputs

General Description

The MAX555 is an advanced, monolithic, 12-bit digital-to-analog converter (DAC) with complementary 50Ω outputs. Fabricated using an oxide-isolated bipolar process, the MAX555 is designed for signal-reconstruction applications at an output update rate of 250Msps. It incorporates an analog multiplying function with 10MHz usable-input bandwidth. The voltage-output DAC uses precision laser trimming to achieve 12-bit accuracy with ±1/2LSB integral and differential linearity (±0.0012% FS). Absolute gain error is a low 1% of full scale. Full-scale transitions occur in less than 0.5ns. On-chip registers and a unique decoder reduce glitching and allow the MAX555 to achieve precise RF performance with over 70dBc of spurious-free dynamic range at 50Msps and f_{OUT} = 3.125MHz, or 64dBc at 250Msps and f_{OUT} = 12.625MHz.

The MAX555 operates from a single -5.2V supply and dissipates 900mW (nominal) of power. It comes in a 68-pin thermally enhanced PLCC package capable of accepting a heatsink.

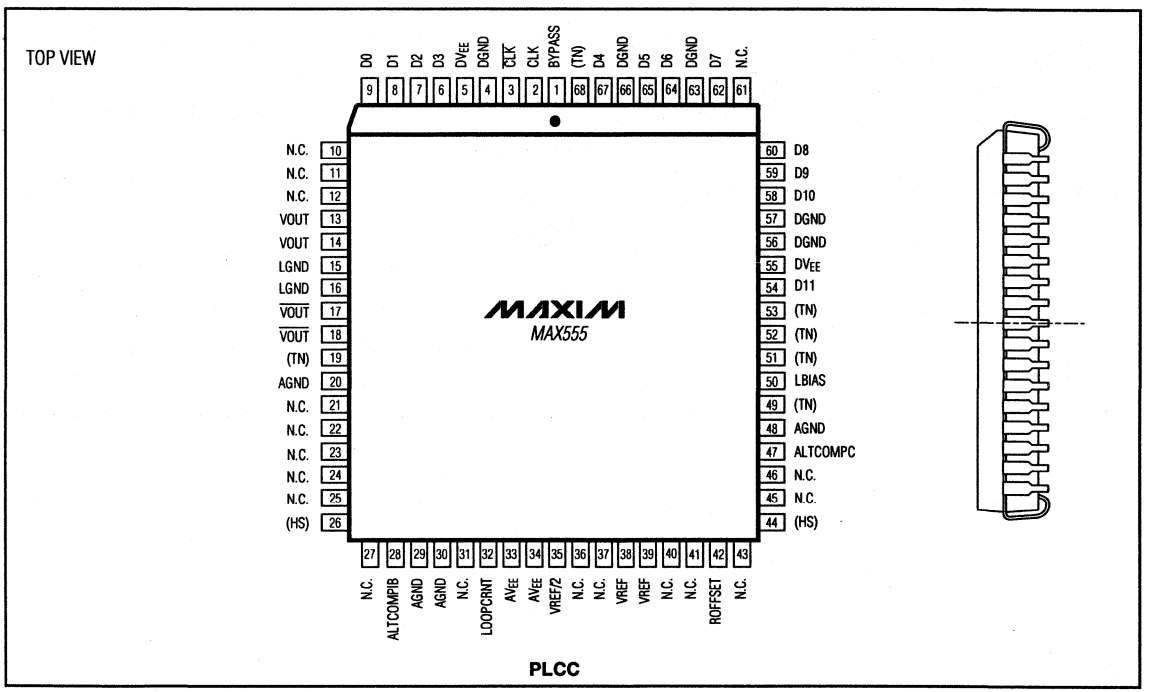
Features

- ♦ **12-Bit Resolution**
- ♦ **1/2 LSB Integral and Differential Linearity**
- ♦ **Capable of 250Msps Min Update Rate**
- ♦ **Complementary 50Ω Outputs**
- ♦ **Multiplying Reference Input**
- ♦ **Low Glitch Energy**
- ♦ **Single 5.2V Power Supply**
- ♦ **On-Chip Data Registers**

Applications

Direct Digital Synthesis
Arbitrary Waveform Generation
Professional Video Reconstruction
Instrumentation

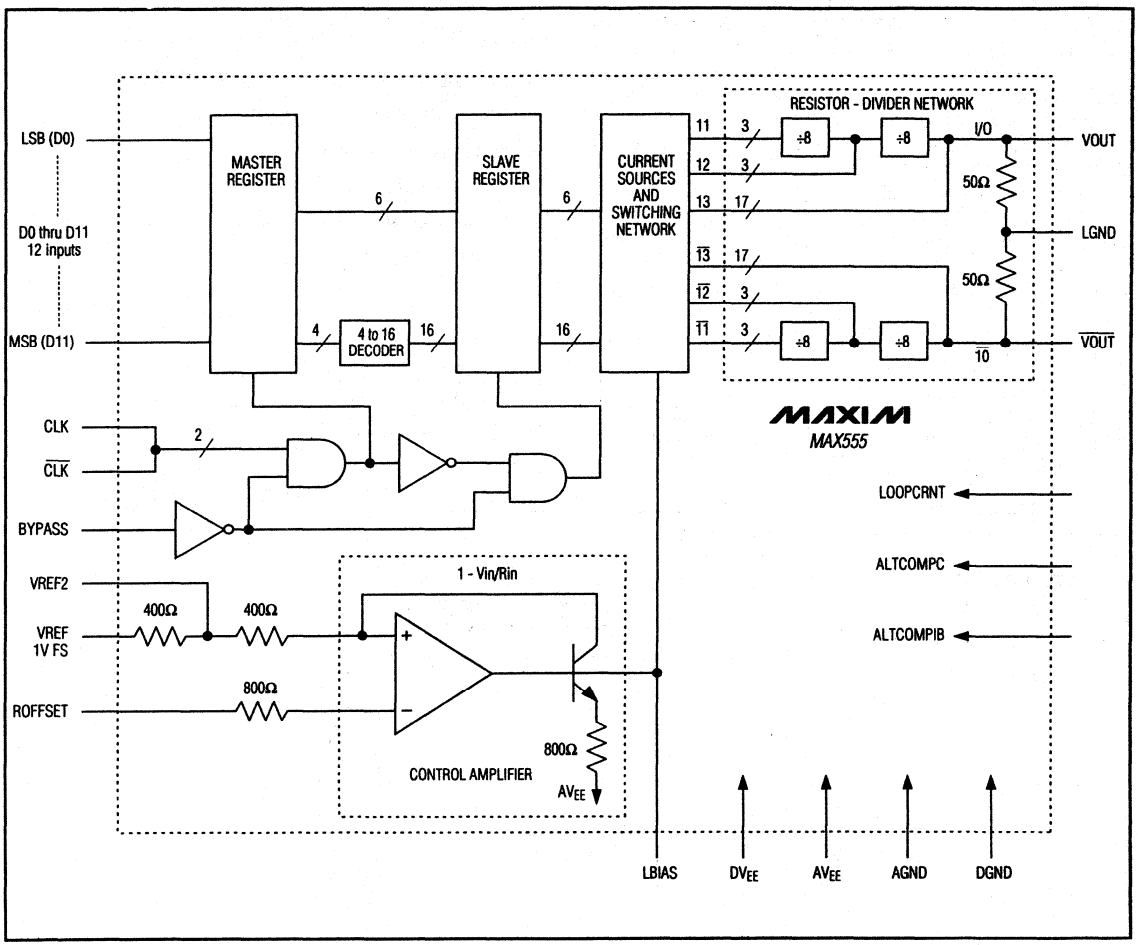
Pin Configuration



Functional Diagram on next page.

250MHz, 12-Bit Multiplying DAC with Complementary Voltage Outputs

Functional Diagram



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/94

MAXIM

5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC

General Description

The MAX503 is a low-power, 10-bit, voltage-output digital-to-analog converter (DAC) that uses single 5V or dual ±5V supplies. This device has an on-chip voltage reference plus an output buffer amplifier. Operating current is only 250µA from a single 5V supply, making it ideal for portable and battery-powered applications. In addition, the SSOP (Shrink Small-Outline Package) measures only 0.1 square inches, using less board area than an 8-pin DIP. 10-bit resolution is achieved through laser trimming of the DAC, op amp, and reference. No further adjustments are necessary.

Internal gain-setting resistors can be used to define a DAC output voltage range of 0V to +2.048V, 0V to +4.096V, or ±2.048V. Four-quadrant multiplication is possible without the use of external resistors or op amps. The parallel logic inputs are double buffered and are compatible with 4-bit, 8-bit, and 16-bit microprocessors. For a hardware and software compatible 12-bit upgrade, refer to the MAX530 data sheet. For DACs with similar features but with a serial data interface, refer to the MAX504/MAX515 data sheet.

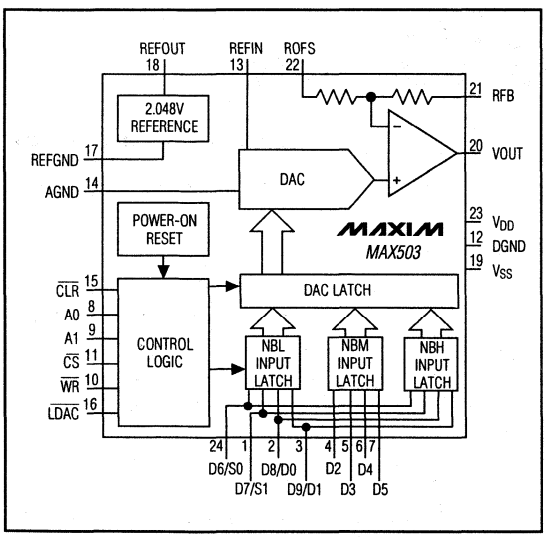
Features

- ♦ **Buffered Voltage Output**
- ♦ **Internal 2.048V Voltage Reference**
- ♦ **Operates from Single +5V or Dual ±5V Supplies**
- ♦ **Low Power Consumption:**
  250µA Operating Current
  40µA Shutdown-Mode Current
- ♦ **SSOP Package Saves Space**
- ♦ **Relative Accuracy: ±½ LSB Max Over Temperature**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **4-Quadrant Multiplication with No External Components**
- ♦ **Power-On Reset**
- ♦ **Double-Buffered Parallel Logic Inputs**
- ♦ **Hardware and Software Compatible with the 12-Bit MAX530**

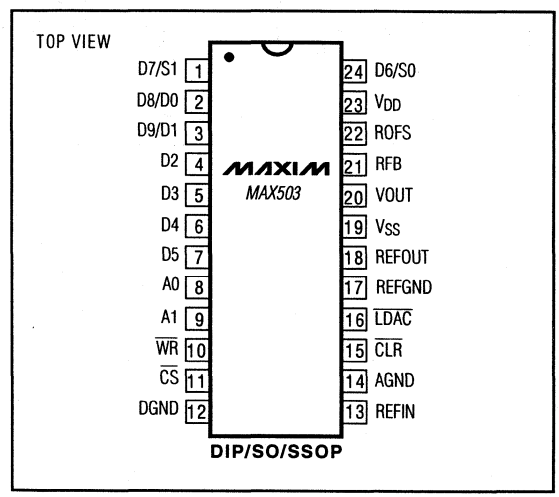
Applications

Battery-Powered Data-Conversion Products
Minimum Component-Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment
Microprocessor-Controlled Calibration

Typical Operating Circuit



Pin Configuration



9

MAXIM

5V, Low-Power, Voltage-Output, Serial 10-Bit DACs

General Description

The MAX504/MAX515 are low-power, voltage-output, 10-bit digital-to-analog converters (DACs) specified for single +5V power-supply operation. In addition, the MAX504 can be operated with ±5V supplies. The MAX515 draws only 140µA, and the MAX504, with internal reference, draws only 260µA. The MAX515 comes in 8-pin DIP and SO packages, while the MAX504 comes in 14-pin DIP and SO packages. All parts have been trimmed for offset voltage, gain, and linearity, so no further adjustment is necessary.

The MAX515's buffer is fixed at a gain of 2. The MAX504's internal op amp may be configured for a gain of 1 or 2, as well as for unipolar or bipolar output voltages. The MAX504 can also be used as a four-quadrant multiplier without external resistors or op amps.

For parallel data inputs, see the MAX503 data sheet. For a hardware and software compatible 12-bit upgrade, refer to the MAX531/MAX538/MAX539 data sheet.

Applications

Battery-Powered Test Instruments

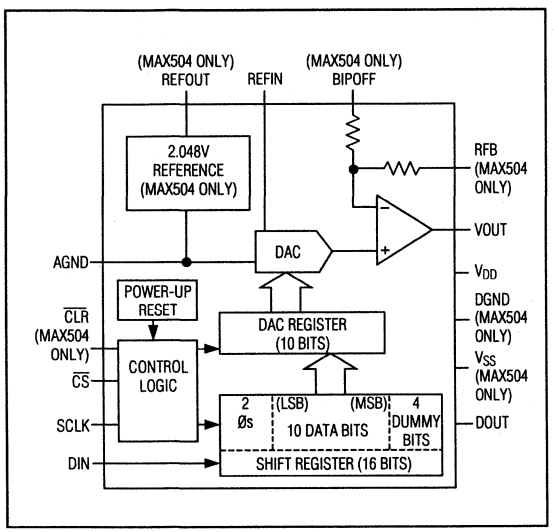
Digital Offset and Gain Adjustment

Battery-Operated/Remote Industrial Controls

Machine and Motion Control Devices

Cellular Telephones

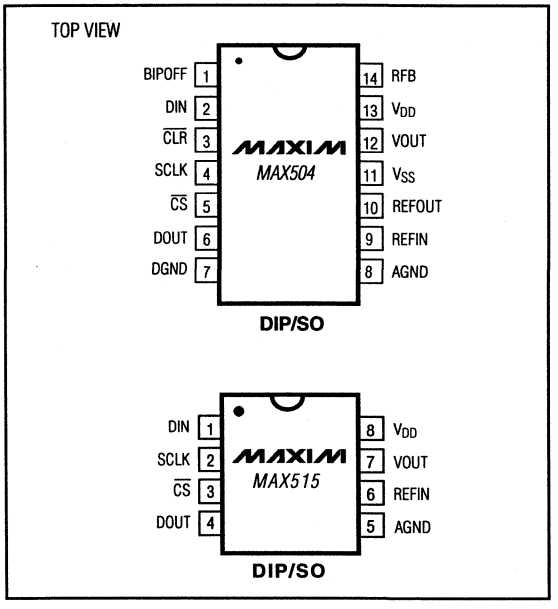
Functional Diagram



Features

- ♦ **Operate from Single +5V Supply**
- ♦ **Buffered Voltage Output**
- ♦ **Internal 2.048V Reference (MAX504)**
- ♦ **140µA Supply Current (MAX515)**
- ♦ **INL = ±1/2LSB (Max)**
- ♦ **Guaranteed Monotonic Over Temperature**
- ♦ **Flexible Output Ranges:**
  0V to V_{DD} (MAX504/MAX515)
  ±4.5V (MAX504)
  0V to 2.6V (MAX504)
- ♦ **8-Pin SO/DIP (MAX515)**
- ♦ **Power-On Reset**
- ♦ **Serial Data Output for Daisy-Chaining**
- ♦ **Hardware and Software Compatible with the 12-Bit MAX531/MAX538/MAX539**

Pin Configurations



Waveform Generator

Delay Lines

Quadrature Digitizer

10

*Advance Information–first page of data sheet in preparation.

19-0266; Rev 0; 6/94

MAXIM

High-Frequency Waveform Generator

General Description

The MAX038 is a high-frequency, precision function generator producing accurate, high-frequency triangle, sawtooth, sine, square, and pulse waveforms with a minimum of external components. The output frequency can be controlled over a frequency range of 0.1Hz to 20MHz by an internal 2.5V bandgap voltage reference and an external resistor and capacitor. The duty cycle can be varied over a wide range by applying a ±2.3V control signal, facilitating pulse-width modulation and the generation of sawtooth waveforms. Frequency modulation and frequency sweeping are achieved in the same way. The duty cycle and frequency controls are independent.

Sine, square, or triangle waveforms can be selected at the output by setting the appropriate code at two TTL-compatible select pins. The output signal for all waveforms is a $2V_{P-P}$ signal that is symmetrical around ground. The low-impedance output can drive up to ±20mA.

The TTL-compatible SYNC output from the internal oscillator maintains a 50% duty cycle—regardless of the duty cycle of the other waveforms—to synchronize other devices in the system. The internal oscillator can be synchronized to an external TTL clock connected to PDI.

Features

- ♦ **0.1Hz to 20MHz Operating Frequency Range**
- ♦ **Triangle, Sawtooth, Sine, Square, and Pulse Waveforms**
- ♦ **Independent Frequency and Duty-Cycle Adjustments**
- ♦ **350 to 1 Frequency Sweep Range**
- ♦ **15% to 85% Variable Duty Cycle**
- ♦ **Low-Impedance Output Buffer: 0.1Ω**
- ♦ **Low-Distortion Sine Wave: 0.75%**
- ♦ **Low 200ppm/°C Temperature Drift**

Ordering Information

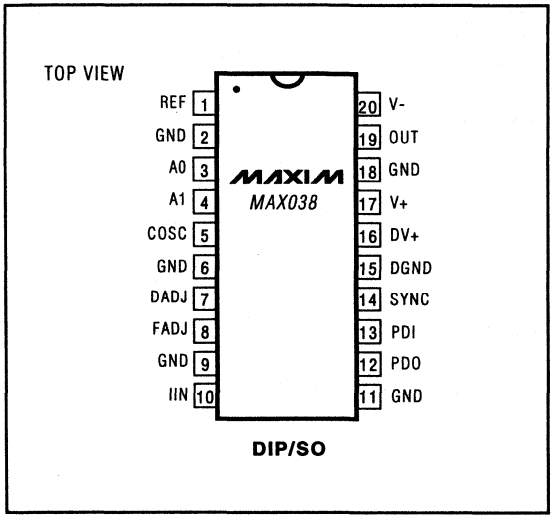
PART	TEMP. RANGE	PIN-PACKAGE
MAX038CPP	0°C to +70°C	20 Plastic DIP
MAX038CWP	0°C to +70°C	20 Wide SO
MAX038C/D	0°C to +70°C	Dice*
MAX038EPP	-40°C to +85°C	20 Plastic DIP
MAX038EWP	-40°C to +85°C	20 Wide SO

** Contact factory for dice specifications.*

Applications

Precision Function Generators
Voltage-Controlled Oscillators
Frequency Modulators
Pulse-Width Modulators
Phase-Locked Loops
Frequency Synthesizer
FSK Generator—Sine and Square Waves

Pin Configuration



High-Frequency Waveform Generator

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +6V
DV+ to DGND .....-0.3V to +6V
V- to GND .....+0.3V to -6V
Pin Voltages
  IIN, FADJ, DADJ, PDO .....(V- - 0.3V) to (V+ + 0.3V)
  COSC .....+0.3V to V-
  A0, A1, PDI, SYNC, REF .....-0.3V to V+
  GND to DGND .....±0.3V
Maximum Current into Any Pin .....±50mA
OUT, REF Short-Circuit Duration to GND, V+, V- 30sec

Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
  SO (derate 10.00mW/°C above +70°C) 800mW
  CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
  MAX038C_ _ .....0°C to +70°C
  MAX038E_ _ .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, GND = DGND = 0V, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, C_F = 100pF, R_{IN} = 25kΩ, R_L = 1kΩ, C_L = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY CHARACTERISTICS						
Maximum Operating Frequency	F_O	15pCF ≤ 15pF, I_{IN} = 500µA	20.0	40.0		MHz
Frequency Programming Current	I_{IN}	V_{FADJ} = 0V	2.50		750	µA
		V_{FADJ} = -3V	1.25		375	
IIN Offset Voltage	V_{IN}			±1.0	±2.0	mV
Frequency Temperature Coefficient	$\Delta F_O/°C$	V_{FADJ} = 0V		600		ppm/°C
	$F_O/°C$	V_{FADJ} = -3V		200		
Frequency Power-Supply Rejection	$\frac{(\Delta F_O/F_O)}{\Delta V+}$	V- = -5V, V+ = 4.75V to 5.25V		±0.4	±2.00	%/V
	$\frac{(\Delta F_O/F_O)}{\Delta V-}$	V+ = 5V, V- = -4.75V to -5.25V		±0.2	±1.00	
OUTPUT AMPLIFIER (applies to all waveforms)						
Output Peak-to-Peak Symmetry	V_{OUT}			±4		mV
Output Resistance	R_{OUT}			0.1	0.2	Ω
Output Short-Circuit Current	I_{OUT}	Short circuit to GND		40		mA
SQUARE-WAVE OUTPUT (R_L = 100Ω)						
Amplitude	V_{OUT}		1.9	2.0	2.1	V_{P-P}
Rise Time	t_R	10% to 90%		12		ns
Fall Time	t_F	90% to 10%		12		ns
Duty Cycle	dc	V_{DADJ} = 0V, dc = t_{ON}/t x 100%	47	50	53	%
TRIANGLE-WAVE OUTPUT (R_L = 100Ω)						
Amplitude	V_{OUT}		1.9	2.0	2.1	V_{P-P}
Nonlinearity		F_O = 100kHz, 5% to 95%		0.5		%
Duty Cycle	dc	V_{DADJ} = 0V (Note 1)	47	50	53	%
SINE-WAVE OUTPUT (R_L = 100Ω)						
Amplitude	V_{OUT}		1.9	2.0	2.1	V_{P-P}
Total Harmonic Distortion	THD	Duty cycle adjusted to 50%		0.75		%
		Duty cycle unadjusted		1.50		

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, GND = DGND = 0V, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, C_F = 100pF, R_{IN} = 25kΩ, R_L = 1kΩ, C_L = 20pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC OUTPUT						
Output Low Voltage	V_{OL}	I_{SINK} = 3.2mA		0.3	0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 400µA	2.8	3.5		V
Rise Time	t_R	10% to 90%, R_L = 3kΩ, C_L = 15pF		10		ns
Fall Time	t_F	90% to 10%, R_L = 3kΩ, C_L = 15pF		10		ns
Duty-Cycle	dc_{SYNC}			50		%
DUTY-CYCLE ADJUSTMENT (DADJ)						
DADJ Input Current	I_{DADJ}		190	250	320	µA
DADJ Voltage Range	V_{DADJ}			±2.3		V
Duty-Cycle Adjustment Range	dc	-2.3V ≤ V_{DADJ} ≤ 2.3V	15		85	%
DADJ Nonlinearity	dc/V_{FADJ}	-2V ≤ V_{DADJ} ≤ 2V		2	4	%
Change in Output Frequency with DADJ	F_O/V_{DADJ}	-2V ≤ V_{DADJ} ≤ 2V		±2.5	±8	%
Maximum DADJ Modulating Frequency	F_{DC}			2		MHz
FREQUENCY ADJUSTMENT (FADJ)						
FADJ Input Current	I_{FADJ}		190	250	320	µA
FADJ Voltage Range	V_{FADJ}			±2.4		V
Frequency Sweep Range	F_O	-2.4V ≤ V_{FADJ} ≤ 2.4V		±70		%
FM Nonlinearity with FADJ	F_O/V_{FADJ}	-2V ≤ V_{FADJ} ≤ 2V		±0.2		%
Change in Duty Cycle with FADJ	dc/V_{FADJ}	-2V ≤ V_{FADJ} ≤ 2V		±2		%
Maximum FADJ Modulating Frequency	F_F			2		MHz
VOLTAGE REFERENCE						
Output Voltage	V_{REF}	I_{REF} = 0	2.48	2.50	2.52	V
Temperature Coefficient	$V_{REF}/°C$			20		ppm/°C
Load Regulation	V_{REF}/I_{REF}	0mA ≤ I_{REF} ≤ 4mA (source)		1	2	mV/mA
		-100µA ≤ I_{REF} ≤ 0µA (sink)		1	4	
Line Regulation	$V_{REF}/V+$	4.75V ≤ V+ ≤ 5.25V (Note 1)		1	2	mV/V
LOGIC INPUTS (A0, A1, PDI)						
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.4			V
Input Current (A0, A1)	I_{IL}, I_{IH}	V_{A0}, V_{A1} = V_{IL}, V_{IH}			±5	µA
Input Current (PDI)	I_{IL}, I_{IH}	V_{PDI} = V_{IL}, V_{IH}			±25	µA
POWER SUPPLY						
Positive Supply Voltage	V+		4.75		5.25	V
SYNC Supply Voltage	DV+		4.75		5.25	V
Negative Supply Voltage	V-		-4.75		-5.25	V
Positive Supply Current	I+			35	45	mA
SYNC Supply Current	I_{DV+}			1	2	mA
Negative Supply Current	I-			45	55	mA

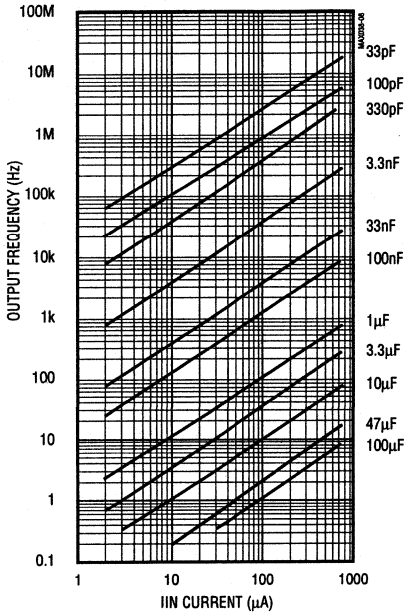
Note 1: Guaranteed by duty cycle test on square wave.
Note 2: V_{REF} is independent of V-.

High-Frequency Waveform Generator

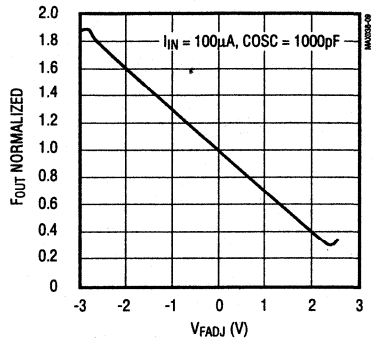
Typical Operating Characteristics

(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

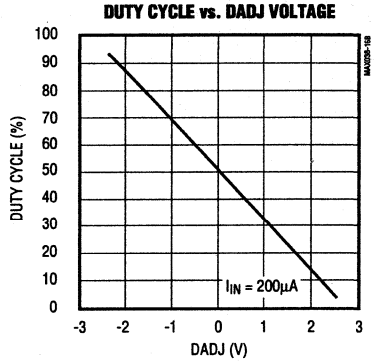
OUTPUT FREQUENCY vs. IIN CURRENT



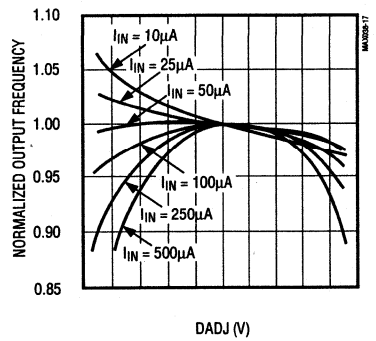
NORMALIZED OUTPUT FREQUENCY vs. FADJ VOLTAGE



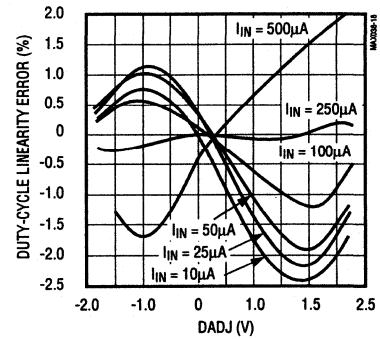
DUTY CYCLE vs. DADJ VOLTAGE



NORMALIZED OUTPUT FREQUENCY vs. DADJ VOLTAGE



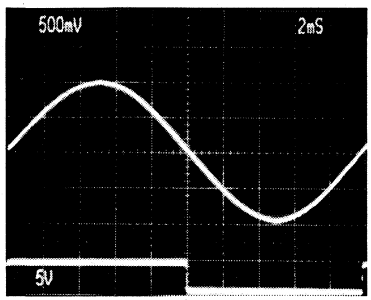
DUTY-CYCLE LINEARITY vs. DADJ VOLTAGE



Typical Operating Characteristics (continued)

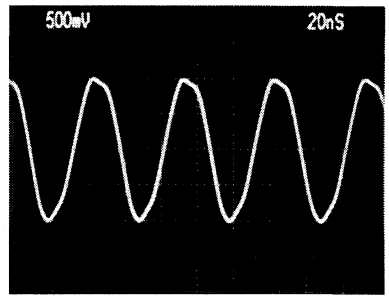
(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

SINE-WAVE OUTPUT (50Hz)



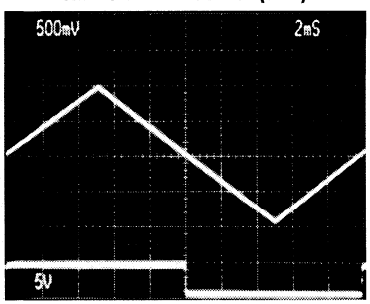
TOP: OUTPUT 50Hz = F_O
BOTTOM: SYNC
I_{IN} = 50µA
C_F = 1µF

SINE-WAVE OUTPUT (20MHz)



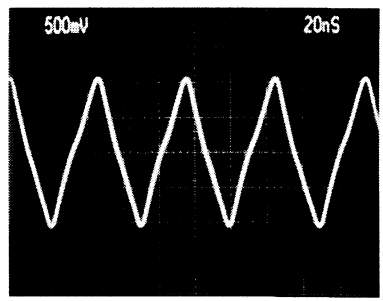
I_{IN} = 400µA
C_F = 20pF

TRIANGLE-WAVE OUTPUT (50Hz)



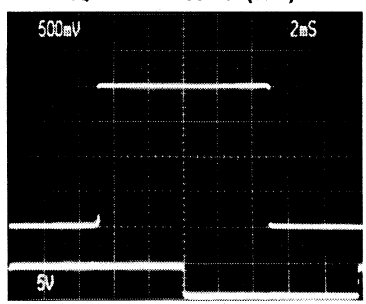
TOP: OUTPUT 50Hz = F_O
BOTTOM: SYNC
I_{IN} = 50µA
C_F = 1µF

TRIANGLE-WAVE OUTPUT (20MHz)



I_{IN} = 400µA
C_F = 20pF

SQUARE-WAVE OUTPUT (50Hz)



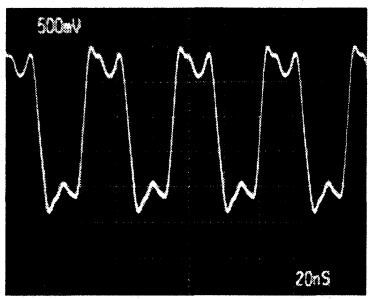
TOP: OUTPUT 50Hz = F_O
BOTTOM: SYNC
I_{IN} = 50µA
C_F = 1µF

High-Frequency Waveform Generator

Typical Operating Characteristics (continued)

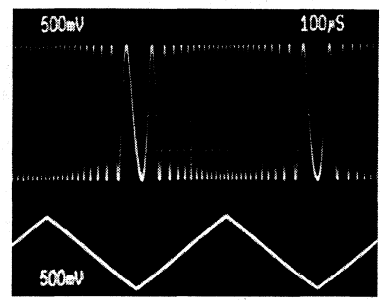
(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

SQUARE-WAVE OUTPUT (20MHz)



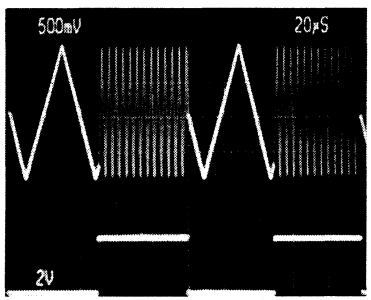
I_{IN} = 400µA
C_F = 20pF

FREQUENCY MODULATION USING FADJ



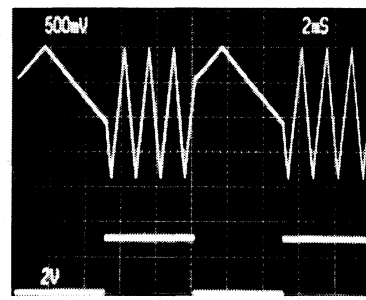
TOP: OUTPUT
BOTTOM: FADJ

FREQUENCY MODULATION USING I_{IN}



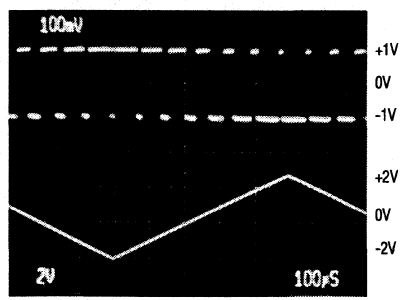
TOP: OUTPUT
BOTTOM: I_{IN}

FREQUENCY MODULATION USING I_{IN}



TOP: OUTPUT
BOTTOM: I_{IN}

PULSE-WIDTH MODULATION USING DADJ

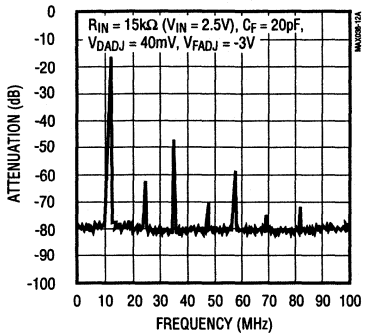


TOP: SQUARE-WAVE OUT, $2V_{P-P}$
BOTTOM: V_{DADJ}, -2V to +2.3V

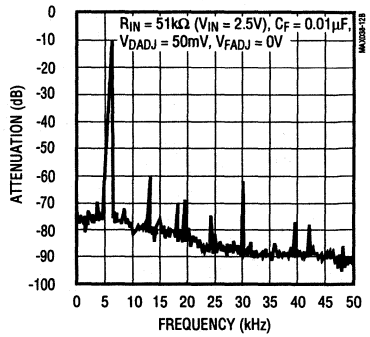
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V+ = DV+ = 5V, V- = -5V, V_{DADJ} = V_{FADJ} = V_{PDI} = V_{PDO} = 0V, R_L = 1kΩ, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

OUTPUT SPECTRUM, SINE WAVE
F_0 = 11.5MHz



OUTPUT SPECTRUM, SINE WAVE
F_0 = 5.9kHz



Pin Description

PIN	NAME	FUNCTION
1	REF	2.50V bandgap voltage reference output
2	GND	Ground*
3	A0	Waveform selection input; TTL/CMOS compatible
4	A1	Waveform selection input; TTL/CMOS compatible
5	COSC	External capacitor connection
6	GND	Ground*
7	DADJ	Duty-cycle adjust input
8	FADJ	Frequency adjust input
9	GND	Ground*
10	IIN	Current input for frequency control
11	GND	Ground*
12	PDO	Phase detector output. Connect to GND if phase detector is not used
13	PDI	Phase detector reference clock input. Connect to GND if phase detector is not used
14	SYNC	TTL-/CMOS-compatible output, referenced between DGND and DV+. Permits the internal oscillator to be synchronized with an external signal. Leave open if unused
15	DGND	Digital ground. Leave open to disable SYNC, or if SYNC is not used
16	DV+	Digital +5V supply input. Can be left open if SYNC is not used
17	V+	+5V supply input
18	GND	Ground*
19	OUT	Sine, square, or triangle output
20	V-	-5V supply input

* The five GND pins are not internally connected. Connect all five GND pins to a quiet ground close to the device. A ground plane is recommended (see *Layout Considerations*).

High-Frequency Waveform Generator

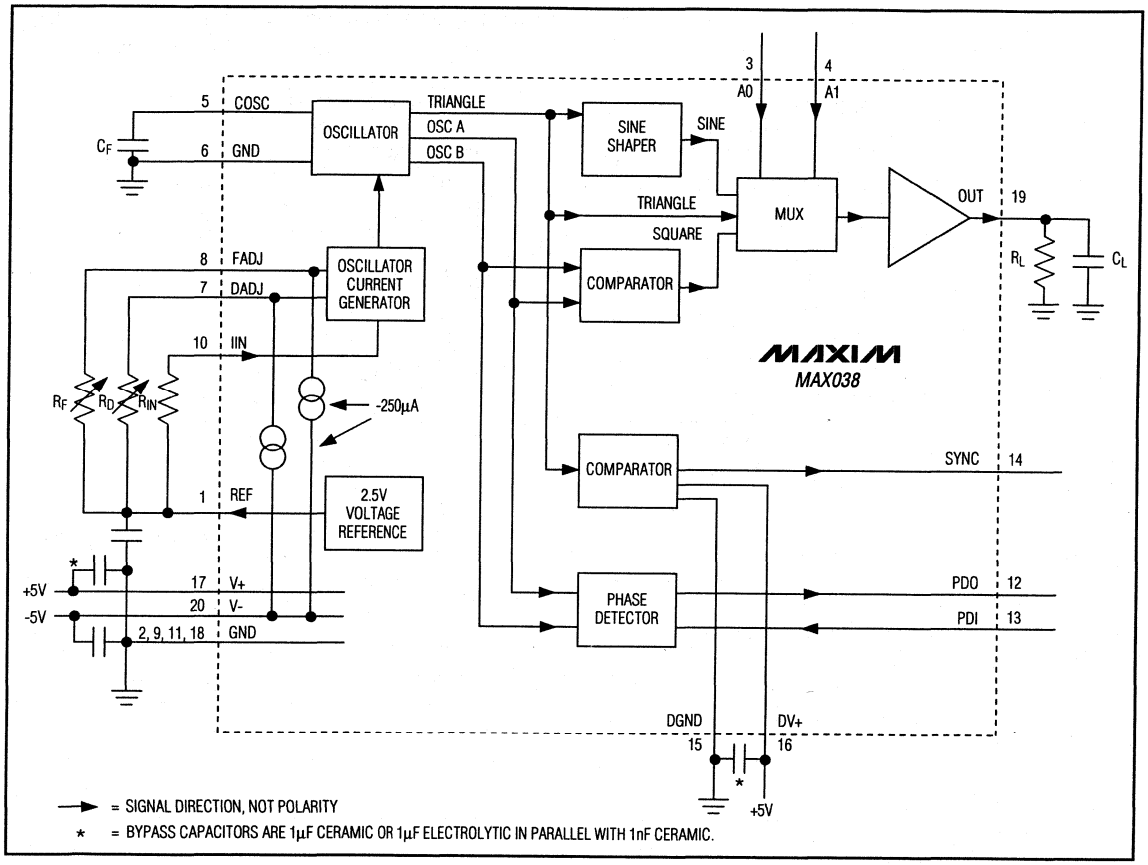


Figure 1. Block Diagram and Basic Operating Circuit

Detailed Description

The MAX038 is a high-frequency function generator that produces low-distortion sine, triangle, sawtooth, or square (pulse) waveforms at frequencies from less than 1Hz to 20MHz or more, using a minimum of external components. Frequency and duty cycle can be independently controlled by programming the current, voltage, or resistance. The desired output waveform is selected under logic control by setting the appropriate code at the A0 and A1 inputs. A SYNC output and phase detector are included to simplify designs requiring tracking to an external signal source.

The MAX038 operates with ±5V ±5% power supplies. The basic oscillator is a relaxation type that operates by alternately charging and discharging a capacitor, C_F, with constant currents, simultaneously producing a triangle wave and a square wave (Figure 1). The charging and discharging currents are controlled by the current flowing into IIN, and are modulated by the voltages applied to FADJ and DADJ. The current into IIN can be varied from 2µA to 750µA, producing more than two decades of frequency for any value of C_F. Applying ±2.4V to FADJ changes the nominal frequency (with V_{FADJ} = 0V) by ±70%; this procedure can be used for fine control.

Duty cycle (the percentage of time that the output waveform is positive) can be controlled from 10% to 90% by applying ±2.3V to DADJ. This voltage changes the C_F charging and discharging current ratio while maintaining nearly constant frequency.

High-Frequency Waveform Generator

A stable 2.5V reference voltage, REF, allows simple determination of IIN, FADJ, or DADJ with fixed resistors, and permits adjustable operation when potentiometers are connected from each of these inputs to REF. FADJ and/or DADJ can be grounded, producing the nominal frequency with a 50% duty cycle.

The output frequency is inversely proportional to capacitor C_F. C_F values can be selected to produce frequencies above 20MHz.

A sine-shaping circuit converts the oscillator triangle wave into a low-distortion sine wave with constant amplitude. The triangle, square, and sine waves are input to a multiplexer. Two address lines, A0 and A1, control which of the three waveforms is selected. The output amplifier produces a constant $2V_{P-P}$ amplitude (±1V), regardless of wave shape or frequency.

The triangle wave is also sent to a comparator that produces a high-speed square-wave SYNC waveform that can be used to synchronize other oscillators. The SYNC circuit has separate power-supply leads and can be disabled.

Two other phase-quadrature square waves are generated in the basic oscillator and sent to one side of an "exclusive-OR" phase detector. The other side of the phase-detector input (PDI) can be connected to an external oscillator. The phase-detector output (PDO) is a current source that can be connected directly to FADJ to synchronize the MAX038 with the external oscillator.

Waveform Selection

The MAX038 can produce either sine, square, or triangle waveforms. The TTL-/CMOS-logic address pins (A0 and A1) set the waveform, as shown below:

A0	A1	WAVEFORM
X	1	Sine wave
0	0	Square wave
1	0	Triangle wave

X = Don't care

Waveform switching can be done at any time, without regard to the phase of the output. Switching occurs within 0.3µs, but there may be a small transient in the output waveform that lasts 0.5µs.

Waveform Timing

Output Frequency

The output frequency is determined by the current injected into the IIN pin, the COSC capacitance (to ground), and the voltage on the FADJ pin. When V_{FADJ} = 0V, the fundamental output frequency (F_O) is given by the formula:

$$F_O\ (MHz) = I_{IN}\ (\mu A) \div C_F\ (pF) \qquad [1]$$

The period (t_O) is:

$$t_O\ (\mu s) = C_F\ (pF) \div I_{IN}\ (\mu A) \qquad [2]$$

where:

I_{IN} = current injected into IIN (between 2µA and 750µA)

C_F = capacitance connected to COSC and GND (20pF to >100µF).

For example:

0.5MHz = 100µA ÷ 200pF

and

2µs = 200pF ÷ 100µA

Optimum performance is achieved with I_{IN} between 10µA and 400µA, although linearity is good with I_{IN} between 2µA and 750µA. Current levels outside of this range are not recommended. For fixed-frequency operation, set I_{IN} to approximately 100µA and select a suitable capacitor value. This current produces the lowest temperature coefficient, and produces the lowest frequency shift when varying the duty cycle.

The capacitance can range from 20pF to more than 100µF, but stray circuit capacitance must be minimized by using short traces. Surround the COSC pin and the trace leading to it with a ground plane to minimize coupling of extraneous signals to this node. Oscillation above 20MHz is possible, but waveform distortion increases under these conditions. The low frequency limit is set by the leakage of the COSC capacitor and by the required accuracy of the output frequency. Lowest frequency operation with good accuracy is usually achieved with 10µF or greater non-polarized capacitors.

An internal closed-loop amplifier forces IIN to virtual ground, with an input offset voltage less than ±2mV. IIN may be driven with either a current source (I_{IN}), or a voltage (V_{IN}) in series with a resistor (R_{IN}). (A resistor between REF and IIN provides a convenient method of generating I_{IN}: $I_{IN} = V_{REF}/R_{IN}$.) When using a voltage in series with a resistor, the formula for the oscillator frequency is:

$$F_O\ (MHz) = V_{IN} \div [R_{IN} \times C_F\ (pF)] \qquad [3]$$

and:

$$t_O\ (\mu s) = C_F\ (pF) \times R_{IN} \div V_{IN} \qquad [4]$$

High-Frequency Waveform Generator

When the MAX038's frequency is controlled by a voltage source (V_{IN}) in series with a fixed resistor (R_{IN}), the output frequency is a direct function of V_{IN} as shown in the above equations. Varying V_{IN} modulates the oscillator frequency. For example, using a 10kΩ resistor for R_{IN} and sweeping V_{IN} from 20mV to 7.5V produces large frequency deviations (up to 375:1). Select R_{IN} so that I_{IN} stays within the 2µA to 750µA range. The bandwidth of the IIN control amplifier, which limits the modulating signal's highest frequency, is typically 2MHz.

IIN can be used as a summing point to add or subtract currents from several sources. This allows the output frequency to be a function of the sum of several variables. As V_{IN} approaches 0V, the I_{IN} error increases due to the offset voltage of IIN.

Output frequency will be offset 1% from its final value for 10 seconds after power-up.

FADJ Input

The output frequency can be modulated by FADJ, which is intended principally for fine frequency control, usually inside phase-locked loops. Once the fundamental, or center frequency (F_O) is set by I_{IN}, it may be changed further by setting FADJ to a voltage other than 0V. This voltage can vary from -2.4V to +2.4V, causing the output frequency to vary from 1.7 to 0.30 times the value when FADJ is 0V (F_O ±70%). Voltages beyond ±2.4V can cause instability or cause the frequency change to reverse slope.

The voltage on FADJ required to cause the output to deviate from F_O by D_X (expressed in %) is given by the formula:

$$VFADJ = -0.0343 \times D_X \quad [5]$$

where V_{FADJ}, the voltage on FADJ, is between -2.4V and +2.4V.

Note: While I_{IN} is directly proportional to the fundamental, or center frequency (F_O), V_{FADJ} is linearly related to % deviation from F_O. V_{FADJ} goes to either side of 0V, corresponding to plus and minus deviation.

The voltage on FADJ for any frequency is given by the formula:

$$V_{FADJ} = (F_O - F_X) \div (0.2915 \times F_O) \quad [6]$$

where:

F_X = output frequency

F_O = frequency when V_{FADJ} = 0V.

Likewise, for period calculations:

$$V_{FADJ} = 3.43 \times (t_X - t_O) \div t_X \quad [7]$$

where:

t_X = output period

t_O = period when V_{FADJ} = 0V.

Conversely, if V_{FADJ} is known, the frequency is given by:

$$F_X = F_O \times (1 - [0.2915 \times V_{FADJ}]) \quad [8]$$

and the period (t_X) is:

$$t_X = t_O \div (1 - [0.2915 \times V_{FADJ}]) \quad [9]$$

Programming FADJ

FADJ has a 250µA constant current sink to V- that must be furnished by the voltage source. The source is usually an op-amp output, and the temperature coefficient of the current sink becomes unimportant. For manual adjustment of the deviation, a variable resistor can be used to set V_{FADJ}, but then the 250µA current sink's temperature coefficient becomes significant. Since external resistors cannot match the internal temperature-coefficient curve, using external resistors to program V_{FADJ} is intended only for manual operation, when the operator can correct for any errors. This restriction does not apply when V_{FADJ} is a true voltage source.

A variable resistor, R_F, connected between REF (+2.5V) and FADJ provides a convenient means of manually setting the frequency deviation. The resistance value (R_F) is:

$$R_F = (V_{REF} - V_{FADJ}) \div 250\mu A \quad [10]$$

V_{REF} and V_{FADJ} are signed numbers, so use correct algebraic convention. For example, if V_{FADJ} is -2.0V (+58.3% deviation), the formula becomes:

$$R_F = (+2.5V - (-2.0V)) \div 250\mu A$$
$$= (4.5V) \div 250\mu A$$
$$= 18k\Omega$$

Disabling FADJ

The FADJ circuit adds a small temperature coefficient to the output frequency. For critical open-loop applications, it can be turned off by connecting FADJ to GND (not REF) through a 12kΩ resistor (R1 in Figure 2). The -250µA current sink at FADJ causes -3V to be developed across this resistor, producing two results. First, the FADJ circuit remains in its linear region, but disconnects itself from the main oscillator, improving temperature stability. Second, the oscillator frequency doubles. If FADJ is turned off in this manner, be sure to correct equations 1-4 and 6-9 above, and 12 and 14 below by doubling F_O or halving t_O. Although this method doubles the normal output frequency, it does not double the upper frequency limit. Do not operate FADJ open circuit or with voltages more negative than -3.5V. Doing so may cause transistor saturation inside the IC, leading to unwanted changes in frequency and duty cycle.

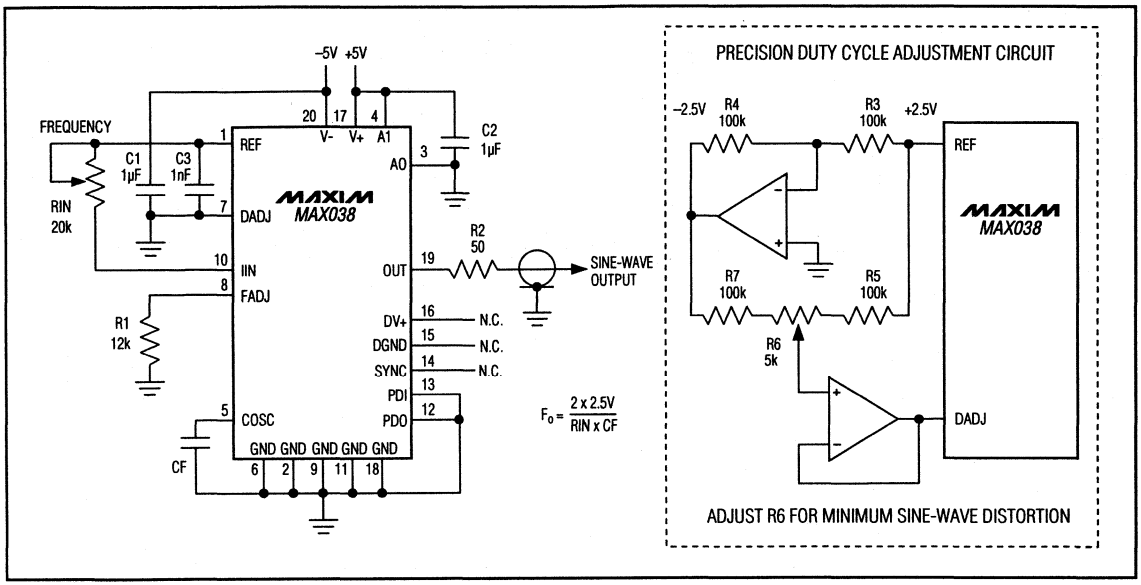


Figure 2. Operating Circuit with Sine-Wave Output and 50% Duty Cycle; SYNC and FADJ Disabled

With FADJ disabled, the output frequency can still be changed by modulating I_{IN}.

Swept Frequency Operation

The output frequency can be swept by applying a varying signal to IIN or FADJ. IIN has a wider range, slightly slower response, lower temperature coefficient, and requires a single polarity current source. FADJ may be used when the swept range is less than ±70% of the center frequency, and it is suitable for phase-locked loops and other low-deviation, high-accuracy closed-loop controls. It uses a sweeping voltage symmetrical about ground.

Connecting a resistive network between REF, the voltage source, and FADJ or IIN is a convenient means of offsetting the sweep voltage.

Duty Cycle

The voltage on DADJ controls the waveform duty cycle (defined as the percentage of time that the output waveform is positive). Normally, V_{DADJ} = 0V, and the duty cycle is 50% (Figure 2). Varying this voltage from +2.3V to -2.3V causes the output duty cycle to vary from 15% to 85%, about -15% per volt. Voltages beyond ±2.3V can shift the output frequency and/or cause instability.

DADJ can be used to reduce the sine-wave distortion. The unadjusted duty cycle (V_{DADJ} = 0V) is 50% ±2%; any deviation from exactly 50% causes even order harmonics to be generated. By applying a small adjustable voltage (typically less than ±100mV) to V_{DADJ}, exact symmetry can be attained and the distortion can be minimized (see Figure 2).

The voltage on DADJ needed to produce a specific duty cycle is given by the formula:

$$V_{DADJ} = (50\% - dc) \times 0.0575 \quad [11]$$

or:

$$V_{DADJ} = (0.5 - [t_{ON} \div t_o]) \times 5.75 \quad [12]$$

where:

V_{DADJ} = DADJ voltage (observe the polarity)

dc = duty cycle (in %)

t_{ON} = ON (positive) time

t_o = waveform period.

Conversely, if V_{DADJ} is known, the duty cycle and ON time are given by:

$$dc = 50\% - (V_{DADJ} \times 17.4) \quad [13]$$

$$t_{ON} = t_o \times (0.5 - [V_{DADJ} \times 0.174]) \quad [14]$$

High-Frequency Waveform Generator

Programming DADJ

DADJ is similar to FADJ; it has a 250µA constant current sink to V- that must be furnished by the voltage source. The source is usually an op-amp output, and the temperature coefficient of the current sink becomes unimportant. For manual adjustment of the duty cycle, a variable resistor can be used to set V_{DADJ}, but then the 250µA current sink's temperature coefficient becomes significant. Since external resistors cannot match the internal temperature-coefficient curve, using external resistors to program V_{DADJ} is intended only for manual operation, when the operator can correct for any errors. This restriction does not apply when V_{DADJ} is a true voltage source.

A variable resistor, R_D, connected between REF (+2.5V) and DADJ provides a convenient means of manually setting the duty cycle. The resistance value (R_D) is:

$$R_D = (V_{REF} - V_{DADJ}) \div 250\mu A \qquad [15]$$

Note that both V_{REF} and V_{DADJ} are signed values, so observe correct algebraic convention. For example, if V_{DADJ} is -1.5V (23% duty cycle), the formula becomes:

$$R_D = (+2.5V - (-1.5V)) \div 250\mu A$$
$$= (4.0V) \div 250\mu A = 16k\Omega$$

Varying the duty cycle in the range 15% to 85% has minimal effect on the output frequency—typically less than 2% when $25\mu A < I_{IN} < 250\mu A$. The DADJ circuit is wideband, and can be modulated at up to 2MHz (see photos, *Typical Operating Characteristics*).

Output

The output amplitude is fixed at $2V_{P-P}$, symmetrical around ground, for all output waveforms. OUT has an output resistance of under 0.1Ω, and can drive ±20mA with up to a 50pF load. Isolate higher output capacitance from OUT with a resistor (typically 50Ω) or buffer amplifier.

Reference Voltage

REF is a stable 2.50V bandgap voltage reference capable of sourcing 4mA or sinking 50µA. It is principally used to furnish a stable current to IIN or to bias DADJ and FADJ. It can also be used for other applications external to the MAX038. Bypass REF with 100nF to minimize noise.

Selecting Resistors and Capacitors

The MAX038 produces a stable output frequency over time and temperature, but the capacitor and resistors that determine frequency can degrade performance if they are not carefully chosen. Resistors should be metal film, 1% or better. Capacitors should be chosen for low temperature coefficient over the whole temperature range. NPO ceramics are usually satisfactory.

The voltage on COSC is a triangle wave that varies between 0V and -1V. Polarized capacitors are generally not recommended (because of their outrageous temperature dependence and leakage currents), but if they are used, the negative terminal should be connected to COSC and the positive terminal to GND. Large-value capacitors, necessary for very low frequencies, should be chosen with care, since potentially large leakage currents and high dielectric absorption can interfere with the orderly charge and discharge of C_F. If possible, for a given frequency, use lower IIN currents to reduce the size of the capacitor.

SYNC Output

SYNC is a TTL-/CMOS-compatible output that can be used to synchronize external circuits. The SYNC output is a square wave whose rising edge coincides with the output rising sine or triangle wave as it crosses through 0V. When the square wave is selected, the rising edge of SYNC occurs in the middle of the positive half of the output square wave, effectively 90° ahead of the output. The SYNC duty cycle is fixed at 50% and is independent of the DADJ control.

Because SYNC is a very high-speed TTL output, the high-speed transient currents in DGND and DV+ can radiate energy into the output circuit, causing a narrow spike in the output waveform. (This spike is difficult to see with oscilloscopes having less than 100MHz bandwidth). The inductance and capacitance of IC sockets tend to amplify this effect, so sockets are not recommended when SYNC is on. SYNC is powered from separate ground and supply pins (DGND and DV+), and it can be turned off by making DV+ open circuit. If synchronization of external circuits is not used, turning off SYNC by DV+ opening eliminates the spike.

Phase Detector

The MAX038 contains a TTL/CMOS phase detector that can be used in a phase-locked loop (PLL) to synchronize its output to an external signal. The external source is connected to the phase-detector input (PDI) and the phase detector output is taken from PDO. PDO is the output of an exclusive-OR gate, and produces a rectangular current waveform at the MAX038 output frequency, even with PDI grounded. PDO is normally connected to FADJ and a resistor, R_{PD}, and a capacitor C_{PD}, to GND. R_{PD} sets the gain of the phase detector, while the capacitor attenuates high-frequency components and forms a pole in the phase-locked loop filter.

PDO is a rectangular current-pulse train, alternating between 0µA and 500µA. It has a 50% duty cycle when the MAX038 output and PDI are in phase-quadrature (90° out of phase). The duty cycle approaches 100% as the phase difference approaches 180° and conversely, approaches 0% as the phase difference approaches 0°. The gain of the phase detector (K_D) can be expressed as:

$$K_D = 0.318 \times R_{PD} \text{ (volts/radian)} \quad [16]$$

where R_{PD} = phase-detector gain-setting resistor.

When the loop is in lock, the input signals to the phase detector are in approximate phase quadrature, the duty cycle is 50%, and the average current at PDO is 250µA (the current sink of FADJ). This current is divided between FADJ and R_{PD}; 250µA always goes into FADJ and any difference current is developed across R_{PD}, creating V_{FADJ} (both polarities). For example, as the phase difference increases, PDO duty cycle increases, the average current increases, and the voltage on R_{PD} (and V_{FADJ}) becomes more positive. This in turn decreases the oscillator frequency, reducing the phase difference, thus maintaining phase lock. The higher R_{PD} is, the greater V_{FADJ} is for a given phase difference; in other words, the greater the loop gain, the less the capture range. The current from PDO must also charge C_{PD}, so the rate at which V_{FADJ} changes (the loop bandwidth) is inversely proportional to C_{PD}.

The phase error (deviation from phase quadrature) depends on the open-loop gain of the PLL and the initial frequency deviation of the oscillator from the external signal source. The oscillator conversion gain (K_O) is:

$$K_O = \Delta\omega_O \div \Delta V_{FADJ} \quad [17]$$

which, from equation [6] is:

$$K_O = 3.43 \times \omega_O \text{ (radians/sec)} \quad [18]$$

The loop gain of the PLL system (K_V) is:

$$K_V = K_D \times K_O \quad [19]$$

where:

K_D = detector gain

K_O = oscillator gain.

With a loop filter having a response F(s), the open-loop transfer function, T(s), is:

$$T(s) = K_D \times K_O \times F(s) \div s \quad [20]$$

Using linear feedback analysis techniques, the closed-loop transfer characteristic, H(s), can be related to the open-loop transfer function as follows:

$$H(s) = T(s) \div [1 + T(s)] \quad [21]$$

The transient performance and the frequency response of the PLL depends on the choice of the filter characteristic, F(s).

When the MAX038 internal phase detector is not used, PDI and PDO should be connected to GND.

Layout Considerations

Realizing the full performance of the MAX038 requires careful attention to power-supply bypassing and board layout. Use a low-impedance ground plane, and connect all five GND pins directly to it. Bypass V+ and V- directly to the ground plane with 1µF ceramic capacitors or 1µF tantalum capacitors in parallel with 1nF ceramics. Keep capacitor leads short (especially with the 1nF ceramics) to minimize series inductance.

If SYNC is used, DV+ must be connected to V+, DGND must be connected to the ground plane, and a second 1nF ceramic should be connected as close as possible between DV+ and DGND (pins 16 and 15). It is not necessary to use a separate supply or run separate traces to DV+. If SYNC is to be disabled, DGND must be open circuit, but DV+ can either be connected to V+ or left open.

Minimize the trace area around COSC (and the ground plane area under COSC) to reduce parasitic capacitance, and surround this trace with ground to prevent coupling with other signals. Take similar precautions with DADJ, FADJ, and IIN. Place C_F so its connection to the ground plane is close to pin 6 (GND).

High-Frequency Waveform Generator

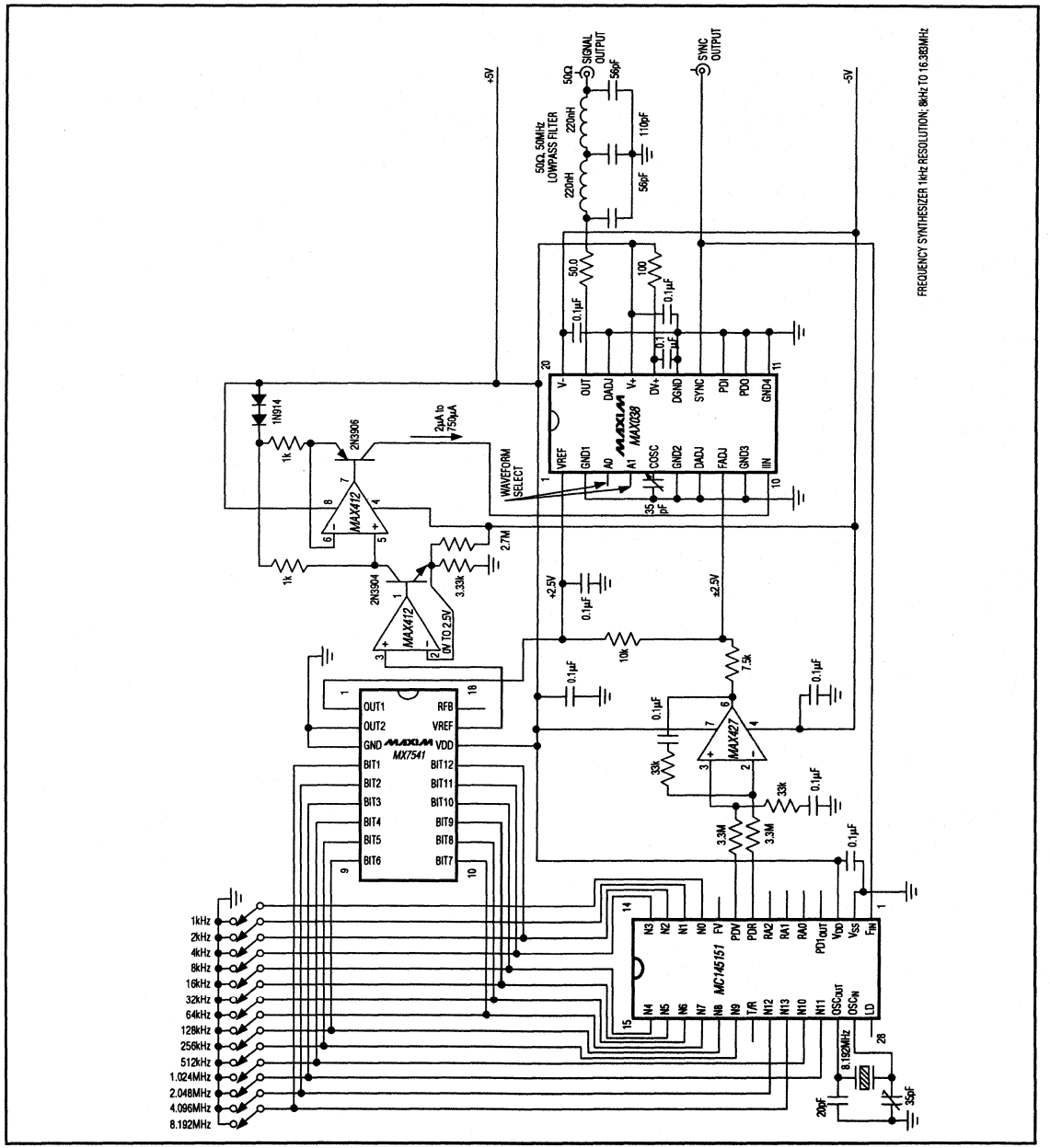


Figure 3. Crystal-Controlled, Digitally Programmed Frequency Synthesizer—8kHz to 16MHz with 1kHz Resolution

High-Frequency Waveform Generator

Applications Information

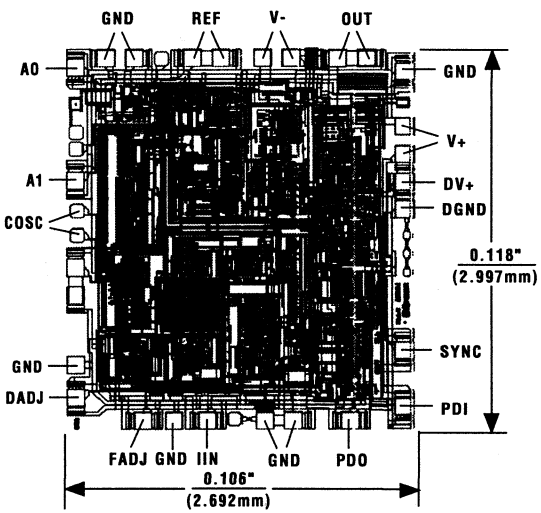
Frequency Synthesizer

Figure 3 shows a frequency synthesizer that produces accurate and stable sine, square, or triangle waves with a frequency range of 8kHz to 16.383MHz in 1kHz increments. A Motorola MC145151 provides the crystal-controlled oscillator, the ÷N circuit, and a high-speed phase detector. The manual switches set the output frequency; opening any switch increases the output frequency. Each switch controls both the ÷N output and an MX7541 12-bit DAC, whose output is converted to a current by using both halves of the MAX412 op amp. This current goes to the MAX038 IIN pin, setting its coarse frequency over a very wide range.

Fine frequency control (and phase lock) is achieved from the MC145151 phase detector through the differential amplifier and lowpass filter, U5. The phase detector compares the ÷N output with the MAX038 SYNC output and sends differential phase information to U5. U5's single-ended output is summed with an offset into the FADJ input. (Using the DAC and the IIN pin for coarse frequency control allows the FADJ pin to have very fine control with reasonably fast response to switch changes.)

A 50MHz, 50Ω lowpass filter in the output allows passage of 16MHz square waves and triangle waves with reasonable fidelity, while stopping high-frequency noise generated by the ÷N circuit.

Chip Topography



TRANSISTOR COUNT: 855;

SUBSTRATE CONNECTED TO GND.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

5-Tap Silicon Delay Line

General Description

The MXD1000 silicon delay line has five equally spaced taps providing 5ns to 500ns delays with a nominal accuracy of ±5% or ±2ns, whichever is greater. The part reproduces the input logic level at the output after a fixed delay (see *Delay Table*). The MXD1000 is designed to reproduce leading and trailing edges with equal precision. Each tap is capable of driving up to ten 74LS loads.

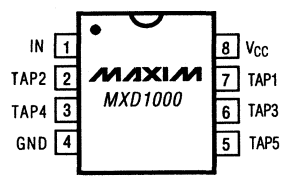
Maxim can customize standard delays to meet special needs.

Features

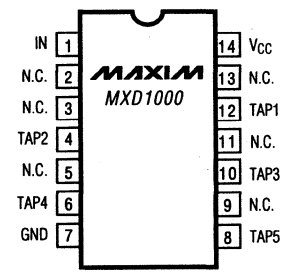
- ♦ **Delay Tolerances ±2ns**
- ♦ **Stability and Precision Over Temperature and Supply Voltage**
- ♦ **Leading and Trailing Edge Accuracy**
- ♦ **Custom Delays Available**
- ♦ **TTL/CMOS Compatible**

Pin Configurations

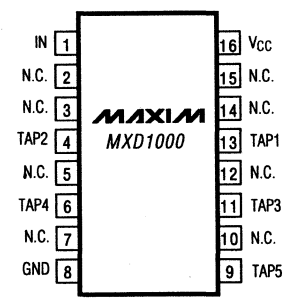
TOP VIEW



DIP/SO



DIP



SO

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MXD1000-__CPA	0°C to +70°C	8 Plastic DIP
MXD1000-__CPD	0°C to +70°C	14 Plastic DIP
MXD1000-__CSA	0°C to +70°C	8 SO
MXD1000-__CWE	0°C to +70°C	16 Wide SO
MXD1000-__C/D	0°C to +70°C	Dice*
MXD1000-__EPA	-40°C to +85°C	8 Plastic DIP
MXD1000-__EPD	-40°C to +85°C	14 Plastic DIP
MXD1000-__ESA	-40°C to +85°C	8 SO
MXD1000-__EWE	-40°C to +85°C	16 Wide SO

** Contact factory for dice specifications.*

***To complete the part number, simply consult the Delay Table, select the part-number extension corresponding to the desired delay times, and fill-in the blank in the Ordering Information.*

Delay Table (t_{PHL}, t_{PLH})

PART NO. EXTEN-SION	TAP1 DELAY TIME (ns)	TAP2 DELAY TIME (ns)	TAP3 DELAY TIME (ns)	TAP4 DELAY TIME (ns)	TAP5 DELAY TIME (ns)
25	5	10	15	20	25
30	6	12	18	24	30
35	7	14	21	28	35
40	8	16	24	32	40
45	9	18	27	36	45
50	10	20	30	40	50
60	12	24	36	48	60
75	15	30	45	60	75
100	20	40	60	80	100
125	25	50	75	100	125
150	30	60	90	120	150
175	35	70	105	140	175
200	40	80	120	160	200
250	50	100	150	200	250
350	70	140	210	280	350
500	100	200	300	400	500

Custom delays available.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Three-in-One Silicon Delay Line

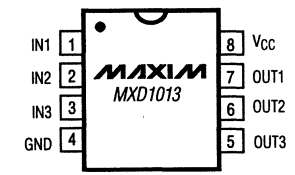
General Description

The MXD1013 silicon delay line offers three independent logic-buffered delays in a single package. Each provides a nominal accuracy of ±2ns for delay times between 10ns and 75ns, increasing to 5% for delays of 150ns. The MXD1013 reproduces the input logic level at the output after a fixed delay (see *Delay Table*). The part is designed to reproduce leading and trailing edges with equal precision. Each output is capable of driving up to ten 74LS loads.

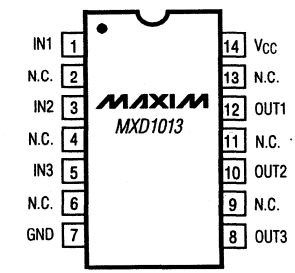
Maxim can customize standard delays to meet special needs.

Pin Configurations

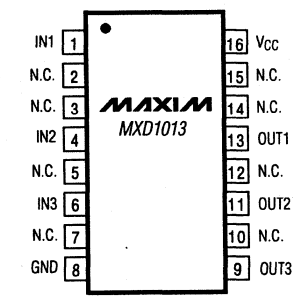
TOP VIEW



DIP/SO



DIP



Wide SO

Features

- ♦ **Delay Tolerances ±2ns**
- ♦ **Stability and Precision Over Temperature and Supply Voltage**
- ♦ **Leading and Trailing Edge Accuracy**
- ♦ **Custom Delays Available**
- ♦ **TTL/CMOS Compatible**

Ordering Information

PART**	TEMP. RANGE	PIN-PACKAGE
MXD1013-__CPA	0°C to +70°C	8 Plastic DIP
MXD1013-__CPD	0°C to +70°C	14 Plastic DIP
MXD1013-__CSA	0°C to +70°C	8 SO
MXD1013-__CWE	0°C to +70°C	16 Wide SO
MXD1013-__C/D	0°C to +70°C	Dice*
MXD1013-__EPA	-40°C to +85°C	8 Plastic DIP
MXD1013-__EPD	-40°C to +85°C	14 Plastic DIP
MXD1013-__ESA	-40°C to +85°C	8 SO
MXD1013-__EWE	-40°C to +85°C	16 Wide SO

** Contact factory for dice specifications.*

*** To complete the part number, simply consult the Delay Table, select the part-number extension corresponding to the desired delay times, and fill-in the blank in the Ordering Information.*

Delay Table (tPHL, tPLH)

PART NO. EXTENSION	DELAY PER OUTPUT (ns)
10	10/10/10
12	12/12/12
15	15/15/15
20	20/20/20
25	25/25/25
30	30/30/30
35	35/35/35
40	40/40/40
45	45/45/45
50	50/50/50
55	55/55/55
60	60/60/60
65	65/65/65
70	70/70/70
75	75/75/75
80*	80/80/80
90*	90/90/90
100*	100/100/100
150**	150/150/150

Custom delays available.
*±3% tolerance. **±5% tolerance.

Three-in-One Silicon Delay Line

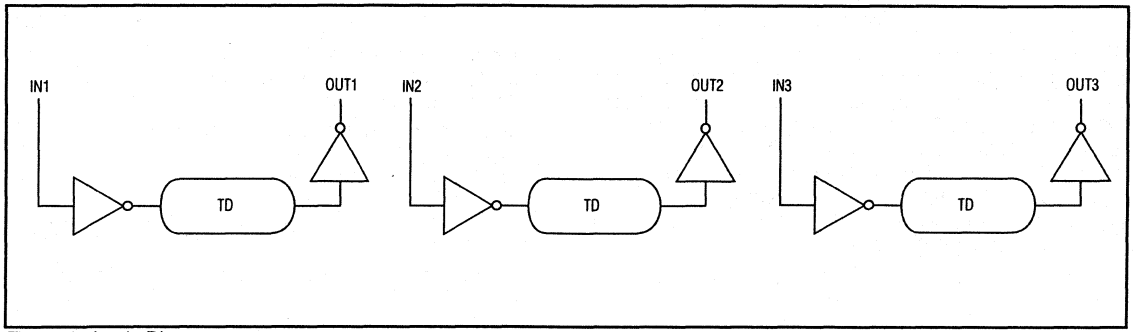


Figure 1. Logic Diagram

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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EVALUATION KIT AVAILABLE

MAXIM

6-Bit Quadrature Digitizer

General Description

The MAX2101 6-bit quadrature digitizer combines quadrature demodulation with analog-to-digital conversion on a single bipolar silicon die. This unique RF-to-Bits™ function bridges the gap between existing RF downconverters and CMOS digital signal processors (DSP).

The MAX2101's simple receiver subsystem is designed for digital communications systems such as those used in DBS, TVRO, WLAN, and other applications.

The MAX2101 accepts input signals from 400MHz to 700MHz and applies adjustable gain, providing at least 40dB of dynamic range.

Each baseband is filtered by an on-chip, 5th-order Butterworth lowpass filter, or the user can select an external filter path. Baseband sample rate is 60Msps. The MAX2101 is available in a commercial temperature range, 100-pin MQFP package.

Applications

Recovery of PSK and QAM Modulated RF Carriers

Direct-Broadcast Satellite (DBS) Systems

Television Receive-Only (TVRO) Systems

Cable Television (CATV) Systems

Wireless Local Area Networks (WLANs)

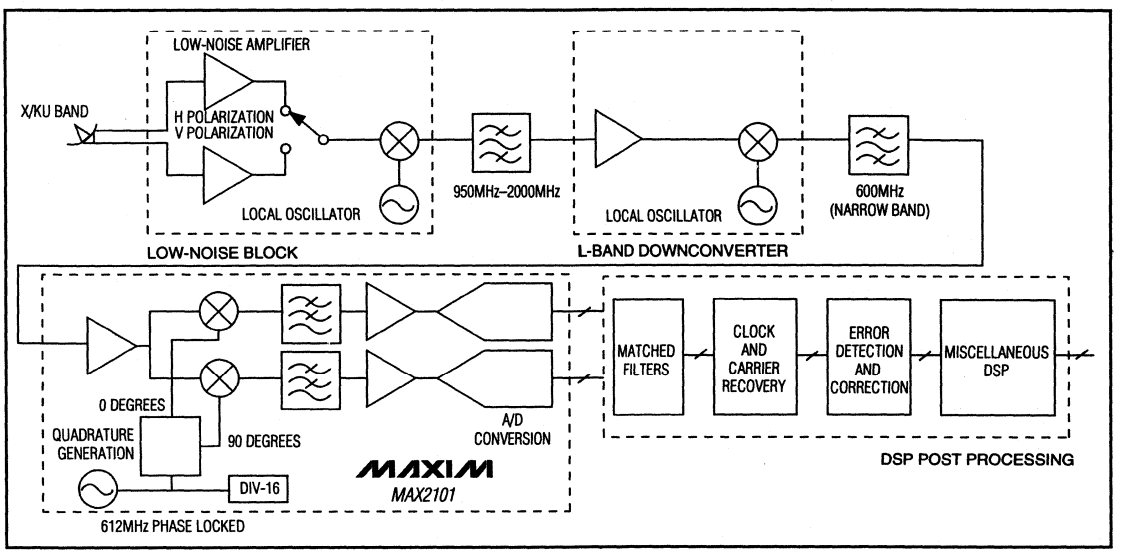
Features

- **ADCs Provide Greater than 5.3 Effective Bits at f_S = 60Msps, f_{IN} = 15MHz**
- **Fully Integrated Lowpass Filters with Externally Variable Bandwidth (10MHz to 30MHz)**
- **40dB Dynamic Range**
- **Integrated VCO and Quadrature Generation Network for I/Q Demodulation**
- **Divide-by-16 Prescaler for Oscillator PLL**
- **Programmable Counter for Variable Sample Rates**
- **Signal-Detection Function**
- **Selectable Offset Binary or Twos-Complement Output Data Format**
- **Automatic Baseband Offset Cancellation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2101CMQ	0°C to +70°C	100 MQFP

Typical Application Circuit



™RF-to-Bits is a registered trademark of Tektronix, Inc.

MAXIM

Appendix

A

Package Unit Process Flow

Wafer Inspection

All wafers are fabricated using custom processes with extremely tight control. Each wafer must pass numerous in-process checkpoints for oxide thickness, critical dimensions, pin-hole densities, and other requirements. And each must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are optically inspected for physical defects. Then they are parametrically tested to ensure full conformity to Maxim's specifications. Our precision parametric measurement capability ensures reliability and reproducibility in analog circuits. We believe this quality-control technology to be the best in the industry, capable of resolving current levels below 1pA and capacitance less than 1pF. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters that are crucial to predicting long-term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

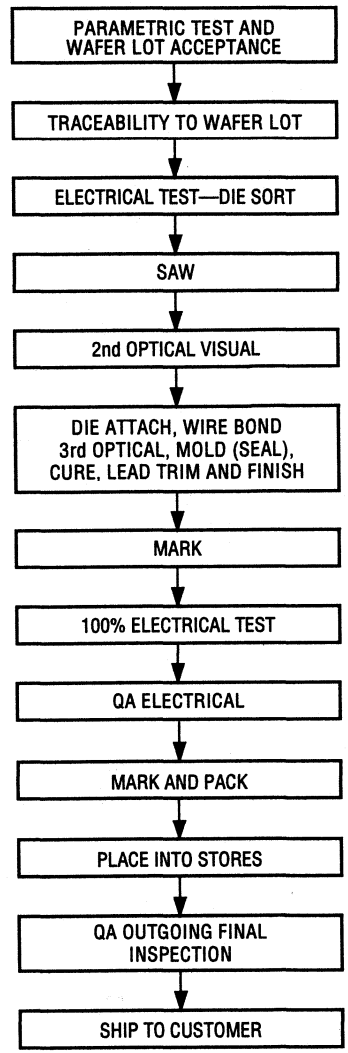
Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested over temperature: This is not a common practice in the industry. By using the latest high-speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data-acquisition products. Maxim's analog test capability is a significant improvement in accuracy, noise performance, and speed compared to current industry standards. This provides our customers with assurance that they will receive the part they paid for every time, without fail.

Product Conditioning and Qualification

Maxim also runs parts through qualification cycles, including accelerated life tests equivalent to 20 million operating hours and pressure/humidity cycles (85°C/85%).



A

Surface-Mount Products

Maxim is committed to providing high-quality, high-reliability 8- to 60-pin plastic surface-mount products. Nearly every monolithic device is offered in a surface-mount package. Except for 100% burn-in and cold test, they are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels. They receive the same product conditioning and lot qualification as the DIPs. Maxim assures lot reliability by subjecting a sample from each lot to a long-term life test prior to shipment.

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout when packaged in a 0.300" DIP.

0.300" JEDEC SOIC (W) parts also have the same pinout when packaged in a 0.300" DIP, except selected 16-pin devices.

14-pin devices too large for the 0.150" 14-pin (S) package are available in the 0.300" 16-pin (W) package.

Flatpack Pin Convention

No fixed convention exists for 40-pin devices assembled in either a 44- or 60-pin flatpack. Consult Applications for specific pinouts.

Quad Pack Pin Convention

Devices in the 28-pin Quad Pack have the same pinout when packaged in a 28-pin DIP.

All 40-pin devices planned for the 44-pin Quad Pack will have the following pinout:

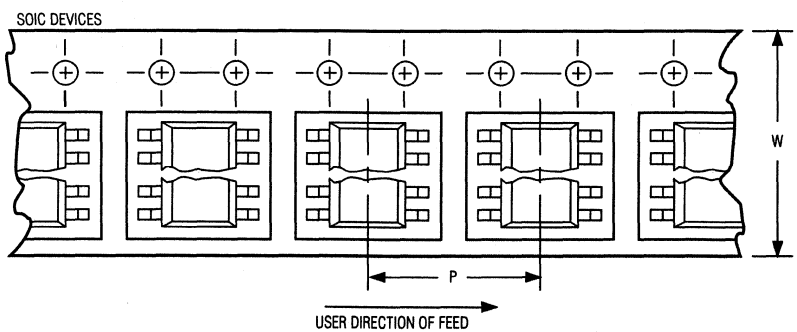
PIN NUMBER							
DIP	QUAD	DIP	QUAD	DIP	QUAD	DIP	QUAD
	1 N.C.		12 N.C.		23 N.C.		34 N.C.
1	2	11	13	21	24	31	35
2	3	12	14	22	25	32	36
3	4	13	15	23	26	33	37
4	5	14	16	24	27	34	38
5	6	15	17	25	28	35	39
6	7	16	18	26	29	36	40
7	8	17	19	27	30	37	41
8	9	18	20	28	31	38	42
9	10	19	21	29	32	39	43
10	11	20	22	30	33	40	44

Surface-Mount Packages in Reeled Tape

Maxim surface-mount packages are normally shipped in anti-static plastic rails. For customers using automatic placement systems, parts also come mounted in pockets on embossed tape. The tape is wound and shipped on reels.

The table and diagram below indicate the tape sizes used for various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12	8
	14L	16	8
	16L	16	8
SOIC	16L	16	12
	18L	24	12
	20L	24	12
	24L	24	12
	28L	24	12
PLCC	28L	24	16
	44L	32	24
QFP	44L	24	16



All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow," the standard that ensures lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet's +25°C worst-case limits.

Generally, the parameters or parameter limits listed in the product data sheets are tested during electrical probe. However, some parameters are impossible to test, or to test with absolute accuracy on unassembled product. Information regarding any of these parameters or parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	VALUE	UNITS
Chip Thickness Backlapped Wafers	15 ±1	mils
Die Length/Width Tolerance	±1	mils
Bonding Pad Dimensions (minimum)	typical min = 4x4	mils
Bonding Pad and Interconnect Material Thickness	10-12	kÅ
Storage Temperature	-40 to +150	°C
Operating Temperature	0 to +70	°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010, Condition B, with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation, except for bonding pads and scribe lines. Surface passivation is removed from bonding pad areas by plasma etching. The bonding pads may appear discolored at low magnification due to the aluminum's surface roughness after the etching process.

Maxim guarantees die and wafer AQL levels as follows:

Visual.....1.0%
Functional Electrical Testing.....0.65%
Parametric DC Testing.....2.5%
Untested Parameters.....6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry environment—preferably an inert gas such as nitrogen. Extreme care should be taken when handling die. An unclean environment or mishandling may result in electrical and visual failure.

Die Attach

To prevent oxidation, die attach should be done in a gaseous nitrogen ambient atmosphere. For eutectic die attach, we recommend using a 98% gold/2% silicon preform, at a die attach temperature between 385°C and 435°C. For epoxy die attach, the epoxy cure temperature should not exceed 150°C.

Bonding

When thermosonic or thermocompression gold ball bonding, use 1.0 or 1.3 mil diameter, 99.99% pure gold wire. When ultrasonic bonding, use 1.0 or 1.25 mil diameter, 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Figures 1 and 2 show how die and wafers are packaged for shipping:

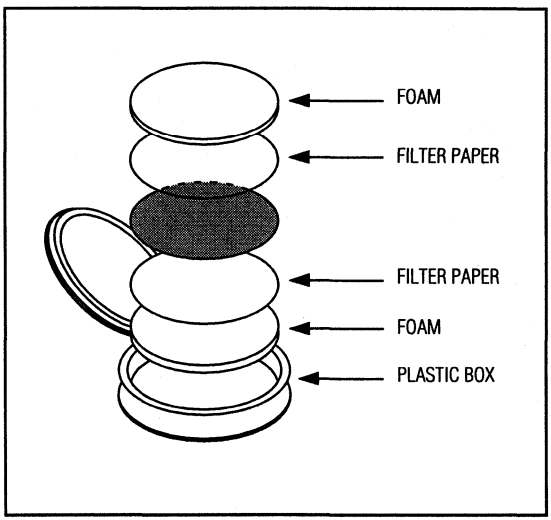


Figure 1. Wafer Carrier Package

A

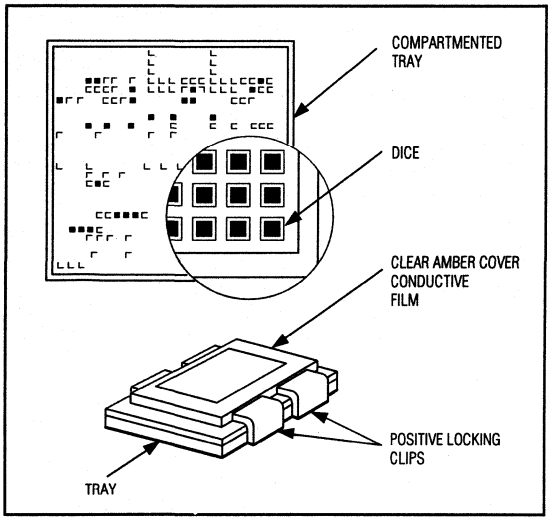


Figure 2. Die Carrier Package

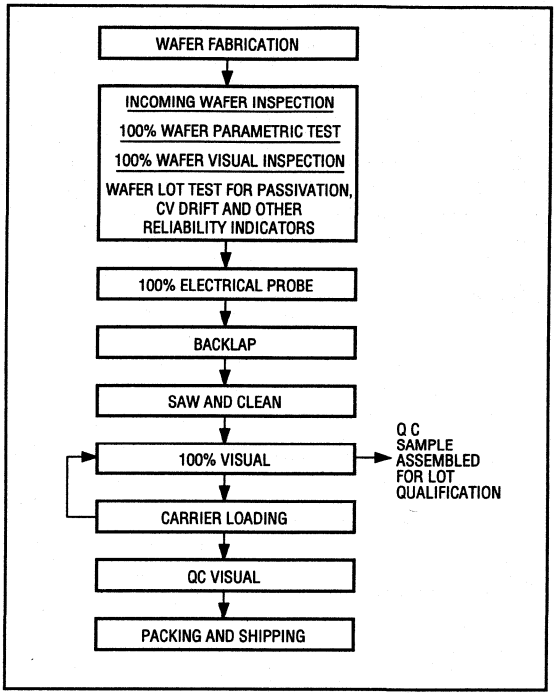
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Though these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the date the die is shipped to the user. Maxim assumes no responsibility for the die after 75 days or after further user processing such as, but not limited to, die attach or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a "/D" suffix. Example: ICL7109C/D.

When ordering dice as wafers, replace the "D" with a "W" in the part number. Example: MAX7231C/D die = MAX7231C/W wafer.

Maxim's /883 and High-Reliability Program

/883 Flow

Maxim's /883 program is fully compliant to MIL-STD-883, paragraph 1.2.1. Environmental and electrical screening are performed per Method 5004, Class B of MIL-STD-883. Quality conformance inspection is performed per method 5005 (Groups A, B, C, and D).

Maxim /883 Class B Flow

- FULL-MATERIAL TRACEABILITY AND PROCESS GENEALOGY
- WAFER FABRICATION AND DEVICE ASSEMBLY
- PRESEAL INTERNAL VISUAL MIL-STD-883, METHOD 2010, CONDITION B
- SEAL
- TEMPERATURE CYCLING MIL-STD-883, METHOD 1010, CONDITION C
- CONSTANT ACCELERATION MIL-STD-883, METHOD 2001, CONDITION E (Y1 ONLY)
- FINE LEAK TEST MIL-STD-883, METHOD 1014, CONDITION C
- GROSS LEAK TEST MIL-STD-883, METHOD 1014, CONDITION C
- +25°C ELECTRICAL TEST
- BURN-IN PER METHOD 1015 160 HOURS AT +125°C (OR EQUIVALENT)
- FINAL ELECTRICAL SCREEN +25°C, +125°C, –55°C (5% PDA APPLIES)
- QUALITY CONFORMANCE INSPECTION PER METHOD 5005, GROUPS A, B, C AND D IN COMPLIANCE TO MIL-STD-883, PARAGRAH 1.2.1
- EXTERNAL VISUAL MIL-STD-883, METHOD 2009
- BOX STOCK

Hi-Rel Plastic Flow

In addition to the /883B and /HR screening flows, Maxim offers a high-reliability screening flow for plastic-encapsulated packages including SOIC package types. Products screened to this flow can be used in high-reliability applications when hermetically sealed devices screened to MIL-STD-883 may not be justified. SOICs with full burn-in and screening not only offer excellent reliability, but also save on valuable PC board space. Customers should contact the factory for availability of the specific device types currently offered.

Maxim Hi-Rel Plastic Flow

- TEMPERATURE CYCLING -65°C TO +150°C, MIL-STD-883, METHOD 1010, 10 CYCLES
- BURN-IN PER METHOD 1015 160 HOURS AT +125°C MINIMUM (UNLESS OTHERWISE SPECIFIED BY CUSTOMER)
- POST BURN-IN ELECTRICAL TEST +25°C FUNCTIONAL, AC, DC 5% PDA APPLIES TO DC TESTS
- 100% ELECTRICAL TEST - MIN/MAX OPERATING TEMPERATURE
- QA ELECTRICAL TEST AQL=0.1%, ACC=0 +25°C, MIN/MAX OPERATING TEMPERATURE
- EXTERNAL VISUAL
- BOX STOCK

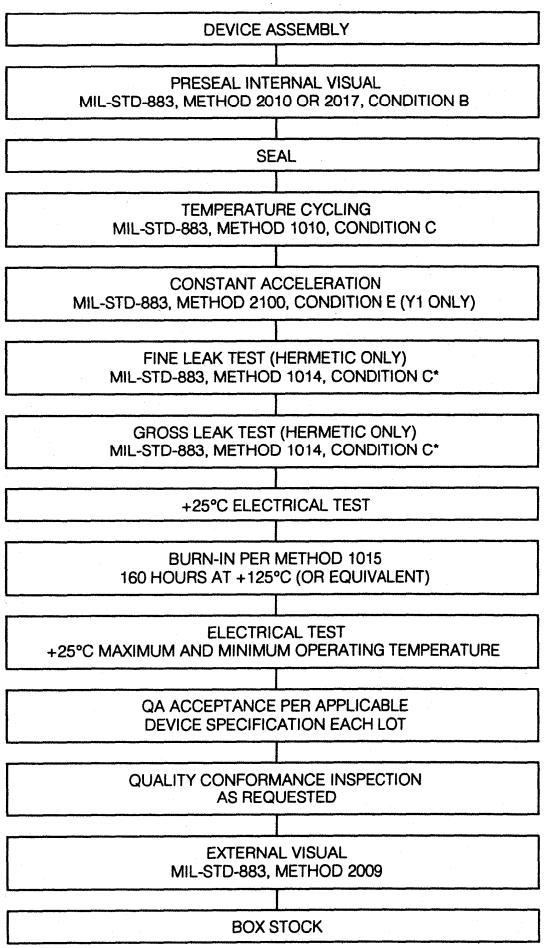
A

_Maxim's /883 and High-Reliability Program (cont.)

/HR Flow

Maxim's High Reliability (/HR) flow is offered for hybrid products as well as for products that have not yet been fully certified compliant to MIL-STD-883, and are therefore non-compliant. The /HR flow will not be offered for parts certified to MIL-STD-883. As seen by the adjacent flow chart, the /HR flow follows the steps and requirements of the MIL-STD-883 flow closely. Product processed to this flow is not documented in as much detail, nor does it have to adhere to the operating temperature range required by MIL-STD-883. Product may follow this flow but be tested over the commercial (0°C to +70°C) or extended (–40°C to +85°C) temperature ranges. This flow applies to hermetic packaged product only. It is Maxim's experience that this flow is desired by companies having older government projects or projects requiring an inherently higher reliability screening for critical application environments. Full QCI testing will be performed when requested. Only Group A will be performed per each inspection lot.

Maxim /HR Flow

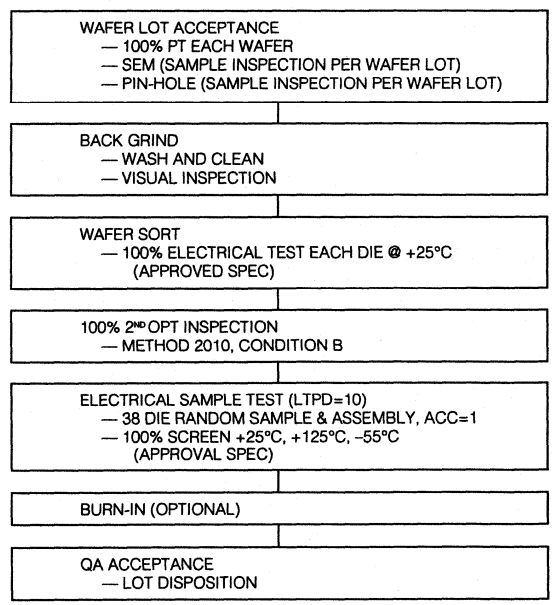


** If seal perimeter is greater than 2.0 inches, Condition A applies.*

Military Die Flow

Manufacturers of military hybrid components or modules have found Maxim's die product offerings to be a tremendous manufacturing asset due to the complete and thorough wafer sort programs used. As a result, a high demand has been created for qualified die used in products sold to the military market. Maxim has created the following flow, as a direct derivative of the MIL-STD-5008 Element Evaluation Sequence, which serves to qualify a die lot for use in the military environment. This flow is applied per product on a case by case basis. Contact the factory for availability per product.

Maxim Military Die Flow



DESC Approved Devices to Standard Military Drawings (SMDs) Currently Available

MAXIM P/N	SMD NUMBER
MAX1044	5962-38707
MAX1232	5962-94514
MAX1259	5962-93264
MAX220/22/ 32A/42/43	5962-94565
MAX232	5962-89877
MAX280	5962-91595
MAX310/311	5962-94556
MAX333	5962-93180
MAX358	77052
MAX359	5962-85131
MAX4420/29	5962-88770
MAX452-455	5962-94512
MAX500	5962-94527
MAX502	5962-88767
MAX543	5962-92345
MAX630	5962-94540
MAX631-633	5962-92141
MAX634	5962-92124
MAX638	5962-92127
MAX660	5962-94632
MAX663/4/6/7	5962-92126
MAX674	5962-94681
MAX680	5962-93120
MAX690/692/694	5962-90712
MAX691/693/695	5962-90711
MAX696/697	5962-93125
MAX705-708	5962-93267
MAX731/2/3	5962-94621
MAX738	5962-93121
MAX813L	5962-93267
MAX8211/8212	5962-90811
MX536A	5962-89805
MX574A	5962-85127
MX580	5962-86861
MX584	5962-38128
MX7226	5962-87802
MX7524	5962-87700
MX7528	5962-87701
MX7537	5962-87763
MX7541	5962-89481
MX7545	5962-87702
MX7547	5962-89657
MX7572	5962-87591
MX7574	5962-89616
MX7820	5962-88650
MX7824/28	5962-88764
MXL1062	5962-91595
DG201A	77053
DG403	5962-89763
DG405	5962-89961
DG408/409	5962-92042
DG411/412/413	5962-90731
DG417/418/419	5962-90737
DG441/442	5962-92041
DG506A/7A/9A	5962-85131
DG508A	77052
DG528	5962-87689
HI-201	77053
ICL7660A	5962-38707
ICL7667	5962-87660
IH5040-5045	81006
IH5047	81006
IH5140-5145	81006
IH5148-5151	81006
REF01	5962-89581
REF02	85514
TSC426/427/428	5962-88503

Parts Currently /883 Compliant

MAX1044
MAX122
MAX1232
MAX1259
MAX154/158
MAX160/161/164
MAX170/172
MAX176
MAX180/181
MAX220/222
MAX231/232/236
MAX232A
MAX242/243
MAX274
MAX280
MAX310/311
MAX333
MAX358/359
MAX378/379
MAX4420/4426-9
MAX452-455
MAX500
MAX502
MAX516
MAX526/527
MAX543
MAX626/627/628
MAX630-634/638
MAX660
MAX663/4/6/7
MAX674
MAX680
MAX690-697
MAX705-708
MAX730-733
MAX738
MAX813L
MAX8211/8212
MX536A
MX574A
MX580/581/584
MX674A
MX7225/7226
MX7501/2/3
MX7520/1/4/8
MX7533/7537
MX7541/2/3/5/7
MX7572/7574
MX7820/1/4/8
MXL1062
DG200A/201A/202
DG300A-309
DG381A/4A/7A
DG390A
DG401/403/405
DG406-409
DG411/412/413
DG417/418/419
DG441/442
DG506A-509A
DG528/529
HI-201/201HS
ICL7660A/7667
IH5040-5049
IH5050/5051
IH5140-5145
IH5148-5151
IH5341/5352
OP07
REF01/02
TSC426/427/428

A

Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped into categories, according to their functions. Maxim currently adds a "MAX" prefix to the part's unique number. The categories are as follows (with some exceptions):

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface Products and Analog Filters
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op Amps, Buffers, and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power-Supply Circuits and Voltage References
MAX700-799	µP Peripherals and Display Drivers
MAX800-899	µP Supervisory
MAX900-999	Comparators

Within each category, blocks of numbers are reserved for subgroups.

3-Letter Suffixes

EXAMPLE:

MAX358CPD

- C — Operating Temperature Range
- P — Package Type
- D — Number of Pins

4-Letter Suffixes

When a part has a four-letter suffix, the first letter of the suffix denotes product grade. For example, the first "A" in MAX631ACPA indicates 5% output accuracy; the remaining three letters denote temperature range, package type, and number of pins. Therefore, the MAX631ACPA has 5% output accuracy, operates over the 0°C to +70°C range, comes in a plastic DIP package, and has eight pins.

Temperature Ranges

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package Type

"A"	SSOP (Shrink Small-Outline Package)
"B"	CERQUAD
"C"	TO-220, TQFP (Thin Quad Flat Pack)
"D"	Ceramic Sidebraze
"F"	Ceramic Flat Pack
"H"	Module
"J"	CERDIP Dual-In-Line
"K"	TO-3, PPGA
"L"	LCC (Leadless Ceramic Chip Carrier)
"M"	Plastic Quad Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	PLCC (Plastic Leaded Chip Carrier)
"R"	Narrow CERDIP (300 mil)
"S"	Small Outline (150 mil)
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-99, TO-100)
"U"	TSSOP, µMAX, SOT
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"X"	J Leaded Ceramic Chip Carrier (JLCC)
"Y"	Narrow Sidebraze (300 mil)
"Z"	TO-92, MQUAD
"/D"	Dice
"/W"	Wafer

Number of Pins

"A"	8	"P"	20
"B"	10, 64	"Q"	2, 100
"C"	12	"R"	3, 84
"D"	14	"S"	4
"E"	16	"T"	6
"F"	22	"U"	60
"G"	24	"V"	8 (0.200" pin circle, isolated case)
"H"	44		
"I"	28	"W"	10 (0.230" pin circle, isolated case)
"J"	32		
"K"	5, 68	"X"	36
"L"	40	"Y"	8 (0.200" pin circle, case to pin 4)
"M"	48, 7		
"N"	18	"Z"	10 (0.230" pin circle, case to pin 5)

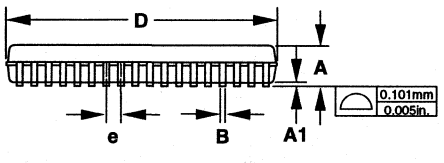
Second-Source Numbering System

In most cases, Maxim's part number for a second-source product follows the industry's most widely accepted numbering system for that particular part, rather than our own convention. This includes the most commonly recognized prefix as well as the original designators for product grade, temperature range, package type, and number of pins.

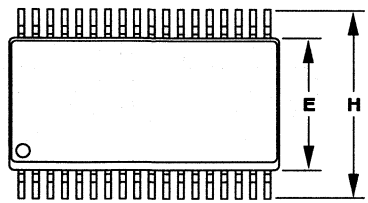
Maxim frequently supplies second-source products in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, these devices are given a part number that follows the original numbering convention.

Package Information

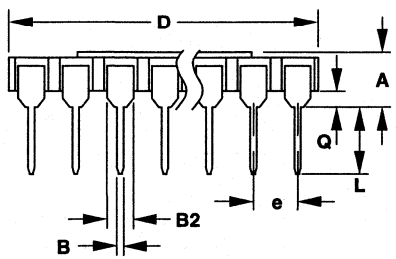
This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two-letter code, indicating package type (Plastic DIP, Small-Outline, etc.) and number of pins. Along with indicators for temperature range and device grade (where appropriate), the two-letter code is also used in the part number suffix for each of Maxim's proprietary devices.



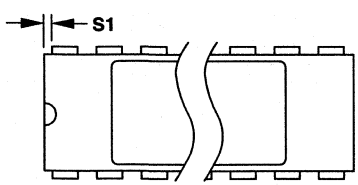
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.012	0.016	0.305	0.406
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
E	0.291	0.299	7.40	7.60
e	0.0315		0.800	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



A PACKAGE (36 PINS)
SSOP
(SHRINK SMALL OUTLINE)



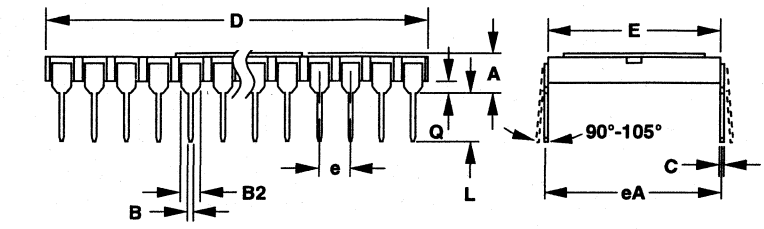
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
eA	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	–	0.13	–



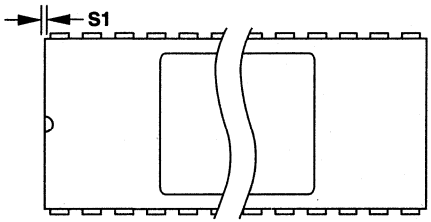
D PACKAGE
(0.300 in.)
CERAMIC
SIDEBRAZE

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.550	–	13.97
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

A

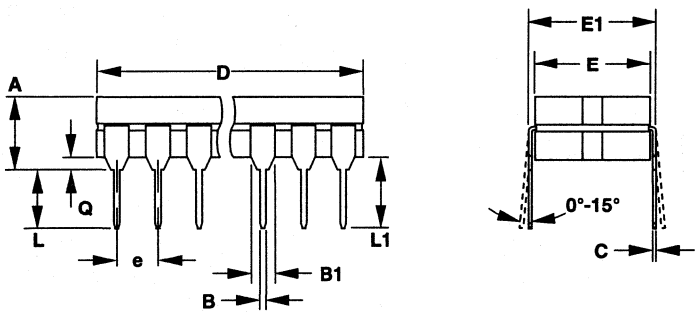


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.510	0.610	12.95	15.49
eA	0.600		15.24	
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	–	0.13	–

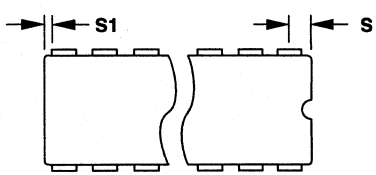


D PACKAGE
(0.600 in.)
CERAMIC
SIDEBRAZE

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	–	1.29	–	32.77
D	28	–	1.49	–	37.85
D	40	–	2.096	–	53.24

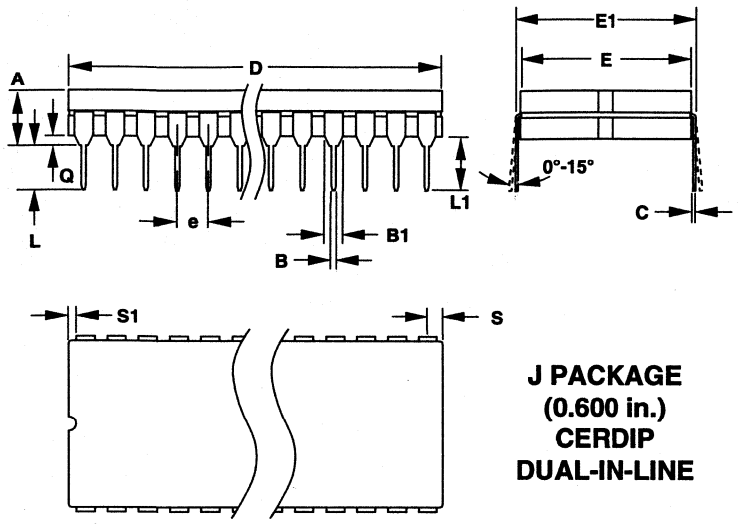


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–



J PACKAGE
(0.300 in.)
CERDIP
DUAL-IN-LINE

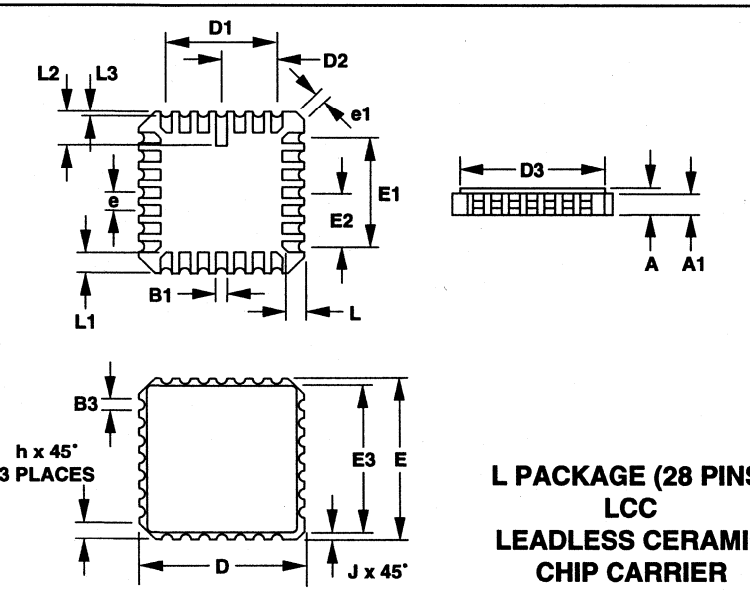
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.232	–	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	–	3.81	–
Q	0.015	0.075	0.38	1.91
S	–	0.100	–	2.54
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	–	1.290	–	32.77
D	28	–	1.490	–	37.85
D	40	–	2.096	–	53.24

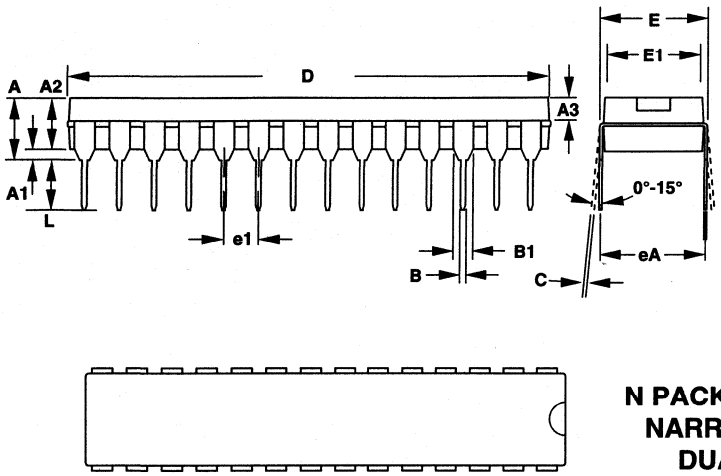
J PACKAGE
(0.600 in.)
CERDIP
DUAL-IN-LINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300		7.62	
D2/E2	0.150		3.81	
D3/E3	–	0.460	–	11.68
e	0.050		1.27	
e1	0.015	–	0.38	–
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

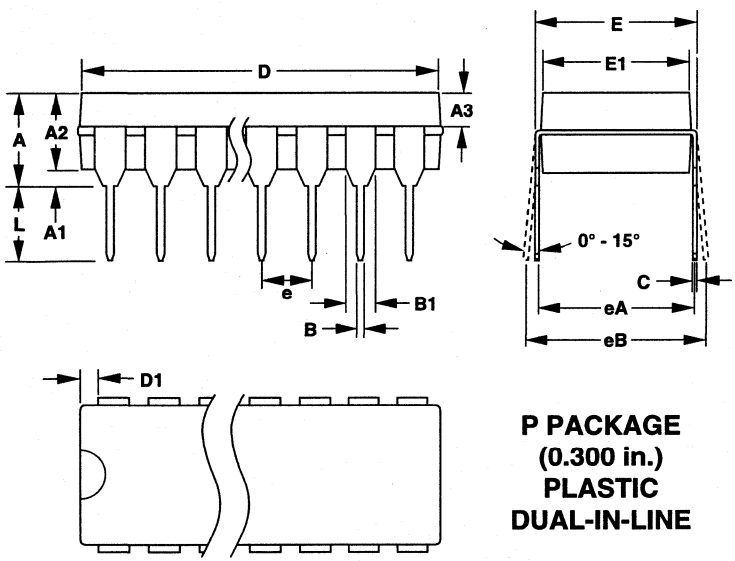
L PACKAGE (28 PINS)
LCC
LEADLESS CERAMIC
CHIP CARRIER

A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.180	–	4.572
A1	0.020	–	0.508	–
A2	0.125	0.150	3.175	3.810
B	0.015	0.022	0.381	0.559
B1	0.045	0.060	1.143	1.524
B2	0.035	0.045	0.889	1.143
C	0.008	0.012	0.203	0.305
D	1.350	1.380	34.290	35.052
E	0.300	0.325	7.620	8.255
E1	0.275	0.295	6.985	7.493
e1	0.100		2.54	
eA	0.300		7.62	
L	0.115	0.150	2.921	3.810

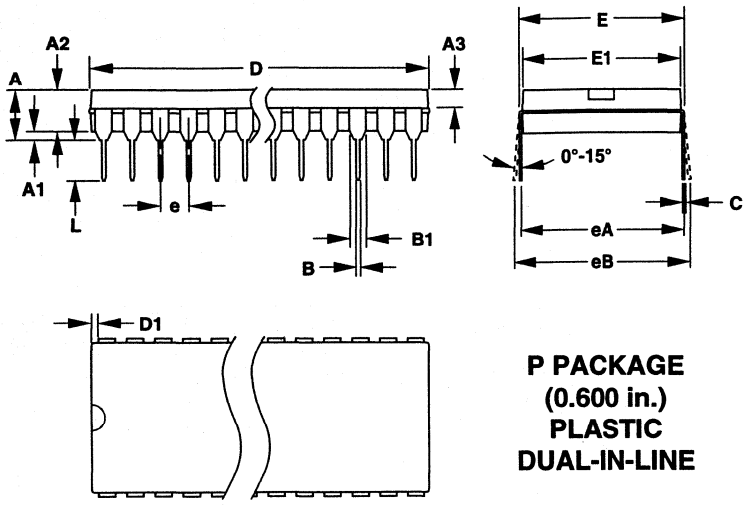
N PACKAGE (28 PINS)
NARROW PLASTIC
DUAL-IN-LINE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

P PACKAGE
(0.300 in.)
PLASTIC
DUAL-IN-LINE

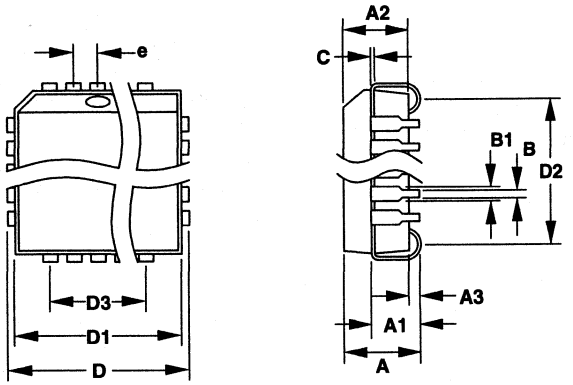
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.348	0.390	8.84	9.91
D	14	0.735	0.765	18.67	19.43
D	16	0.745	0.765	18.92	19.43
D	18	0.885	0.915	22.48	23.24
D	20	1.015	1.045	25.78	26.54
D	24	1.14	1.265	28.96	32.13



P PACKAGE
(0.600 in.)
PLASTIC
DUAL-IN-LINE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	–	2.54	–
eA	0.600	–	15.24	–
eB	–	0.700	–	17.78
L	0.120	0.150	3.05	3.81

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	24	1.230	1.270	31.24	32.26
D	28	1.430	1.470	36.32	37.34
D	40	2.025	2.075	51.44	52.71

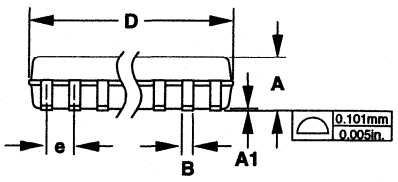


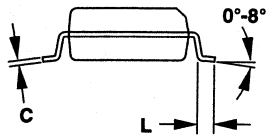
Q PACKAGE
PLASTIC
LEADED CHIP CARRIER

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

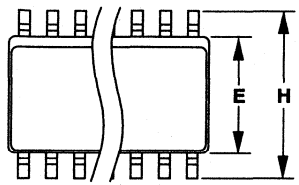
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3		0.200 REF		5.08 REF	
D	28	0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3		0.300 REF		7.62 REF	
D	44	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3		0.500 REF		12.62 REF	

A





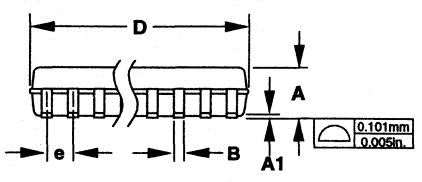
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

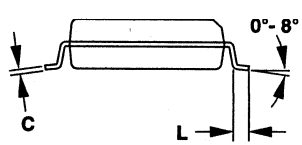


S PACKAGE
(0.150 in.)
SMALL
OUTLINE

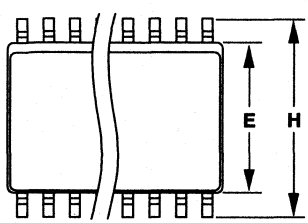
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A





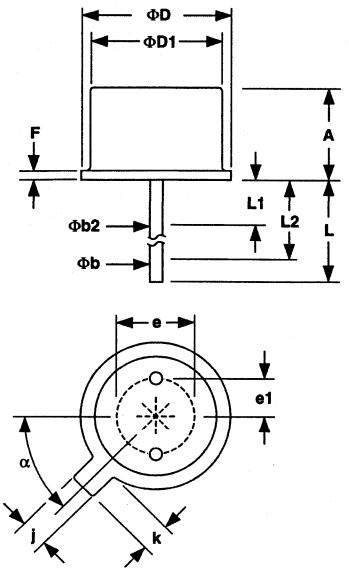
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



S PACKAGE
(0.300 in.)
SMALL
OUTLINE

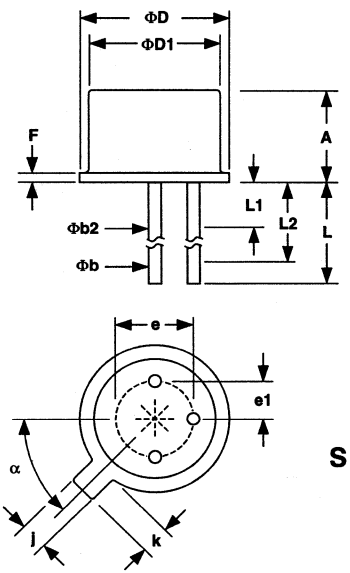
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.115	0.150	2.92	3.81
Φb	–	0.021	–	0.533
Φb2	0.016	0.019	0.406	0.483
ΦD	0.209	0.230	5.31	5.84
ΦD1	0.178	0.195	4.52	4.95
e	0.100		2.54	
e1	0.050		1.27	
F	–	0.030	–	0.762
j	0.036	0.046	0.914	1.17
k	0.028	0.048	0.711	1.22
L	0.500	–	12.70	–
L1	–	0.050	–	1.27
L2	0.250	–	6.35	–
α	45°		45°	

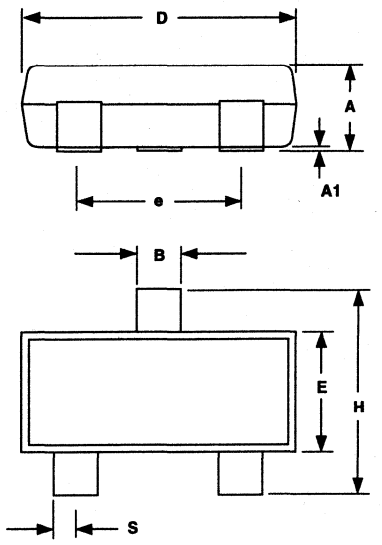
S PACKAGE (2 PINS)
TO-52



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.115	0.150	2.92	3.81
Φb	–	0.021	–	0.533
Φb2	0.016	0.019	0.406	0.483
ΦD	0.209	0.230	5.31	5.84
ΦD1	0.178	0.195	4.52	4.95
e	0.100		2.54	
e1	0.050		1.27	
F	–	0.030	–	0.762
j	0.036	0.046	0.914	1.17
k	0.028	0.048	0.711	1.22
L	0.500	–	12.70	–
L1	–	0.050	–	1.27
L2	0.250	–	6.35	–
α	45°		45°	

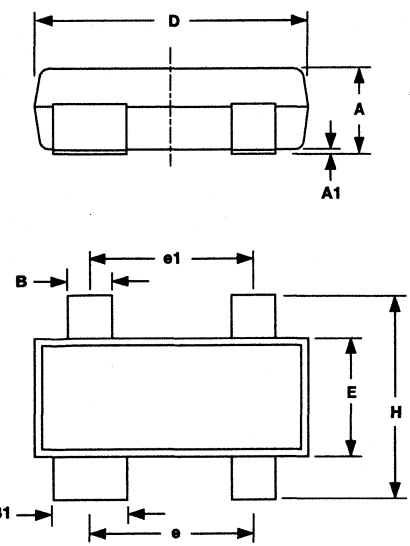
S PACKAGE (3 PINS)
TO-52

A



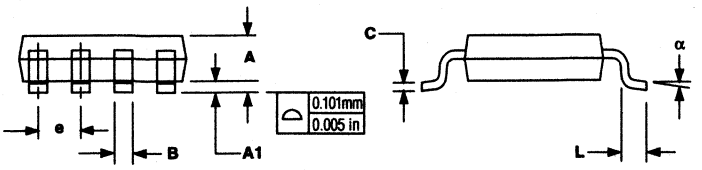
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
H	0.082	0.098	2.083	2.489
I	0.004	0.012	0.102	0.305
S	0.017	0.022	0.432	0.559

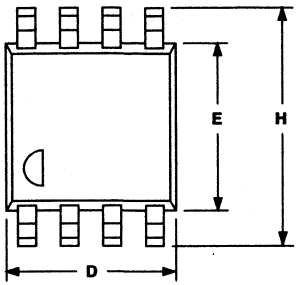
U PACKAGE (3 PINS)
SOT
(SMALL-OUTLINE TRANSISTOR)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
B1	0.030	0.038	0.762	0.965
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
e1	0.071	0.079	1.803	2.007
H	0.082	0.098	2.083	2.489
I	0.004	0.012	0.102	0.305

U PACKAGE (4 PINS)
SOT
(SMALL-OUTLINE TRANSISTOR)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

U PACKAGE (8 PINS)
μMAX

A